

N-channel 800 V, 0.29 Ω typ., 14 A MDmesh™ K5 Power MOSFET in a TO-220 package

Datasheet - production data

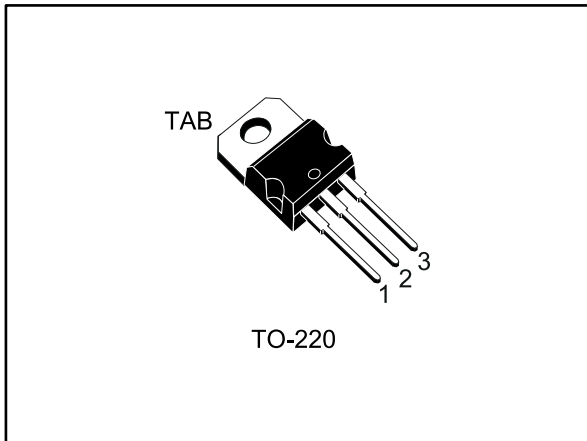
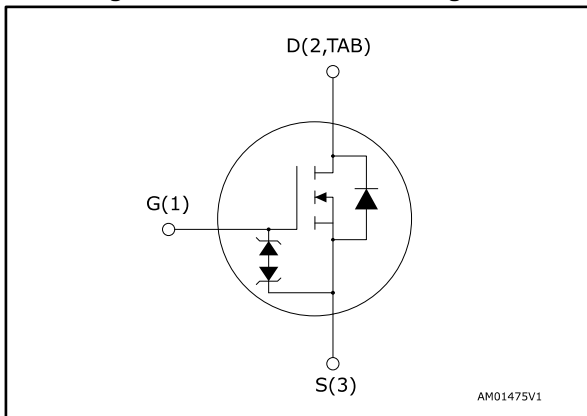


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STP17N80K5	800 V	0.34 Ω	14 A

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STP17N80K5	17N80K5	TO-220	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	14	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	56	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	170	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾ $I_{SD} \leq 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 640\text{ V}$

⁽³⁾ $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.74	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{Jmax})	4.7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	340	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DD} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$		0.29	0.34	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	866	-	pF
C_{oss}	Output capacitance		-	64	-	pF
C_{rss}	Reverse transfer capacitance		-	0.42	-	pF
$C_{o(tr)}$ ⁽¹⁾	Equivalent capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$	-	142	-	pF
$C_{o(er)}$ ⁽²⁾	Equivalent capacitance energy related		-	51	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	26	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	15.2	-	nC

Notes:

⁽¹⁾ $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	14.8	-	ns
t_r	Rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	84.3	-	ns
t_f	Fall time		-	10.1	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	439		ns
Q_{rr}	Reverse recovery charge		-	6.37		μC
I_{RRM}	Reverse recovery current		-	29		A
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	626		ns
Q_{rr}	Reverse recovery charge		-	8.36		μC
I_{RRM}	Reverse recovery current		-	26.7		A

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

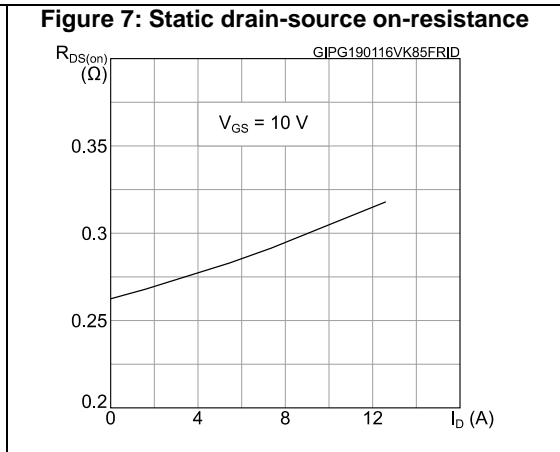
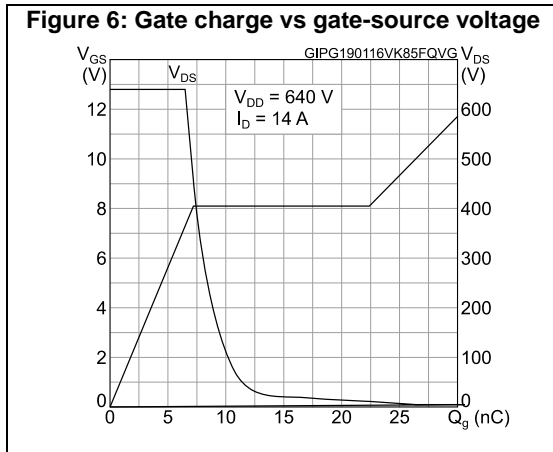
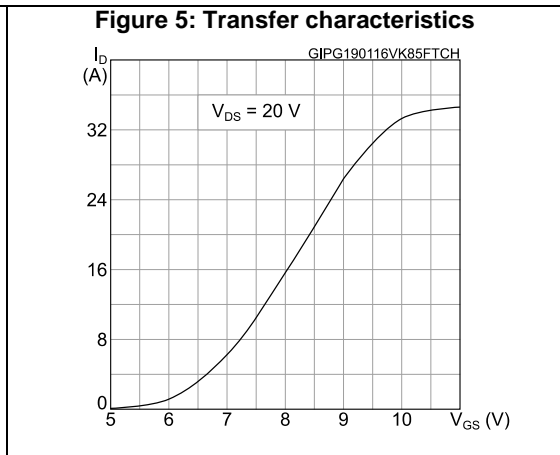
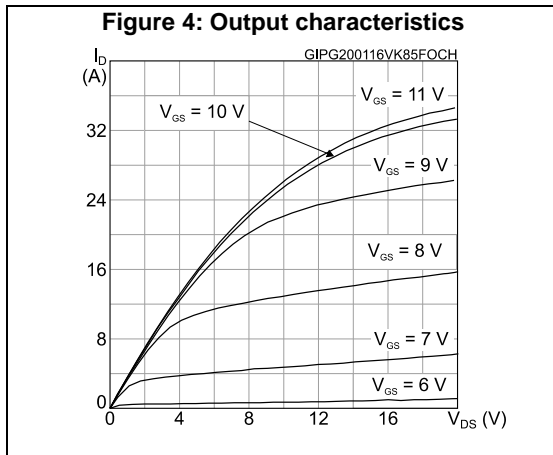
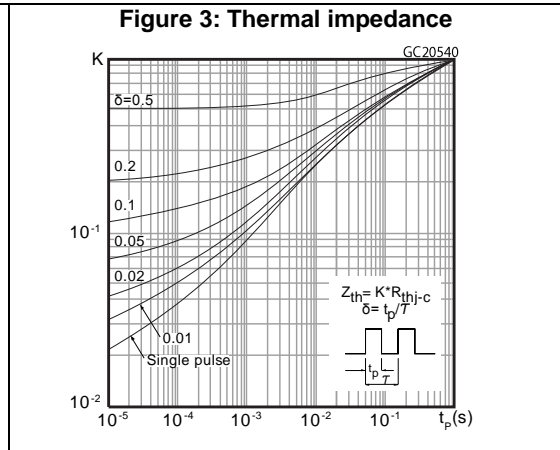
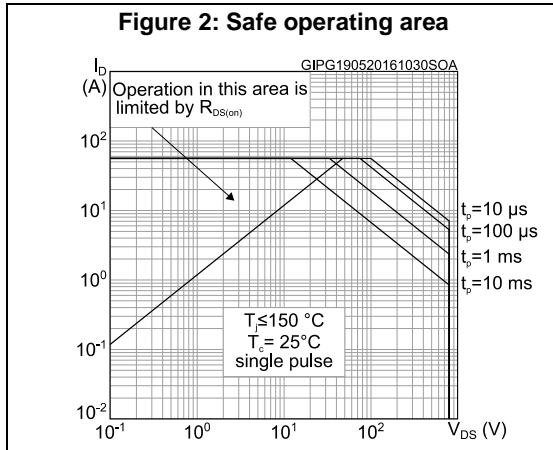


Figure 8: Capacitance variations

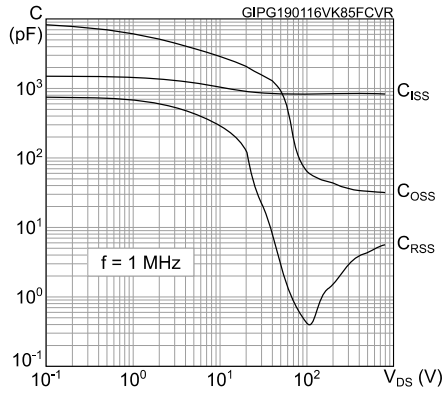


Figure 9: Normalized gate threshold voltage vs temperature

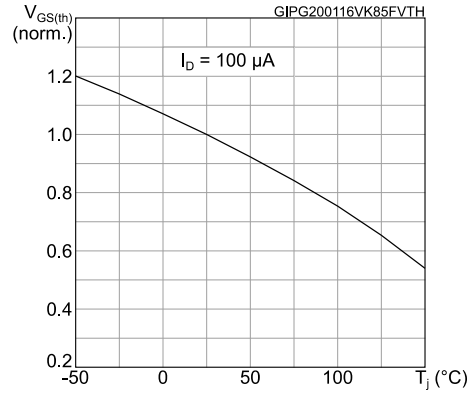


Figure 10: Normalized on-resistance vs temperature

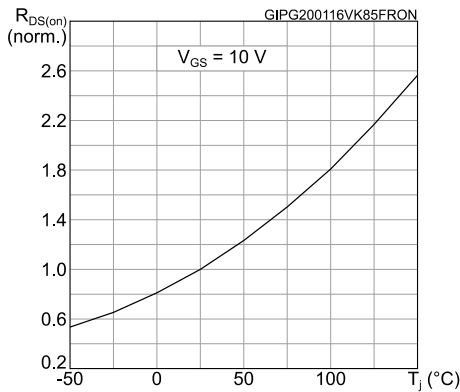


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

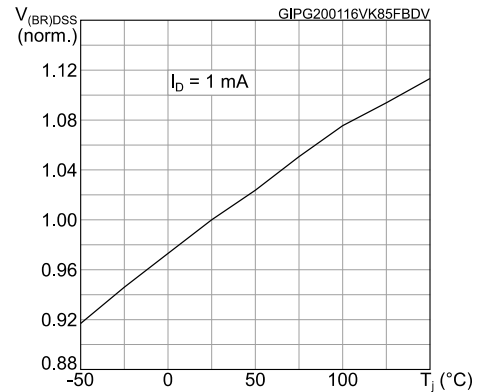


Figure 12: Source-drain diode forward characteristics

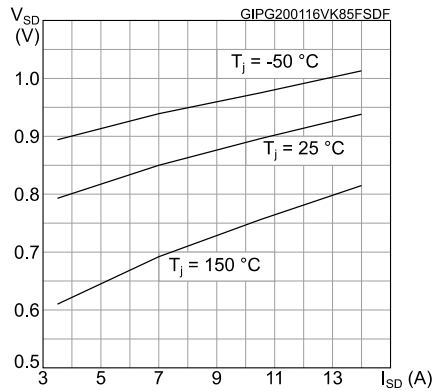
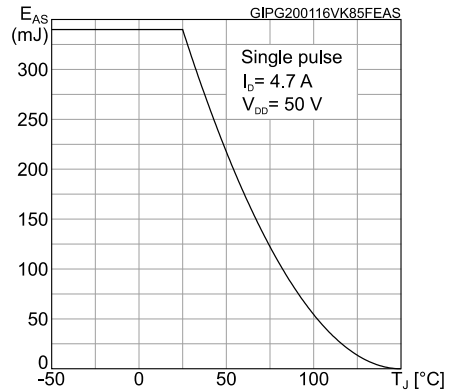
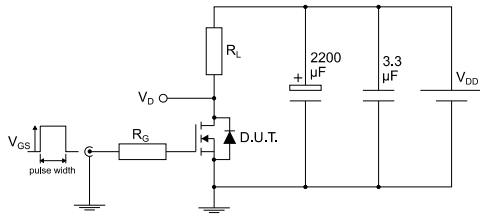


Figure 13: Maximum avalanche energy vs starting T_J



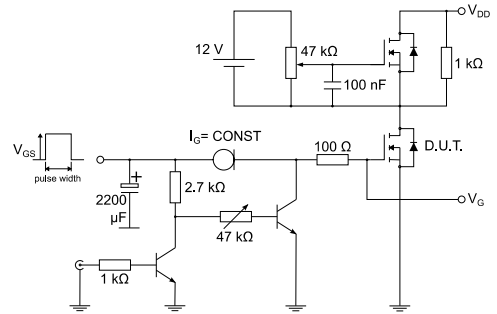
3 Test circuits

Figure 14: Test circuit for resistive load switching times



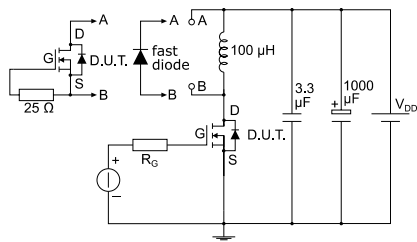
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Figure 15: Test circuit for gate charge behavior



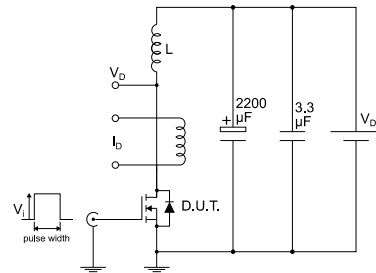
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Figure 16: Test circuit for inductive load switching and diode recovery times



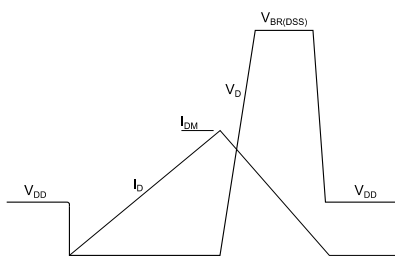
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Figure 17: Unclamped inductive load test circuit



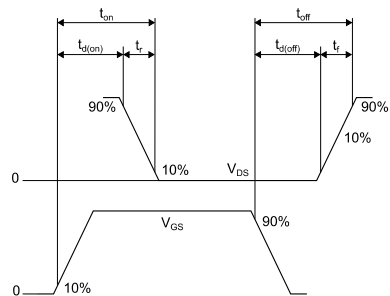
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



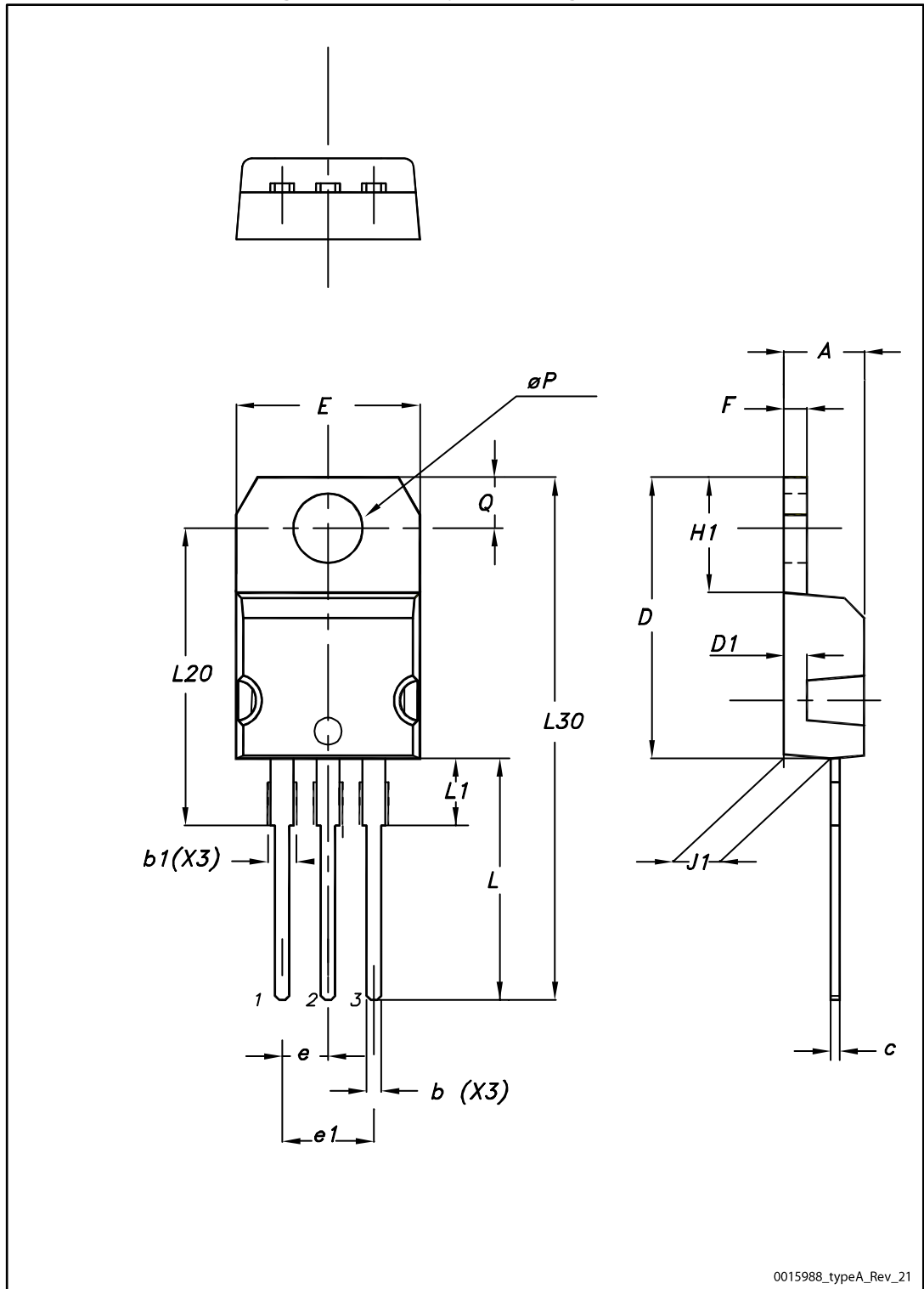
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220 type A package information

Figure 20: TO-220 type A package outline



0015988_typeA_Rev_21

Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
03-Apr-2015	1	First release.
19-May-2016	2	Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> Added: <i>Section 3.1: "Electrical characteristics (curves)"</i> Minor text changes

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