RAA210825

Pin-Configurable 25A DC/DC Power Module with PMBus Interface

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The RAA210825 is a pin-strap configurable 25A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally-enhanced HDA packaging technology, the module can deliver up to 25A of continuous output current without the need for airflow or additional heat sinking. The RAA210825 simplifies configuration and control of Renesas digital power technology while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8277M.

The RAA210825 uses ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. The RAA210825 comes with a preprogrammed configuration for operating in a pin-strap mode. Output voltage, switching frequency, input UVLO, soft-start/stop delay and ramp times, and the device SMBus address can be programmed with external pin-strap resistors. A standard PMBus interface addresses fault management, in addition to real-time full telemetry and point-of-load monitoring.

The RAA210825 is available in a 41 Ld compact 17mm x 19mm HDA module with very low profile height of 3.6mm, suitable for automated assembly by standard surface mount equipment. The RAA210825 is RoHS compliant by exemption.

Related Literature

For a full list of related documents, visit our website

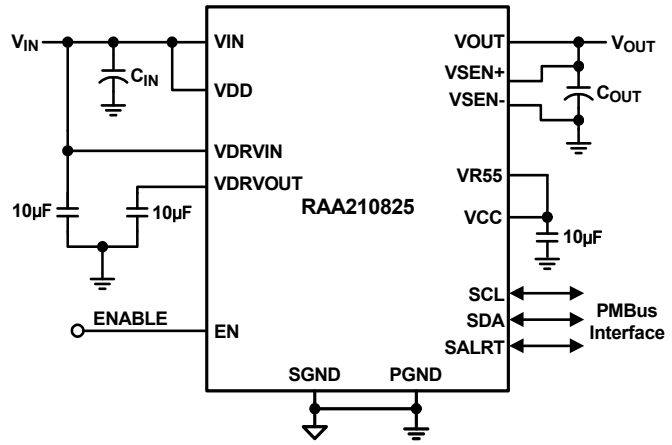
- RAA210825 product page

Features

- 25A single channel output current
- Wide V_{IN} range: 4.5V to 14V
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - ±1.2% accuracy over line/load/temperature
- PMBus interface and/or Pin-Strap mode
  - Pin-strap mode for standard settings
  - V_{OUT}, switching frequency, input UVLO, soft-start/stop and external sync
  - Real time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and switching frequency
- ChargeMode control loop architecture
  - 296kHz to 1.06MHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- Complete input and output over/undervoltage, output current, and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced HDA package

Applications

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory



Note:
1. Only bulk input and output capacitors are required to finish the design.

Figure 1. Complete Digital Switch-Mode Power Supply

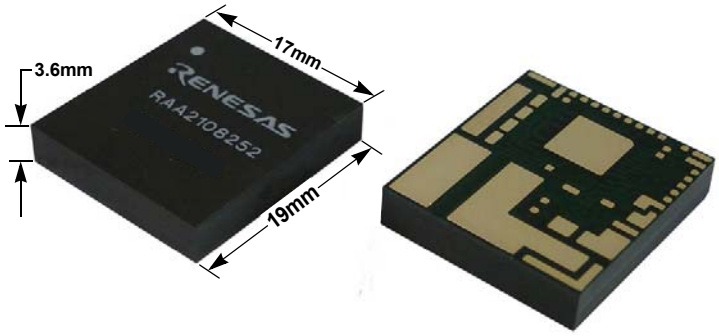
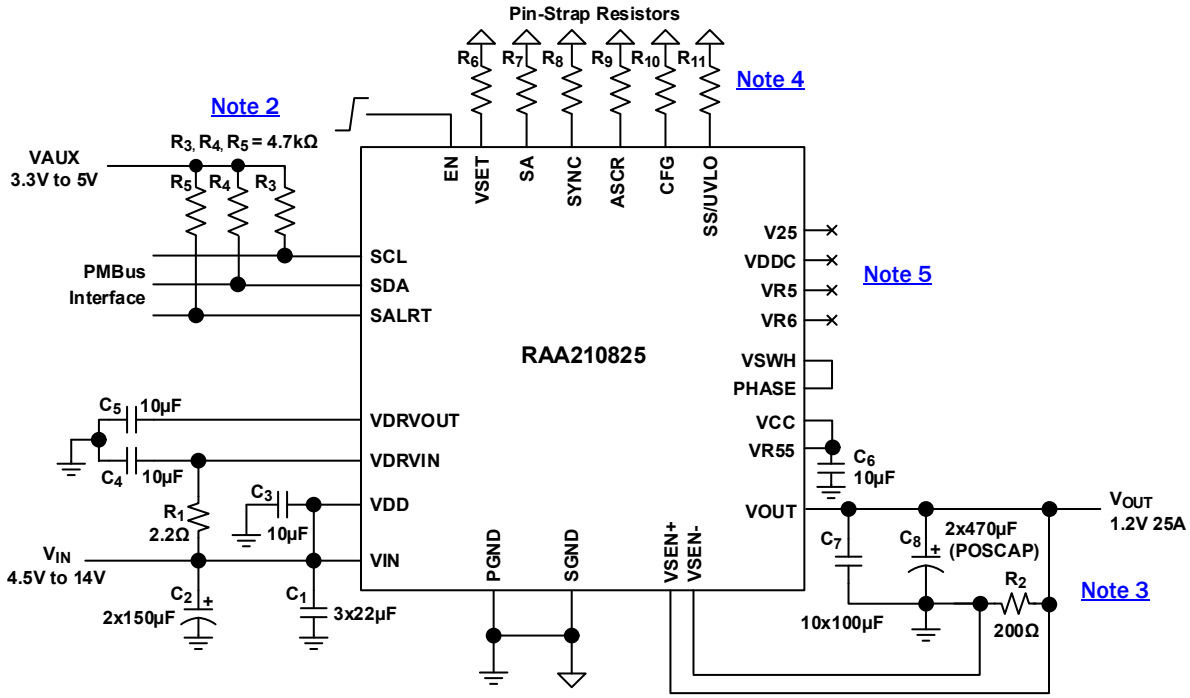


Figure 2. Small Package for High Power Density

Contents

1. Overview

1.1 Typical Application Circuit



Notes:

2. R_3 and R_4 are not required if the PMBus host already has I^2C pull-up resistors.
3. R_2 is optional but recommended to sink possible ~100µA back-flow current from the V_{SEN+} pin. Back-flow current is present only when the module is in a disabled state with power still available at the VDD pin.
4. R_6 through R_{11} can be selected according to the tables for the pin-strap resistor setting in this document .
5. Internal reference supply pins (V25, VDDC, VR5, VR6) do not need external capacitors and can be no connect. Refer to "PCB Layout Guidelines" on page 29 for more information.

Figure 3. Typical Single-Phase Application Circuit for 1.2V/25A Output

Table 1. RAA210825 Design Matrix Guide and Output Voltage Response

V_{IN} (V)	V_{OUT} (V)	Input Capacitors (Note 6)	Output Capacitors	ASCR Gain (Note 7)	ASCR Residual (Note 7)	Frequency (kHz)	V_{OUT} Dev Peak-Peak (mV) (Note 8)
5	0.7	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 6x470µF POS	300	70	296	51
5	0.7	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 4x470µF POS	500	90	615	66
12	0.7	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 6x470µF POS	270	70	296	70
12	0.7	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 4x470µF POS	500	90	615	70
5	0.8	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 5x470µF POS	300	80	296	59.5
5	0.8	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 3x470µF POS	400	90	615	80
12	0.8	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 5x470µF POS	350	80	296	65
12	0.8	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 3x470µF POS	400	90	615	80
5	0.9	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 4x470µF POS	350	80	364	70
5	0.9	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 2x470µF POS	400	80	615	90
12	0.9	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 4x470µF POS	350	80	364	70
12	0.9	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 2x470µF POS	400	80	615	88

Table 1. RAA210825 Design Matrix Guide and Output Voltage Response (Continued)

V_{IN} (V)	V_{OUT} (V)	Input Capacitors (Note 6)	Output Capacitors	ASCR Gain (Note 7)	ASCR Residual (Note 7)	Frequency (kHz)	V_{OUT} Dev Peak-Peak (mV) (Note 8)
5	1	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 3x470µF POS	300	80	364	83
5	1	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 2x470µF POS	400	90	615	92
12	1	3x22µF Ceramic + 2x150µF POS	12x100µF Ceramic + 3x470µF POS	350	90	364	79
12	1	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 2x470µF POS	400	90	615	100
5	1.2	3x22µF Ceramic + 2x150µF POS	10x100µF Ceramic + 2x470µF POS	250	90	364	90
5	1.2	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 2x470µF POS	400	80	727	100
12	1.2	3x22µF Ceramic + 2x150µF POS	10x100µF Ceramic + 2x470µF POS	250	100	364	115
12	1.2	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 2x470µF POS	400	80	727	105
5	1.5	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 2x470µF POS	300	80	471	93
5	1.5	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 2x470µF POS	400	80	727	104
12	1.5	3x22µF Ceramic + 2x150µF POS	8x100µF Ceramic + 2x470µF POS	270	90	471	120
12	1.5	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 2x470µF POS	400	80	727	111
5	1.8	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 1x470µF POS	200	100	471	150
5	1.8	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	300	90	727	155
12	1.8	3x22µF Ceramic + 2x150µF POS	6x100µF Ceramic + 1x470µF POS	200	100	471	165
12	1.8	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	270	90	727	155
5	2.5	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	230	90	615	166
12	2.5	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	250	100	615	166
12	3.3	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	250	100	615	175
12	5	3x22µF Ceramic + 2x150µF POS	4x100µF Ceramic + 1x470µF POS	270	90	727	190

Notes:

6. C_{IN} bulk capacitor is optional only for energy buffer from the long input power supply cable.
7. ASCR gain and residual are selected to ensure that the phase margin is higher than 60° at ambient room temperature (+25°C).
8. Peak-to-peak voltage deviation is measured under 0%-50% load transient and slew rate = 15A/µs.
9. Frequency is selected to achieve best efficiency at full load. Higher frequency can be selected because less output capacitance is required to meet the transient response specification.

Table 2. Recommended I/O Capacitor in Table 1

Vendors	Value	Part Number
MURATA, Input Ceramic	22µF, 25V, 1210	GRM32ER71E226KE15L
Taiyo Yuden, Input Ceramic	22µF, 25V, 1210	TMK325BJ226MM-T
MURATA, Output Ceramic	100µF, 6.3V, 1210	GRM32EC80J107ME20L
TDK, Output Ceramic	100µF, 6.3V, 1210	C3225X5R0J107M
SANYO POSCAP, Input Bulk	150µF, 16V	16TQC150MYF
SANYO POSCAP, Output Bulk	470µF, 6.3V	6TPE470MI

1.2 RAA210825 Internal Block Diagram

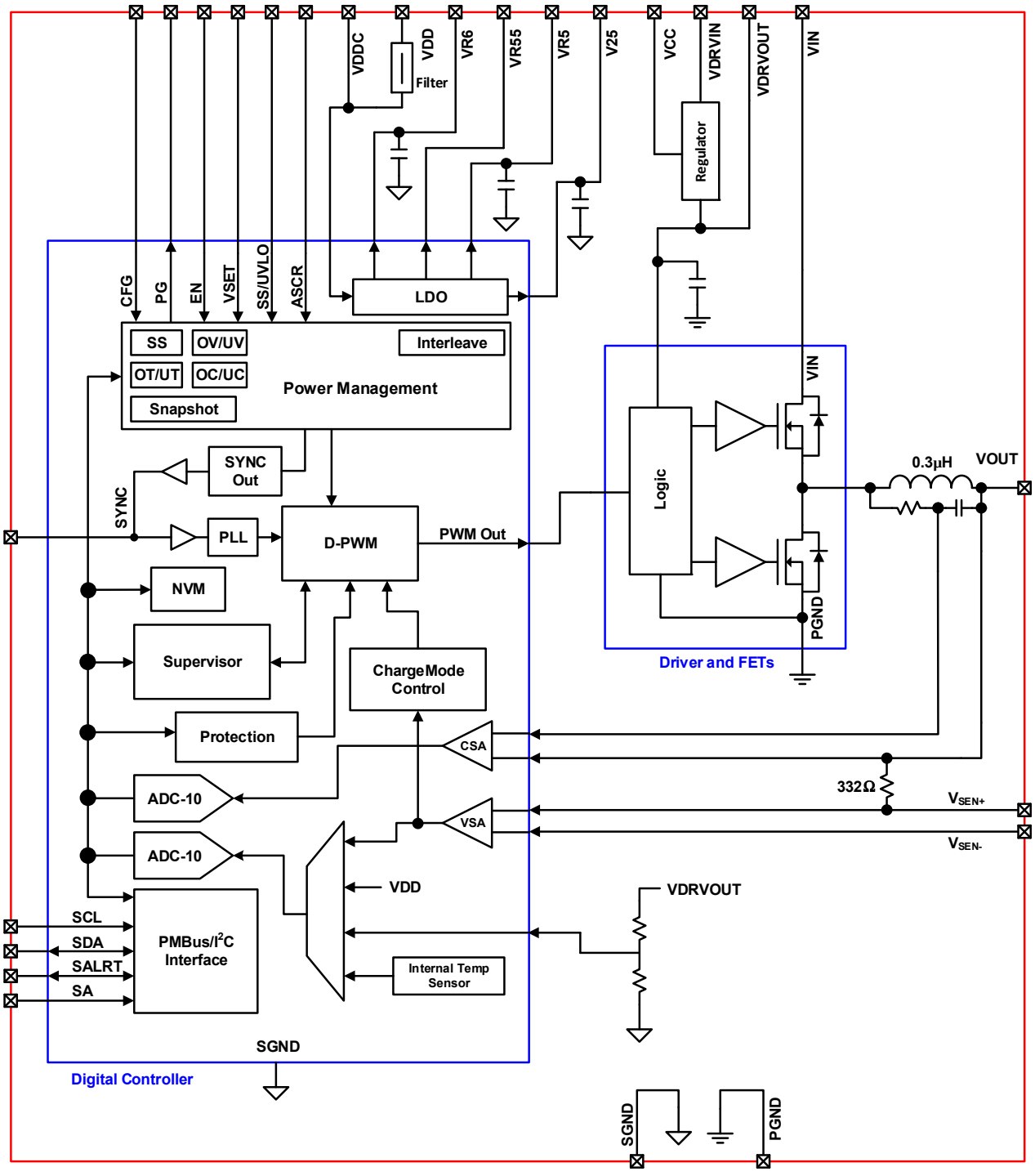


Figure 4. Block Diagram

1.3 Ordering Information

Part Number (Notes 11, 12)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 10)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2108252GLG#AG0	RAA2108252	-40 to +85	-	41 Ld 17x19 HDA	Y41.17x19
RAA2108252GLG#HG0	RAA2108252	-40 to +85	500	41 Ld 17x19 HDA	Y41.17x19
RAA2108252GLG#MG0	RAA2108252	-40 to +85	100	41 Ld 17x19 HDA	Y41.17x19
RTKA2108252H00000BU	Evaluation Board				

Notes:

10. RSee TB347 for details about reel specifications.
11. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
12. For Moisture Sensitivity Level (MSL), see the RAA210825 device page. For more information about MSL, see TB363.

Table 3. Key Differences Between Family of Parts

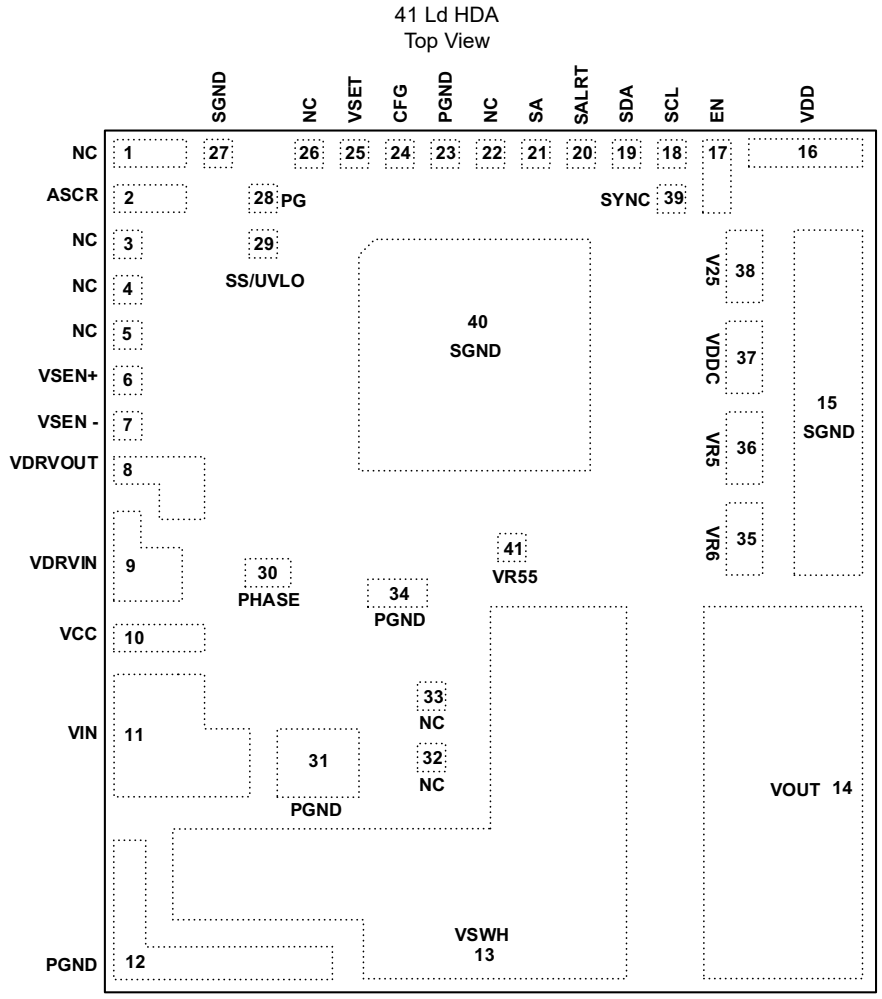
Part Number	Description	V_{IN} Range (V)	V_{OUT} Range (V)	I_{OUT} (A)
RAA210825	25A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	25
RAA210833	33A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	33
RAA210850	50A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	50
RAA210870	70A DC/DC single channel Power Module	4.5 - 14	0.6 - 2.5	70
RAA210925	25A/25A DC/DC dual channel Power Module	4.5 - 14	0.6 - 5	25/25

Table 4. Comparison of Simple Digital and Full Digital Parts

	ISL8277M	RAA210825
V_{IN} (V)	4.5-14	4.5-14
V_{OUT} (V)	0.6-5	0.6-5
I_{OUT} (Max) (A)	25	25
f_{SW} (kHz)	296-1067	296-1067
Digital PMBus Programmablility for Configuration of Modules	All PMBus commands, NVM access to store module configuration	Configuration of modules supported using pin-strap resistors. Digital programmability supports configuration changes during run-time operation with a subset of PMBus commands. No NVM access to store module configuration
Power Navigator Support	Yes	Yes
SYNC Capability	Yes	Yes
Current Sharing Multi-Modules	No	No
DDC Pin (Inter-Device Communication)	Yes	No

Note: For a full comparison of all the RAA210XXX and ISL827XM product offerings please visit the simple-digital module family page.

1.4 Pin Configurations



1.5 Pin Descriptions

Pin	Label	Type	Description
2	ASCR	I	ChargeMode control ASCR parameters selection pin. Used to set ASCR gain and residual values.
6	VSEN+	I	Differential output voltage sense feedback. Connect to the positive output regulation point.
7	VSEN-	I	Differential output voltage sense feedback. Connect to the negative output regulation point.
8	VDRVOUT	PWR	Output of internal regulator for powering internal MOSFET driver. Connect a 10µF bypass capacitor to this pin. The regulator output is dedicated to powering internal MOSFET drivers. Do not use this regulator for any other purpose. For applications with VIN less than 5.2V, use an external 5V supply or connect this pad to VIN.
9	VDRVIN	PWR	Input supply to internal regulator for powering internal MOSFET drivers. Connect this pad to VIN.
10	VCC	PWR	Bias pin for internal regulator. Connect VCC pad to VR55 pin directly with a short loop trace. Not recommended to power external circuit.
11	VIN	PWR	Main input supply. Refer to "PCB Layout Guidelines" on page 29 for the decoupling capacitors placement from VIN to PGND.
12, 23, 31, 34	PGND	PWR	Power ground. Refer to "PCB Layout Guidelines" on page 29 for the PGND pad connections and decoupling capacitors placement.

Pin	Label	Type	Description
13	VSWH	PWR	Switch node. Refer to "PCB Layout Guidelines" on page 29 for connecting VSWH pads to electrically isolate the PCB copper island to dissipate internal heat.
14	VOUT	PWR	Power supply output. Range: 0.6V to 5V. Refer to the "Derating Curves" on page 17 for maximum recommended output current at various output voltages.
15, 27, 40	SGND	PWR	Controller signal ground. Refer to "PCB Layout Guidelines" on page 29 for the SGND pad connections.
16	VDD	PWR	Input supply to digital controller. Connect VDD pad to VIN supply.
17	EN	I	External enable input. Logic high enables the module.
18	SCL	I/O	Serial clock input. A pull-up resistor is required for this application.
19	SDA	I/O	Serial data. A pull-up resistor is required for this application.
20	SALRT	O	Serial alert. A pull-up resistor is required for this application.
21	SA	I	Serial bus address select pin. Refer to Table 11 on page 25 for list of resistor values to set various serial bus address.
24	CFG	I	Clock source configuration. If the clock source is set to internal, the internal FREQUENCY_SWITCH needs to be set according to SYNC pin resistor setting. If the clock source is external, the internal FREQUENCY_SWITCH is set according to the CFG pin resistor, see Table 8 on page 23.
25	VSET	I	Output voltage selection pin. Refer to Table 5 on page 19 for list of resistor values to set various output voltages.
28	PG	O	Power-good output configured as an open drain.
29	SS/UVLO	I	Soft-start/stop and undervoltage lockout selection pin. Used to set turn on/off delay and ramp time in addition to input UVLO threshold levels. Refer to Table 6 on page 21 and Table 10 on page 24 for list of resistors.
30	PHASE	PWR	Switch node pad for DCR sensing. Electrically shorted inside to VSWH, but for higher current sensing accuracy connect PHASE pad to VSWH pad externally. Refer to "PCB Layout Guidelines" on page 29.
35	VR6	PWR	6V Internal reference supply voltage.
36	VR5	PWR	5V Internal reference supply voltage.
37	VDDC	PWR	VDD Clean. Noise at the VDD pin is filtered by an internal ferrite bead and capacitor. For VDD > 6V, leave this pin as no connect. For 5.5 ≤ VDD ≤ 6V, connect the VDDC pin to the VR6 pin. For 4.5 ≤ VDD < 5.5V, connect the VDDC pin to the VR6 and VR5 pin.
38	V25	PWR	2.5V Internal reference supply voltage.
39	SYNC	I/O	Clock synchronization input. Used to set the frequency of the internal switch clock or to sync to an external clock. If using external synchronization, the external clock must be active before enable. Refer to Table 7 on page 22 for list of resistor values to program various switching frequencies.
41	VR55	PWR	Internal 5.5V bias for internal regulator use only. Connect VR55 pin directly to VCC pin. Not recommended to power external circuit.
1, 3, 4, 5, 22, 26, 32, 33	NC		These are test pins and are not electrically isolated. Leave these pins as no connect.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Supply Voltage, VIN Pin	-0.3	17	V
Input Supply Voltage for Controller, VDD, VDDC Pin	-0.3	17	V
Input Gate Driver Supply Voltage, VDRVIN Pin	-0.3	17	V
Output Voltage, VOUT Pin	-0.3	6	V
Output Gate Driver Supply Voltage, VDRVOUT Pin	-0.3	6	V
Switch Node Referenced to PGND Pin, VSWH Pin	-0.3	25	V
Switch Node for DCR Sensing Referenced to SGND Pin, PHASE Pin	-0.3	25	V
Input Bias Voltage for internal Regulator, VCC Pin	-0.3	6.5	V
6V Internal Reference Supply Voltage, VR6 Pin	-0.3	6.6	V
Internal Reference Supply Voltage, V_{R5}, VR55 Pin	-0.3	6.5	V
2.5V Internal Reference Supply Voltage, V25 Pin	-0.3	3	V
Logic I/O Voltage for EN, PG, ASCR, SA, SCL, SDA, SALRT, SYNC, SS/UVLO, V_{SET}	-0.3	6.0	V
Analog Input Voltages			
VSEN+, XTEMP+	-0.3	6.0	V
VSEN-, XTEMP-	-0.3	0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
41 Ld HDA Package (Notes 13, 14)	7.5	2.2

Notes:

13. θ_{JA} is measured in free air with the module mounted on an evaluation board 3x4.5 inch in size with 2oz surface and 2oz buried planes and multiple via interconnects as specified the RTKA2108252H00000BU Evaluation Board User Guide on the RAA210825 product page.
14. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+125	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	Refer to Figure 29		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{IN}	4.5	14	V
Input Supply Voltage Range for Controller, V_{DD}	4.5	14	V
Output Voltage Range, V_{OUT}	0.6	5	V
Output Current Range, $I_{OUT(DC)}$ (Note 17)	0	25	A
Operating Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

V_{IN} = V_{DD} = 12V, f_{SW} = 533kHz, C_{OUT} = 1340µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +85°C.

Parameter	Symbol	Test Conditions	Min (Note 15)	Typ	Max (Note 15)	Unit
Input and Supply Characteristics						
Input Supply Current for Controller	I_{DD}	V_{IN} = V_{DD} = 12V, V_{OUT} = 0V, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
Internal Regulator Output Voltage	VDRVOUT	V_{CC} connected to VR_{55}		5.2		V
5V Internal Reference Supply Voltage	V_{R5}	I_{VR5} < 5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply Voltage	V_{25}		**2.25**	2.50	**2.75**	V
5.5V Internal Reference Supply Voltage	V_{R55}	V_{DD} > 6V; 0 - 80mA		5.7		V
Input Supply Voltage for Controller Readback Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Readback Total Error (Note 18)	$V_{DD\_READ\_ERR}$	PMBus read		±2		%FS
Output Characteristics						
Output Voltage Adjustment Range	V_{OUT_RANGE}	V_{IN} > V_{OUT} + 1.8V	**0.54**		**5.50**	V
Output Voltage Set-Point Range	V_{OUT_RES}			±0.025		%
Output Voltage Set-Point Accuracy (Notes 16, 18)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ TA ≤ +85°C)	**-1.2**		**+1.2**	$\%V_{OUT}$
Output Voltage Readback Resolution	$V_{OUT\_READ\_RES}$			±20		mV
Output Voltage Readback Total Error (Note 18)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**+2**	$\%V_{OUT}$
Output Current Readback Resolution	$I_{OUT\_READ\_RES}$			10		Bits
Output Current Range (Note 17)	I_{OUT_RANGE}				**25**	A
Output Current Readback Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load at ambient room temperature		±3		A

V_{IN} = V_{DD} = 12V, f_{SW} = 533kHz, C_{OUT} = 1340µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)

Parameter	Symbol	Test Conditions	Min (Note 15)	Typ	Max (Note 15)	Unit
Soft-Start and Sequencing						
Delay Time From Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using pin-strap resistor or PMBus	**2**		**300**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using pin-strap resistor or PMBus	**0.5**		**120**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs
Delay Time From Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using pin-strap resistor or PMBus	**2**		**300**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms
Output Voltage Fall Time	t_{OFF_FALL}	Configured using pin-strap resistor or PMBus	**0.5**		**120**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
Power-Good						
Power-Good Delay	V_{PG_DELAY}			4		ms
Temperature Sense						
Temperature Sense Range	T_{SENSE_RANGE}	Configured using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	**-5**		**+5**	°C
Fault Protection						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 18)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using pin-strap resistor or PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using pin-strap resistor or PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 16)	V_{OUT_OV/UV_ACCY}		**-2**		**+2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 18)	I_{LIMIT_ACCY}	Tested at I_{OUT}_OC_FAULT_LIMIT = 30A		±10		%FS
Output Current Fault Response Time (Note 19)	I_{LIMIT_DELAY}	Factory default		5		t_{SW}
Over-temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		+115		°C
		Configured using PMBus	**-40**		**+125**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			+15		°C

V_{IN} = V_{DD} = 12V, f_{SW} = 533kHz, C_{OUT} = 1340µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)

Parameter	Symbol	Test Conditions	Min (Note 15)	Typ	Max (Note 15)	Unit
Oscillator and Switching Characteristics						
Switching Frequency Range	f_{SW_RANGE}	Configured using pin-strap resistor or PMBus	**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**+5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC clock equal to 500kHz is not supported	**-10**		**+10**	%
Logic Input/Output Characteristics						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	EN, CFG, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V_{SET}	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus Interface Timing Characteristic						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

Notes:
15. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design.
16. V_{OUT} measured at the termination of the V_{SEN+} and V_{SEN-} sense points.
17. The MAX load current is determined by the thermal "Derating Curves" on page 17.
18. "FS" stand for full scale of recommended maximum operation range.
19. "t_{SW}" stands for time period of operation switching frequency.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating conditions: T_A = +25°C, no air flow. C_{OUT} = 1340µF. Typical values are used unless otherwise noted.

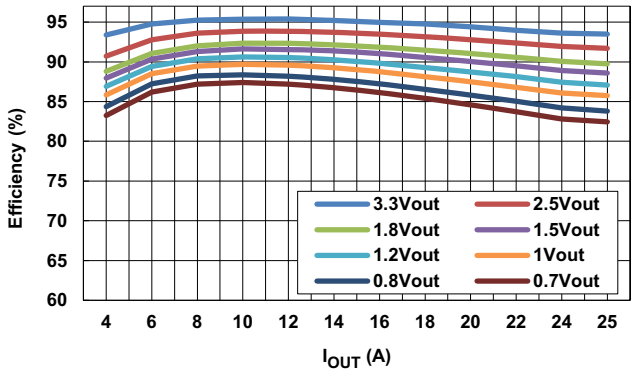


Figure 5. Efficiency vs Output Current at V_{IN} = 5V, f_{SW} = 364kHz for Various Output Voltages

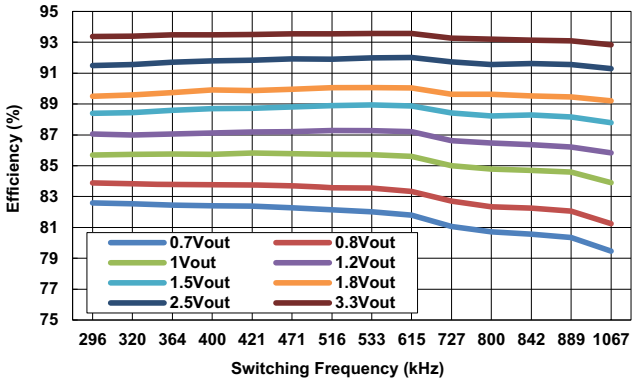


Figure 6. Efficiency vs Switching Frequency at V_{IN} = 5V, I_{OUT} = 25A for Various Output Voltages

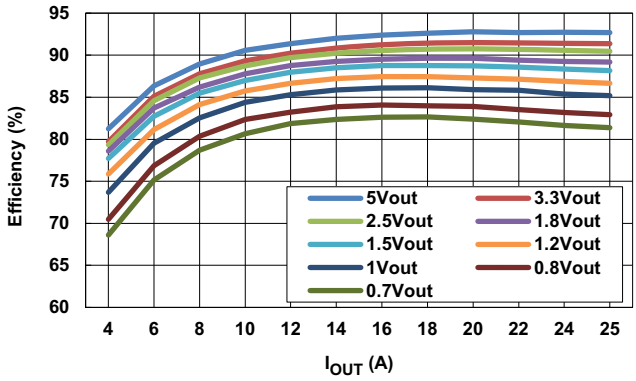


Figure 7. Efficiency vs Output Current at V_{IN} = 12V, f_{SW} = 364kHz for Various Output Voltages

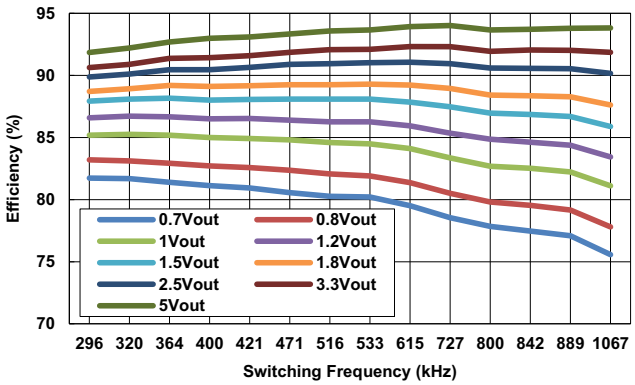


Figure 8. Efficiency vs Switching Frequency at V_{IN} = 12V, I_{OUT} = 25A for Various Output Voltages

3.2 Transient Response Performance

Operating conditions: Step load 0A to 12.5A, I_{OUT} slew rate = 15A/µs, T_A = +25°C, OLFM airflow. Typical values used unless otherwise noted.

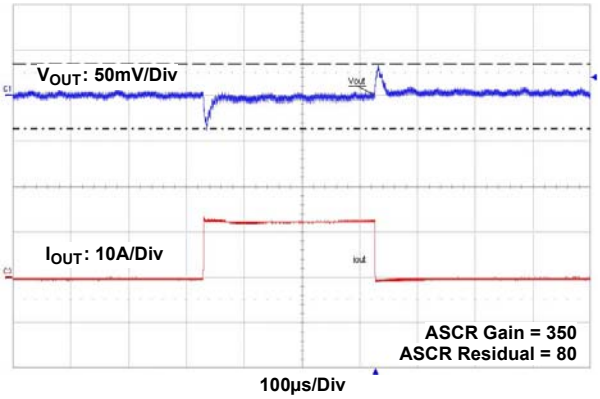


Figure 9. $5V_{IN}$ to $0.9V_{OUT}$ Transient Response, f_{SW} = 364kHz, C_{OUT} = 12x100µF Ceramic + 4x470µF POSCAP

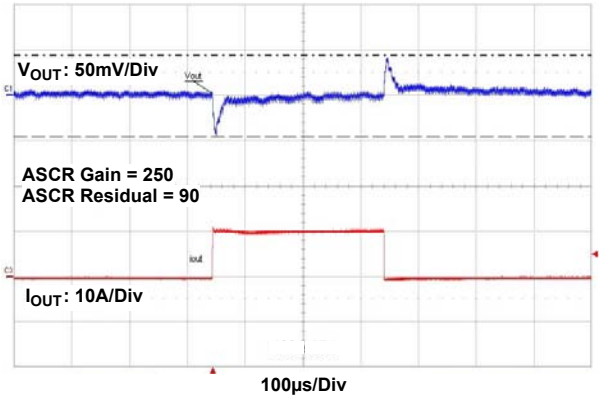


Figure 10. $5V_{IN}$ to $1.8V_{OUT}$ Transient Response, f_{SW} = 615kHz, C_{OUT} = 3x100µF Ceramic + 2x470µF POSCAP

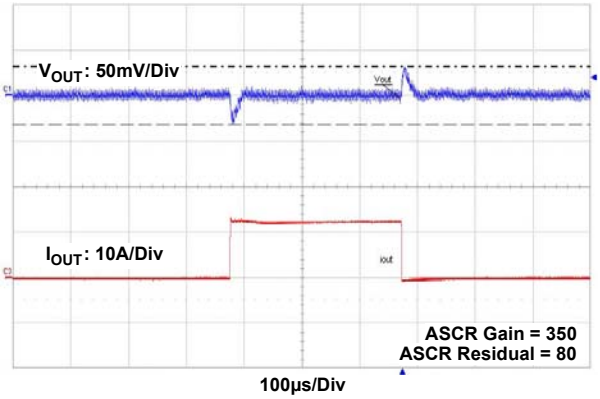


Figure 11. $12V_{IN}$ to $0.8V_{OUT}$ Transient Response, f_{SW} = 296kHz, C_{OUT} = 12x100µF Ceramic + 5x470µF POSCAP

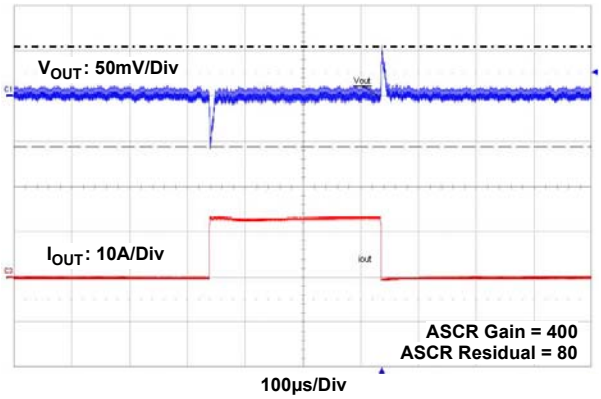


Figure 12. $12V_{IN}$ to $1.5V_{OUT}$ Transient Response, f_{SW} = 727kHz, C_{OUT} = 4x100µF Ceramic + 2x470µF POSCAP

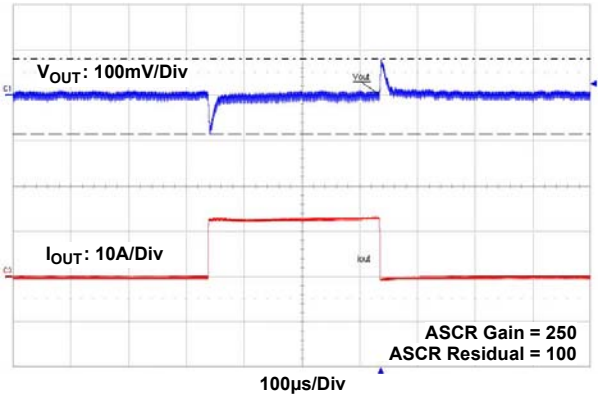


Figure 13. $12V_{IN}$ to $2.5V_{OUT}$ Transient Response, f_{SW} = 615kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

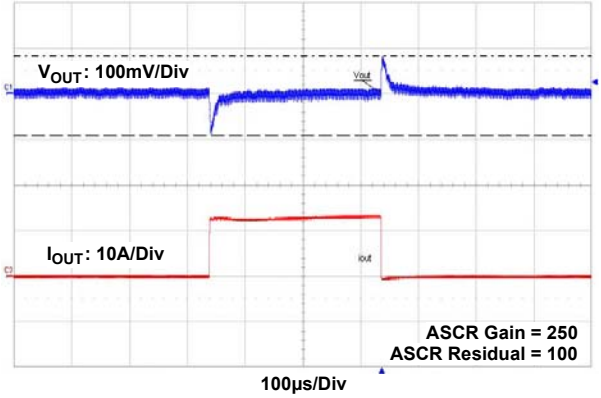


Figure 14. $12V_{IN}$ to $3.3V_{OUT}$ Transient Response, f_{SW} = 615kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

3.3 Derating Curves

All of the following curves were plotted at T_J = +120°C

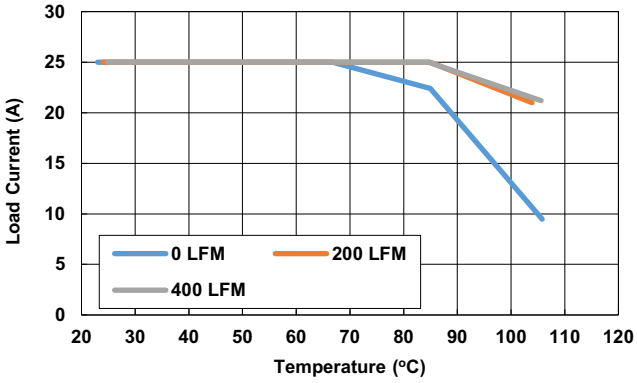


Figure 15. $5V_{IN}$ to $1V_{OUT}$, 364kHz

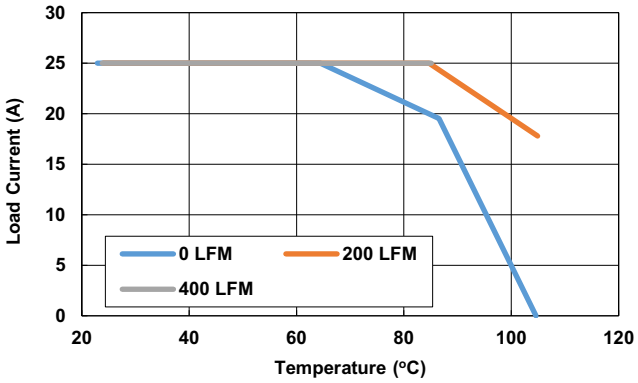


Figure 16. $12V_{IN}$ to $1V_{OUT}$, 364kHz

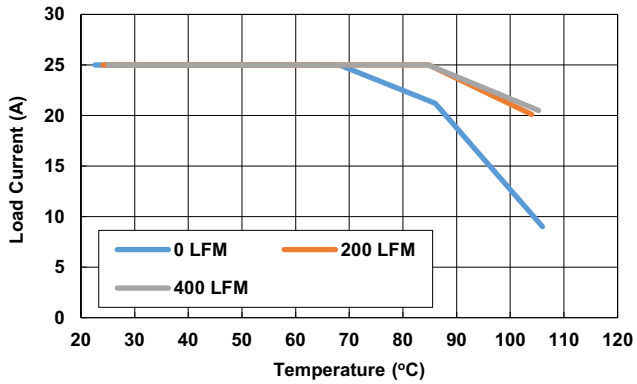


Figure 17. $5V_{IN}$ to $1.2V_{OUT}$, 364kHz

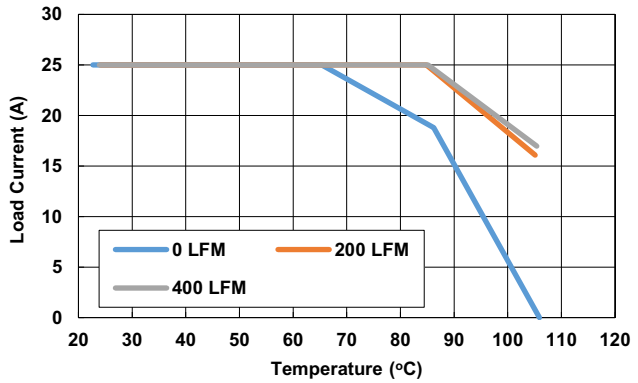


Figure 18. $12V_{IN}$ to $1.2V_{OUT}$, 364kHz

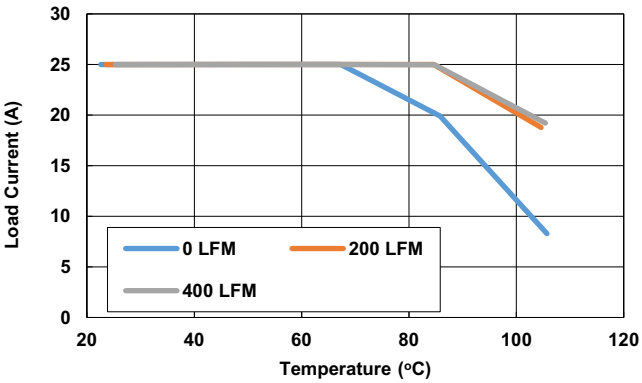


Figure 19. $5V_{IN}$ to $1.8V_{OUT}$, 471kHz

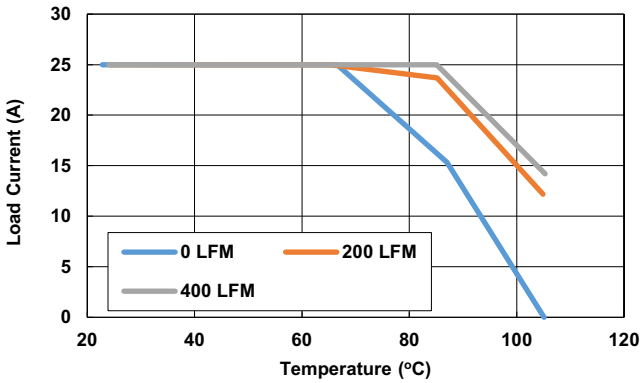


Figure 20. $12V_{IN}$ to $1.8V_{OUT}$, 471kHz

All of the following curves were plotted at T_J = +120°C **(Continued)**

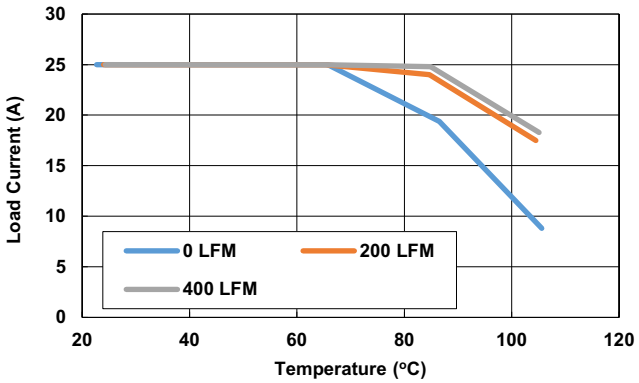


Figure 21. $5V_{IN}$ to $2.5V_{OUT}$, 615kHz

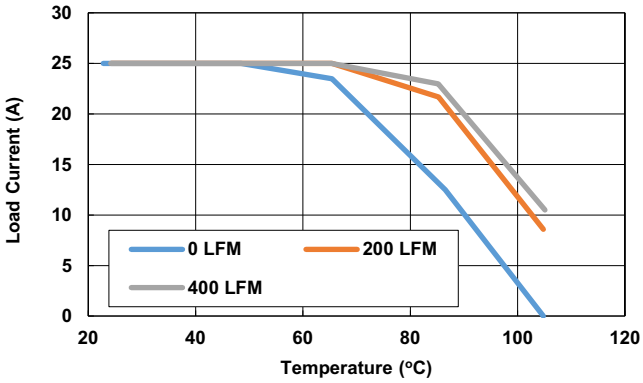


Figure 22. $12V_{IN}$ to $2.5V_{OUT}$, 615kHz

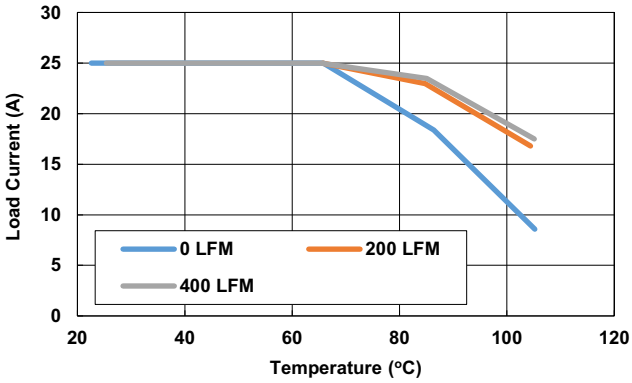


Figure 23. $5V_{IN}$ to $3.3V_{OUT}$, 615kHz

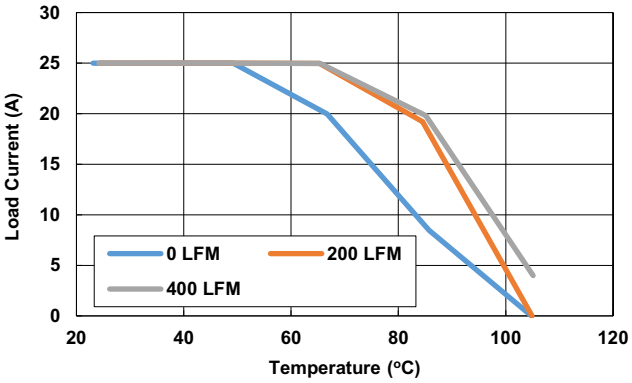


Figure 24. $12V_{IN}$ to $3.3V_{OUT}$, 615kHz

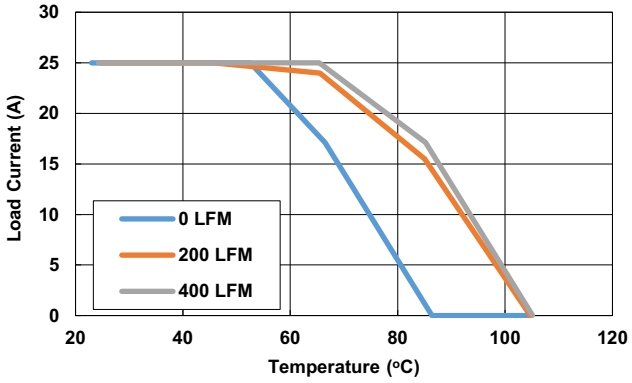


Figure 25. $12V_{IN}$ to $5V_{OUT}$, 727kHz

4. Functional Description

4.1 SMBus Communications

The RAA210825 provides an SMBus digital interface that enables the user to configure the module operation in addition to monitoring the input and output parameters. The RAA210825 can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I & II version 1.2. The RAA210825 accepts most standard PMBus commands. Renesas recommends tying the enable pin to SGND when PMBus commands are issued.

The SMBus device address is the only parameter that must be set by external pins.

4.2 Output Voltage Selection

The output voltage may be set to a voltage between 0.6V and 5V provided that the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET pin sets the output voltage to any values between 0.6V and 5V, as shown in Table 5. The R_{SET} resistor is placed between the VSET pin and SGND. A standard 1% resistor is recommended.

Table 5. Output Voltage Resistor Settings

V_{OUT} (V)	VSET_GROUP (set by SA pin)	R_{SET} (kΩ)
0.600	Group 0	10
0.650	Group 0	11
0.675	Group 0	12.1
0.690	Group 0	13.3
0.700	Group 0	14.7
0.710	Group 0	16.2
0.720	Group 0	17.8
0.730	Group 0	19.6
0.740	Group 0	21.5
0.750	Group 0	23.7
0.760	Group 0	26.1
0.770	Group 0	28.7
0.780	Group 0	31.6
0.790	Group 0	34.8
0.800	Group 0	38.3
0.810	Group 0	42.2
0.820	Group 0	46.4
0.830	Group 0	51.1
0.840	Group 0	56.2
0.850	Group 0	61.9
0.860	Group 0	68.1
0.870	Group 0	75
0.880	Group 0	82.5
0.890	Group 0	90.9
0.900	Group 0	100
0.910	Group 0	110
0.920	Group 0	121
0.930	Group 0	133

Table 5. Output Voltage Resistor Settings (Continued)

V_{OUT} (V)	VSET_GROUP (set by SA pin)	R_{SET} (kΩ)
0.940	Group 0	147
0.950	Group 0	162
0.960	Group 0	178
0.970	Group 0	Connect to SGND
0.980	Group 0	OPEN
0.990	Group 0	Connect to V25
1.000	Group 1	Connect to SGND
1.030	Group 1	10
1.050	Group 1	11
1.100	Group 1	12.1
1.120	Group 1	13.3
1.150	Group 1	14.7
1.200	Group 1	OPEN
1.250	Group 1	16.2
1.300	Group 1	17.8
1.350	Group 1	19.6
1.400	Group 1	21.5
1.500	Group 1	23.7
1.600	Group 1	26.1
1.650	Group 1	28.7
1.700	Group 1	31.6
1.800	Group 1	34.8
1.850	Group 1	38.3
1.900	Group 1	42.2
2.000	Group 1	46.4
2.100	Group 1	51.1
2.200	Group 1	56.2
2.300	Group 1	61.9
2.400	Group 1	68.1
2.500	Group 1	Connect to V25
2.600	Group 1	75
2.700	Group 1	82.5
2.800	Group 1	90.9
2.900	Group 1	100
3.000	Group 1	110
3.200	Group 1	121
3.300	Group 1	133
3.400	Group 1	147
3.600	Group 1	162
5.000	Group 1	178

By default, V_{OUT_MAX} is set 110% higher than V_{OUT} by the pin-strap resistor, which can be changed to any value up to 5.5V with PMBus Command VOUT_MAX.

4.3 Soft-Start Delay and Ramp Times

The RAA210825 follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. When this process is complete, the device is ready to accept commands from the PMBus interface and the module is ready to be enabled. If the module is synchronizing to an external clock source, the clock frequency must be stable prior to asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The RAA210825 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay (TON_DELAY) and ramp-up time (TON_RISE) can be set to custom values with pin-strap resistors or PMBus. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. In general, set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay (TOFF_DELAY) and ramp-down time (TOFF_FALL) for soft-stop/off can be set to custom values with pin-strap resistors or PMBus. In addition, the module can be configured as “immediate off” with the command ON_OFF_CONFIG, such that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/UVLO pin can program the soft-start/stop delay time and ramp time to some typical values as shown in Table 6. A standard 1% resistor is required.

Table 6. Soft-Start/Stop Resistor Settings

Resistor (kΩ)	Delay Time (ms)	Ramp Time (ms)
Open	5	5
Connect to V25	10	10
Connect to SGND	5	2
12.1	5	2
13.3	5	5
14.7	5	10
16.2	10	2
17.8	10	5
19.6	10	10
21.5	20	5
23.7	20	10
26.1	5	2
28.7	5	5
31.6	5	10
34.8	10	2
38.3	10	5
42.2	10	10
46.4	20	5
51.1	20	10
56.2	5	2

Table 6. Soft-Start/Stop Resistor Settings (Continued)

Resistor (kΩ)	Delay Time (ms)	Ramp Time (ms)
61.9	5	5
68.1	5	10
75	10	2
82.5	10	5
90.9	10	10
100	20	5
110	20	10

4.4 Power-Good

The RAA210825 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the polarity of the pin may be changed with PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the RAA210825 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A fixed PG delay of 4ms is programmed for RAA210825.

4.5 Switching Frequency and PLL

The device's switching frequency is configurable from 296kHz to 1067kHz using the pin-strap method as shown in Table 7, or by using a PMBus command FREQUENCY_SWITCH.

Table 7. Switching Frequency Resistor Settings

f_{SW} (kHz)	R_{SET} (kΩ)
296	14.7, or connect to SGND
320	16.2
348	17.8
364	19.6
400	21.5
421	23.7
471	26.1
516	28.7
533	31.6, or OPEN
615	34.8
640	38.3
696	42.2
727	46.4
800	51.1
842	56.2
889	61.9
1067	68.1, or connect to V25

The RAA210825 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can also be driven by an external clock source connected to the SYNC pin. Set this configuration by connecting a resistor to the CFG pin. If the clock source is internal, the internal frequency is set according to the SYNC pin resistor settings. If the clock source is external, the internal frequency is set according to the resistor connected to the CFG pin as shown in Table 8. The incoming clock signal must be stable when the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.
Note: If the pin-strap method is used, a standard 1% resistor is required.

Table 8. External Frequency Sync Settings

Clock Source	Internal FREQUENCY_SWITCH (kHz)	R_{SET} (kΩ)
Internal	Determined by SYNC resistor	10, or OPEN
External	296	11
External	340	12.1
External	390	13.3
External	444	14.7
External	516	16.2, or connect to SGND
External	593	17.8
External	696	19.6
External	800	21.5
External	941	23.7
External	1067	26.1, or Connect to V25

4.6 Loop Compensation

The module loop response is programmable using the pin-strap method or the PMBus command ASCR_CONFIG according to Table 9. A standard 1% resistor is required. The RAA210825 uses the ChargeMode control algorithm that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

Table 9. ASCR Resistor Settings

ASCR Gain	ASCR Residual	R_{SET} (kΩ)
80	70	10
120	70	Connect to SGND
200	70	OPEN
250	70	11
270	70	12.1
300	70	13.3
120	80	14.7
160	80	16.2
200	80	17.8
230	80	19.6
300	80	21.5
350	80	23.7
400	80	26.1
120	90	28.7
160	90	31.6
210	90	34.8

Table 9. ASCR Resistor Settings (Continued)

ASCR Gain	ASCR Residual	R_{SET} (kΩ)
230	90	38.3
250	90	42.2
270	90	46.4
300	90	51.1
350	90	56.2
380	90	61.9
400	90	68.1
500	90	75
600	90	82.5
120	100	90.9
160	100	100
200	100	110
250	100	Connect to V25
300	100	121
350	100	133
400	100	147
500	100	162
600	100	178

4.7 Input Undervoltage Lockout (UVLO)

The Input Undervoltage Lockout (UVLO) prevents the RAA210825 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V using the pin-strap method as shown in Table 10, or by using a PMBus command VIN_UV_FAULT_LIMIT. A standard 1% resistor is required.

The module shuts down immediately when the UVLO threshold is reached. The fault needs to be cleared for the module to restart.

Table 10. UVLO Resistor Settings

Resistor (kΩ)	UVLO (V)
Open	4.2
Connect to V25	4.5
Connect to SGND	4.5
12.1	4.5
13.3	4.5
14.7	4.5
16.2	4.5
17.8	4.5
19.6	4.5
21.5	4.5
23.7	4.5
26.1	4.2
28.7	4.59

Table 10. UVLO Resistor Settings (Continued)

Resistor (kΩ)	UVLO (V)
31.6	5.06
34.8	5.57
38.3	6.13
42.2	6.75
46.4	7.42
51.1	8.18
56.2	10.8
61.9	10.8
68.1	10.8
75	10.8
82.5	10.8
90.9	10.8
100	10.8
110	10.8

4.8 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 11 lists the available module addresses. This pin can also be used to make VSET_Group selection as shown in Table 11. A standard 1% resistor is required.

Table 11. SMBus Address and VSET Group Resistor Settings

R_{SET} (kΩ)	SMBus Address	VSET_GROUP
10	19h	Group 0
11	1Ah	Group 0
12.1	1Bh	Group 0
13.3	1Ch	Group 0
14.7	1Dh	Group 0
16.2	1Eh	Group 0
17.8	1Fh	Group 0
19.6	20h	Group 0
21.5	21h	Group 0
23.7	22h	Group 0
26.1	23h	Group 0
28.7	24h	Group 0
31.6	25h	Group 0
34.8	26h	Group 0
38.3	27h	Group 0
42.2	28h	Group 0
46.4	29h	Group 0
51.1	19h	Group 1
56.2	1Ah	Group 1

Table 11. SMBus Address and VSET Group Resistor Settings (Continued)

R_{SET} (kΩ)	SMBus Address	VSET_GROUP
61.9	1Bh	Group 1
68.1	1Ch	Group 1
75	1Dh	Group 1
82.5	1Eh	Group 1
90.9	1Fh	Group 1
100	20h	Group 1
110	21h	Group 1
121	22h	Group 1
133	23h	Group 1
147	24h	Group 1
162	25h	Group 1
Connect to SGND	26h	Group 1
178	27h	Group 1
OPEN	28h	Group 1

4.9 Output Overvoltage Protection

The RAA210825 has an internal output overvoltage protection circuit that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator compares the actual output voltage (seen at the V_{SEN+} and V_{SEN-} pins) to a threshold set to 15% higher than the target output voltage. The fault threshold can be programmed to a desired level with PMBus command VOUT_OV_FAULT_LIMIT. If the V_{SEN+} voltage exceeds this threshold, the module initiates an immediate shutdown without retry.

Internal to the module, a 332Ω resistor is populated from VOUT to VSEN+ to protect the device from overvoltage conditions in case of an open at VSENSE pin and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not sacrificed.

4.10 Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The RAA210825 provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage, however, the total time elapsed from when the delay period expires and when the output reaches its target value matches the preconfigured ramp time (see Figure 26 on page 27).

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

When the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage, and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition.

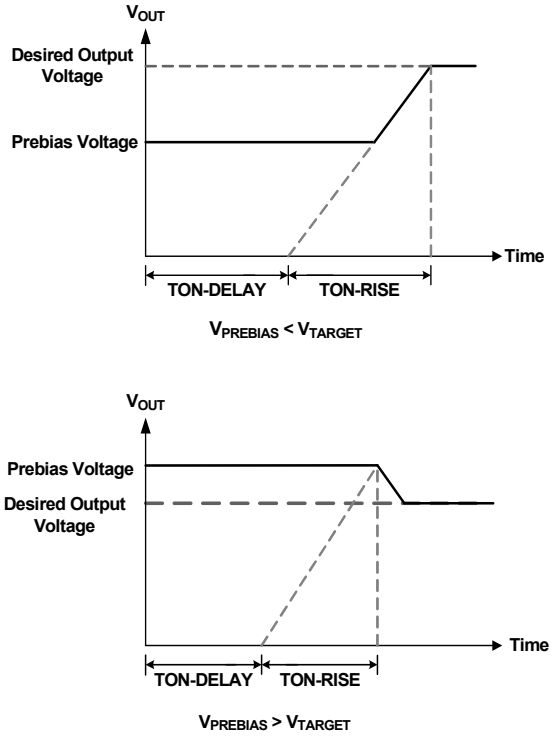


Figure 26. Output Responses to Prebias Voltages

4.11 Output Overcurrent Protection

The RAA210825 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Average output overcurrent fault threshold can be programmed with PMBus command IOUT_OC_FAULT_LIMIT. The module automatically programs the peak inductor current fault threshold by reading real-time input voltage, switching frequency, and VOUT_COMMAND to calculate the inductor ripple current.

The default response from an overcurrent fault is an immediate shutdown with a continuous retry of 70ms delay.

4.12 Thermal Overload Protection

The RAA210825 includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +115°C in the factory, but can be changed with PMBus command OT_FAULT_LIMIT.

The response from an over-temperature fault is an immediate shutdown without retry.

4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device, such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset between devices is determined from the lower four bits of the SMBus address of each interleaved device. The phase offset of each device can set to any value between 0° and 360° in 22.5° increments. This functionality can also be accessed using the PMBus command INTERLEAVE.

Table 12. INTERLEAVE Settings from SA

SA	SA in Binary	Low 4-Bits	INTERLEAVE	Phase Shift in Degrees
19h	00011001	1001	9	202.5
1Ah	00011010	1010	10	225
1Bh	00011011	1011	11	247.5
1Ch	00011100	1100	12	270
1Dh	00011101	1101	13	292.5
1Eh	00011110	1110	14	315
1Fh	00011111	1111	15	337.5
20h	00100000	0000	0	0
21h	00100001	0001	1	22.5
22h	00100010	0010	2	45
23h	00100011	0011	3	67.5
24h	00100100	0100	4	90
25h	00100101	0101	5	112.5
26h	00100110	0110	6	135
27h	00100111	0111	7	157.5
28h	00101000	1000	8	180
29h	00101001	1001	9	202.5

4.14 Monitoring Using SMBus

A system controller can monitor a wide variety of different RAA210825 system parameters using the following PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQUENCY
- MFR_READ_VMON

4.15 Snapshot Parameter Capture

The RAA210825 offers a special feature to capture parametric data and fault status following a fault event. A detailed description is provided in the "SNAPSHOT (EAh)" and "SNAPSHOT_CONTROL (F3h)" sections of the "PMBus Command Descriptions" on page 35.

5. PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

- For V_{DD} > 6V, the recommended PCB layout is shown in Figure 27. Leave V25, V_{DDC}, VR5, and VR6 as "No Connect (NC)".
- For 5.5V ≤ V_{DD} ≤ 6V, connect the VDDC pin to the VR6 pin. For 4.5 ≤ V_{DD} < 5.5V, connect the VDDC pin to the VR6 and VR5 pin. An RC filter is required at the input of the VDRVIN pin if input supply is shared with the VIN pin.
- Establish a separate SGND plane and PGND plane, then connect the SGND to the PGND plane as shown in Figure 28 in the middle layer. For making connections between SGND/PGND on the top layer and other layers, use multiple vias for each pin to connect to the inner SGND/PGND layer. Do not connect SGND directly to PGND on a top layer. Connecting SGND directly to PGND without establishing an SGND plane bypasses the decoupling capacitor at internal reference supplies, making the controller susceptible to noise.
- Place ceramic capacitors between VIN and PGND, VOUT and PGND, and the bypass capacitors between VDD and the ground plane, as close to the module as possible to minimize high frequency noise.
- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. Extra ceramic capacitors at VIN and VOUT can be placed on the bottom layer under VIN and VOUT pads when multiple vias are used for connecting copper pads on top and bottom layers.
- Connect differential remote-sensing traces to the regulation point to achieve a tight output voltage regulation. Route a trace from and V_{SEN+} to the point-of-load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENSE signal near VSWH pads.
- For noise sensitive applications, Renesas recommends that the user connect the VSWH pads only on the top layer; however, thermal performance is sacrificed. External airflow might be required to keep module heat at desired level. For applications where switching noise is less critical, an excellent thermal performance can be achieved in the RAA210825 module by increasing copper mass attached to VSWH pad. To increase copper mass on the VSWH node, create copper islands in the middle and bottom layers under the VSWH pad and connect them to the top layer with multiple vias. Make sure to shield those copper islands with a PGND layer to avoid any interference to noise sensitive signals.

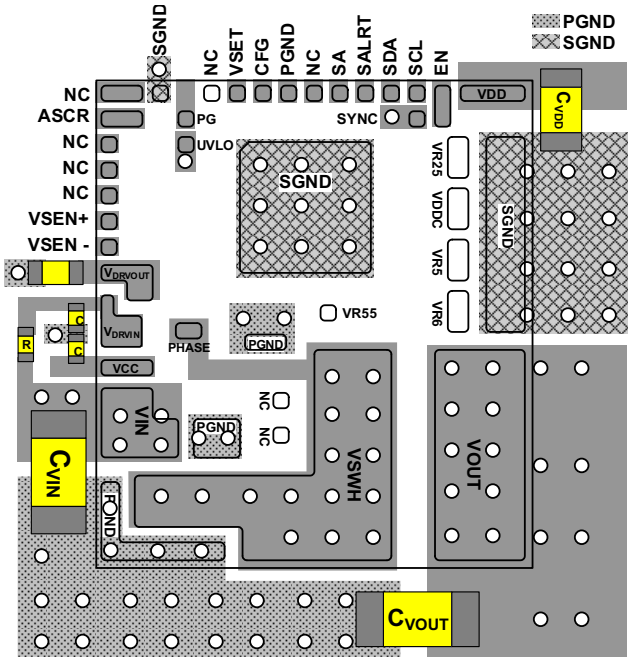


Figure 27. Recommended Layout - Top PCB Layer

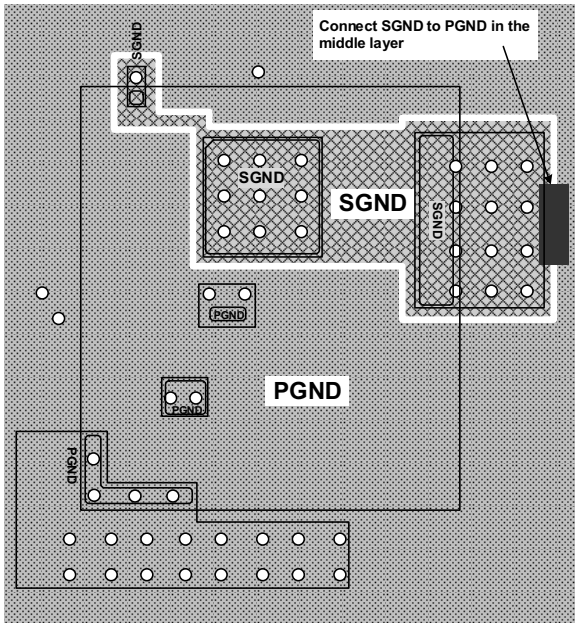


Figure 28. Recommended Layout - Connect SGND to PGND in the Middle PCB Layer After Establishing Separate SGND and PGND

5.1 Thermal Considerations

Experimental power loss curves, along with θ_{JA} from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, consider other heat sources and design margins.

5.2 Package Description

The RAA210825 uses the High Density Array (HDA) no-lead package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210825 contains several types of devices, including resistors, capacitors, inductors, and control ICs. The RAA210825 is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi-component assembly is overmolded with polymer mold compound to protect these devices.

The package outline, a typical PCB land pattern design, and a typical stencil opening edge position are shown in the "Package Outline Drawing" section starting on page 49. The module has a small size of 17mmx19mmx3.6mm. Figure 29 on page 31 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to their application.

5.3 PCB Layout Pattern Design

The bottom of the RAA210825 is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB land pattern is shown in the "Package Outline Drawing" section starting on page 49.

The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and that your board design rules allow.

5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints.

The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the "Package Outline Drawing" section starting on page 49.

Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

5.6 Reflow Parameters

Due to the low mount height of the HDA, a "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, thus it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 29 is provided as a guideline, to be customized for varying manufacturing practices and applications.

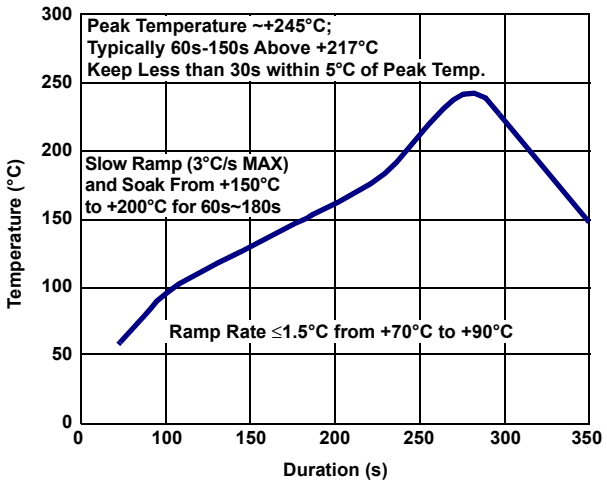


Figure 29. Typical Reflow Profile

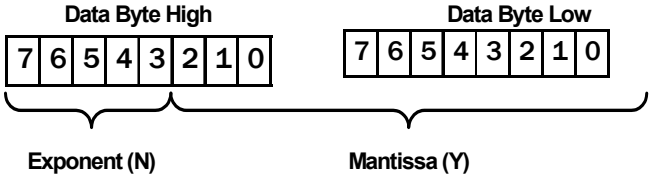
6. PMBus Command Summary

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Pg#
01h	OPERATION	Sets Enable, Disable	R/W Byte	BIT			35
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF.	R/W Byte	BIT	16h	Hardware Enable, Soft Off	35
03h	CLEAR_FAULTS	Clears fault indications.	Send Byte				35
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W Word	L16u		Pin-Strap	36
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W Word	L16u		1.1 x V_{OUT} Pin-Strap	36
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W Word	L11		Pin-Strap	36
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W Word	BIT		Set based on PMBus Address	36
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W Word	L16u		1.15 x V_{OUT} Pin-Strap	37
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W Word	L16u		0.85 x V_{OUT} Pin-Strap	37
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W Word	L11	DBC0h	30A	37
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W Word	L11	DC3Fh	-30A	37
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W Word	L11	EB98h	+115°C	38
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W Word	L11	E530h	-45°C	38
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W Word	L11	D3A0h	14.5V	38
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W Word	L11		Pin-Strap	38
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-good indication.	R/W Word	L16u		0.9 x V_{OUT} Pin-Strap	39
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W Word	L11		Pin-Strap	39
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W Word	L11		Pin-Strap	39
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W Word	L11		Pin-Strap	39
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W Word	L11		Pin-Strap	40
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	Read Byte	BIT	00h	No Faults	40
79h	STATUS_WORD	Returns information with a summary of the unit's fault condition.	Read Word	BIT	0000h	No Faults	41

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Pg#
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	Read Byte	BIT	00h	No Faults	41
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	Read Byte	BIT	00h	No Faults	42
7Ch	STATUS_INPUT	Returns specific status specific to the input.	Read Byte	BIT	00h	No Faults	42
7Dh	STATUS_TEMP	Returns the temperature specific status.	Read Byte	BIT	00h	No Faults	42
7Eh	STATUS_CML	Returns the communication, logic, and memory specific status.	Read Byte	BIT	00h	No Faults	43
80h	STATUS_MFR_SPECIFIC	Returns the VMON and external sync clock specific status.	Read Byte	BIT	00h	No Faults	43
88h	READ_VIN	Returns the input voltage reading.	Read Word	L11			44
8Bh	READ_VOUT	Returns the output voltage reading.	Read Word	L16u			44
8Ch	READ_IOUT	Returns the output current reading.	Read Word	L11			44
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	Read Word	L11			44
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	Read Word	L11			44
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	Read Word	L11			44
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W Block	CUS		Pin-Strap	45
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	Read Block	ASCII		Reads Device Version	45
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W Byte	BIT	B9h	Disable and Retry with 70ms delay	45
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W Byte	BIT	B9h	Disable and Retry with 70ms delay	46
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	Read Block	BIT			46
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W Byte	BIT			47
F5h	MFR_VMON_OV_FAULT_LIMIT	Returns the VMON overvoltage threshold.	Read Word	L11	CB00h	6V	47
F6h	MFR_VMON_UV_FAULT_LIMIT	Returns the VMON undervoltage threshold.	Read Word	L11	CA00h	4V	47
F7h	MFR_READ_VMON	Returns the VMON voltage reading. VMON is used to monitor VDRVOUT (Pin 8) voltage through an internal 16:1 resistor divider.	Read Word	L11			47

6.1 PMBus Data Formats

- **Linear-11 (L11)** - L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$



- **Linear-16 Unsigned (L16u)** - The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$
- **Linear-16 Signed (L16s)** - The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X).
  Relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$
- **Bit Field (BIT)** - An explanation of Bit Field is provided in PMBus on "PMBus Command Descriptions" on page 35.
- **Custom (CUS)** - An explanation of custom data format is provided in PMBus "PMBus Command Descriptions" on page 35. A combination of Bit Field and integer are common type of custom data format.
- **ASCII (ASC)** - A variable length string of text characters that uses the ASCII data format.

6.2 PMBus Use Guidelines

The PMBus is a powerful tool for configuring devices for circuit performance optimization. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, and ASCCR_CONFIG. Any command can be read while the device is enabled. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands may result in unexpected operation

7. PMBus Command Descriptions

OPERATION (01h)

Definition: Sets the Enable and Disable.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 40h

Units: N/A

Settings	Actions
00h	Immediate off
40h	Soft off
80h	On

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 16h (Device starts from ENABLE pin with soft off)

Units: N/A

Settings	Actions
00h	Device starts any time power is present regardless of the ENABLE pin or OPERATION command states.
16h	Device starts from the ENABLE pin with soft off.
17h	Device starts from the ENABLE pin with immediate off.
1Ah	Device starts from the OPERATION command.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

Data Length in Bytes: 0

Data Format: N/A

Type: Send only

Default Value: N/A

Units: N/A

Reference: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than either VOUT_MAX or 110% of the pin-strap V_{OUT} setting.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The command provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. The default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10 x V_{OUT} pin-strap setting

Units: Volts

Range: 0V to 5.5V

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command using PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 296kHz to 1067kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting of SA

Bits	Purpose	Value	Description
15:8	Reserved	0	Reserved
7:4	Group Number	0 to 15	Sets the number of rails in the group. A value of 0 is interpreted as 16
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15 x V_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85 x V_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. The device automatically calculates the peak inductor overcurrent fault limit.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: DBC0h (30A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} average undercurrent fault threshold. The device automatically calculates the valley inductor undercurrent fault limit.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: DC3Fh (-30A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_FAULT_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB98h (+115˚C)

Units: Celsius

Range: 0°C to +150°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above UT_FAULT_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: Celsius

Range: -55°C to +25°C

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0h (14.5V)

Units: V

Range: 0V to 16V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts after the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. Renesas recommends to set POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x V_{OUT} pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: CA80h (5ms)

Units: ms

Range: 2ms to 300ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: CA80h (5ms)

Units: ms

Range: 1ms to 120ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: CA80h (5ms)

Units: ms

Range: 2ms to 300ms

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: CA80h (5ms)

Units: ms

Range: 0ms to 120ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	IOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault occurred.
1	CML	A communications, memory, or logic fault occurred.
0	NONE OF THE ABOVE	A fault not listed in Bits 7:1 occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read only

Default Value: 0000h

Units: N/A

Bit Number	Status Bit Name	Meaning
15	VOUT	An output voltage fault occurred.
14	IOUT/POUT	An output current or output power fault occurred.
13	INPUT	An input voltage, input current, or input power fault occurred.
12	MFG_SPECIFIC	A manufacturer specific fault occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	Reserved	Reserved
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD was detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	IOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault occurred.
1	CML	A communications, memory, or logic fault occurred.
0	NONE OF THE ABOVE	A fault not listed in Bits 7:1 occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6:5	Reserved	Reserved
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault occurred.
6:5	Reserved	Reserved
4	IOUT_UC_FAULT	An output undercurrent fault occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns input voltage status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault occurred.
6:5	Reserved	Reserved
4	VIN_UV_FAULT	An input undervoltage fault occurred.
3:0	N/A	These bits are not used.

STATUS_TEMP (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault occurred.
6:5	Reserved	Reserved
4	UT_FAULT	An under-temperature fault occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Meaning
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4	Memory/logic fault was detected.
3:2	Reserved
1	A PMBus command tried to write to a Read only or protected command, or a communication fault other than the ones listed in this table occurred.
0	Reserved

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default value: 00h

Units: N/A

Bit Number	Field Name	Meaning
7:4	Reserved	Reserved
3	External Switching Period Fault	Loss of external clock synchronization occurred.
2	Reserved	Reserved
1	VMON UV Fault	The voltage on the VMON pin dropped below the level set by VMON_UV_FAULT.
0	VMON OV Fault	The voltage on the VMON pin rose above the level set by VMON_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read only

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: kHz

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain is analogous to bandwidth and ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

BIT	Purpose	Data Format	Value	Description
31:25	Not used		0000000h	Not used
24	Reserved			Reserved
23:16	ASCR Residual Setting	Integer		
15:0	ASCR Gain Setting	Integer		

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASCII

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and Continuous Retry with 70ms delay)

Units: N/A

Settings	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and Continuous Retry with 70ms delay)

Units: N/A

Settings	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay.

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, the most recently updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is stored, the device no longer automatically captures parametric and status values following a fault until stored data are erased. Use the SNAPSHOT_CONTROL command to erase stored data and clear the status bit before the next ramp up. Data erased is not allowed when the module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

Byte Number	Value	PMBus Command	FORMAT
31:23	Reserved	Reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	NVM Status Byte	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	Reserved	Reserved	
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Reserved	Reserved	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h causes the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h causes the device to write the current Snapshot values to NVRAM. Writing a 03h erases all Snapshot values from NVRAM. Write (02h) and Erase (03h) can only be used when the device is disabled. All other values are ignored.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W Byte

Value	Description
01h	Read Snapshot values from NVRAM.
02h	Write Snapshot values to NVRAM.
03h	Erase Snapshot values stored in NVRAM.

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VMON OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CB00h (6V)

Units: V

Range: 4V to 6V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VMON UV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CA00h (4V)

Units: V

Range: 4V to 6V

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage. VMON is used to monitor VDRVOUT (Pin 8) voltage through an internal 16:1 resistor divider.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: V

Range: 4V to 6V

8. Revision History

8.1 Firmware

Table 13. RAA210825 Nomenclature Guide

Firmware Revision Code	Change Description	Note
RAA210825--G0100	Initial Release	

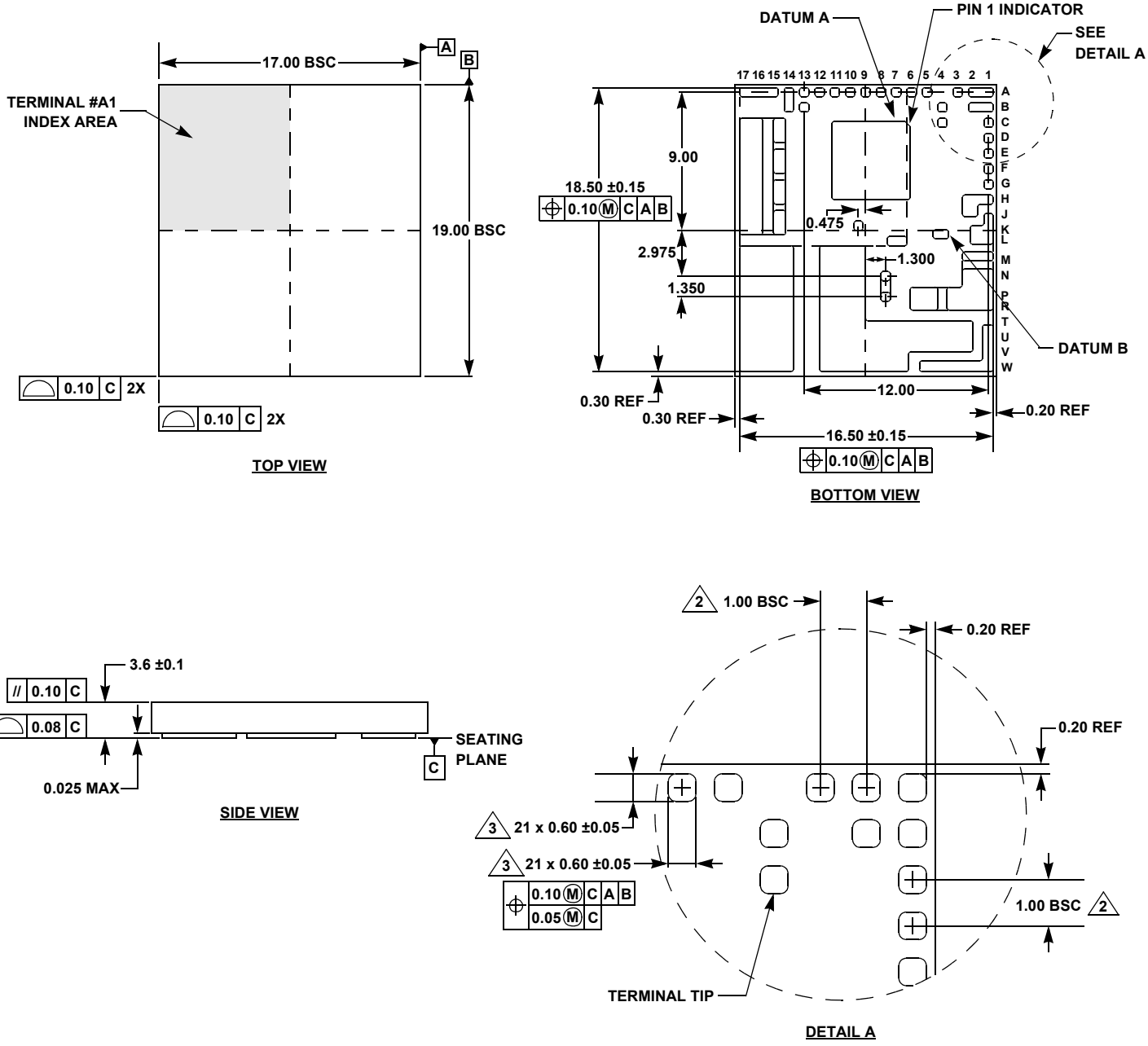
8.2 Datasheet

Rev.	Date	Description
1.01	Apr 23, 2020	Updated links throughout. Updated Figures 3 and 4.
1.00	Feb 8, 2019	Updated the PG pin description on page 10. Updated 80h action under OPERATION (01h) command on page 35.
0.00	Sep 12, 2018	Initial release

9. Package Outline Drawing

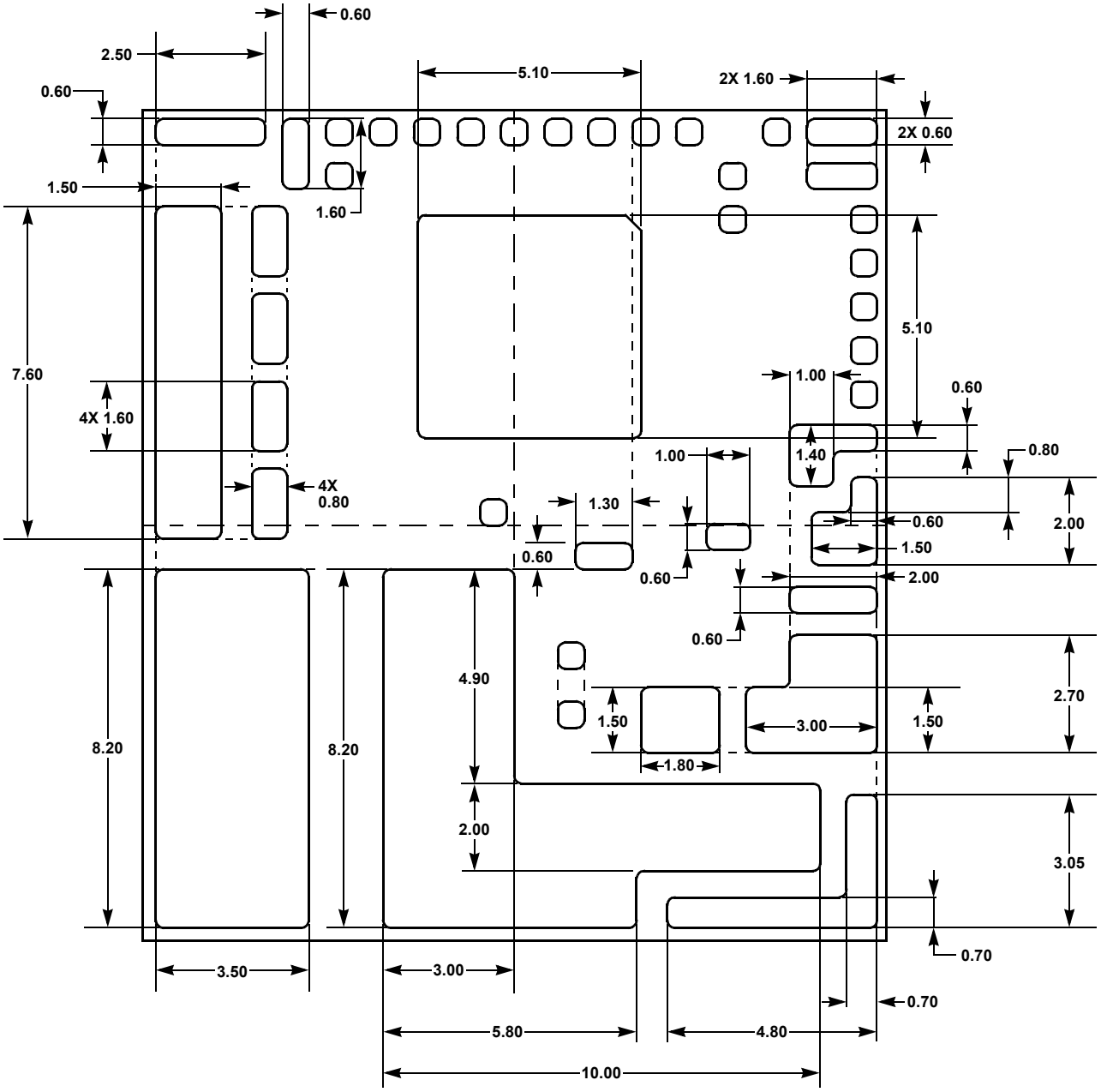
For the most recent package outline drawing, see Y41.17x19.

Y41.17x19
41 I/O 17.0mm x 19.0mmx3.6mm HDA Module
Rev 1, 5/16

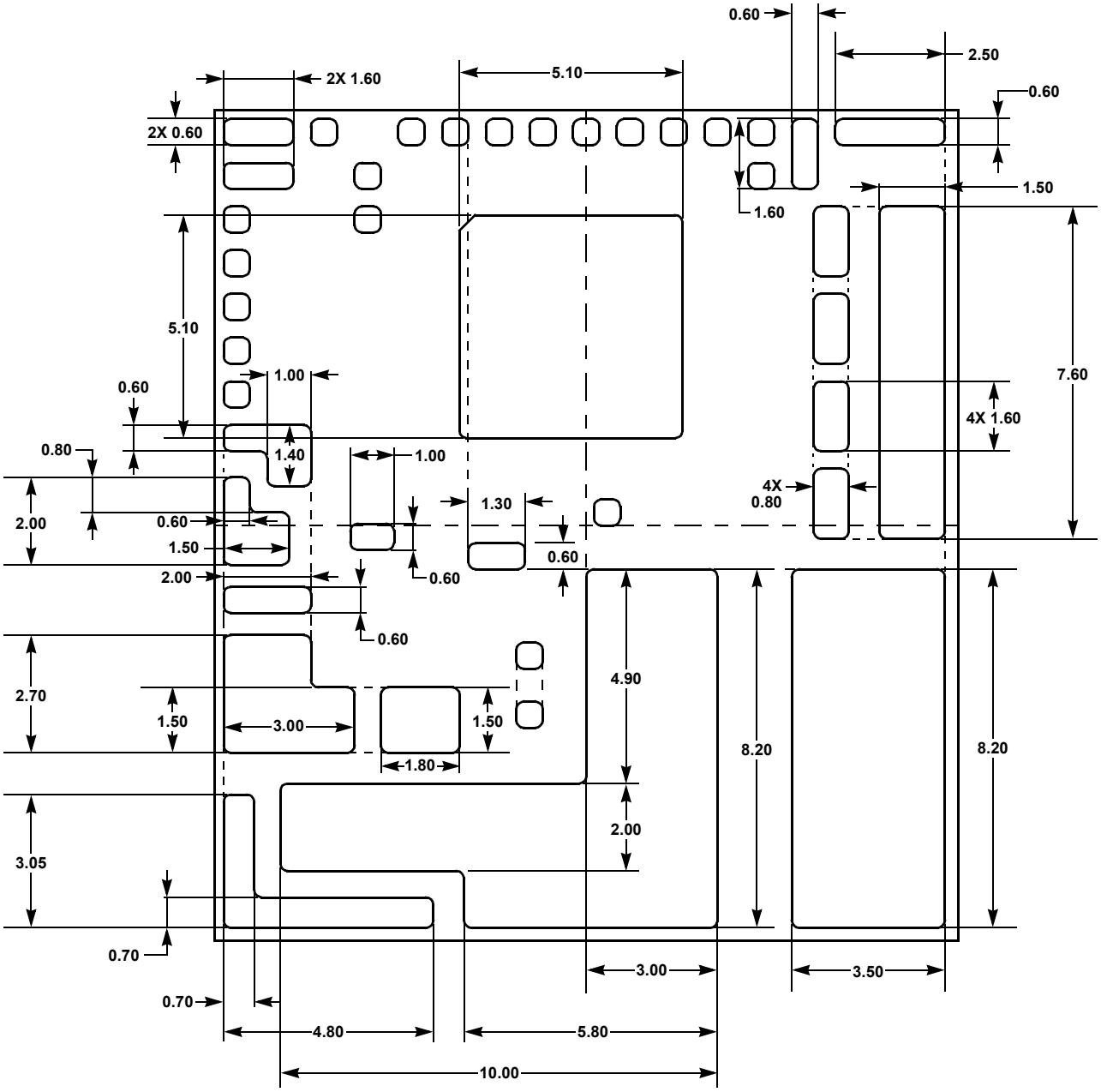


NOTES:

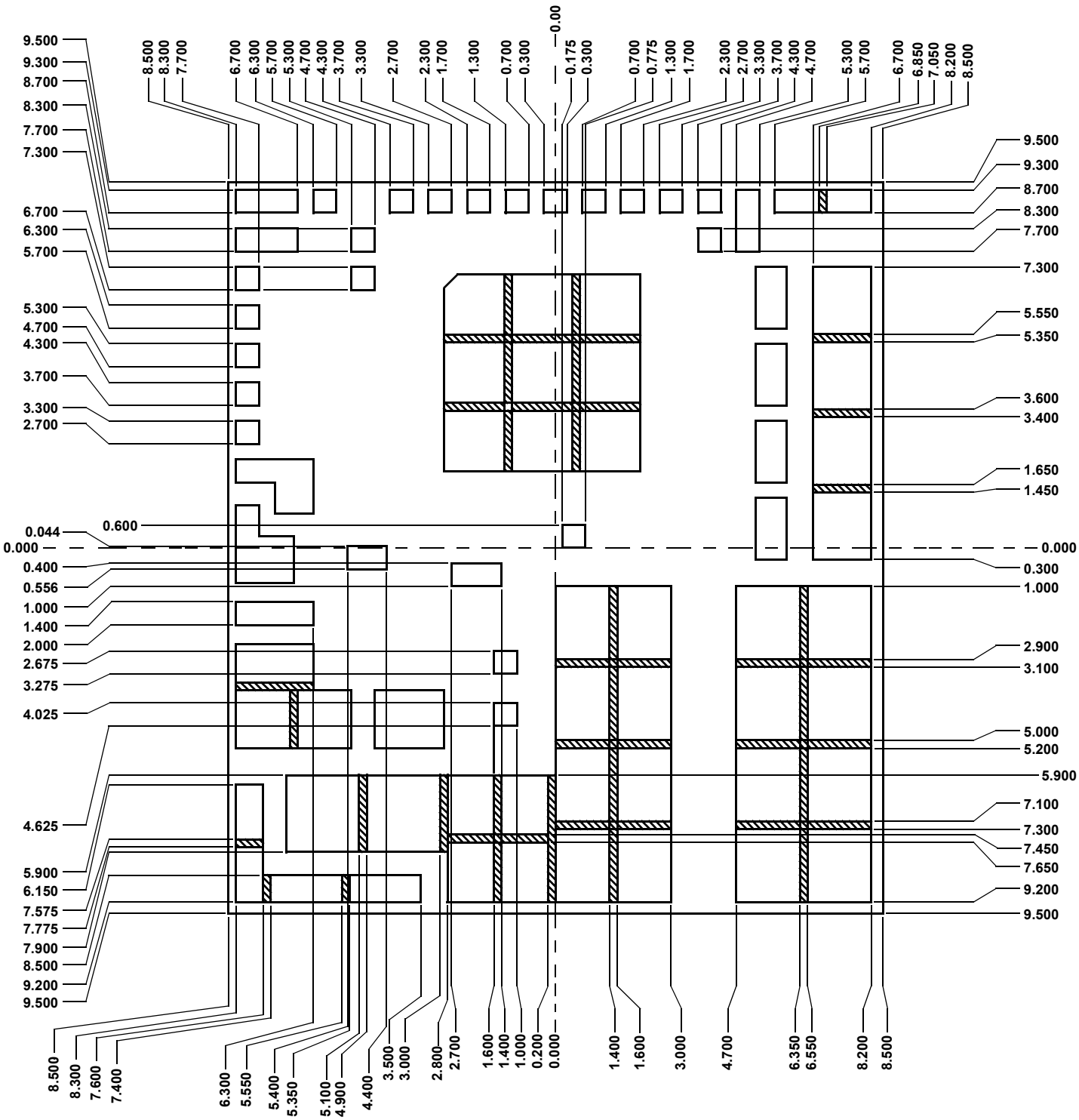
1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. The total number of I/O (excluding dummy pads).
4. Unless otherwise specified, tolerance: decimal ±0.10.
5. Dimensioning and tolerancing per ASME Y14.M-2009.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



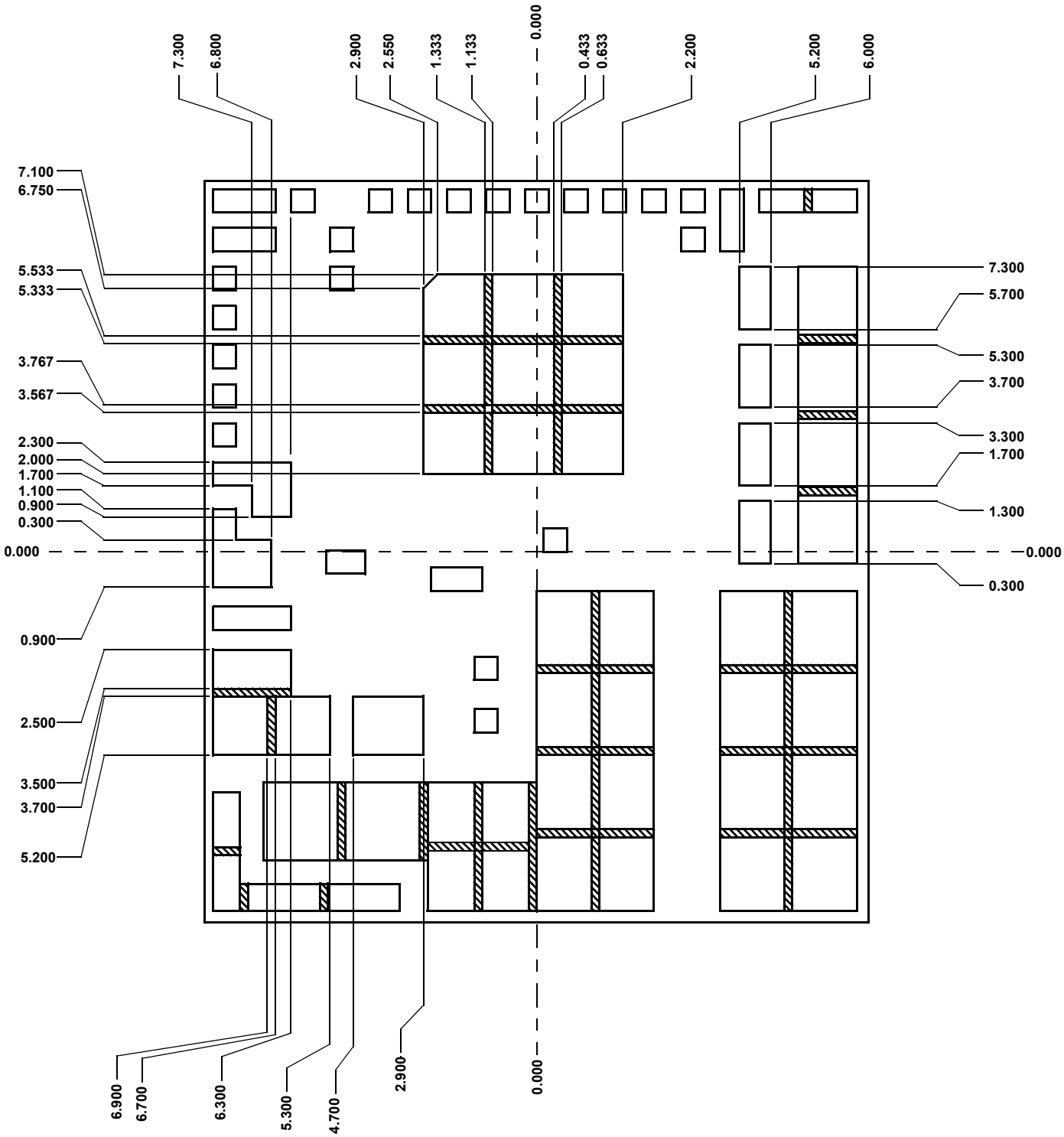
SIZE DETAILS FOR THE 16 EXPOSED DAPS
BOTTOM VIEW



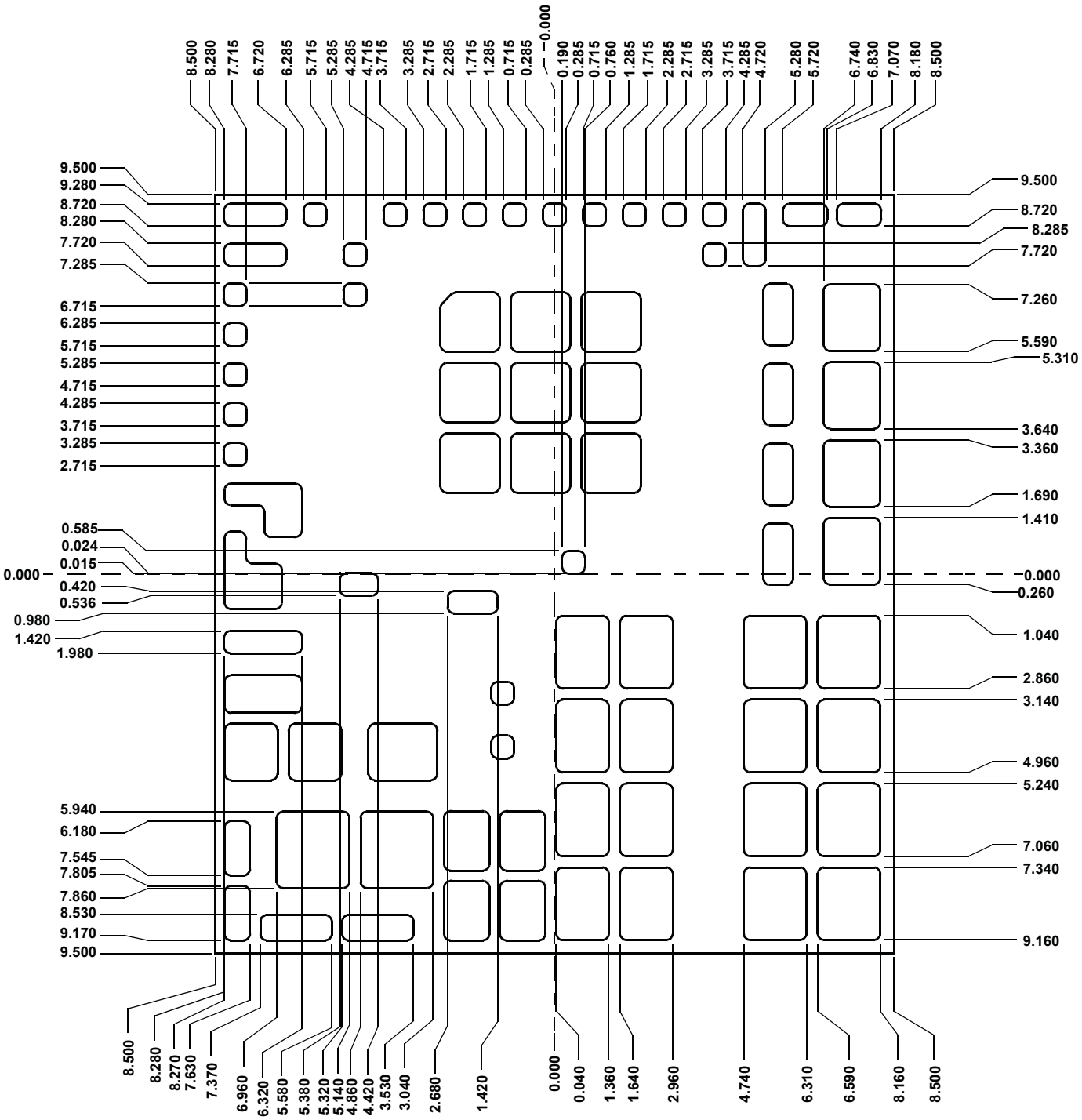
SIZE DETAILS FOR THE 16 EXPOSED DAPS
TOP VIEW



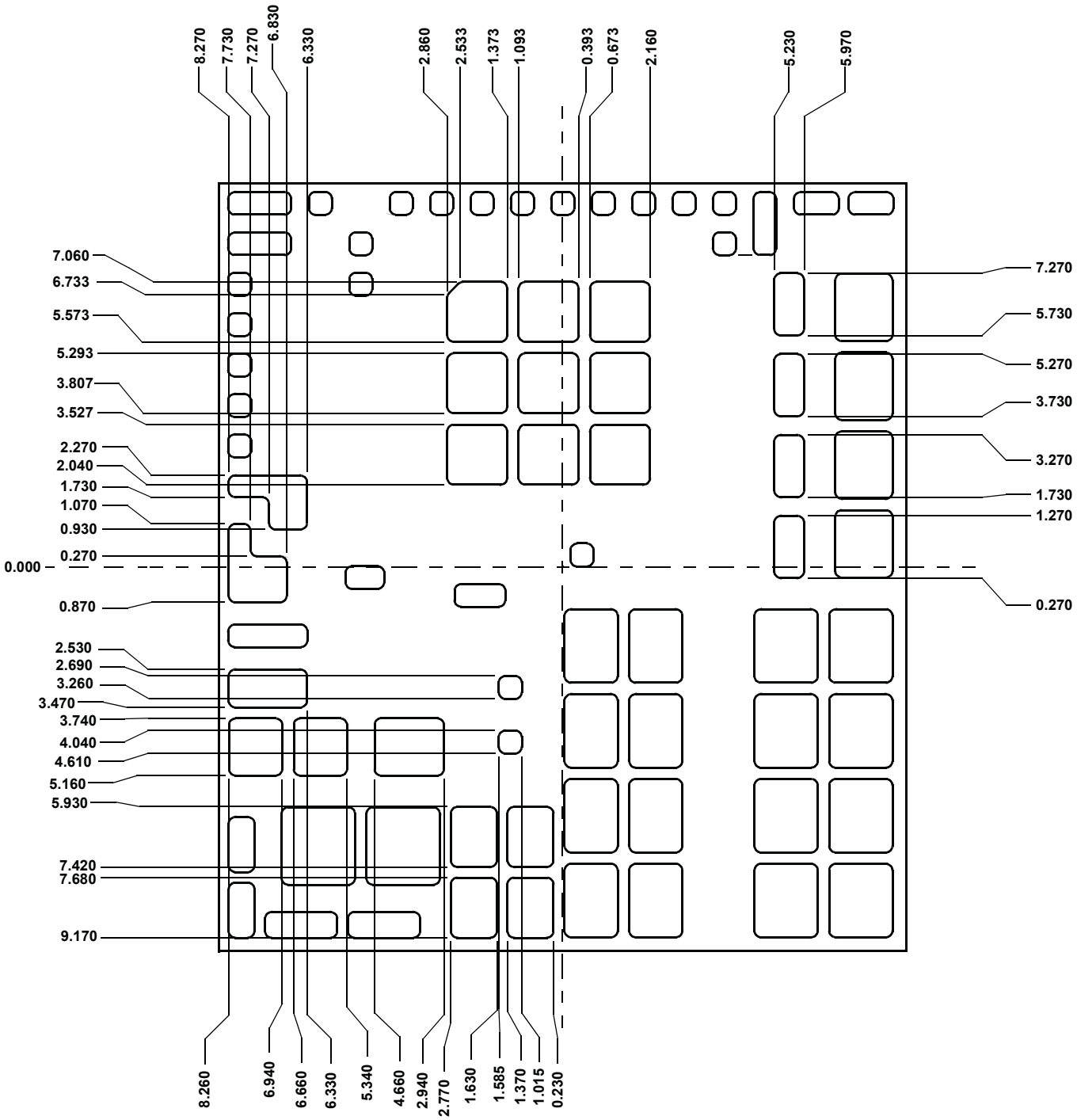
RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (1)
TOP VIEW



RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (2)
TOP VIEW



RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (1)
TOP VIEW



RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (2)
TOP VIEW

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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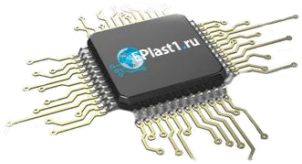
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.