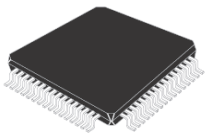
L99DZ81EP

Door actuator driver

Datasheet - production data



TQFP-64

Features

- One full bridge for 6 A load (R_{ON} = 150 mΩ)
- One half bridges for 3 A load (R_{ON} = 300 mΩ)
- One configurable high-side driver for up to 1.5 A (R_{ON} = 500 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- One configurable high-side driver for 0.7 A (R_{ON} = 800 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- Two high-side drivers for 0.5 A load (R_{ON} = 1600 mΩ)
- Programmable softstart function to drive loads with higher inrush currents as current limitation value
- Very low V_S current consumption in standby mode (I_S < 6 µA typ; $T_j \leq 85°C$)
- Current monitor output for all high-side drivers
- Central two-stage charge pump
- Motor bridge driver with full R_{dson} down to 6 V
- Device contains temperature warning and protection
- Open-load detection for all outputs
- Overcurrent protection for all outputs
- Separated half bridges for door lock motor
- Programmable PWM control of all outputs
- STM standard serial peripheral interface (ST-SPI 3.1)
- Prepared for additional fail-safe path for H-bridge

Applications

- Door actuator driver with 3 bridges for double door lock control, 4 high-side drivers for bulbs and LEDs control.
- H-bridge control for external power transistors

Description

The L99DZ81EP is a microcontroller driven multifunctional door actuator driver for automotive applications. Up to two DC motors and four grounded resistive loads can be driven with three half bridges and four high-side drivers. Four external MOS transistors in bridge configuration can be driven. The integrated SPI controls all operating modes (forward, reverse, brake and high impedance). Also all diagnostic information is available via SPI read.

Table 1. Device summary

Package	Order codes	
	Tray	Tape and reel
TQFP-64	L99DZ81EP	L99DZ81EPTR

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

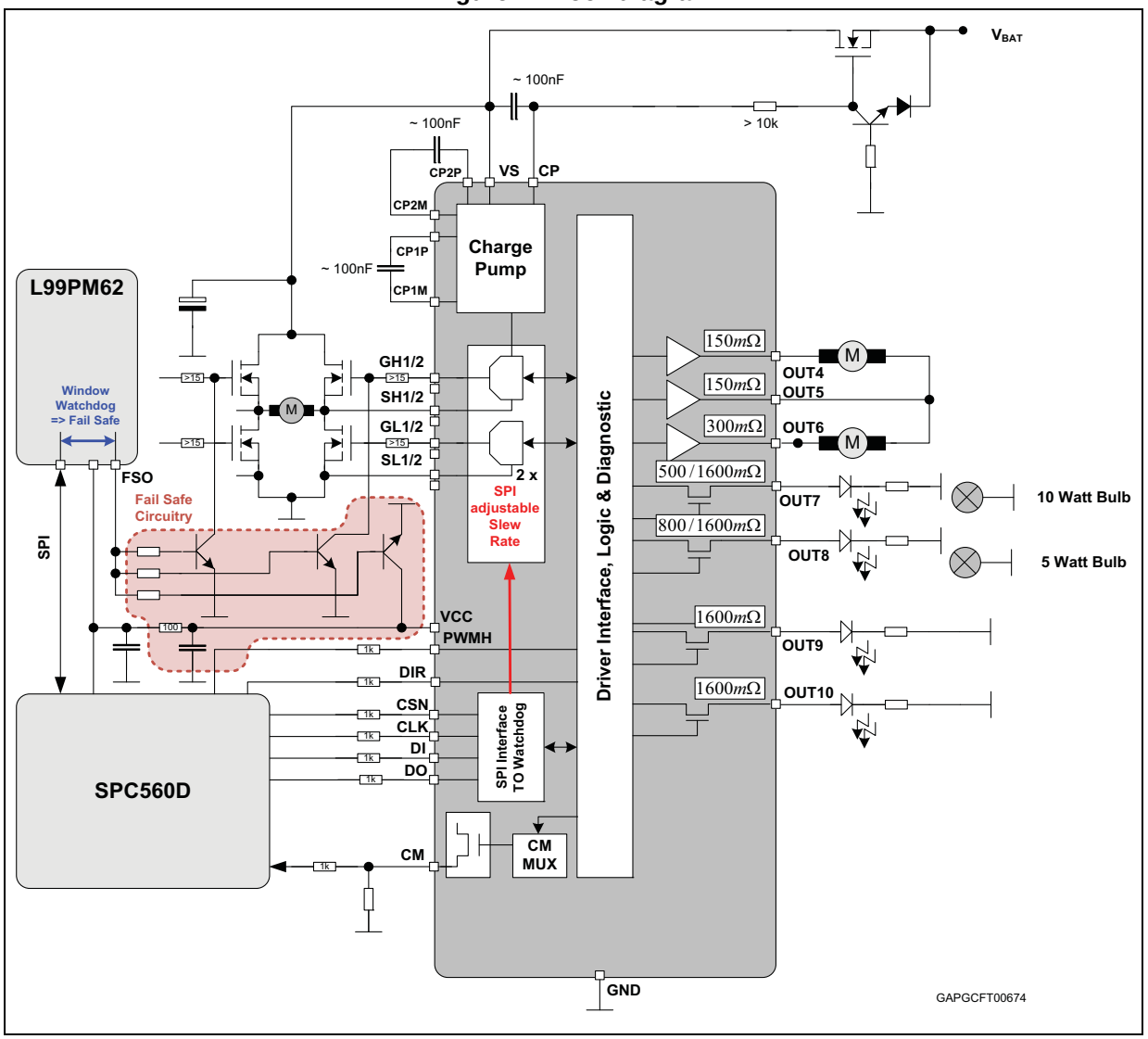


Table 2. Pin definitions and functions

Pin	Symbol	Function
58	GND_1	Ground: reference potential. GND1 and GND2 are internally connected. GND2 supplies OUT4-6. Important: For the capability of driving the full current at the outputs, all pins of GND must be externally connected!
17, 18, 26, 31, 32	GND_2	
17, 57	SGND	Signal Ground: this pin is shared with GND2 pin.

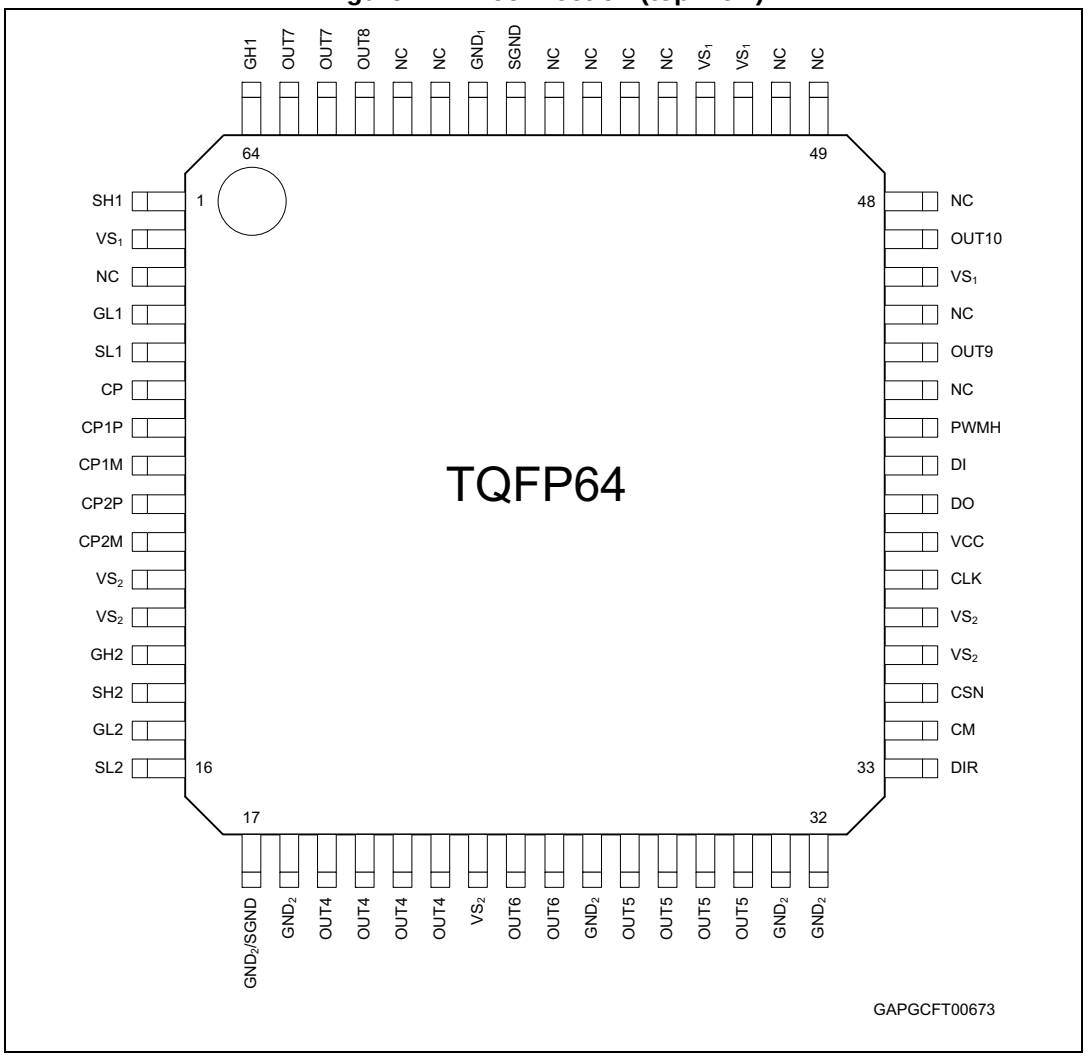
Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
2, 46, 51, 52	VS_1	Power supply voltage for power stage outputs (external reverse protection required): for this input a ceramic capacitor as close as possible to GND is recommended. VS1 supplies OUT7-10 and the internal VS supply, VS2 supplies OUT4-6. Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected!
11, 12, 23, 36, 37	VS_2	
19, 20, 21, 22	OUT4	Half-bridge outputs 4,5,6: the output is built by a high side and a low side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high side driver from output to VS, low side driver from GND to output). This output is over current and open load protected.
27, 28, 29, 30	OUT5	
24, 25	OUT6	
40	DO	Serial data output: the diagnosis data is available via the SPI and this 3-state-output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high).
34	CM	Current monitor output: depending on the selected multiplexer bits of the Control Register this output sources an image of the instant current through the corresponding high side driver with a fixed ratio.
35	CSN	Chip-Select-Not input: this input is low active and requires CMOS logic levels. The serial data transfer between the device and the micro controller is enabled by pulling the input CSN to low level.
41	DI	Serial data input: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB, bit 23) is transferred first.
38	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.
33	DIR	Direction Input: this input controls the H-Bridge Drivers.
39	VCC	Supply Voltage: 5 V supply. A ceramic capacitor as close as possible to GND is recommended.
44	OUT9	High-side-driver output 9: the output is built by a high side switch and is intended for resistive loads; hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over current and open load protected.
42	PWMH	PWMH input: this input signal can be used to control the H-Bridge Gate drivers.
3, 43, 45, 48, 49, 50, 53, 54, 55, 56, 59, 60	NC	Not connected.
62, 63	OUT7	High side driver output 8: see OUT9. Important: This output can be configured to supply a bulb with low on-resistance or a LED with higher on-resistance in a different application.
61	OUT8	
47	OUT10	High-side-driver-output 10: see OUT9.

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
13	GH2	GH2: gate driver for power MOS high side switch in half-bridge 2.
14	SH2	SH2: source of high-side switch in half-bridge 2.
15	GL2	GL2: gate driver for power MOS low side switch in half-bridge 2.
16	SL2	SL2: source of low side switch in half-bridge 2.
64	GH1	GH1: gate driver for power MOS high side switch in half-bridge 1.
1	SH1	SH1: source of high-side switch in half-bridge 1.
4	GL1	GL1: gate driver for power MOS low side switch in half-bridge 1.
5	SL1	SL1: source of low side switch in half-bridge 1.
7	CP1P	CP1P: charge pump pin for capacitor 1, positive side.
8	CP1M	CP1M: charge pump pin for capacitor 1, negative side.
9	CP2P	CP2P: charge pump pin for capacitor 2, positive side.
10	CP2M	CP2M: charge pump pin for capacitor 2, negative side.
6	CP	CP: charge pump output.

Figure 2. Pin connection (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter/test condition		Value [DC Voltage]	Unit
V_{S1}, V_{S2}	DC supply voltage		-0.3 to +28	V
	Single pulse / t_{max} < 400 ms “transient load dump”		-0.3 to +40	V
V_{CC}	Stabilized supply voltage, logic supply		-0.3 to V_S + 0.3	V
$V_{DI,}$ V_{CLK}, V_{CSN}, V_{DO}, V_{CM}, V_{DIR}, V_{PWMH}, V_{DIR}	Logic input / output voltage range		-0.3 to V_{CC} + 0.3	V
V_{OUTn}	Output voltage (n = 4 to 10)		-0.3 to V_S + 0.3	V
V_{SL1}, V_{SH1}, V_{SL2}, V_{SH2} (V_{Sxy})	High voltage signal pins		-6 to 40	V
V_{GL1}, V_{GH1}, V_{GL2}, V_{GH2} (V_{Gxy})	High voltage signal pins		V_{Sxy} - 1 to V_{Sxy} + 10; V_{CP} + 0.3	V
V_{CP1P}	High voltage signal pins		V_S - 0.3 to V_S + 10	V
V_{CP2P}	High voltage signal pins		V_S - 0.6 to V_S + 10	V
V_{CP1M}, V_{CP2M}	High voltage signal pins		-0.3 to V_S + 0.3	V
V_{CP}	High voltage signal pin	$V_{S1,2} \leq 26$ V	V_S - 0.3 to V_S + 14	V
		$V_{S1,2} > 26$ V	V_S - 0.3 to +40	V
$I_{OUT9,10}$	Output current(1)		±1.25	A
$I_{OUT6,7}$	Output current(1) (low on-resistance mode)		±5	A
I_{OUT7}	Output current(1) (high on-resistance mode)		±5	A
I_{OUT8}	Output current(1)		±2.5	A
$I_{OUT4,5}$	Output current(1)		±10	A
I_{VS1cum}	Maximum cumulated input current at VS_1 pins(1)		±12.5	A
I_{VS2cum}	Maximum cumulated input current at VS_2 pins(1)		±12.5	A
$I_{GND1cum}$	Maximum cumulated output current at GND_1 pins(1)		±5	A
$I_{GND2cum}$	Maximum cumulated output current at GND_2 pins(1)		±12.5	A

1. Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	±2(1)	kV
Power output pins: OUT4 – OUT10	±4(1)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold (junction temperature)		130		150	°C
$T_{jTS\ ON}$	Thermal shutdown threshold (junction temperature)		150		170	°C
T_{jtft}	Thermal warning / shutdown filter time			32		µs

Table 7. Package thermal impedance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient (max)	See *Figure 5*	K/W

2.4 Package and PCB thermal data

2.4.1 TQFP-64 thermal data

Figure 3. TQFP-64 2 layer PCB

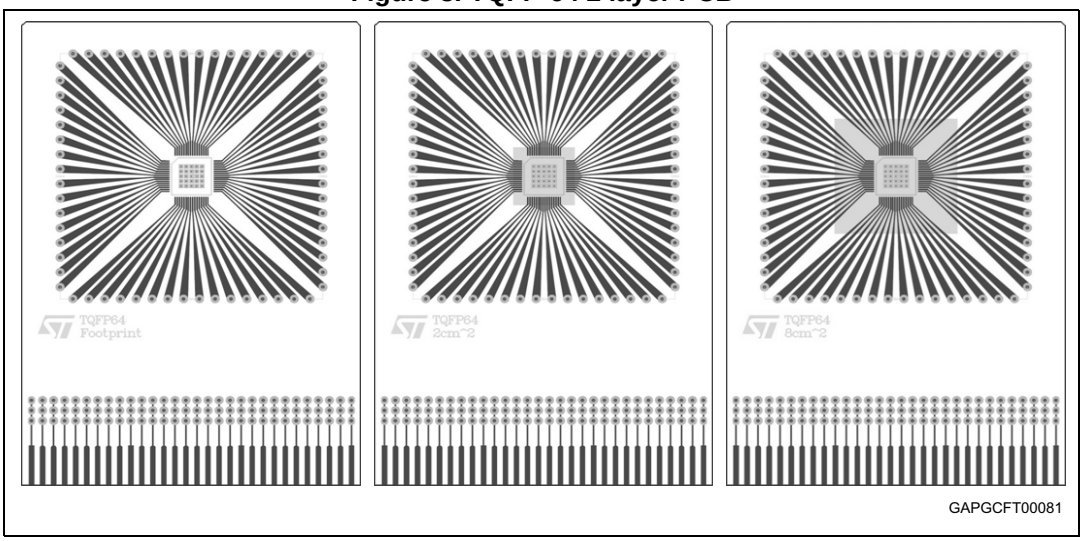
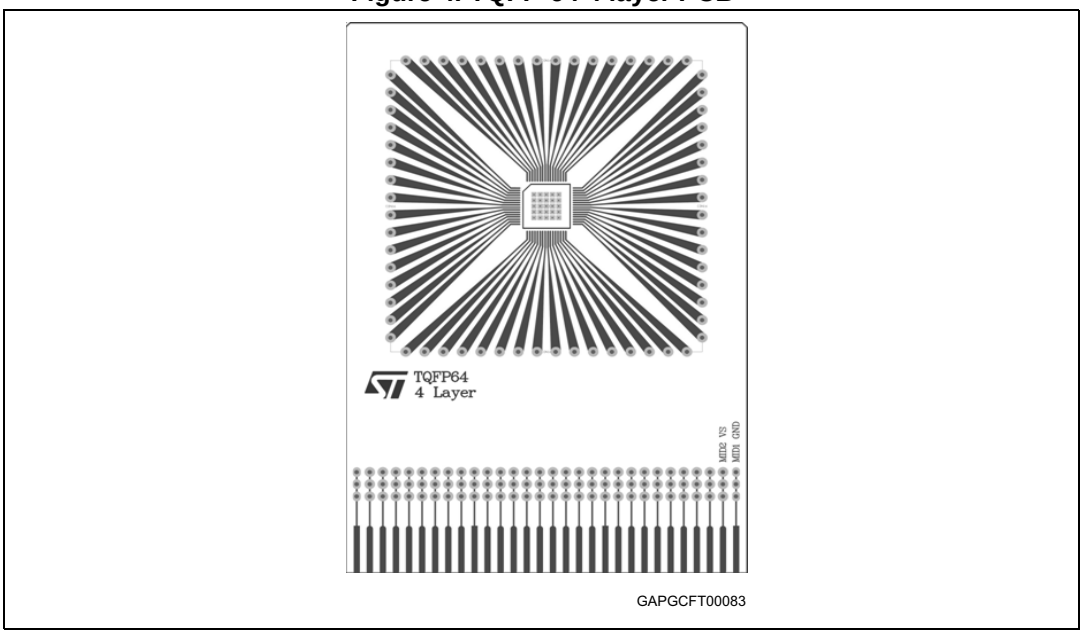
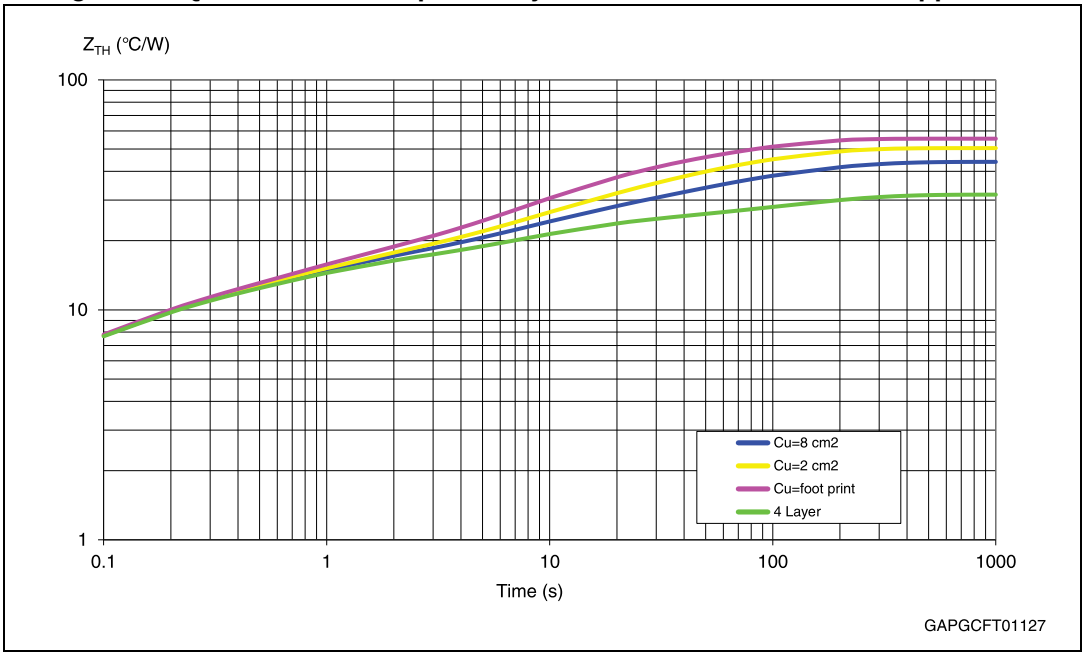


Figure 4. TQFP-64 4 layer PCB



Note: Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%, board double layer and four layers, board dimension 77 mm x114 mm, board material FR4, Cu thickness 0.070mm (outer layers), Cu thickness 0.035mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 6 mm x 6 mm). 4-layer PCB: Cu on mid1 layer, Cu on mid2 layer and Cu on bottom layer: 62 cm^2. Z_{th} measured on the major power dissipator contributor

Figure 5. TQFP-64 thermal impedance junction to ambient vs PCB copper area



2.5 Electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V, 4.75 V ≤ V_{CC} ≤ 5.5 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 8. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating voltage range		5		28	V
$I_{VS(act)}$	Current consumption in active mode	V_S = 13.5 V(1)		5	10	mA
$I_{VS(stby)}$	Current consumption in standby mode	V_S = 16 V; V_{CC} = 5.3 V; standby mode; OUT4 - OUT10 floating; T_{TEST} = -40 °C to 25 °C		4	12	µA
		T_{TEST} = 85 °C(1)		6	25	µA
V_{CC}	Operating voltage range		4.5		5.5	V
$I_{VCC(active)}$	V_{CC} supply current	V_S = 16 V; V_{CC} = 5.3 V; CSN = V_{CC}; active mode; OUT4 - OUT10 floating		5	10	mA
$I_{VCC(stby)}$	V_{CC} standby current	V_S = 16 V; V_{CC} = 5.0 V; CSN = V_{CC}; active mode; OUT4 - OUT10 floating; T_{TEST} = -40 °C to 25 °C		3	6	µA
		T_{TEST} = 85 °C(1)		4	8	µA
		V_S = 16 V; V_{CC} = 5.3 V; CSN = V_{CC}; active mode; OUT4 - OUT10 floating; T_{TEST} = -40 °C to 125 °C			25	µA

1. This parameter is guaranteed by design

Table 9. Overvoltage and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	VS UV threshold voltage(1)	V_S increasing	5.6		7.2	V
$V_{SUV\ OFF}$	VS UV threshold voltage(1)	V_S decreasing	5		5.9	V
$V_{SUV\ hyst}$	VS UV hysteresis(1)	$V_{SUV\ ON}$-$V_{SUV\ OFF}$		0.5		V
$t_{vsuvfilt}$	VS UV filter time			48		µs
$V_{SOV\ OFF}$	VS OV threshold voltage(1)	V_S increasing	18.5		24.5	V
$V_{SOV\ ON}$	VS OV threshold voltage(1)	V_S decreasing	18.0		23.5	V
$V_{SOV\ hyst}$	VS OV hysteresis(1)	$V_{SOV\ OFF}$-$V_{SOV\ ON}$		1		V
$t_{vsovfilt}$	VS OV filter time			48		µs
$V_{VCCRESHU}$	Upper V_{CC} reset threshold(2)	V_{CC} increasing	5.8		7.5	V

Table 9. Overvoltage and undervoltage detection (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{VCCRESHD}$	Upper V_{CC} reset threshold	V_{CC} decreasing	5.5		7.1	V
$V_{VCCRES\ hysth}$	Upper reset hysteresis	$V_{VCCRESHU}$ - $V_{VCCRESHD}$		0.1		V
V_{POROFF}	Power-on-reset threshold	V_{CC} increasing	3.4		4.4	V
V_{PORON}	Power-on-reset threshold	V_{CC} decreasing	3.1		4.1	V
$V_{POR\ hystL}$	Power-on-reset hysteresis	$V_{POROFFL}$ - V_{PORONL}		0.3		V

1. VS = 5V to 28V
2. If V_{CC} exceeds this value all registers are reset and the device enters standby mode.

Table 10. Current monitor output (CM)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range		0		V_{CC} - 1 V	V
$I_{CM\ r}$	Current monitor output ratio: $I_{CM}/I_{OUT4,5,6,7}$ (low on-resistance)	0 V ≤ V_{CM} ≤ V_{CC} - 1 V		1/10000		
	I_{CM}/I_{OUT8} (low on-resistance)			1/6500		
	$I_{CM}/I_{OUT7,8,9,10}$ and 7,8 (high on-resistance)			1/2000		
$I_{CM\ acc}$	Current monitor accuracy $accI_{CMOUT4,5,6}$ and 7(low on-resistance)	0 V ≤ V_{CM} ≤ V_{CC} - 1 V; I_{OUTmin} = 500 mA; $I_{OUT4,5max}$ = 5.9 A; $I_{OUT6max}$ = 2.9 A; $I_{OUT7max}$ = 1.4 A		4 % + 1 % FS (1)	8 % + 2 % FS (1)	
	$accI_{CMOUT7,8,9,10}$(high on-resistance	0 V ≤ V_{CM} ≤ V_{CC} - 1 V; $I_{OUT.min}$ = 100 mA; $I_{OUT9,10max}$ = 0.4A; $I_{OUT7max}$ = 0.3 A; $I_{OUT8(low\ rdson)max}$ = 0.6 A; $I_{OUT8(high\ rdson)max}$ = 0.3 A				
t_{cmb}	Current monitor blanking time			32		µs

1. FS (full scale) = I_{OUTmax} * I_{CMr}

Table 11. Charge pump

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 6 V; I_{CP} = -10 mA	V_S + 6	V_S + 7	V_S + 7.85	V
		V_S ≥ 10 V; I_{CP} = -15 mA	V_S + 11	V_S + 12	V_S + 13.5	V
I_{CP}	Charge pump output current(1)	V_{CP} = V_S + 10 V; V_S = 13.5 V; C_1 = C_2 = C_{CP} = 100 nF	25		47	mA
I_{CPlim}	Charge pump output current limitation(2)	V_{CP} = V_S; V_S = 13.5 V; C_1 = C_2 = C_{CP} = 100 nF	29		70	mA

Table 11. Charge pump (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP_low}	Charge pump low threshold voltage		V_S + 4.6	V_S + 5	V_S + 5.4	V
T_{CP}	Charge pump low filter time			64		µs

1. I_{CP} is the minimum current the device can provide to an external circuit without V_{CP} going below V_S + 10 V
2. I_{CPlim} is the maximum current, which flows out of the device in case of a short to V_S

2.6 Outputs OUT4 - OUT10

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V, 4.75 V ≤ V_{CC} ≤ 5.5 V; all outputs open; T_j = -40°C to 150°C, unless otherwise specified.

Table 12. On-resistance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT4,5}$	On-resistance to supply or GND	V_S = 13.5 V; T_{amb} = +25 °C; $I_{OUT4,5}$ = ±3.0 A		150	200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; $I_{OUT4,5}$ = ±3.0 A		225	300	mΩ
$r_{ON\ OUT6}$	On-resistance to supply or GND	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT6} = ±1.5 A		300	400	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT6} = ±1.5 A		450	600	mΩ
$r_{ON\ OUT7}$	On-resistance to supply in low resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT7} = -0.8 A		500	700	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT7} = -0.8 A		700	950	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT7} = -0.2 A		1600	2400	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT7} = -0.2 A		2500	3400	mΩ
$r_{ON\ OUT8}$	On-resistance to supply in low resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT8} = -0.4 A		800	1200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT8} = -0.4 A		1200	1700	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT8} = -0.2 A		1600	2400	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT8} = -0.2 A		2500	3400	mΩ

Table 12. On-resistance (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT9,10}$	On-resistance to supply	V_S = 13.5 V; T_{amb} = +25 °C; $I_{OUT9,10}$ = -0.4 A		1600	2200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; $I_{OUT9,10}$ = -0.4 A		2500	3400	mΩ
I_{QLH}	Switched-off output current high side drivers of $OUT_{4,6,9,10}$	V_{OUT} = 0 V; standby mode	-5	-2		µA
		V_{OUT} = 0 V; active mode	-10.2	-7		µA
$I_{QLH7,8}$	Switched-off output current high side drivers of $OUT_{7,8}$	V_{OUT} = 0 V; standby mode	-5	-2		µA
		V_{OUT} = 0 V; active mode	-15	-10		µA
I_{QLL}	Switched-off output current low side drivers of OUT_{4-6}	V_{OUT} = V_S; standby mode		80	165	µA
		V_{OUT} = V_S - 0.5 V; active mode	-10	-7		µA

Table 13. Power outputs switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ ON\ H}$	Output delay time high side driver on (all OUT except $OUT_{7,8}$)	V_S = 13.5 V; V_{CC} = 5 V; corresponding low side driver is not active(1)(2)(3)	10	40	80	µs
	Output delay time high side driver on ($OUT_{7,8}$ in high R_{DSON} mode)		15	35	60	µs
	Output delay time high side driver on ($OUT_{7,8}$ in low R_{DSON} mode)		10	35	80	µs
$t_{d\ OFF\ H}$	Output delay time high side driver off ($OUT_{4,5,6}$)	V_S = 13.5 V; V_{CC} = 5 V(1)(2)(3)	50	150	300	µs
	Output delay time high side driver off ($OUT_{7,8,9,10}$)		40	70	100	µs
$t_{d\ ON\ L}$	Output delay time low side driver on	V_S = 13.5 V; V_{CC} = 5 V; corresponding low side driver is not active(1)(2)(3)	15	30	70	µs
$t_{d\ OFF\ L}$	Output delay time low side driver (OUT_{4-6}) off	V_S = 13.5 V; V_{CC} = 5 V (1)(2)(3)	40	150	300	µs
$t_{d\ HL}$	Cross current protection time (OUT_{4-6})	$t_{cc\ ONLS\_OFFHS} - t_{d\ OFF\ H}$(4)	40	200	400	µs
$t_{d\ LH}$		$t_{cc\ ONHS\_OFFLS} - t_{d\ OFF\ L}$(4)				
dV_{OUT}/dt	Slew rate of OUTx	V_S = 13.5 V; V_{CC} = 5 V(1)(2)(3)	0.08	0.2	0.6	V/µs
$f_{PWMx(low)}$	Low PWM switching frequency	V_S = 13.5 V; V_{CC} = 5 V		122		Hz
$f_{PWMx(high)}$	High PWM switching frequency	V_S = 13.5 V; V_{CC} = 5 V		244		Hz

1. R_{load} = 16 Ω at OUT_6 and $OUT_{7,8}$ in low on-resistance mode

2. R_{load} = 4 Ω at $OUT_{4,5}$
3. R_{load} = 64 Ω at $OUT_{9,10}$ and $OUT_{7,8}$ in high on-resistance mode
4. t_{CC} is the switch-on delay time if complement in half bridge has to switch off

Table 14. Current monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OC4}\|$, $\|I_{OC5}\|$	Overcurrent threshold to supply or GND	V_S = 13.5 V; V_{CC} = 5 V; sink and source	6		9.2	A
$\|I_{OC6}\|$			3		5.3	A
$\|I_{OC7}\|$	Overcurrent threshold to supply in low on-resistance mode	V_S = 13.5 V; V_{CC} = 5 V; source	1.5		2.5	A
	Overcurrent threshold to supply in high on-resistance mode		0.35		0.65	A
$\|I_{OC8}\|$	Overcurrent threshold to supply in low on-resistance mode		0.7		1.3	A
	Overcurrent threshold to supply in high on-resistance mode		0.35		0.65	A
$\|I_{OC9}\|$, $\|I_{OC10}\|$	Overcurrent threshold to supply		0.5		1.0	A
t_{FOC}	Filter time of overcurrent signal	Duration of overcurrent condition to set the status bit	10	55	100	µs
f_{rec0}	Recovery frequency for OC; recovery frequency bit = 0		1		4	kHz
f_{rec1}	Recovery frequency for OC; recovery frequency bit = 1		2		6	kHz
$\|I_{OLD4}\|$, $\|I_{OLD5}\|$	Undercurrent threshold to supply or GND	V_S = 13.5 V; V_{CC} = 5 V; sink and source	60	150	300	mA
$\|I_{OLD6}\|$			8	30	80	mA
$\|I_{OLD7}\|$	Undercurrent threshold to supply in low on-resistance mode	V_S = 13.5 V; V_{CC} = 5 V; source	15	40	60	mA
	Undercurrent threshold to supply in high on-resistance mode		5	10	15	mA
$\|I_{OLD8}\|$	Undercurrent threshold to supply in low on-resistance mode		10	30	45	mA
	Undercurrent threshold to supply in high on-resistance mode		5	10	15	mA
$\|I_{OLD9}\|$, $\|I_{OLD10}\|$	Undercurrent threshold to supply		10	20	30	mA
t_{FOL}	Filter time of open-load signal	Duration of open-load condition to set the status bit	0.5	2.0	3.0	ms

2.7 H-bridge driver

Table 15. Gate drivers for the external Power-MOS (H-bridge)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high-side Power-MOS						
$I_{GHx(Ch)}$	Average charge current (charge stage)	T_j = 25 °C		0.3		A
R_{GHx}	On-resistance (discharge-stage)	V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 25 °C	4	6	8	Ω
		V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 125 °C		8	10	Ω
V_{GHxH}	Gate-on voltage	Outputs floating	V_{SHx} + 8	V_{SHx} + 10	V_{SHx} + 11.5	V
R_{GSHx}	Passive gate-clamp resistance	V_{GHx} = 0.5 V		15		kΩ
Drivers for external low-side Power-MOS						
$I_{GLx(Ch)}$	Average charge-current (charge stage)	T_j = 25 °C		0.3		A
R_{GLx}	On-resistance (discharge-stage)	V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 25 °C	4	6	8	Ω
		V_{SLx} = 0 V; I_{GHx} = 50 mA; T_j = 125 °C		8	10	Ω
V_{GHLx}	Gate-on voltage	Outputs floating	V_{SLx} + 8	V_{SLx} + 10	V_{SLx} + 11.5	V
R_{GSLx}	Passive gate-clamp resistance			15		kΩ

Table 16. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode)(1)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)(1)	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		1.5		µs
$I_{GHxrmax}$	Maximum charge current (current mode)	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 1 V; SLEW < 4:0 ≥ 1 F_H	24.5	31	38.5	mA
$I_{GHxfmax}$	Maximum discharge current (current mode)	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 2 V; SLEW < 4:0 ≥ 1 F_H	18.5	25	33	mA
dI_{IGHxr}	Charge current accuracy	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 1V	See *Figure 6*			
dI_{IGHxf}	Discharge current accuracy	V_S = 13.5 V; V_{SHx} = 0; V_{GHx} = 2 V	See *Figure 7*			

Table 16. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{DSHxrSW}$	Switching Voltage (V_S - V_{SH}) between current mode and switch mode (rising)	V_S = 13.5 V		1.5		V
V_{TDSHxf}(2)	Trigger Voltage to sample the V_{GSH} for switching between switch mode and current mode (falling)	V_S = 13.5 V; V_{GHx} = 4 V		1.5		V
$V_{TGSHxacc}$ (2)	Sampled trigger voltage accuracy	V_S = 13.5 V; V_{SHx} = 0		1		V
$t0_{GHxr}$	Rise time (switch mode)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		45		ns
$t0_{GHxf}$	Fall time (switch mode)	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 2.7 nF		85		ns
$t0_{GLxr}$	Rise time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		45		ns
$t0_{GLxf}$	Fall time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF		85		ns
t_{CCP}	Programmable cross-current protection time		0.1		5	µs
f_{PWMH}	PWMH switching frequency(1)	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 2.7 nF; PWMH - duty cycle = 50 %			50	kHz

1. Without cross-current protection time t_{CCP}
2. Parameter not tested, typical value validated by characterization.

Figure 6. IGHxr ranges

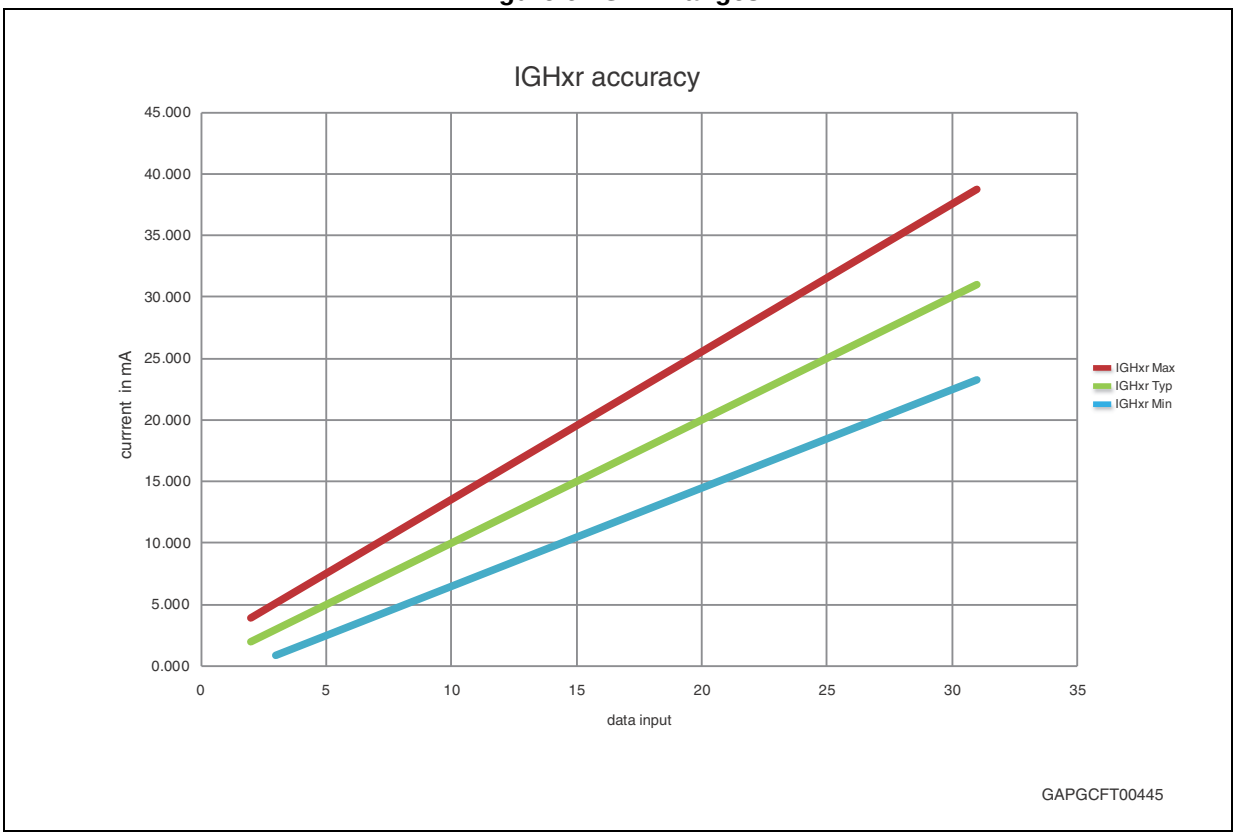


Figure 7. IGHxf ranges

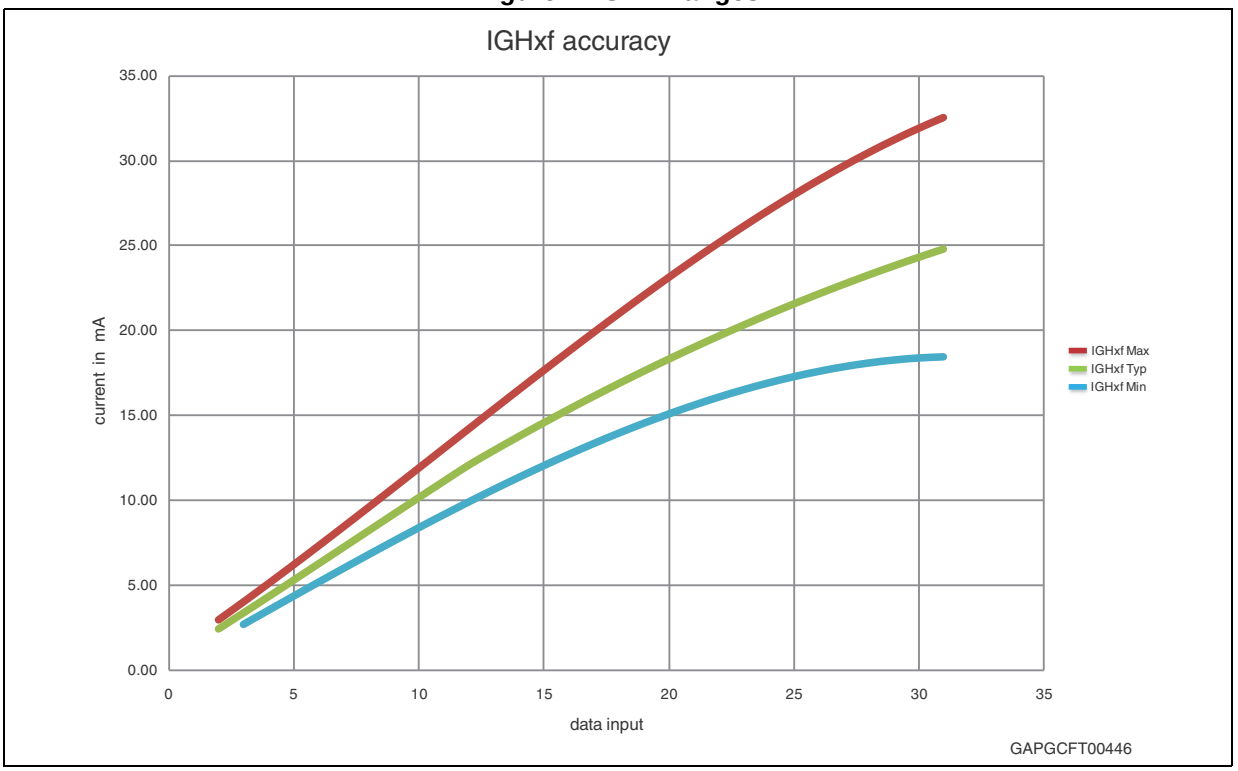


Figure 8. H-driver delay times

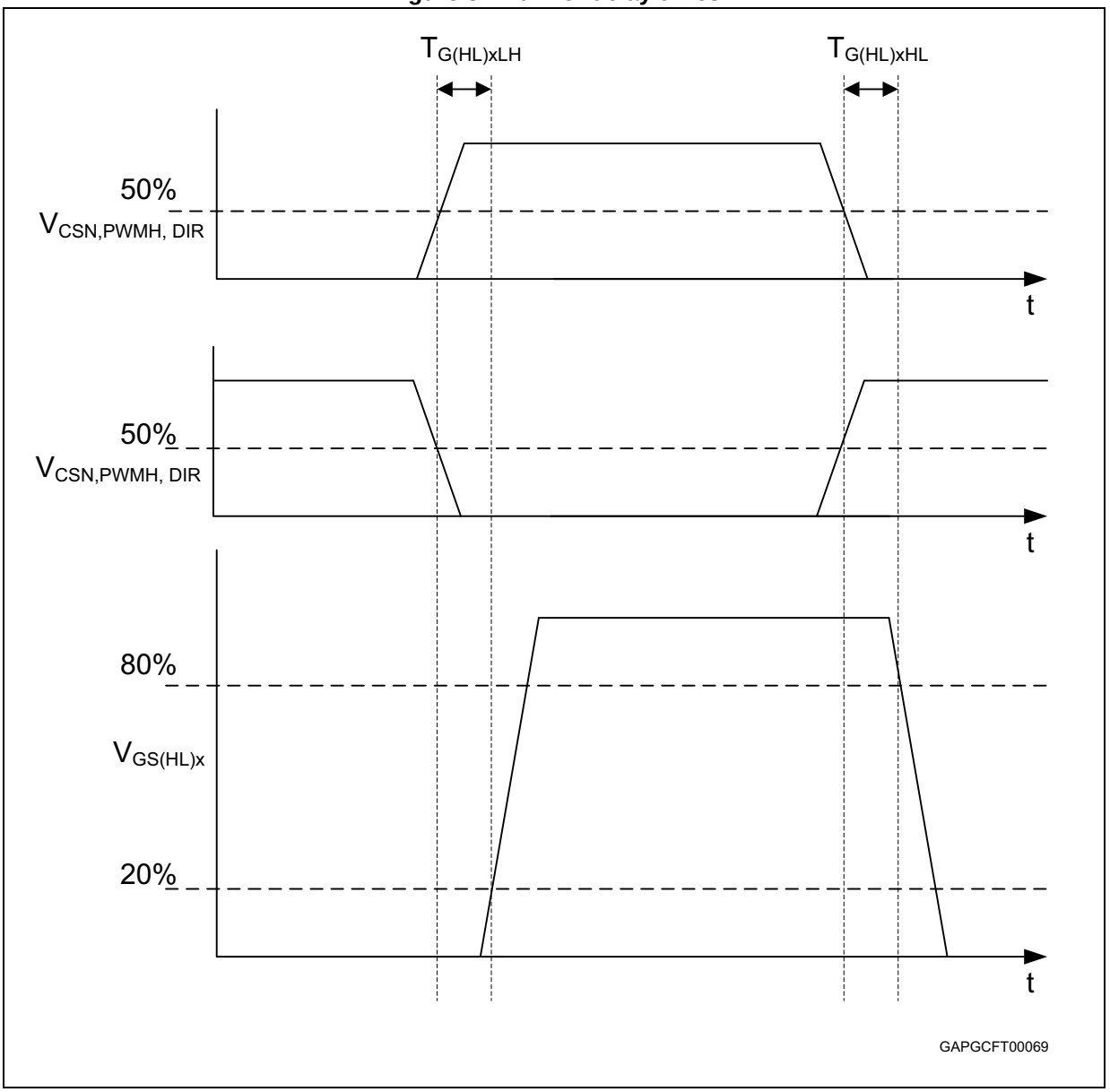


Table 17. Drain source monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SCd1}	Drain-source threshold voltage	V_S = 13.5 V	0.3	0.5	0.7	V
V_{SCd2}	Drain-source threshold voltage	V_S = 13.5 V	0.8	1	1.2	V
V_{SCd3}	Drain-source threshold voltage	V_S = 13.5 V	1.2	1.5	1.8	V
V_{SCd4}	Drain-source threshold voltage	V_S = 13.5 V	1.6	2	2.4	V
t_{SCd}	Drain-source monitor filter time		3	5.5	8	µs
t_{scs}	Drain-source comparator settling time	V_S = 13.5 V; V_{SH} = jump from GND to V_S	—		5	µs

Table 18. Open-load monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ODSL}	Low-side drain-source monitor low off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.14 * V_S	0.18 * V_S	0.21 * V_S	V
V_{ODSH}	Low-side drain-source monitor high off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.75 * V_S	0.85 * V_S	0.95 * V_S	V
V_{OLSHx}	Output voltage of selected SHx in open-load test mode	V_{SLx} = 0 V; V_S = 13.5 V		0.5 * V_S		V
R_{pdOL}	Pull-down resistance of the non-selected SHx pin in open-load mode	V_{SLx} = 0 V; V_S = 13.5 V; V_{SHX} = 4.5 V		20		kΩ
T_{OL}	Open-load filter time			2		ms

2.8 SPI / logic – electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6V ≤ V_S ≤ 18 V, 4.75 V ≤ V_{CC} ≤ 5.5 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 19. Delay time from Standby to Active mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{set}	Delay time	Switching time from standby to active mode. Time until output drivers are enabled after CSN going to high and set bit 0 = 1 of control register 0.	250	310	410	µs
t_{wakup}	Wake-up time	Switching from standby to active mode. Time after the first falling edge of CSN until the first positive CLK edge, which latches EN = 1 correctly into the device	—		20	µs
t_{awake}	Stay awake time	Switching from standby to active mode. After the first rising edge of CSN a second SPI frame with EN = 1 is correctly recognized	—	256		µs

Table 20. Inputs: DI, CSN, CLK, DIR and PWMH

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Inputs: CSN, CLK, DI, DIR, PWMH						
V_{IL}	Input voltage low level	V_S = 13.5 V; V_{CC} = 5.0 V	0.3 * V_{CC}			V
V_{IH}	Input voltage high level	V_S = 13.5 V; V_{CC} = 5.0 V			0.7 * V_{CC}	V
V_{IHYS}	Input hysteresis	V_S = 13.5 V; V_{CC} = 5.0 V	500			mV
$R_{CSN\ in}$	CSN pull-up resistor	V_S = 13.5 V; V_{CC} = 5.0 V; 0 V ≤ V_{CSN} ≤ 0.7 * V_{CC}	60	110	215	kΩ
$R_{CLK\ in}$	CLK pull-down resistor	V_S = 13.5 V; V_{CC} = 5.0 V; 0.3 * V_{CC} ≤ V_{CLK} ≤ V_{CC}	60	110	215	kΩ
$R_{DI\ in}$	DI pull-down resistor	V_S = 13.5 V; V_{CC} = 5.0 V; 0.3 * V_{CC} ≤ V_{DI} ≤ V_{CC}	60	110	215	kΩ
R_{DIR}	DIR pull-down resistor	V_S = 13.5 V; V_{CC} = 5.0 V; 0.3 * V_{CC} ≤ V_{DIR} ≤ V_{CC}	60	110	215	kΩ
R_{PWMH}	PWMH pull-down resistor	V_S = 13.5 V; V_{CC} = 5.0 V; 0.3 * V_{CC} ≤ V_{PWMH} ≤ V_{CC}	60	110	215	kΩ
Output: DO						
V_{OL}	Output voltage low level	I_{OL} = 5 mA; V_S = 13.5 V; V_{CC} = 5.0 V			0.3 * V_{CC}	V
V_{OH}	Output voltage high level	I_{OH} = -5 mA; V_S = 13.5 V; V_{CC} = 5.0 V	0.7 * V_{CC}			V
I_{DOLK}	3-state leakage current	V_{CSN} = V_{CC}; 0 < V_{DO} < V_{CC}	-10		10	µA

Table 21. AC-Characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{OUT}(1)	Output capacitance (DO)		—	—	10	pF
C_{IN}(1)	Input capacitance (DI, CSN, CLK, DIR, PWMH)		—	—	10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

For definition of the parameters please see *Figure 9*, *Figure 10* and *Figure 11*.

Table 22. Dynamic characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CSNQVL}	DO enable from 3-state to low level	C_{DO} = 100 pF; I_{DO} = 1 mA; pull-up load to V_{CC}; V_S = 13.5 V; V_{CC} = 5 V		100	250	ns
t_{CSNQVH}	DO enable from 3-state to high level	C_{DO} = 100pF; I_{DO} = -1 mA; pull-down load to GND; V_S = 13.5 V; V_{CC} = 5 V		100	250	ns
t_{CSNQTL}	DO disable from low level to 3-state	C_{DO} = 100pF; I_{DO} = 4 mA; pull-up load to V_{CC}; V_S = 13.5 V; V_{CC} = 5 V		380	450	ns
t_{CSNQTH}	DO disable from high level to 3-state	C_{DO} = 100 pF; I_{DO} = -4 mA; pull-down load to GND; V_S = 13.5 V; V_{CC} = 5 V		380	450	ns
t_{CLKQV}	CLK falling until DO valid	V_{DO} < 0.3 * V_{CC} or V_{DO} > 0.7 * V_{CC}; C_{DO} = 100 pF; V_S = 13.5 V; V_{CC} = 5 V		50	250	ns
t_{SCSN}	CSN setup time, CSN low before rising edge of CLK	V_S = 13.5 V; V_{CC} = 5 V	400			ns
t_{SDI}	DI setup time, DI stable before rising edge of CLK	V_S = 13.5 V; V_{CC} = 5 V	200			ns
T_{CLK}	Clock Period	V_S = 13.5 V; V_{CC} = 5 V	1000			ns
t_{HCLK}	minimum CLK high time	V_S = 13.5 V; V_{CC} = 5 V	115			ns
t_{LCLK}	minimum CLK low time	V_S = 13.5 V; V_{CC} = 5 V	115			ns
t_{HCSN}	minimum CSN high time	V_S = 13.5 V; V_{CC} = 5 V	4			µs
t_{SCLK}	CLK setup time before CSN rising	V_S = 13.5 V; V_{CC} = 5 V	400			ns
$t_{r\ DO}$	DO rise time	C_{DO} = 100 pF; V_S = 13.5 V; V_{CC} = 5 V		80	140	ns
$t_{f\ DO}$	DO fall time	C_{DO} = 100 pF; V_S = 13.5 V; V_{CC} = 5 V		50	100	ns

Table 22. Dynamic characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ in}$	rise time of input signal DI, CLK, CSN	V_S = 13.5 V; V_{CC} = 5 V			100	ns
$t_{f\ in}$	fall time of input signal DI, CLK, CSN	V_S = 13.5 V; V_{CC} = 5 V			100	ns

Figure 9. SPI timing parameters

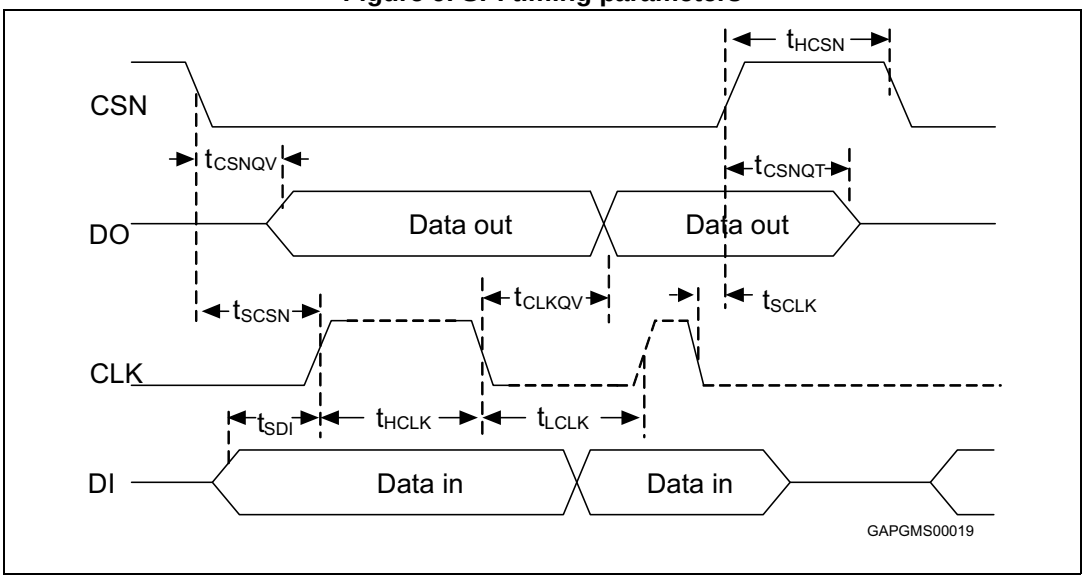


Figure 10. SPI input and output timing parameters

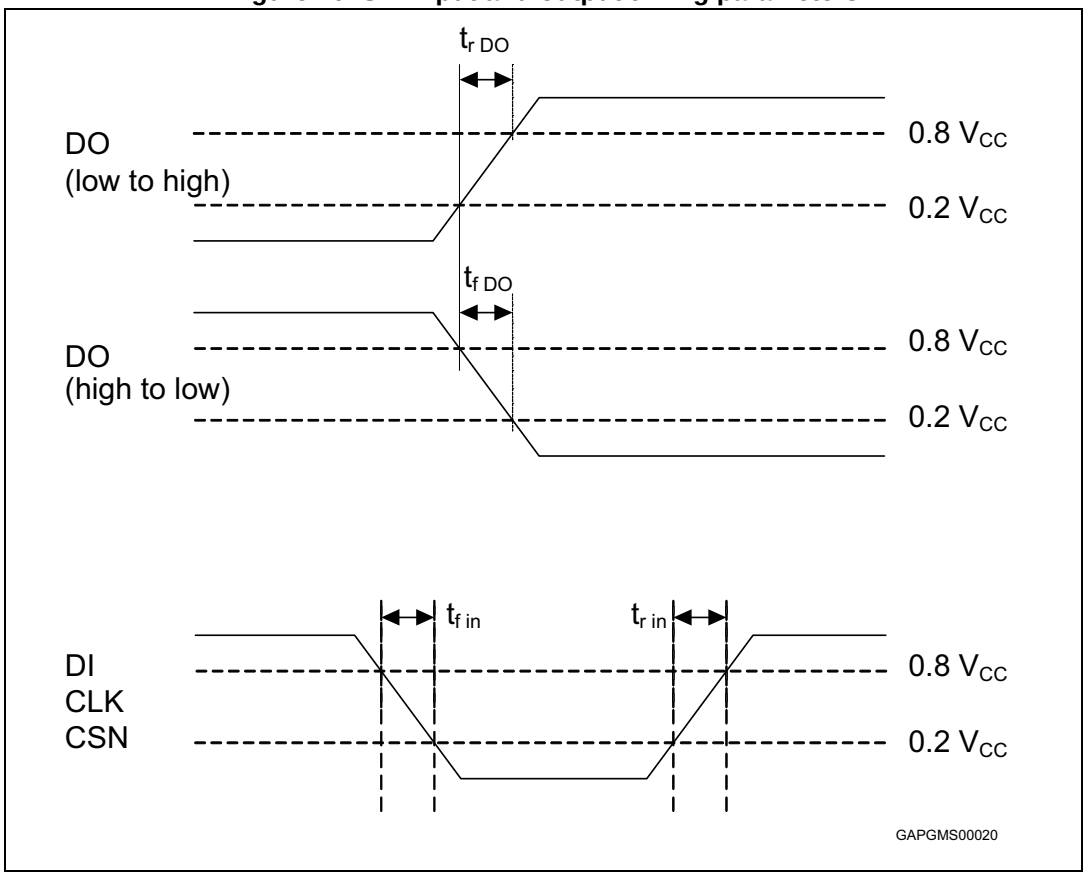


Figure 11. SPI delay description

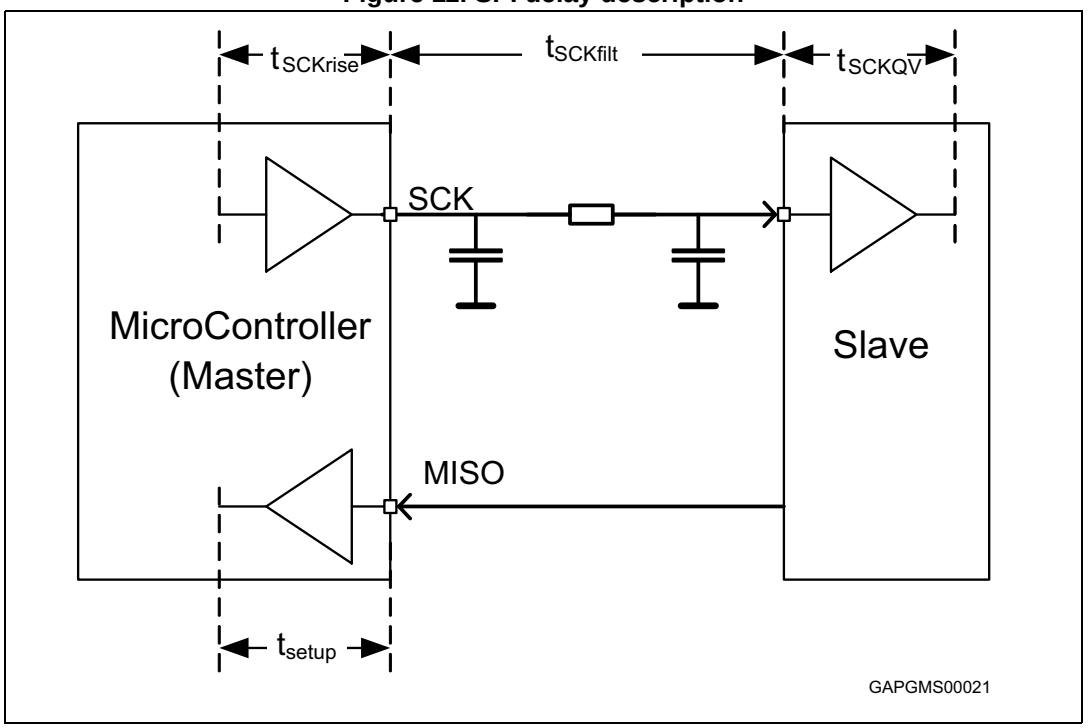
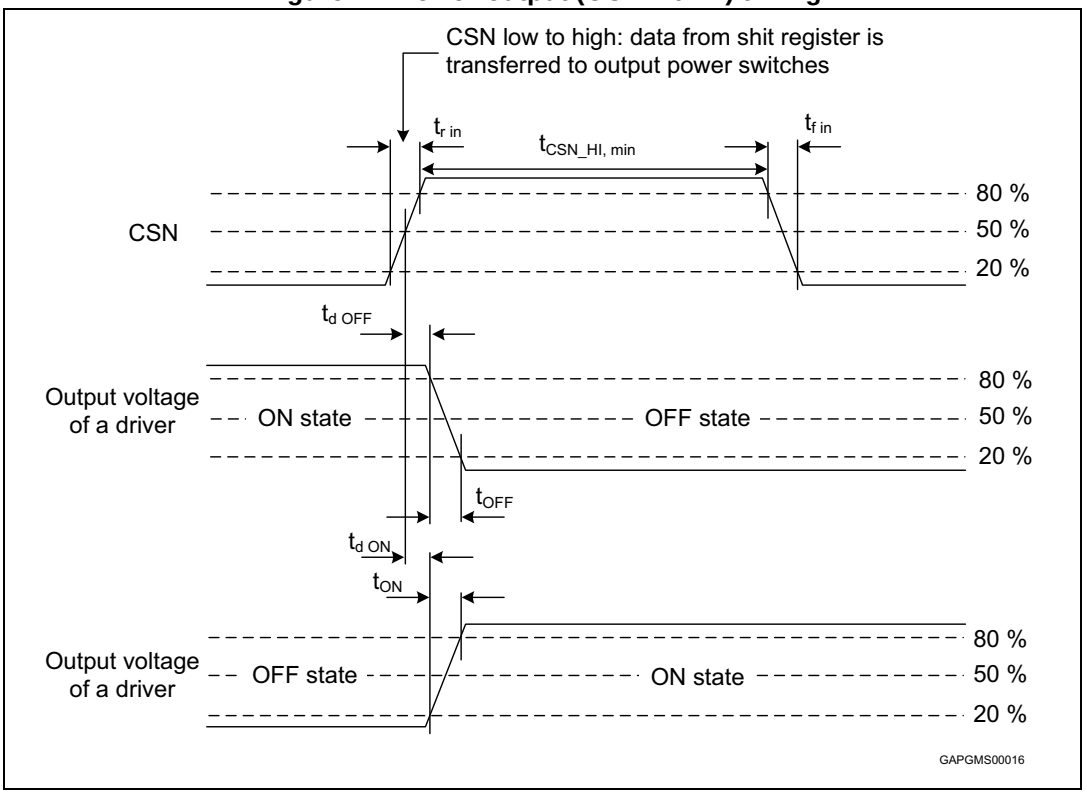


Table 23. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
TC_{WDTO}	Watchdog time out		50	64	100	ms

Figure 12. Power-output (OUT<10:4>) timing



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the power drivers and the Power-MOS gate drivers. For supplying the high-side drivers for the power- and gate-driver outputs, an internal charge-pump is used. The SPI interface and the logic circuitry is supplied by V_{CC}.

Due to the independent V_{CC} supply the control and status information are not lost, if there are spikes or glitches on the power supply voltage.

3.2 Wake up and Active mode/standby mode

After power up of V_S and V_{CC} the device operates in standby-mode. Pulling the signal CSN to low level wakes the device up and the analog part is activated (active mode). After at least 10 µs, the first SPI communication is valid and the EN-bit can be used to set the EN-mode.

The device can be set into active mode writing a ‘1’ into the EN-register. If the EN-register is not set to ‘1’, the device goes back to standby mode typical 256 µs after the rising edge of CSN and all latched data are cleared. In standby mode the current at V_S (V_{CC}) is less than 6 µA (5 µA) for CSN = high (DO in 3-state). It is recommended to switch all outputs off before entering standby mode.

3.3 Charge pump

The charge pump uses two external capacitors, which are switched with a frequency of typically 125 kHz. The output of the charge pump has a current limitation. In standby mode and after a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than T_{CP}, the power-MOS outputs, the EC-control are switched off and the H-Bridge gate drivers are switched to resistive low. The CP_LOW bit has to be cleared through a software reset to reactivate the drivers.

3.4 Diagnostic functions

All diagnostic functions (overcurrent, open-load, power supply overvoltage /undervoltage, temperature warning and thermal shutdown) are internally filtered. The condition has to be valid for at least the associated filter time before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. The open-load and temperature warning functions are intended for information purpose and do not change the state of the output drivers. On contrary, the overcurrent condition disables the corresponding driver and thermal shutdown disables all drivers. Without setting the overcurrent recovery bits in the input data register, the microcontroller has to clear the overcurrent status bits to reactivate the corresponding drivers.

3.5 Overvoltage and undervoltage detection at V_S

If the power supply voltage V_S rises above the overvoltage threshold V_{SOV_OFF}, the outputs OUT4 to OUT10 are switched to high impedance state, the charge pump is disabled and the H-Bridge gate drivers are switched into sink condition to protect the H-bridge and the load. When the voltage V_S drops below the undervoltage threshold V_{SUV_OFF} (UV-switch-OFF voltage), the output stages are switched to high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers to normal operating voltage, the charge pump is switched on again, the CP_LOW bit is cleared and the output stages return to the programmed state. If the undervoltage/overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated.

If the undervoltage/overvoltage recovery disable bit (OV_UV_RD) is set, the microcontroller needs to clear the status bits to reactivate the drivers. It is recommended to set OV_UV_RD bit to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Overvoltage and undervoltage detection at V_{CC}

At power-on (V_{CC} increases from undervoltage to V_{POROFF}) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases below the low threshold (V_{PORON}), the outputs are switched to 3-state (high impedance) and the status registers are cleared. If the voltage at pin V_{CC} increases above the V_{CC} reset high threshold $V_{VCCRESHU}$, the device enters the reset state, all outputs are switched off and all internal registers are cleared. After the voltage at pin V_{CC} has decreased below $V_{VCCRESHL}$, the device enters normal operating mode again and the internal registers are reset.

3.7 Temperature warning and shutdown

If the junction temperature rises above the temperature warning threshold (T_{jTW}), a temperature warning flag is set after the temperature warning filter time (T_{jtft}) and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold (T_{jTS}), the thermal shutdown bit is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The gates of the H-Bridge are discharged by the ‘Resistive Low’ mode.

The temperature warning and thermal shutdown flags are latched and must be cleared by the microcontroller. This is done by a read and clear command on an arbitrary register, because both bits are part of the global status register.

After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after T_{jtft}. Once this bit is set and the temperature is above the temperature shutdown threshold, temperature shutdown is detected after T_{jtft} and the outputs are switched off. Therefore the minimum time after which the outputs are switched off after the bits have been cleared in case the temperature is still above the thermo-shutdown threshold is twice the thermo-warning/-shutdown filter time T_{jtft}.

3.8 Inductive loads

Each half bridge is built by internally connected high- and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT4 to OUT6 without external freewheeling diodes. The high-side drivers OUT7 to OUT10 are intended to drive resistive loads. Therefore only a limited energy (E < 1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 100 µH) an external freewheeling diode connected between GND and the corresponding output is required.

3.9 Open-load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least t_{FOL} the corresponding open-load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.10 Overcurrent detection

In case of an overcurrent condition, a flag is set in the status register. If the overcurrent signal is valid for at least T_{FOC}, the overcurrent flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the overcurrent recovery bit of the output is cleared, the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.11 Current monitor

The current monitor output sources a current image at the current monitor output, which has three fixed ratios of the instantaneous current of the selected high-side driver. Outputs with a resistance of 500 mΩ and higher have a ratio of 1/2000, except for OUT8, which has a ratio of 1/6500, and those with a lower resistance one of 1/10000. The signal at output CM is blanked after switching on the driver until correct settlement of the circuitry. The bits CM_SEL<3:0> define which of the outputs are multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). Moreover, it is possible to control the power of the defroster more precisely by measuring the load current. The current monitor output is enabled after the current-monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high-impedance mode.

3.12 PWM mode of the power outputs

Each driver has a corresponding PWM enable bit, which can be programmed by the SPI interface. If the PWM enable bit is set, the output is controlled by the logically AND-combination of an internally generated PWM signal and the output control bit of the corresponding driver. The PWM-Frequency of all outputs can be programmed to either 122 Hz of 244 Hz typically. The on-duty-cycle is set by the four 7-bit registers, which control one PWM counter each. Therefore the maximum on-time is 100% - 1 LSB.

1 LSB = 100/128 %. Which output uses which corresponding PWM driver can be seen in the SPI register definition. When programming a specific duty-cycle, the output on/off times as well as the slopes must be taken into account.

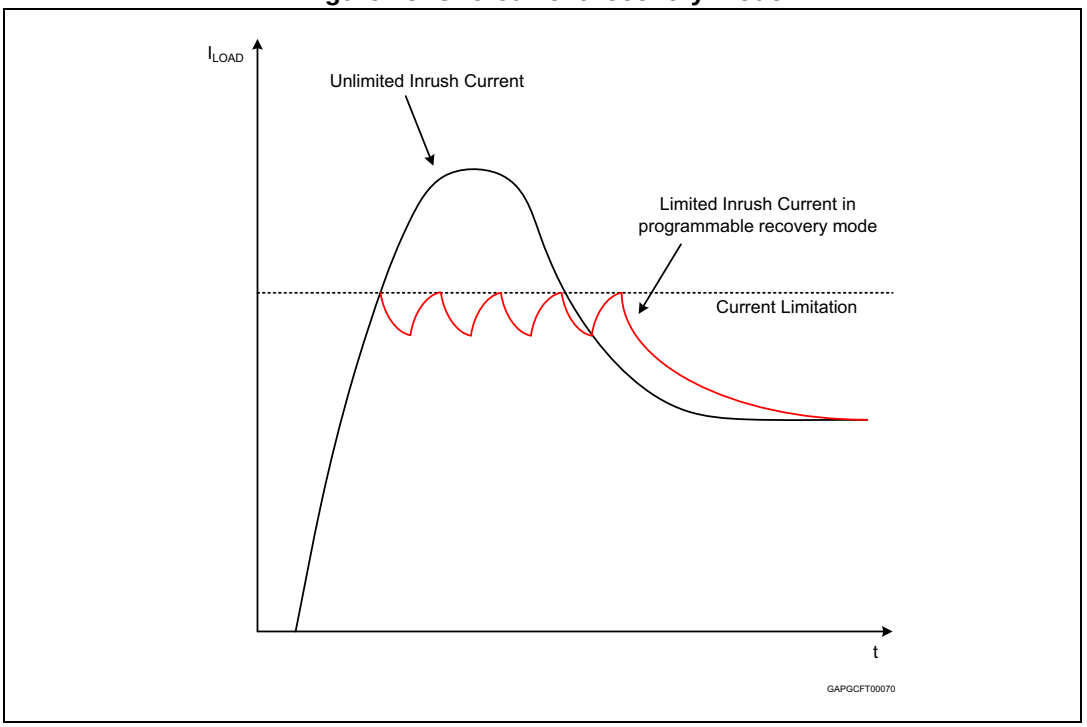
3.13 Cross-current protection

The six half-brides of the device are crosscurrent protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge is automatically delayed by the crosscurrent protection time. After the crosscurrent protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct

3.14 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, Start current of motors and cold resistance of heaters) can be driven by using the programmable softstart function (i.e. overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit. If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The duty cycle in overcurrent condition can be programmed by the SPI interface to about 12 % or 25 %. The PWM modulated current provides sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.7 kHz and 3 kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. For overload detection the microcontroller can switch on the light bulbs by setting the overcurrent recovery bit for the first e.g. 50 ms. After clearing the recovery bit the output is automatically switched off, if the overload condition remains. This overcurrent detection procedure has to be followed in order to make it possible to switch on the low side driver of a bridge output, if the associated high-side driver has been used in recovery mode before.

Figure 13. Overcurrent recovery mode



3.15 H-bridge control (DIR, PWMH, bits SD, SDS)

The PWMH input controls the drivers of the external H-bridge transistors. The motor direction can be chosen with the direction input (DIR), the duty cycle and frequency with the PWMH input. With the SPI-registers SD and SDS four different slow-decay modes (via drivers and via diode) can be selected using the high side or the low side transistors. Unconnected inputs are defined by internal pull-down current.

Table 24. H-bridge control truth table

N°	Control pins		Control bits			Failure bits					Output pin				Comment
	DIR	PWMH	HEN	SD	SDS	CP_LOW	OV	UV	DS	TSD	GH1	GL1	GH2	GL2	
1	X	X	0	X	X	X	X	X	X	X	RL	RL	RL	RL	H-bridge disabled
2	X	X	1	X	X	1	0	0	0	0	RL	RL	RL	RL	Charge pump voltage too low
3	X	X	1	X	X	0	X	X	X	1	RL	RL	RL	RL	Thermo-shutdown
4	X	X	1	X	X	0	1	0	0	0	L	L	L	L	Overvoltage
5	X	X	1	X	X	0	0	0	1	0	L(1)	L(1)	L(1)	L(1)	Short-circuit(1)
6	0	1	1	X	X	0	0	0	0	0	L	H	H	L	Bridge H2/L1 on
7	X	0	1	0	0	0	0	0	0	0	L	H	L	H	Slow-decay mode LS1 and LS2 on
8	0	0	1	0	1	0	0	0	0	0	L	H	L	L	Slow-decay mode LS1 on

Table 24. H-bridge control truth table (continued)

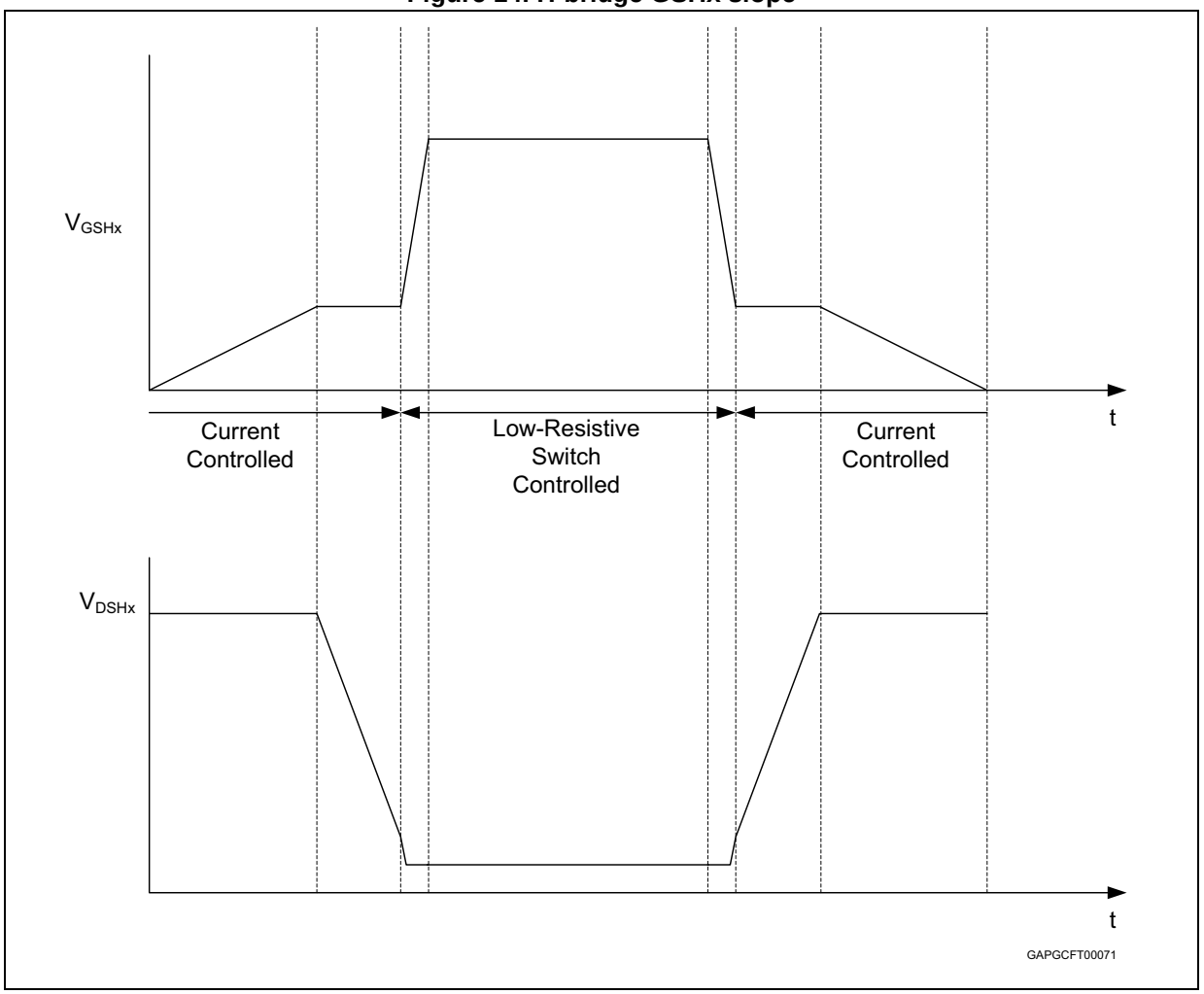
N°	Control pins		Control bits			Failure bits					Output pin				Comment
	DIR	PWMH	HEN	SD	SDS	CP_LOW	OV	UV	DS	TSD	GH1	GL1	GH2	GL2	
9	1	0	1	0	1	0	0	0	0	0	L	L	L	H	Slow-decay mode LS2 on
10	1	1	1	X	X	0	0	0	0	0	H	L	L	H	Bridge H1/L2 on
11	X	0	1	1	0	0	0	0	0	0	H	L	H	L	Slow-decay mode HS1 and HS2 on
12	0	0	1	1	1	0	0	0	0	0	L	L	H	L	Slow-decay mode HS2 on
13	1	0	1	1	1	0	0	0	0	0	H	L	L	L	Slow-decay mode HS1 on

1. Only the half-bridge (low and high-side), in which one MOSFET is in short circuit condition is switched off. Both MOSFETs of the other half-bridge remain active and driven by DIR and PWMH

3.16 H-bridge driver slew-rate control

The rising and falling slope of the drivers for the external high-side Power-MOS can be slew rate controlled. If this mode is enabled the gate of the external high-side Power-MOS is driven by a current source instead of a low-impedance output driver switch as long as the drain-source voltage over this Power-MOS is below the switch threshold. The current is programmed using the bits SLEW<4:0>, which represent a binary number. This number is multiplied by the minimum current step. This minimum current step is the maximum source-/sink-current ($I_{GHxrmax}$ / $I_{GHxfmax}$) divided by 31. Programming SLEW<4:0> to 0 disables the slew rate control and the output is driven by the low-impedance output driver switch.

Figure 14. H-bridge GSHx slope



3.17 Resistive low

The resistive output mode protects the L99DZ81EP and the H-bridge in the standby mode and in some failure modes (thermal shut down (TSD), charge pump low (CP_LOW) and stuck-at-‘1’ at pin DI). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is switched into sink condition for 32 µs to 64 µs to ensure a fast switch-off of the H-bridge transistor. If slew rate control is enabled, the sink condition is slew-rate controlled. Afterwards the driver is switched into the resistive output mode (resistive path to source).

3.18 Short circuit detection/drain source monitoring

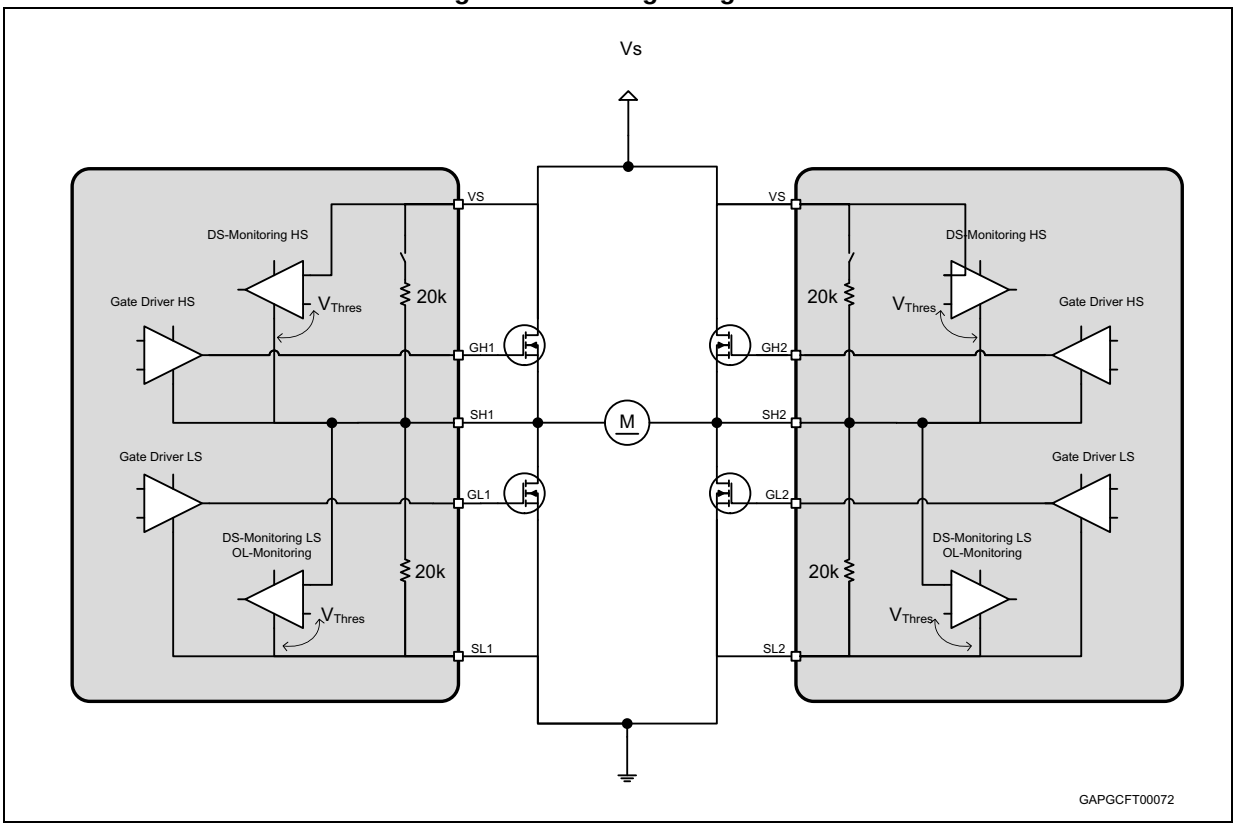
The drain source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage-drop over the external MOSFET exceeds the threshold voltage V_{SCd} for longer than the short current detection time t_{SCd} the corresponding gate driver switches the external MOSFET off and the corresponding drain source monitoring flag (DS_MON[3:0]) is set. The DS_MON bits have

to be cleared through the SPI to reactivate the gate drivers. The drain source monitoring has a filter time of typ. 6 µs. This monitoring is only active while the corresponding gate driver is activated. If a drain-source monitor event is detected, the corresponding gate-driver remains activated for at maximum the filter time. When the gate driver switches on, the drain-source comparator requires the specified settling time until the drain-source monitoring is valid. During this time, this drain-source monitor event may start the filter time. The threshold voltage V_{SCd} can be programmed using the SPI.

Table 25. H-bridge DS-monitor threshold

DIAG<1>	DIAG<0>	Monitoring threshold voltage (typical)
0	0	V_{SCD1} = 0.5 V
0	1	V_{SCD2} = 1.0 V
1	0	V_{SCD3} = 1.5 V
1	1	V_{SCD4} = 2.0 V

Figure 15. H-bridge diagnosis



3.19 H-bridge monitoring in off-mode

The drain source voltages of the H-Bridge driver external transistors can be monitored, while the transistors are switched off. If either bit OL_H1L2 or OL_H2L1 is set to ‘1’, while bit HEN = ‘1’, the H-drivers enter resistive low mode and the drain-source voltages can be monitored. Since the pull-up resistance is equal to the pull-down resistance on both sides of

the bridge a voltage of 2/3 V_S on the pull-up high-side and 1/3 V_S on the low side is expected, if they drive a low-resistive inductive load (e.g. motor). If the drain source voltage on each of these Power-MOS is less than 1/6 V_S, the drain-source monitor bit of the associated driver is set.

In case of a short to ground the drain-source monitor bits of both low-side gate drivers are set. A short to V_S can be diagnosed by setting the “H-Bridge OL high threshold (H-OLTH HIGH)” bit to one.

Figure 16. H-bridge open-load detection (no open-load detected)

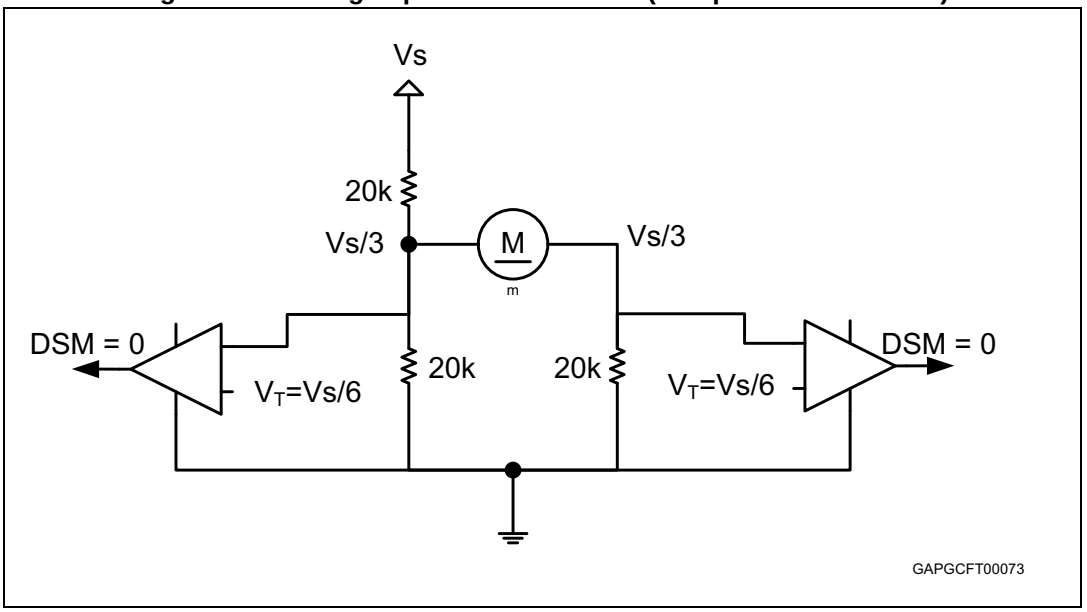


Figure 17. H-bridge open-load detection (open-load detected)

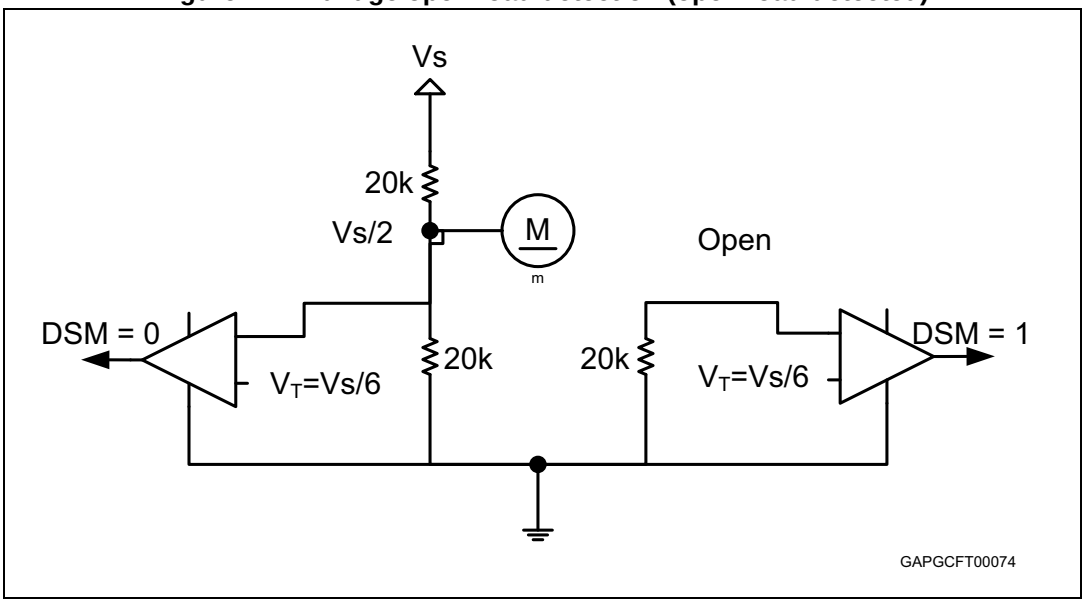


Figure 18. H-bridge open-load detection (short to ground detected)

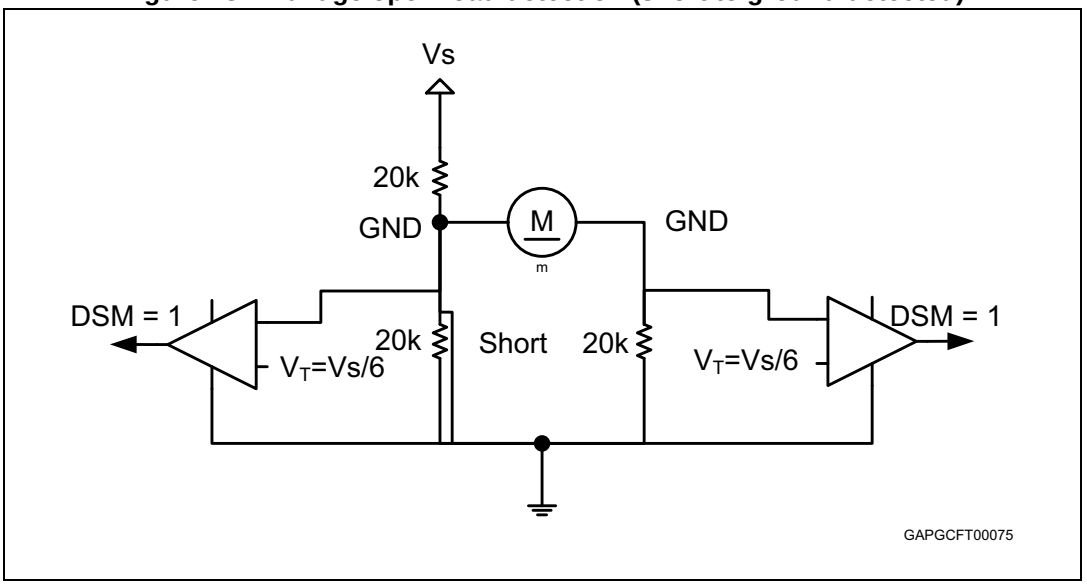
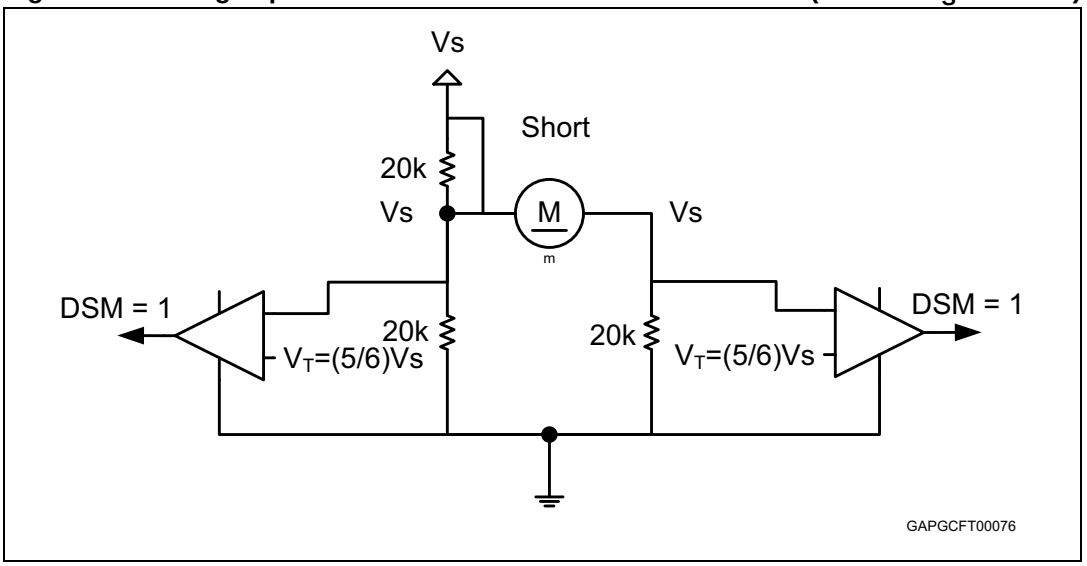


Figure 19. H-bridge open-load detection with H-OLTH HIGH = '1' (short to V_S detected)



3.20 Programmable cross current protection

Both external MOSFET transistors in one half-bridge are disabled for the cross-current protection time (t_{CCP}) after one MOSFET inside this halfbridge is switched off to prevent current flowing from the high-side to the low-side MOSFET.

The cross current protection time t_{CCP} can be programmed by SPI using bits COPT<3:0>.

Table 26. Cross-current protection time

COPT<3>	COPT<2>	COPT<1>	COPT<0>	Min	Typ	Max	unit
0	0	0	0	150	250	360	ns
0	0	0	1	390	500	670	ns
0	0	1	0	590	750	980	ns
0	0	1	1	800	1000	1280	ns
0	1	0	0	1000	1250	1600	ns
0	1	0	1	1210	1500	1910	ns
0	1	1	0	1420	1750	2220	ns
0	1	1	1	1630	2000	2540	ns
1	0	0	0	1830	2250	2850	ns
1	0	0	1	2050	2500	3120	ns
1	0	1	0	2250	2750	3450	ns
1	0	1	1	2460	3000	3760	ns
1	1	0	0	2660	3250	4100	ns
1	1	0	1	2880	3500	4370	ns
1	1	1	0	3080	3750	4680	ns
1	1	1	1	3200	4000	5000	ns

3.21 Watchdog

The watchdog monitors the µC during normal operation within a nominal trigger cycle of 60ms. The watchdog is triggered by toggling the watchdog bit, which restarts the watchdog timer (i.e. content of the watchdog trigger bit has to be inverted). If no watchdog bit inversion has been occurred during the watchdog time-out time T_{WDTO} the H-bridge drivers switch into resistive-low condition, all power outputs are switched off.

4 Functional description of the SPI

4.1 General description

The SPI complies with Standard ST-SPI Interface Version 3.1.

Its communication is based on a Serial Peripheral Interface structure using CSN (Chip Select Not), DI (Serial Data In), DO (Serial Data Out/Error) and CLK (Serial Clock) signal lines.

4.1.1 Chip Select Not (CSN)

The CSN input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal wakes up the device and a serial communication can be started. The state when CSN is going low until the rising edge of CSN is called a communication frame.

4.1.2 Serial Data In (DI)

The DI input pin is used to transfer data serially into the device. The data applied to the DI is sampled at the rising edge of the CLK signal. A stuck-at ‘0’ or ‘1’ enters the standby mode.

4.1.3 Serial Clock (CLK)

The CLK input signal provides the timing of the serial interface. The Data Input (DI) is latched at the rising edge of Serial Clock CLK. The SPI can be driven by a micro controller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. Data on Serial Data Out (DO) is shifted out at the falling edge of the serial clock (CLK). The serial clock CLK must be active only during a frame (CSN low). Any other switching of CLK close to any CSN edge could generate set up/hold violations in the SPI logic of the device. The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of CLK pulses does not correspond to the frame width indicated in the <SPI-frame-ID> (ROM address 03H) the frame is ignored and the <frame error> bit in the <Global Status Byte> is set.

Note: Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.1.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global status bit 7 (Global Error Flag). The content of the selected status or control register is transferred into the data out shift register after the address bits have been transmitted. Each subsequent falling edge of the CLK shifts the next bit out.

4.1.5 SPI communication flow

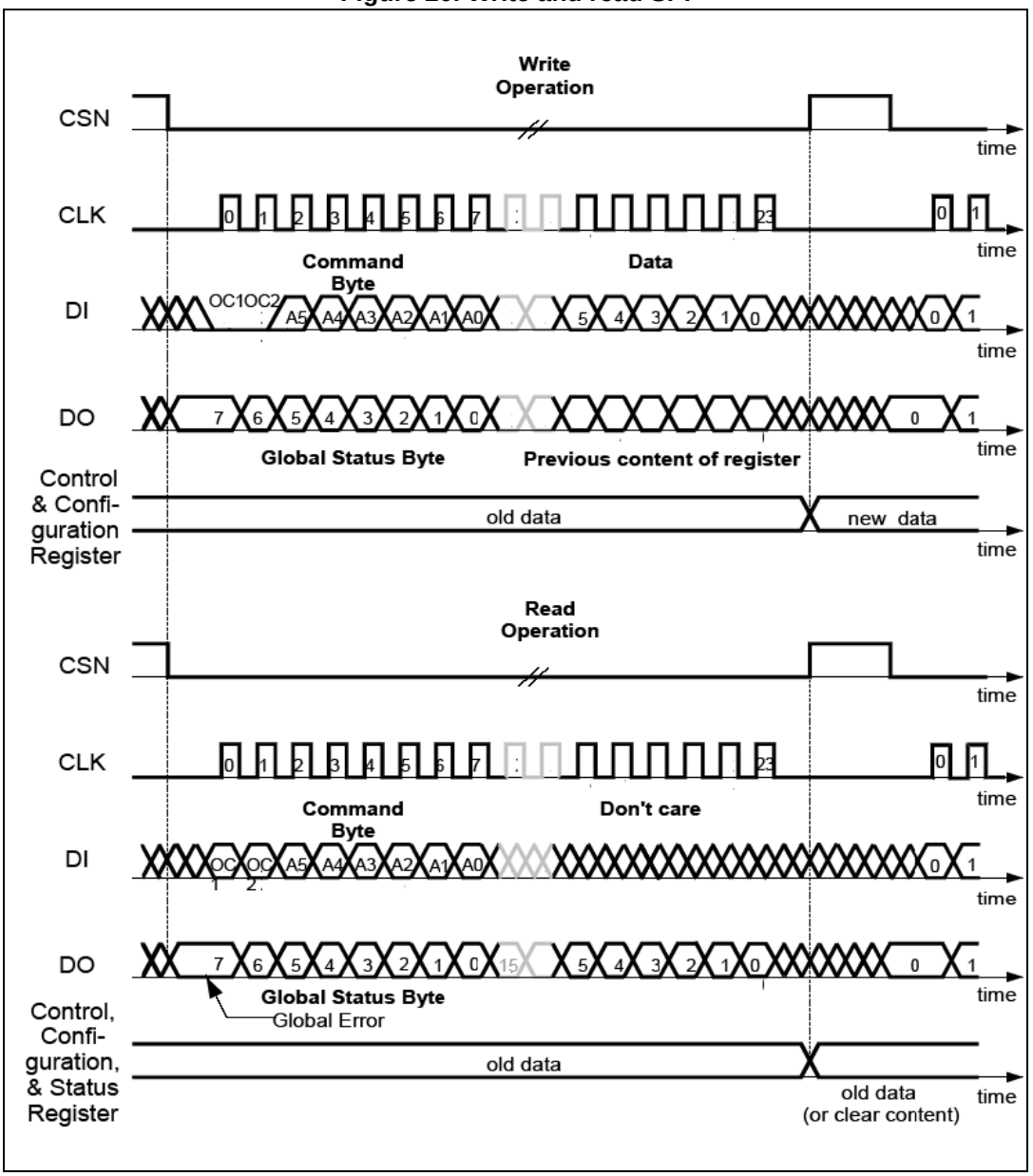
At the beginning of each communication the master can read the contents of the <SPIframe-ID> register (ROM address 03H) of the slave device.

This 8-bit register indicates the SPI frame length (24 bit) and the availability of additional features. Each communication frame consists of a command byte, which is followed by two data bytes.

The data returned on DO within the same frame always starts with the <Global Status> Byte. It provides general status information about the device. It is followed by two data bytes (i. e. 'In-frame-response').

For write cycles the <Global Status> Byte is followed by the previous content of the addressed register.

Figure 20. Write and read SPI



4.2 Command byte

Table 27. Command byte

	Command byte								Data byte 1								Data byte 2							
Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OC1	OC0	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

OCx: operation code

Ax: address

Dx: data bit

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 bits are required, the remaining bits are unused but are reserved.

4.2.1 Operation code definition

Table 28. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clear its content.

The <Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version> and <SPI-frame-ID>.

4.3 Device memory map

Table 29. RAM memory map

Address	Name	Access	Content
00h	Control Register 0	Read/write	Device enable, output bridge and H-bridge open-load control
01h	Control Register 1	Read/write	High-side/ low-side
02h	Control Register 2	Read/write	Bridge recovery mode, PWM

Table 29. RAM memory map (continued)

Address	Name	Access	Content
03h	Control Register 3	Read/write	High-side recovery mode, PWM setup and current-monitor selection
04h	Control Register 4	Read/write	H-bridge driver control
05h	Control Register 5	Read/write	PWM register
06h	Control Register 6	Read/write	PWM register
10h	Status Register 0	Read/clear	Output bridge overcurrent and H-bridge drain-source diagnosis
11h	Status Register 1	Read/clear	Output bridge and H-bridge open-load diagnosis
12h	Status Register 2	Read/clear	High-side overcurrent/open-load
13h	Status Register 3	Read/clear	V_S and chargepump diagnosis
3Fh	Configuration Reg.	Read/write	Mask bits in global status register

Table 30. ROM memory map

Address	Name	Access	Content
00h	ID Header	Read only	4300h (ASSP ST_SPI)
01h	Version	Read only	0200h
02h	Product Code 1	Read only	0100h (01 ST_SPI)
03h	Product Code 2	Read only	5500h (U ST_SPI)
3Eh	SPI-Frame ID.	Read only	4200h SPI-Frame-ID (ST_SPI)

5 SPI - control and status registers

Table 31. Global status byte

Bit	7	6	5	4	3	2	1	0
Name	GL_ER	CO_ER	C_RESET	TSD	TW	UOV_OC_DS	OL	NR
Reset	0	0	1	0	0	0	0	0

GL_ER: Global Error Flag.
Failures of bits 6 to 0 are always linked to the Global Error Flag. This flag is set, if at least one of these bits indicates a failure. It is reflected via the DO pin while CSN is held low and no SPI clock signal is applied. This operation does not cause the Communication Error bit in the <Global Status> to be set. The signal TW bit3 and OL bit1can be masked.

CO_ER: Communication Error.
If the number of clock pulses during the previous frame is not 24, the frame is ignored and this bit is set.

C_RESET: Chip RESET.
If a stuck at ‘1’ on input DI during any SPI frame occurs, or if a Power On Reset (VCC monitor) occurs. C_RESET is reset (‘1’) with any SPI command. When C_RESET is active (‘0’), the gate drivers are switched off (resistive path to source). After a startup of the circuit C_RESET is active due to the power-up reset pulse. Therefore, the gate drivers are switched off. They can only be activated after the C_RESET has been reset by an SPI command.

TSD: Thermal shutdown.
All gate drivers and the charge pump are switched off (resistive path to source). The TSD bit has to be cleared through a read and clear command to reactivate the gate drivers and the chargepump.

TW: Thermal Warning.
This bit can be masked using the configuration register.

UOV_OC_DS: Logical OR of the filtered undervoltage/overvoltage, chargepump-low, overcurrent of the power outputs and the H-bridge drain-source monitor signals.

OL: Open-load.
Logical OR of the filtered output driver open-load signals. This bit can be masked using the configuration register.

NR: Not Ready.
After switching the device from standby mode to active mode an internal timer is started to allow the chargepump to settle before the outputs can be activated. This bit is cleared automatically after the startup time.

5.1 Control Register 0

Table 32. Control Register 0

Bit	Name	Access	Reset	Content
15	0	—	0	Reserved (must be set to ‘0’)
14	0	—	0	
13	0	—	0	
12	0	—	0	
11	0	—	0	
10	0	—	0	
9	OUT4_HS on/off	Read/write	0	The corresponding output driver is activated, if this bit is set. Setting the PWM enable bit, the driver is only switched on, if the PWM timer enables it. An internal cross-current protection prevents, that both the low- and high-side of the half-bridges OUT4-OUT6 are switched on simultaneously.
8	OUT4_LS on/off	Read/write	0	
7	OUT5_HS on/off	Read/write	0	
6	OUT5_LS on/off	Read/write	0	
5	OUT6_HS on/off	Read/write	0	
4	OUT6_LS on/off	Read/write	0	
3	0	—	0	Reserved (must be set to ‘0’)
2	0	—	0	
1	0	—	0	
0	EN	Read/write	0	The device is switched into active mode, if EN is ‘1’. It enters the standby mode, if the EN bit is ‘0’. In standby mode all bits are reset.

5.2 Control Register 1

Table 33. Control Register 1

Bit	Name	Access	Reset	Content
15	OUT7_HS1 on/off	Read/write	0	HS1 / HS2 / Mode: 0 / 0 / Off; 0 / 1 / Low on-resistance; 1 / 0 / High on-resistance; 1 / 1 / Off
14	OUT7_HS2 on/off	Read/write	0	
13	OUT8_HS1 on/off	Read/write	0	
12	OUT8_HS2 on/off	Read/write	0	
11	OUT9_HS on/off	Read/write	0	The corresponding output driver is activated, if this bit is set. Setting the PWM enable bit, the driver is only switched on, if the PWM timer enables it.
10	OUT10_HS on/off	Read/write	0	
9	0	—	0	Reserved (must be set to ‘0’)
8	0	—	0	

Table 33. Control Register 1 (continued)

Bit	Name	Access	Reset	Content
7	0	—	0	Reserved (must be set to ‘0’)
6	0	—	0	
5	0	—	0	
4	0	—	0	
3	0	—	0	
2	0	—	0	
1	0	—	0	
0	0	—	0	

5.3 Control Register 2

Table 34. Control Register 2

Bit	Name	Access	Reset	Content
15	0	—	0	Reserved (must be set to ‘0’)
14	0	—	0	
13	0	—	0	
12	OUT4_OCR	Read/write	0	Setting this bit to high enables the overcurrent recovery mode for the corresponding output.
11	OUT5_OCR	Read/write	0	
10	OUT6_OCR	Read/write	0	
9	0	—	0	Reserved (must be set to ‘0’)
8	0	—	0	
7	0	—	0	
6	0	—	0	
5	0	—	0	
4	OUT4_PWM1	Read/write	0	Setting this bit to ‘1’ enables the PWM mode for the corresponding output.
3	OUT5_PWM2	Read/write	0	
2	OUT6_PWM3	Read/write	0	
1	0	—	0	Reserved (must be set to ‘0’)
0	0	—	0	

5.4 Control Register 3

Table 35. Control Register 3

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Reset</th><th>Content</th></tr>
<tr><td>15</td><td>OUT7_OCR</td><td>Read/write</td><td>0</td><td rowspan="4">Setting this bit to high enables the overcurrent recovery mode for the corresponding output.</td></tr>
<tr><td>14</td><td>OUT8_OCR</td><td>Read/write</td><td>0</td></tr>
<tr><td>13</td><td>OUT9_OCR</td><td>Read/write</td><td>0</td></tr>
<tr><td>12</td><td>OUT10_OCR</td><td>Read/write</td><td>0</td></tr>
<tr><td>11</td><td>0</td><td>—</td><td>0</td><td>Reserved (must be set to ‘0’)</td></tr>
<tr><td>10</td><td>OUT7_PWM1</td><td>Read/write</td><td>0</td><td rowspan="4">Setting this bit to ‘1’ enables the PWM mode for the corresponding output.</td></tr>
<tr><td>9</td><td>OUT8_PWM2</td><td>Read/write</td><td>0</td></tr>
<tr><td>8</td><td>OUT9_PWM3</td><td>Read/write</td><td>0</td></tr>
<tr><td>7</td><td>OUT10_PWM4</td><td>Read/write</td><td>0</td></tr>
<tr><td>6</td><td>0</td><td>—</td><td>0</td><td>Reserved (must be set to ‘0’)</td></tr>
<tr><td>5</td><td>OCR_FREQ</td><td>Read/write</td><td>0</td><td>This bit defines the overcurrent recovery frequency (0: 1.7kHz (typ.) 1: 3kHz (typ.))</td></tr>
<tr><td>4</td><td>OV_UV_RD</td><td>Read/write</td><td>0</td><td>If this bit is set, the associated status bit has to be cleared after an overvoltage /undervoltage event to enable the output drivers again.</td></tr>
<tr><td>3</td><td>CM_SEL<3></td><td>Read/write</td><td>0</td><td rowspan="4">A current image of the selected binary coded output is multiplexed to the CM output. If a corresponding output does not exist, the current monitor is deactivated (especially ‘0000’).

<table>
<tr><th>CM_SEL<3:0></th><th>Selected output</th></tr>
<tr><td>0000</td><td>3-state</td></tr>
<tr><td>0001</td><td>Reserved</td></tr>
<tr><td>0010</td><td>Reserved</td></tr>
<tr><td>0011</td><td>Reserved</td></tr>
<tr><td>0100</td><td>OUT<4></td></tr>
<tr><td>0101</td><td>OUT<5></td></tr>
<tr><td>0110</td><td>OUT<6></td></tr>
<tr><td>0111</td><td>OUT<7></td></tr>
<tr><td>1000</td><td>OUT<8></td></tr>
<tr><td>1001</td><td>OUT<9></td></tr>
<tr><td>1010</td><td>OUT<10></td></tr>
<tr><td>1011</td><td>Reserved</td></tr>
<tr><td>1100</td><td>Reserved</td></tr>
<tr><td>1101-1111</td><td>3-state</td></tr>
</table></td></tr>
<tr><td>2</td><td>CM_SEL<2></td><td>Read/write</td><td>0</td></tr>
<tr><td>1</td><td>CM_SEL<1></td><td>Read/write</td><td>0</td></tr>
<tr><td>0</td><td>CM_SEL<0></td><td>Read/write</td><td>0</td></tr>
</table>

5.5 Control Register 4

Table 36. Control Register 4

Bit	Name	Access	Reset	Content
15	SLEW<4>	Read/write	0	Binary coded Slew Rate Current of the H-Bridge
14	SLEW<3>	Read/write	0	
13	SLEW<2>	Read/write	0	
12	SLEW<1>	Read/write	0	
11	SLEW<0>	Read/write	0	
10	H-OLTH HIGH	Read/write	0	H-bridge OL high threshold (5/6 * V_S) select
9	OL_H1L2	Read/write	0	Test open-load condition between H1 and L2
8	OL_H2L1	Read/write	0	Test open-load condition between H2 and L1
7	SD	Read/write	0	Slow decay
6	SDS	Read/write	0	Slow decay single
5	COPT<3>	Read/write	1	Cross-current protection time (default 4000ns)
4	COPT<2>	Read/write	1	
3	COPT<1>	Read/write	1	
2	COPT<0>	Read/write	1	
1	DIAG<1>	Read/write	0	Drain-source monitoring threshold voltage
0	DIAG<0>	Read/write	0	

5.6 Control Register 5

Table 37. Control Register 5

Bit	Name	Access	Reset	Content
15	0	—	0	Reserved (must be set to ‘0’)
14	PWM2<6>	Read/write	0	Binary coded PWM2 on-duty-cycle
13	PWM2<5>	Read/write	0	
12	PWM2<4>	Read/write	0	
11	PWM2<3>	Read/write	0	
10	PWM2<2>	Read/write	0	
9	PWM2<1>	Read/write	0	
8	PWM2<0>	Read/write	0	
7	PWMFREQ	Read/write	0	PWM-frequency (0: 122 Hz or 1: 244 Hz)

Table 37. Control Register 5 (continued)

Bit	Name	Access	Reset	Content
6	PWM1<6>	Read/write	0	Binary coded PWM1 on-duty-cycle
5	PWM1<5>	Read/write	0	
4	PWM1<4>	Read/write	0	
3	PWM1<3>	Read/write	0	
2	PWM1<2>	Read/write	0	
1	PWM1<1>	Read/write	0	
0	PWM1<0>	Read/write	0	

5.7 Control Register 6

Table 38. Control Register 6

Bit	Name	Access	Reset	Content
15	0	—	0	Reserved (must be set to ‘0’)
14	PWM4<6>	Read/write	0	Binary coded PWM4 on-duty-cycle
13	PWM4<5>	Read/write	0	
12	PWM4<4>	Read/write	0	
11	PWM4<3>	Read/write	0	
10	PWM4<2>	Read/write	0	
9	PWM4<1>	Read/write	0	
8	PWM4<0>	Read/write	0	
7	0	—	0	Reserved (must be set to ‘0’)
6	PWM3<6>	Read/write	0	Binary coded PWM3 on-duty-cycle
5	PWM3<5>	Read/write	0	
4	PWM3<4>	Read/write	0	
3	PWM3<3>	Read/write	0	
2	PWM3<2>	Read/write	0	
1	PWM3<1>	Read/write	0	
0	PWM3<0>	Read/write	0	

5.8 Configuration Register

Table 39. Configuration Register

Bit	Name	Access	Reset	Content
15	0	—	0	Reserved (must be set to ‘0’)
14	0	—	0	
13	0	—	0	
12	0	—	0	
11	0	—	0	
10	0	—	0	
9	0	—	0	
8	0	—	0	
7	0	—	0	
6	HEN	Read/write	0	A ‘1’ enables the H-bridge
5	0	—	0	Reserved (must be set to ‘0’)
4	0	—	0	
3	MASK TW	Read/write	0	Masks thermo warning to global status register
2	0	—	0	Reserved (must be set to ‘0’)
1	MASK OL	Read/write	0	Masks all open-load diagnosis to global status register
0	WD	Read/write	0	Watchdog

5.9 Status Register 0

Table 40. Status Register 0

Bit	Name	Access	Content
15	0	Read	Reserved
14	0	Read	
13	0	Read	
12	0	Read	
11	0	Read	
10	0	Read	
9	OUT4_HS OC	Read/clear	Overcurrent status bit of the corresponding output driver. A ‘1’ indicates that an overcurrent has occurred.
8	OUT4_LS OC	Read/clear	
7	OUT5_HS OC	Read/clear	
6	OUT5_LS OC	Read/clear	
5	OUT6_HS OC	Read/clear	
4	OUT6_LS OC	Read/clear	

Table 40. Status Register 0 (continued)

Bit	Name	Access	Content
3	DS_MON_HS<2>	Read/clear	DS-Monitoring bit. A ‘1’ indicates that a drain-monitoring event (short-circuit or open-load) has occurred.
2	DS_MON_HS<1>	Read/clear	
1	DS_MON_LS<2>	Read/clear	
0	DS_MON_LS<1>	Read/clear	

5.10 Status Register 1

Table 41. Status Register 1

Bit	Name	Access	Content
15	0	Read	Reserved
14	0	Read	
13	0	Read	
12	0	Read	
11	0	Read	
10	0	Read	
9	OUT4_HS OL	Read/clear	Open-Load status bit of the corresponding output driver. A ‘1’ indicates that an open-load event has occurred.
8	OUT4_LS OL	Read/clear	
7	OUT5_HS_OL	Read/clear	
6	OUT5_LS OL	Read/clear	
5	OUT6_HS OL	Read/clear	
4	OUT6_LS OL	Read/clear	
3	0	Read	Reserved
2	0	Read	
1	0	Read	
0	0	Read	

5.11 Status Register 2

Table 42. Status Register 2

Bit	Name	Access	Content
15	OUT7 OC	Read/clear	Overcurrent and open-load status bit of the corresponding output driver
14	OUT7 OL	Read/clear	
13	OUT8 OC	Read/clear	
12	OUT8 OL	Read/clear	
11	OUT9 OC	Read/clear	
10	OUT9 OL	Read/clear	
9	OUT10 OC	Read/clear	
8	OUT10 OL	Read/clear	
7	0	Read	Reserved
6	0	Read	
5	0	Read	
4	0	Read	
3	VS UV	Read/clear	V_S undervoltage and overvoltage status bit.
2	VS OV	Read/clear	
1	0	Read	Reserved
0	0	Read	

5.12 Status Register 3

Table 43. Status Register 3

Bit	Name	Access	Content
15	0	Read	Reserved
14	0	Read	
13	0	Read	
12	0	Read	
11	0	Read	
10	0	Read	
9	0	Read	
8	0	Read	
7	0	Read	
6	0	Read	

Table 43. Status Register 3 (continued)

Bit	Name	Access	Content
5	0	Read	Reserved
4	0	Read	
3	0	Read	
2	0	Read	
1	0	Read	
0	CP LOW	Read/clear	This bit indicates, that the charge pump voltage is too low

6 Package and packing information

6.1 ECOPACK® package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

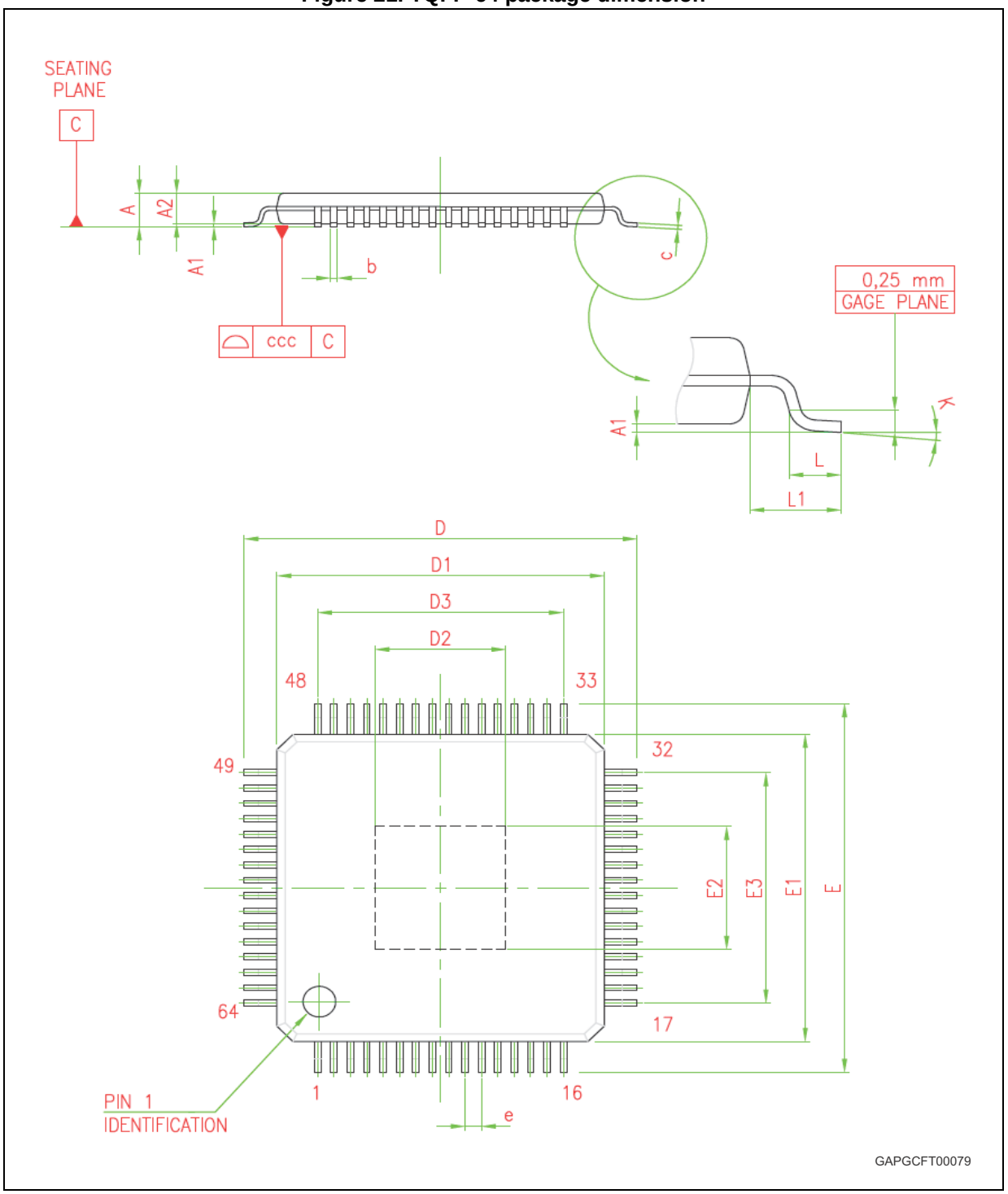
6.2 TQFP-64 mechanical data

Table 44. TQFP-64 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1,20
A1	0,05		0,15
A2	0,95	1,00	1,05
b	0,17	0,22	0,27
c	0,09		0,20
D	11,80	12,00	12,20
D1	9,80	10,00	10,20
D2(1)	5,85	6,00	6,15
D3		7,50	
E	11,80	12,00	12,20
E1	9,80	10,00	10,20
E2(1)	5,85	6,00	6,15
E3		7,50	
e		0,50	
L	0,45	0,60	0,75
L1		1,00	
k	0°	3,50°	7°
ccc			0,08

1. The size of exposed pads is variable depending on lead frame design and pad size end user should verify "D2" and "E2" dimensions for each device application

Figure 21. TQFP-64 package dimension



6.3 TQFP-64 packing information

The devices can be packed in tray or tape and reel shipments (see the *Figure 1: Device summary on page 1* for packaging quantities).

Figure 22. TQFP-64 power lead-less tray shipment (no suffix) (part 1)

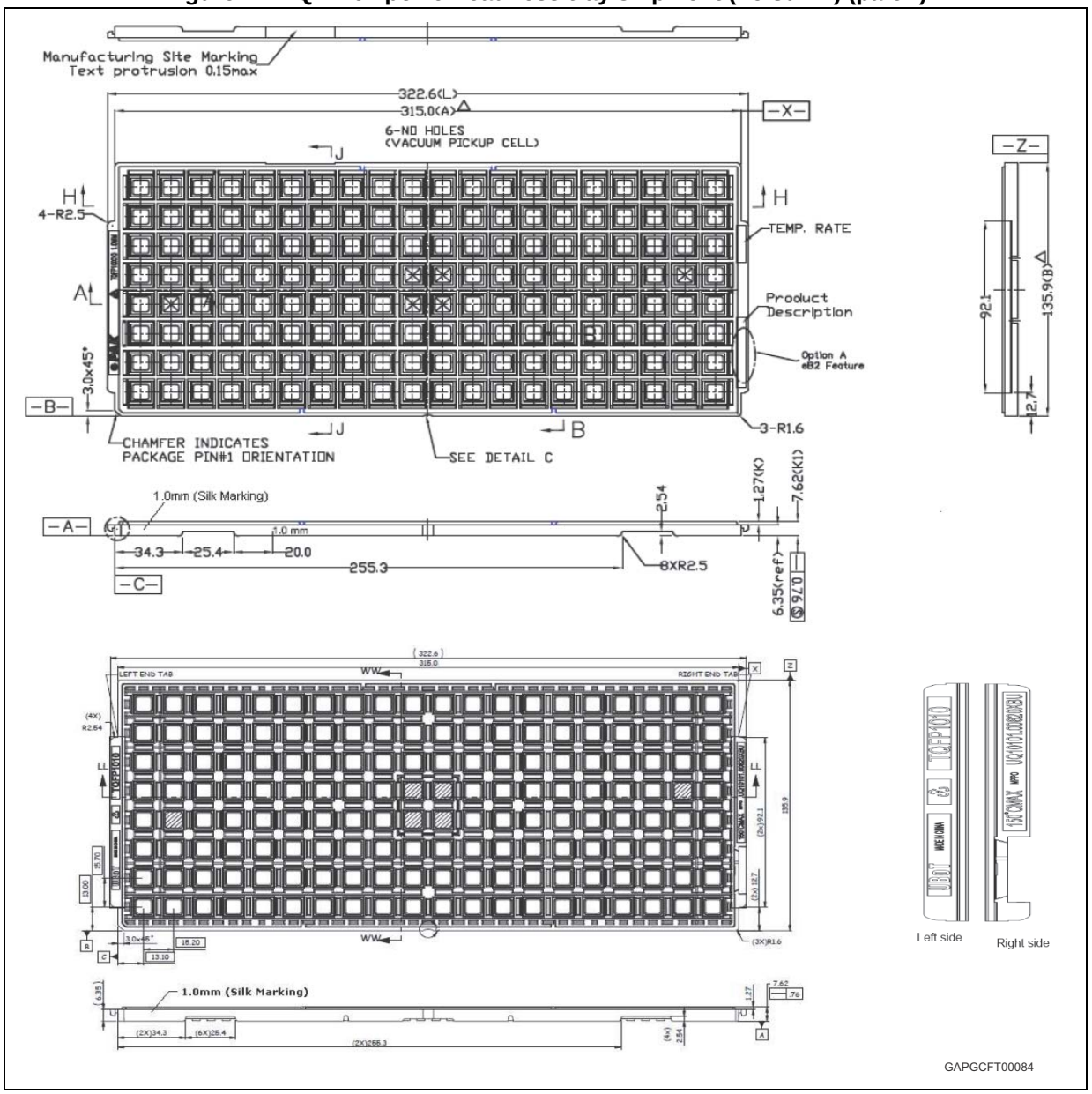


Figure 23. TQFP-64 power lead-less tray shipment (no suffix) (part 2)

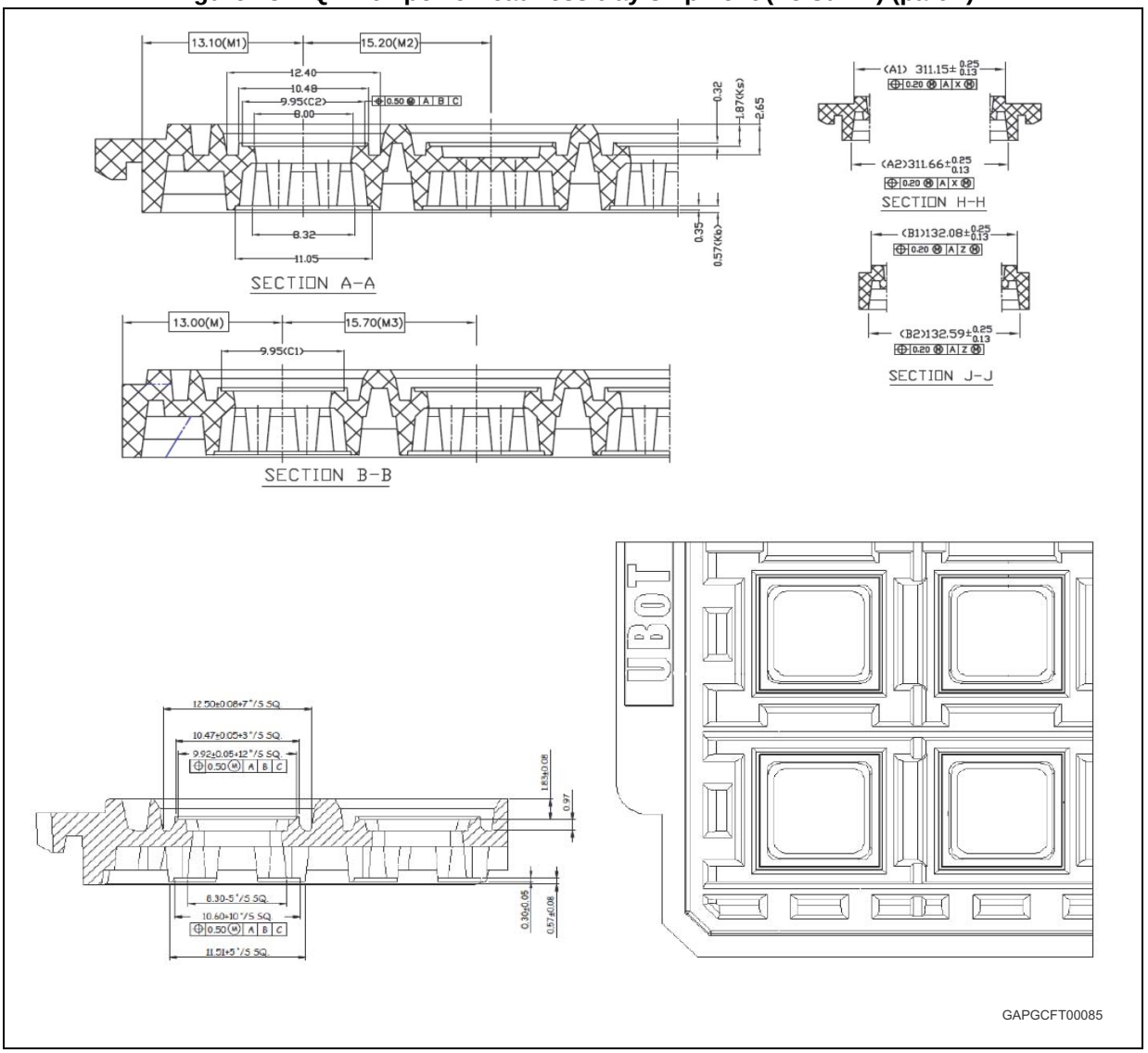
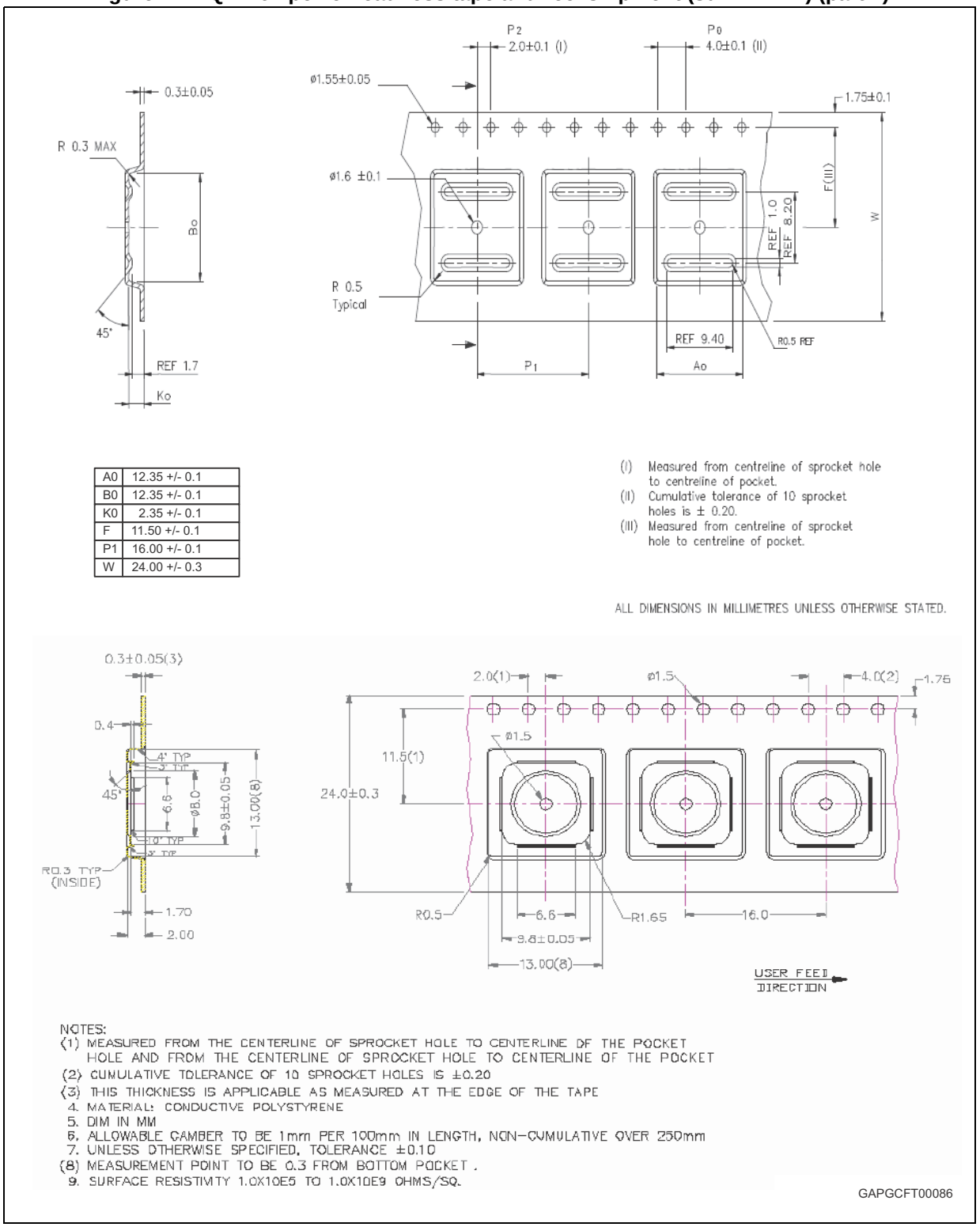
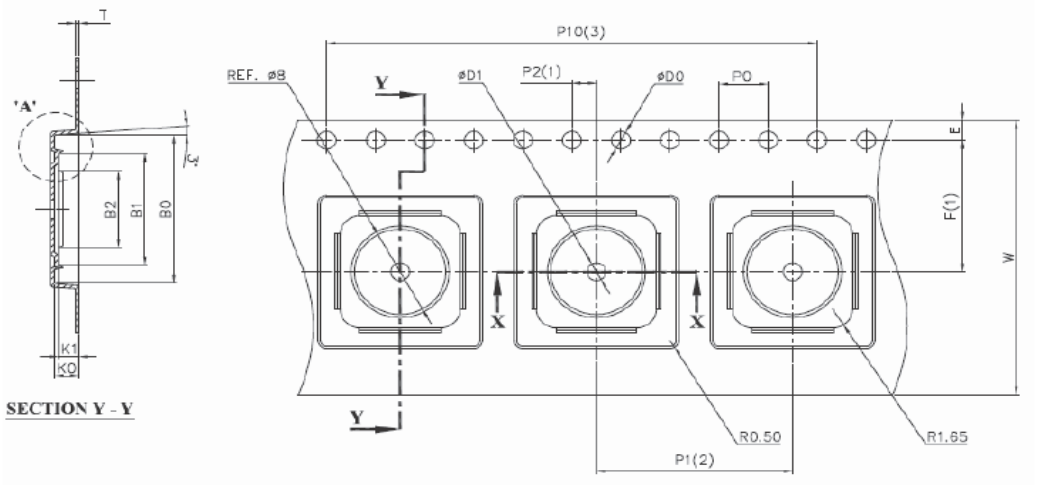


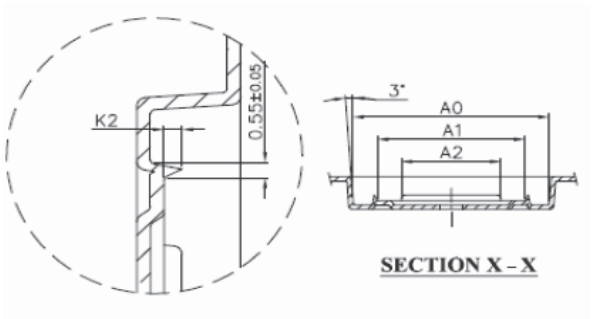
Figure 24. TQFP-64 power lead-less tape and reel shipment (suffix “TR”) (part 1)



A0	12.35 +/- 0.1
B0	12.35 +/- 0.1
K0	2.35 +/- 0.1
F	11.50 +/- 0.1
P1	16.00 +/- 0.1
W	24.00 +/- 0.3

Figure 25. TQFP-64 power lead-less tape and reel shipment (suffix “TR”) (part 2)





Dimension list			
Annote	Milimeter	Annote	Milimeter
A0	1.55+/-0.05	K2	0.40+/-0.10
A1	9.80+/-0.05	P0	4.00+/-0.10
A2	6.60+/-0.10	P1	16.00+/-0.10
B0	13.00+/-0.10	P2	2.00+/-0.10
B1	9.80+/-0.05	P10	40.00+/-0.20
B2	6.60+/-0.10	E	1.75+/-0.10
D0	1.55+/-0.05	F	11.50+/-0.10
D1	1.55+/-0.05	T	0.30+/-0.05
K0	2.00+/-0.10	W	24.00+/-0.30
K1	1.70+/-0.10		

GAPGCFT00087

7 Revision history

Table 45. Document revision history

Date	Revision	Change
12-Jun-2013	1	Initial release.
19-Sep-2013	2	Updated Disclaimer.

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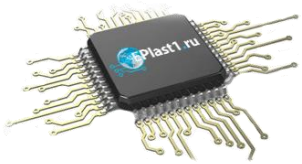

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.