

Automotive P-Channel 60 V (D-S) 175 °C MOSFET

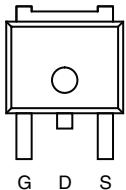
PRODUCT SUMMARY	
V_{DS} (V)	- 60
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.055
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.100
I_D (A)	- 20
Configuration	Single

FEATURES

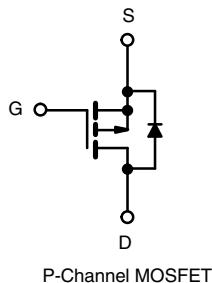
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 Qualified^d



TO-252



Top View



P-Channel MOSFET

ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD19P06-60L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	- 20	
		- 11	
Continuous Source Current (Diode Conduction) ^a	I_S	- 25	A
Pulsed Drain Current ^b	I_{DM}	- 80	
Single Pulse Avalanche Current	I_{AS}	- 24	mJ
Single Pulse Avalanche Energy	E_{AS}	28	
Maximum Power Dissipation ^b	P_D	46	W
		15	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	3.2	

Notes

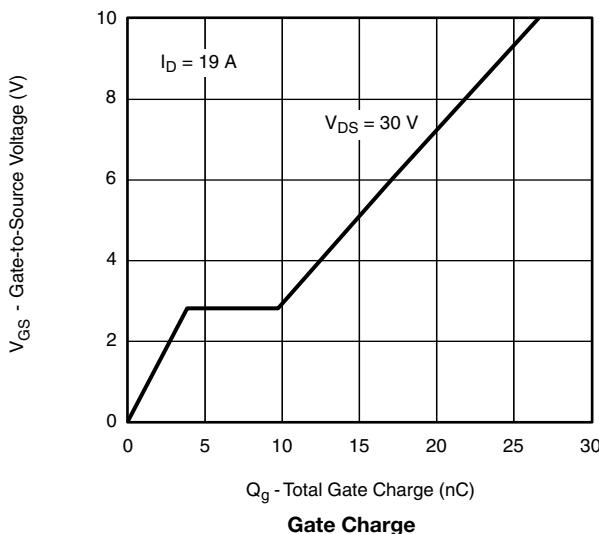
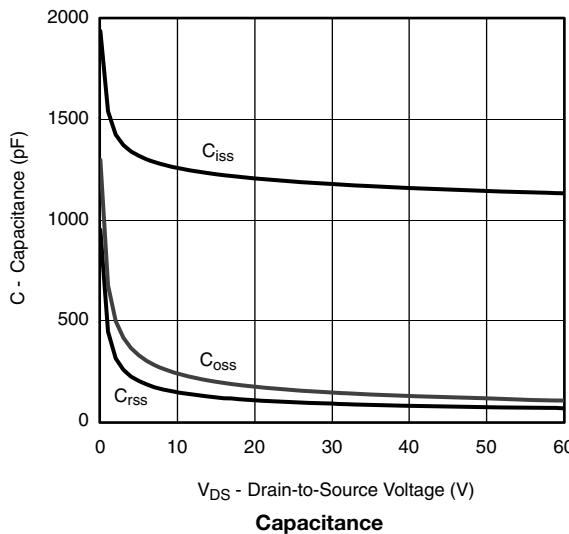
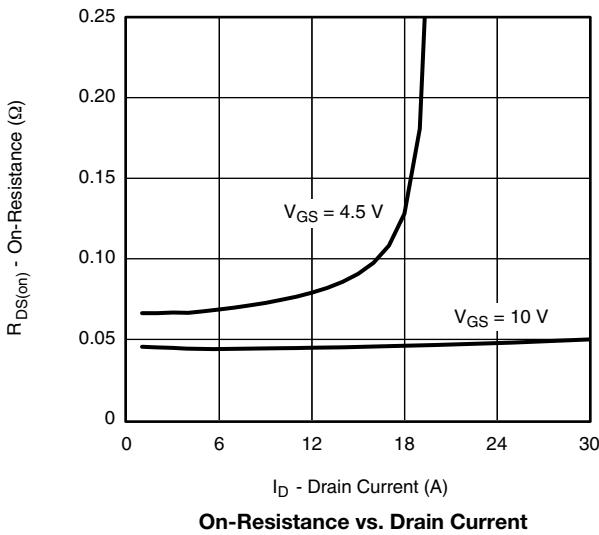
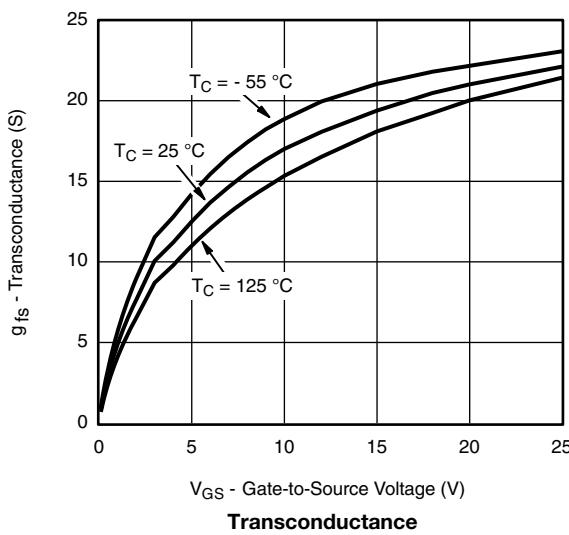
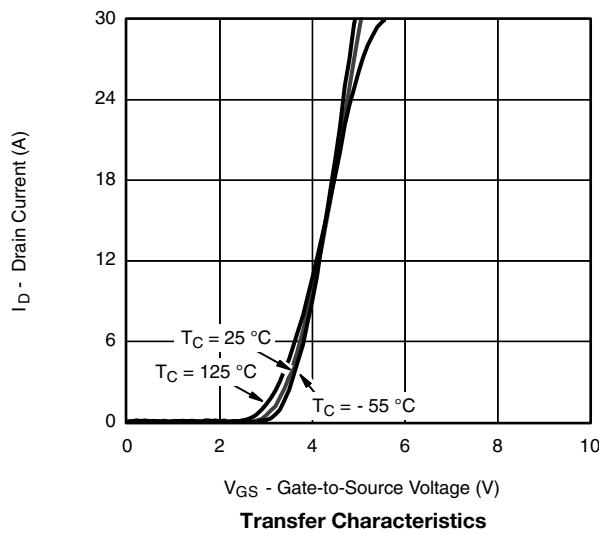
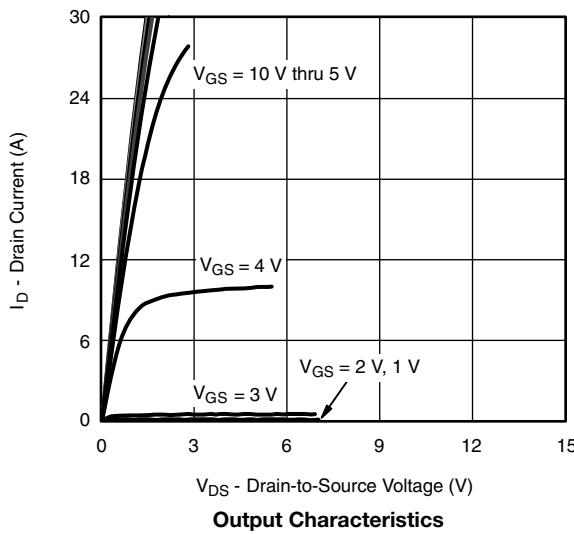
- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

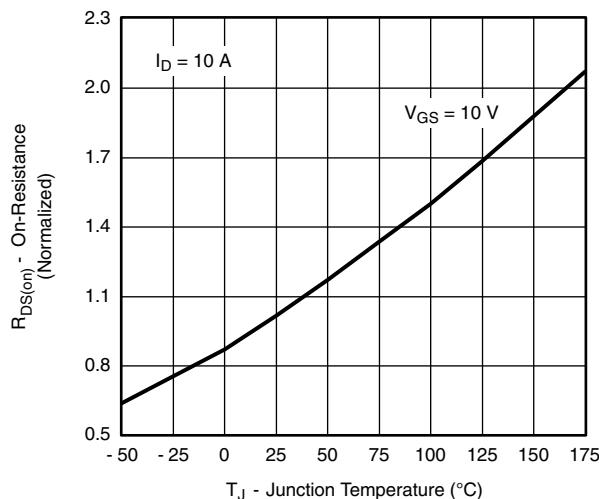
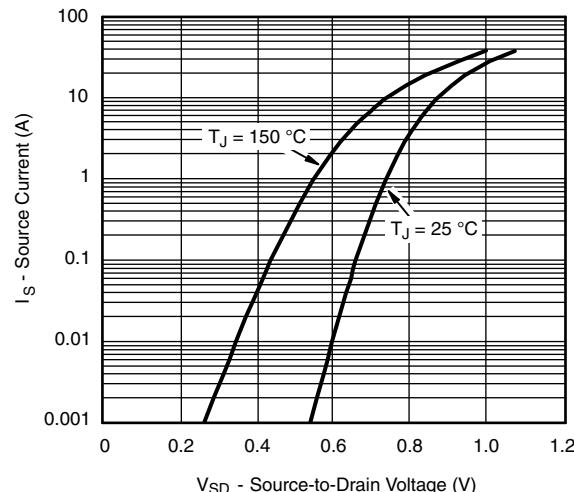
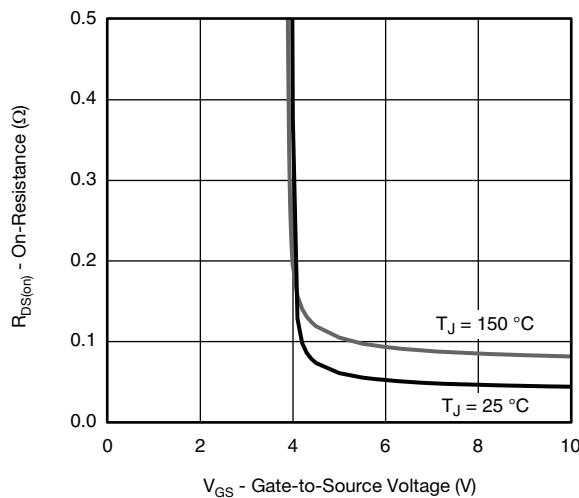
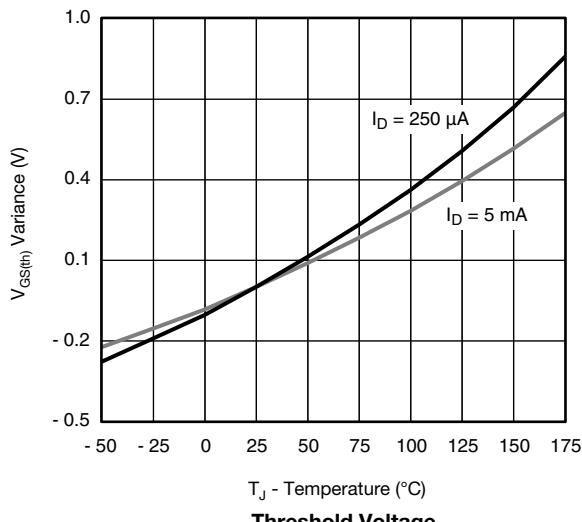
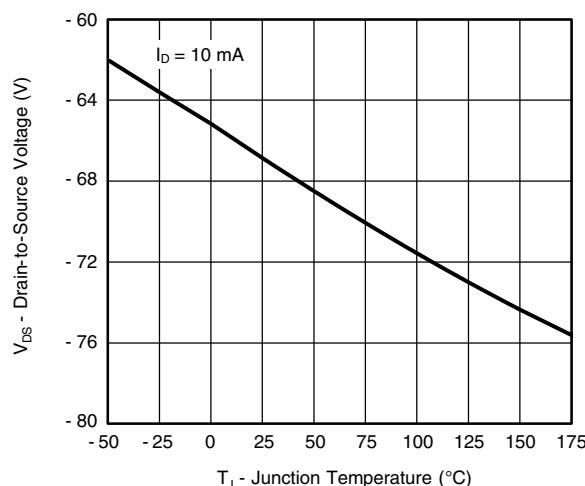
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = - 250 \mu\text{A}$		- 60	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = - 250 \mu\text{A}$		- 1.5	-	- 2.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}$	$V_{DS} = - 60 \text{ V}$	-	-	- 1	μA	
		$V_{GS} = 0 \text{ V}$	$V_{DS} = - 60 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	- 50		
		$V_{GS} = 0 \text{ V}$	$V_{DS} = - 60 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	- 150		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{GS} = - 10 \text{ V}$	$V_{DS} \leq - 5 \text{ V}$	- 20	-	-	A	
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = - 10 \text{ V}$	$I_D = - 19 \text{ A}$	-	0.046	0.055	Ω	
		$V_{GS} = - 10 \text{ V}$	$I_D = - 19 \text{ A}$, $T_J = 125^\circ\text{C}$	-	-	0.095		
		$V_{GS} = - 10 \text{ V}$	$I_D = - 19 \text{ A}$, $T_J = 175^\circ\text{C}$	-	-	0.125		
		$V_{GS} = - 4.5 \text{ V}$	$I_D = - 10 \text{ A}$	-	0.075	0.100		
Forward Transconductance ^a	g_{fs}	$V_{DS} = - 15 \text{ V}$, $I_D = - 17 \text{ A}$		-	20	-	S	
Dynamic^b								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = - 25 \text{ V}$, $f = 1 \text{ MHz}$	-	1192	1490	pF	
Output Capacitance	C_{oss}			-	160	200		
Reverse Transfer Capacitance	C_{rss}			-	96	120		
Total Gate Charge ^c	Q_g	$V_{GS} = - 10 \text{ V}$	$V_{DS} = - 30 \text{ V}$, $I_D = - 19 \text{ A}$	-	27	41	nC	
Gate-Source Charge ^c	Q_{gs}			-	3.9	-		
Gate-Drain Charge ^c	Q_{gd}			-	5.9	-		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		2.3	4.7	7.1	Ω	
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = - 30 \text{ V}$, $R_L = 1.6 \Omega$ $I_D \approx - 19 \text{ A}$, $V_{GEN} = - 10 \text{ V}$, $R_g = 1 \Omega$	$I_D = - 19 \text{ A}$, $V_{DS} = - 30 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	7	11	ns	
Rise Time ^c	t_r			-	9	14		
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			-	25	38		
Fall Time ^c	t_f			-	12	18		
Source-Drain Diode Ratings and Characteristics^b								
Pulsed Current ^a	I_{SM}			-	-	- 80	A	
Forward Voltage	V_{SD}	$I_F = - 10 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	- 0.85	- 1.5	V	

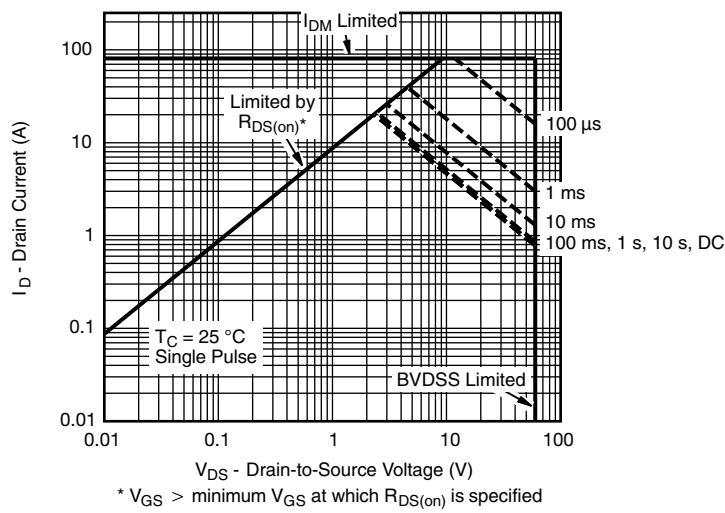
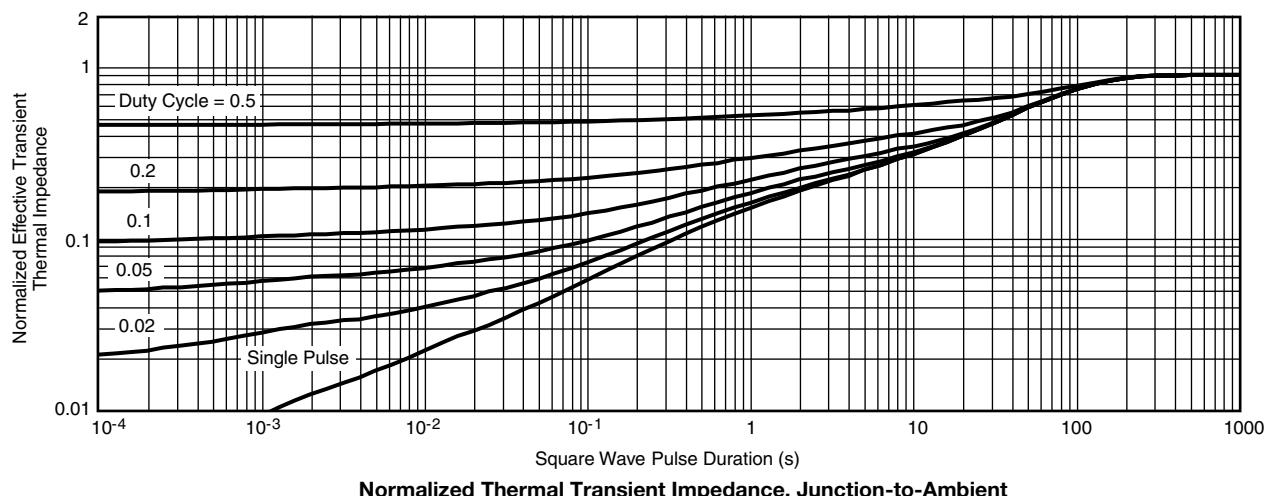
Notes

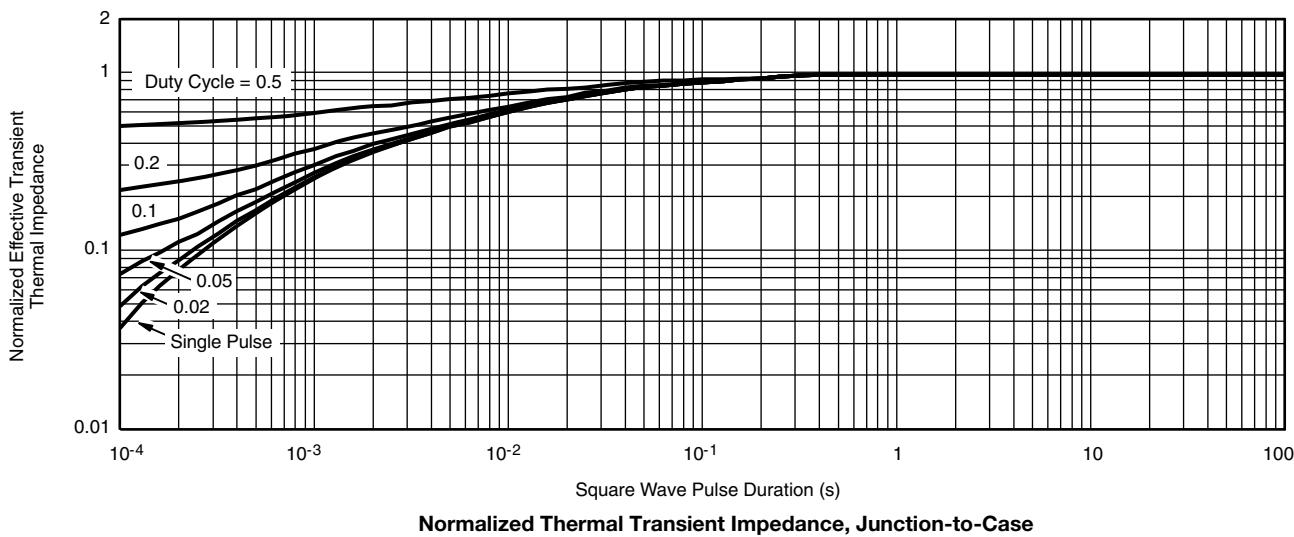
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

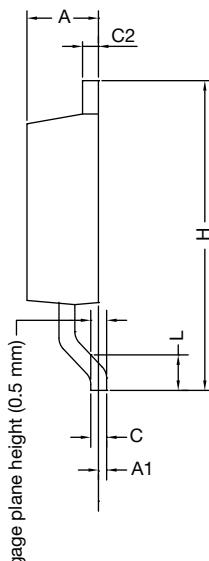
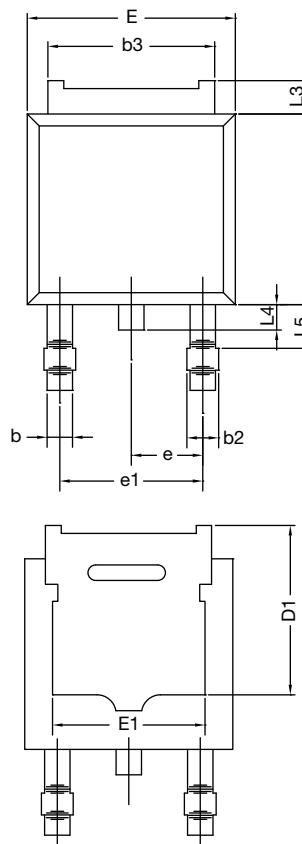
THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25°C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25°C)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65158.

TO-252AA Case Outline

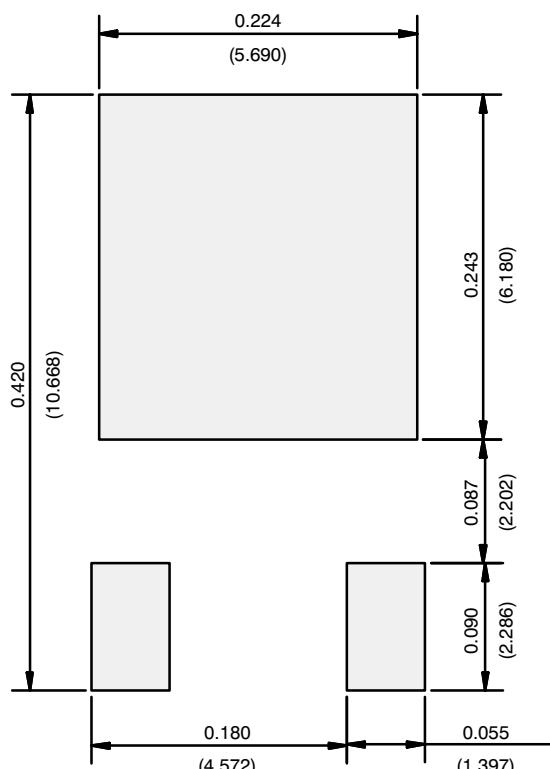


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0592-Rev. A, 02-Sep-13
DWG: 6019

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)

Recommended Minimum Pads
Dimensions in Inches/(mm)

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- Подбор аналогов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.