HN1B01FDW1T1G, SHN1B01FDW1T1G

Complementary Dual General Purpose Amplifier Transistor

PNP and NPN Surface Mount

Features

- High Voltage and High Current: V_{CEO} = 50 V, I_C = 200 mA
- High h_{FE}: h_{FE} = 200～400
- Moisture Sensitivity Level: 1
- ESD Rating
  - Human Body Model: 3A
  - Machine Model: C
- AEC−Q101 Qualified and PPAP Capable
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current − Continuous	I_C	200	mAdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation	P_D	380	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

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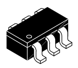
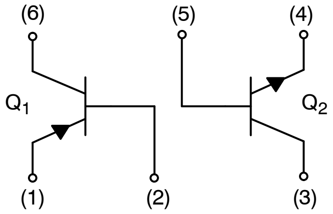
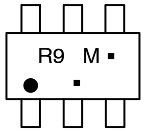


SC−74
CASE 318F
STYLE 3



MARKING DIAGRAM



R9 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
HN1B01FDW1T1G	SC−74 (Pb−Free)	3,000/Tape & Reel
SHN1B01FDW1T1G	SC−74 (Pb−Free)	3,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

November, 2011 − Rev. 3

Publication Order Number:
HN1B01FDW1T1/D

Q1: PNP

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−50	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	−60	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−7.0	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	−	−0.1	μAdc
Collector−Emitter Cutoff Current	I_{CEO}			
(V_{CE} = 10 Vdc, I_B = 0)		−	−0.1	μAdc
(V_{CE} = 30 Vdc, I_B = 0)		−	−2.0	μAdc
(V_{CE} = 30 Vdc, I_B = 0, T_A = 80°C)		−	−1.0	mAdc
DC Current Gain (Note 1) (V_{CE} = 6.0 Vdc, I_C = 2.0 mAdc)	h_{FE}	−200	−400	−
Collector−Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	−0.15	−0.3	Vdc

Q2: NPN

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	7.0	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	−	0.1	μAdc
Collector−Emitter Cutoff Current	I_{CEO}			
(V_{CE} = 10 Vdc, I_B = 0)		−	0.1	μAdc
(V_{CE} = 30 Vdc, I_B = 0)		−	2.0	μAdc
(V_{CE} = 30 Vdc, I_B = 0, T_A = 80°C)		−	1.0	mAdc
DC Current Gain (Note 1) (V_{CE} = 6.0 Vdc, I_C = 2.0 mAdc)	h_{FE}	200	400	−
Collector−Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	0.15	0.25	Vdc

1. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS: PNP Transistor

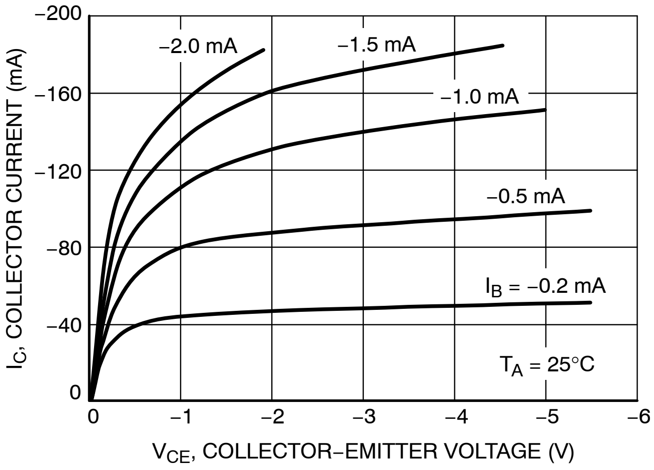


Figure 1. Collector Saturation Region

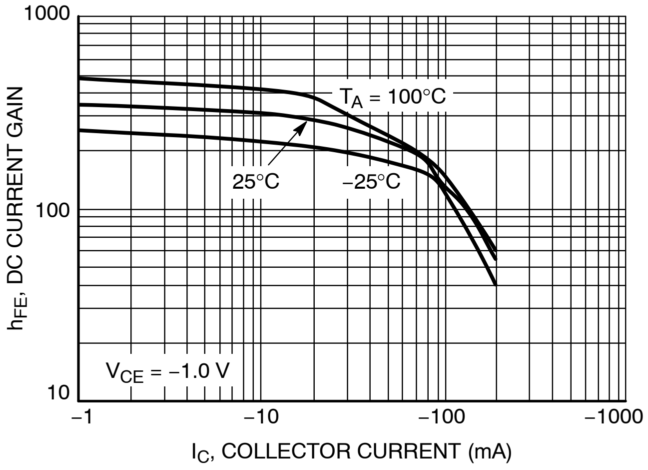


Figure 2. DC Current Gain

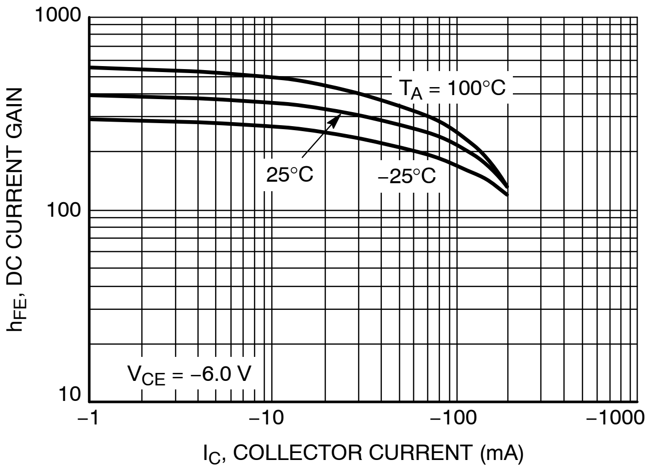


Figure 3. DC Current Gain

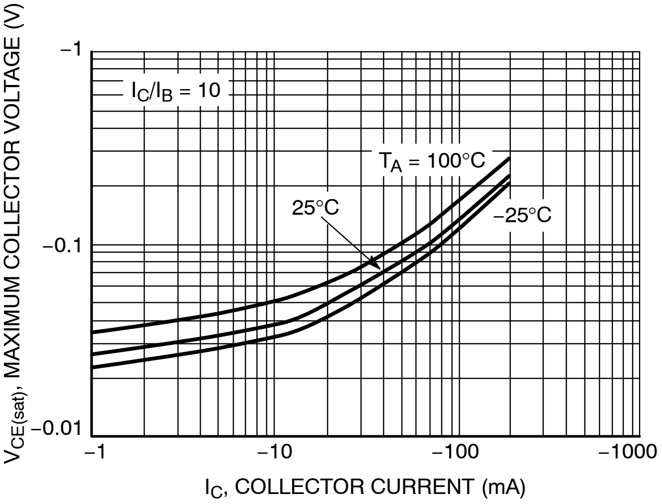


Figure 4. $V_{CE(sat)}$ versus I_C

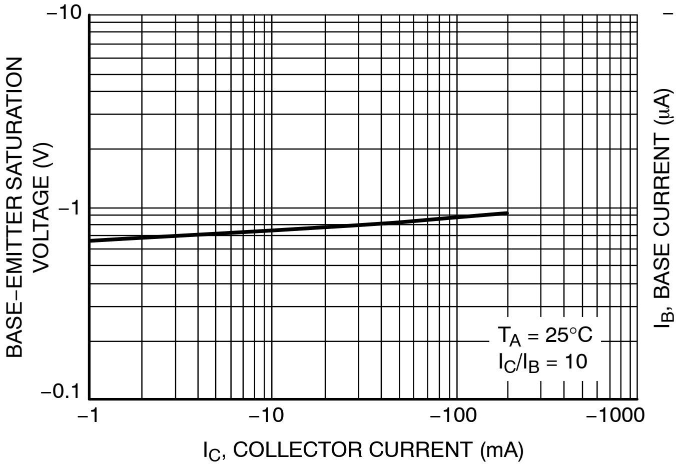


Figure 5. $V_{BE(sat)}$ versus I_C

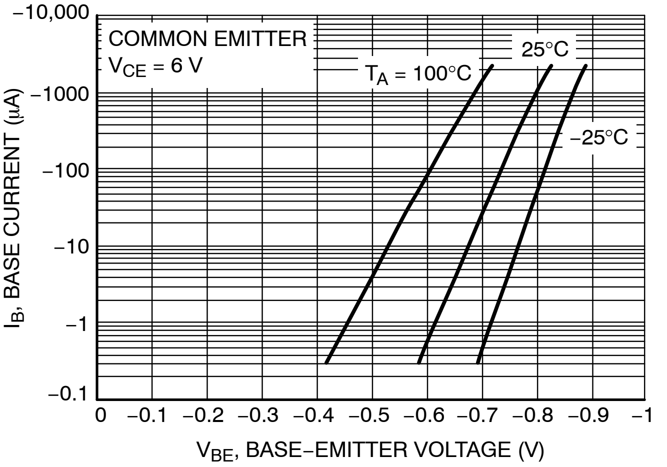


Figure 6. Base−Emitter Voltage

TYPICAL ELECTRICAL CHARACTERISTICS: NPN Transistor

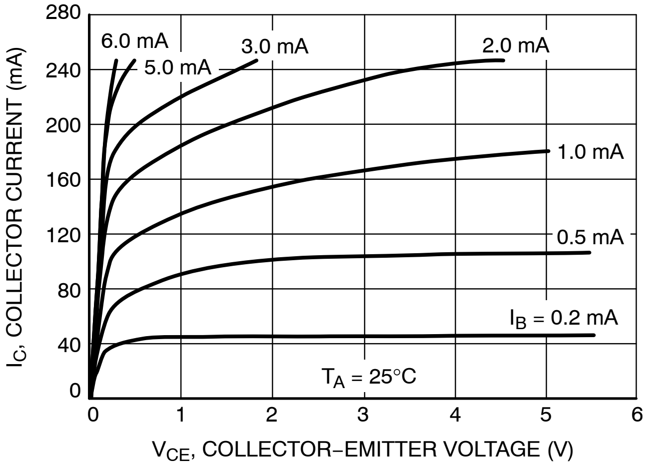


Figure 7. Collector Saturation Voltage

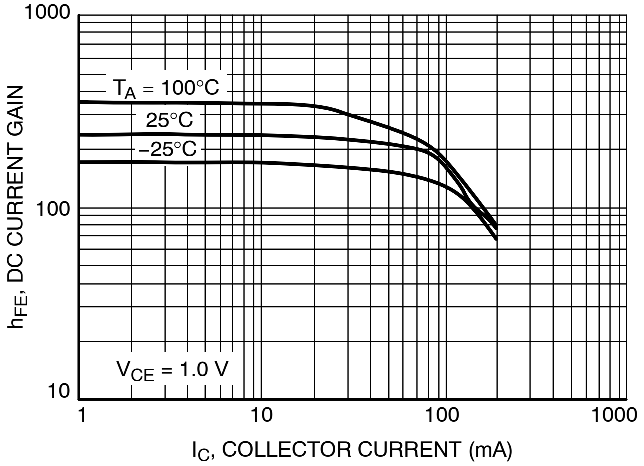


Figure 8. DC Current Gain

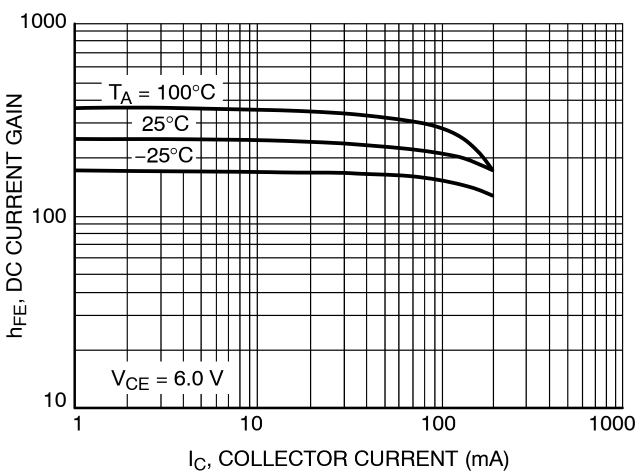


Figure 9. DC Current Gain

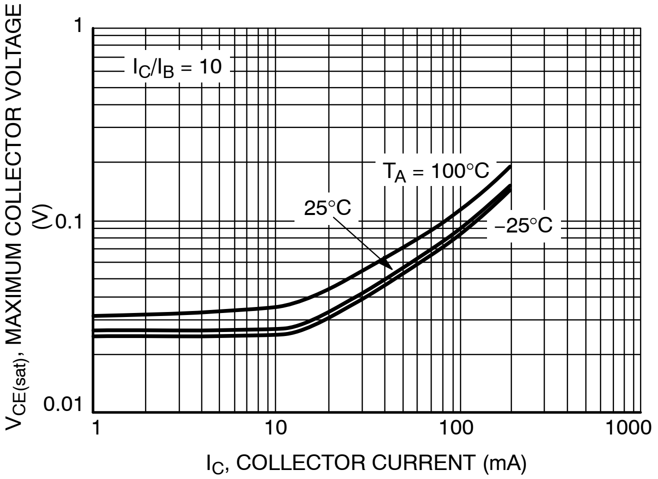


Figure 10. $V_{CE(sat)}$ versus I_C

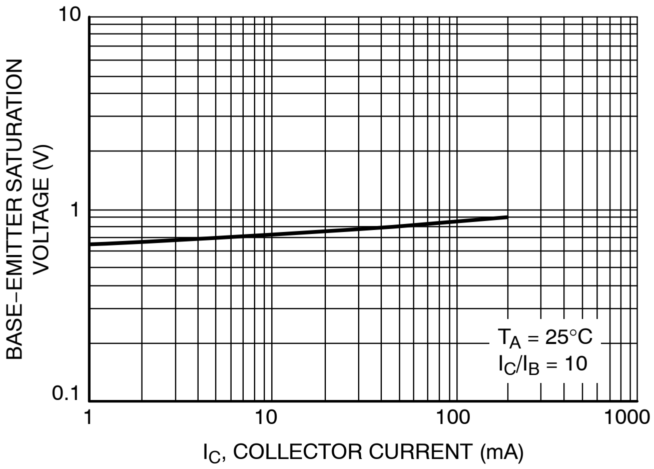


Figure 11. $V_{BE(sat)}$ versus I_C

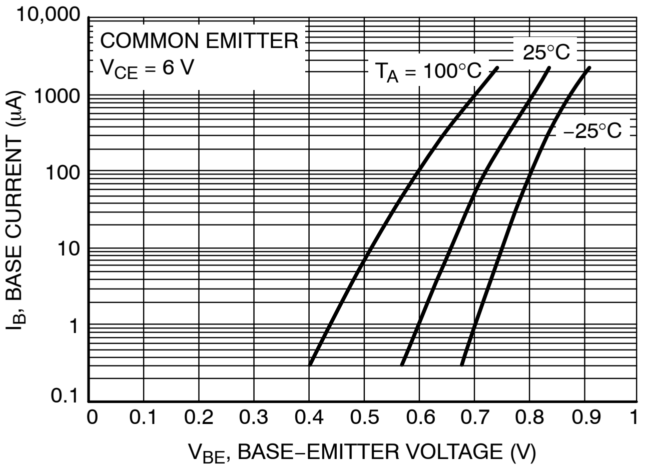


Figure 12. Base−Emitter Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

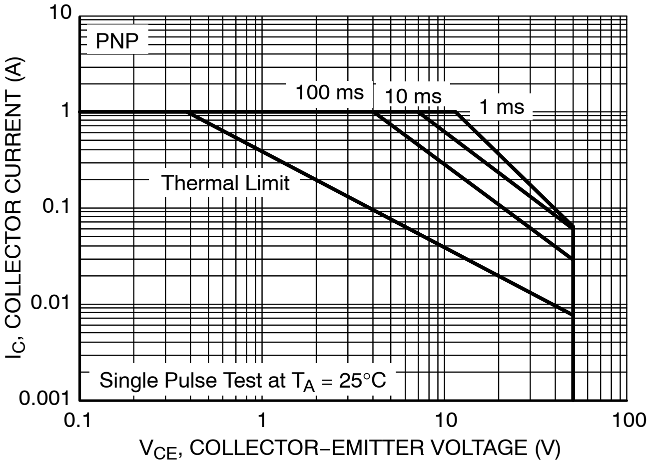


Figure 13. PNP Safe Operating Area

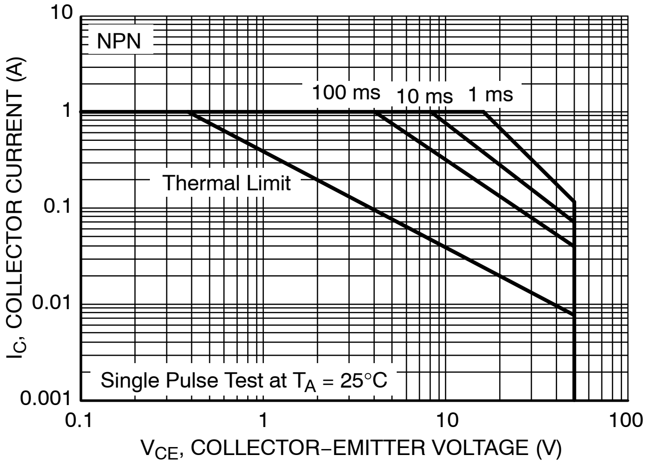
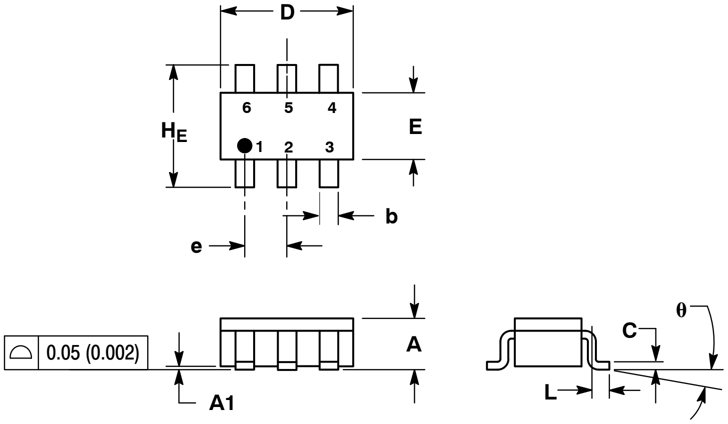


Figure 14. NPN Safe Operating Area

PACKAGE DIMENSIONS

SC−74

CASE 318F−05
ISSUE M

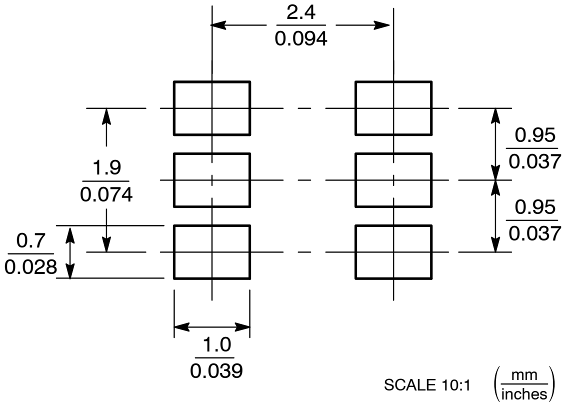


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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