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## PIC18F2X/4XQ10 Product Brief

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### Description

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PIC18F2x/4xQ10 microcontrollers feature Analog, Core Independent, and Communication Peripherals for a wide range of general purpose and low-power applications. These 28/40/44 -pin devices are equipped with a 10-bit ADC with Computation (ADC<sup>2</sup>) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and performing automatic threshold comparisons. They also offer a set of Core Independent Peripherals such as Complementary Waveform Generator (CWG), Windowed Watchdog Timer (WWDT), Cyclic Redundancy Check (CRC)/Memory Scan, Zero-Cross Detect (ZCD), Configurable Logic Cell (CLC), and Peripheral Pin Select (PPS), providing for increased design flexibility and lower system cost.

### Core Features

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- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input over the full  $V_{DD}$  range
  - 62.5 ns minimum instruction cycle
- Programmable 2-Level Interrupt Priority
- 31-Level Deep Hardware Stack
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Low-Current Power-on Reset (POR)
- Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

### Memory

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- Up to 128K Bytes Program Flash Memory
- Up to 3615 Bytes Data SRAM Memory
- Up to 1024 Bytes Data EEPROM
- Programmable Code Protection

- Direct, Indirect and Relative Addressing modes

## Operating Characteristics

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- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

## Power-Saving Operation Modes

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- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Extreme Low-Power mode (XLP)
  - Sleep: 500 nA typical @ 1.8V
  - Sleep and Watchdog Timer: 900 nA typical @ 1.8V

## Digital Peripherals

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- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:
  - Two CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- 10-Bit Pulse-Width Modulators (PWM):
  - Two 10-bit PWMs
- Serial Communications:
  - Up to Two Enhanced USART (EUSART) with Auto-Baud Detect, Auto-wake-up on Start. RS-232, RS-485, LIN compatible
  - SPI
  - I<sup>2</sup>C, SMBus and PMBus™ compatible
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change on all pins

- Input level selection control
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation
- Hardware Limit Timer (TMR2/4/6+HLT):
  - Hardware monitoring and Fault detection
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)

## **Analog Peripherals**

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- 10-Bit Analog-to-Digital Converter with Computation (ADC<sup>2</sup>):
  - Up to 35 external channels
  - Conversion available during sleep
  - Four internal analog channels
  - Internal and external trigger options
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - 8-bit hardware acquisition timer
- Hardware Capacitive Voltage Divider (CVD) Support:
  - 8-bit precharge timer
  - Adjustable sample and hold capacitor array
  - Guard ring digital output drive
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of  $V_{DD}$ ,  $[V_{Ref+} - V_{Ref-}]$ , FVR)
  - Internal connections to comparators and ADC
- Two Comparators (CMP):
  - Four external inputs
  - External output via PPS
- Fixed Voltage Reference (FVR) Module:
  - 1.024V, 2.048V and 4.096V output levels
  - Two buffered outputs: One for DAC/CMP and one for ADC

## **Clocking Structure**

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- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - $\pm 1\%$  at calibration
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)

- External High-frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if external clock stops
- Oscillator Start-up Timer (OST)

## Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

## PIC18F2x/4xQ10 Family Types

**Table 1. Devices included in this family**

| Device      | Program Memory Flash (bytes) | Data SRAM (bytes) | Data EEPROM (bytes) | I/O Pins | 16-bit Timers | Comparators | 10-bit ADC <sup>2</sup> with Computation (ch) | 5-bit DAC | Zero-Cross Detect | CCP/10-bit PWM | CWG | CLC | Low Voltage Detect (LVD) | 8-bit TMR with HLT | Windowed Watchdog Timer | CRC with Memory Scan | EUSART | I <sup>2</sup> C/SPI | PPS | Peripheral Module Disable | Temperature Indicator | Debug <sup>(1)</sup> |
|-------------|------------------------------|-------------------|---------------------|----------|---------------|-------------|-----------------------------------------------|-----------|-------------------|----------------|-----|-----|--------------------------|--------------------|-------------------------|----------------------|--------|----------------------|-----|---------------------------|-----------------------|----------------------|
| PIC18F24Q10 | 16k                          | 1024              | 256                 | 25       | 4             | 2           | 24                                            | 1         | 1                 | 2/2            | 1   | 0   | 1                        | 3                  | Y                       | Y                    | 1      | 1                    | Y   | Y                         | Y                     | I                    |
| PIC18F25Q10 | 32k                          | 2048              | 256                 | 25       | 4             | 2           | 24                                            | 1         | 1                 | 2/2            | 1   | 0   | 1                        | 3                  | Y                       | Y                    | 1      | 1                    | Y   | Y                         | Y                     | I                    |
| PIC18F26Q10 | 64k                          | 3615              | 1024                | 25       | 4             | 2           | 24                                            | 1         | 1                 | 2/2            | 1   | 8   | 1                        | 3                  | Y                       | Y                    | 2      | 2                    | Y   | Y                         | Y                     | I                    |
| PIC18F27Q10 | 128k                         | 3615              | 1024                | 25       | 4             | 2           | 24                                            | 1         | 1                 | 2/2            | 1   | 8   | 1                        | 3                  | Y                       | Y                    | 2      | 2                    | Y   | Y                         | Y                     | I                    |
| PIC18F45Q10 | 32k                          | 2048              | 256                 | 36       | 4             | 2           | 35                                            | 1         | 1                 | 2/2            | 1   | 8   | 1                        | 3                  | Y                       | Y                    | 2      | 2                    | Y   | Y                         | Y                     | I                    |
| PIC18F46Q10 | 64k                          | 3615              | 1024                | 36       | 4             | 2           | 35                                            | 1         | 1                 | 2/2            | 1   | 8   | 1                        | 3                  | Y                       | Y                    | 2      | 2                    | Y   | Y                         | Y                     | I                    |
| PIC18F47Q10 | 128k                         | 3615              | 1024                | 36       | 4             | 2           | 35                                            | 1         | 1                 | 2/2            | 1   | 8   | 1                        | 3                  | Y                       | Y                    | 2      | 2                    | Y   | Y                         | Y                     | I                    |

**Note:** Debugging Methods: (I) – Integrated on Chip.

## Packages



**Important:** For other small form-factor package availability and marking information, visit <http://www.microchip.com/packaging> or contact your local Microchip sales office.

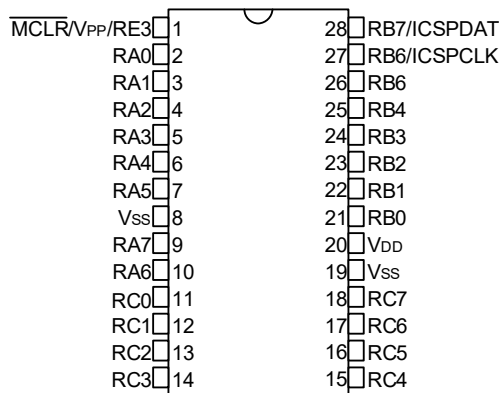
| Packages    | SPDIP<br>(SP) | SOIC<br>(SO) | SSOP<br>(SS) | QFN<br>(ML)<br>(6x6x0.9) | VQFN<br>(STX)<br>(4x4x1) | TQFP<br>(PT) | PDIP<br>(P) | VQFN<br>(NHX)<br>(5x5x0.9) | QFN<br>(ML)<br>(8x8) |
|-------------|---------------|--------------|--------------|--------------------------|--------------------------|--------------|-------------|----------------------------|----------------------|
| PIC18F24Q10 | •             | •            | •            | •                        | •                        |              |             |                            |                      |
| PIC18F25Q10 | •             | •            | •            | •                        | •                        |              |             |                            |                      |
| PIC18F26Q10 | •             | •            | •            | •                        | •                        |              |             |                            |                      |
| PIC18F27Q10 | •             | •            | •            | •                        | •                        |              |             |                            |                      |
| PIC18F45Q10 |               |              |              |                          |                          | •            | •           | •                          | •                    |
| PIC18F46Q10 |               |              |              |                          |                          | •            | •           | •                          | •                    |
| PIC18F47Q10 |               |              |              |                          |                          | •            | •           | •                          | •                    |



**Important:** Pin details are subject to change.

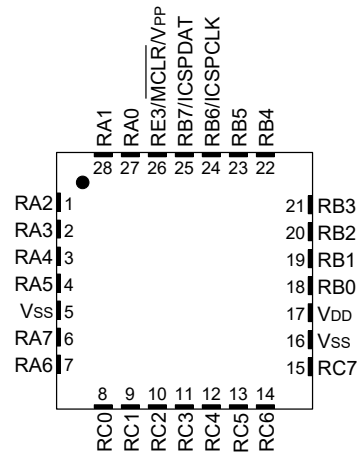
## Pin Diagrams

**Figure 1. 28-pin SPDIP, SSOP, SOIC**



Rev. 00-000-028A  
3/8/2017

**Figure 2. 28-pin QFN, VQFN**



**Note:** It is recommended that the exposed bottom pad be connected to  $V_{SS}$ , however it must not be the only  $V_{SS}$  connection to the device.

**Figure 3. 40-pin PDIP**

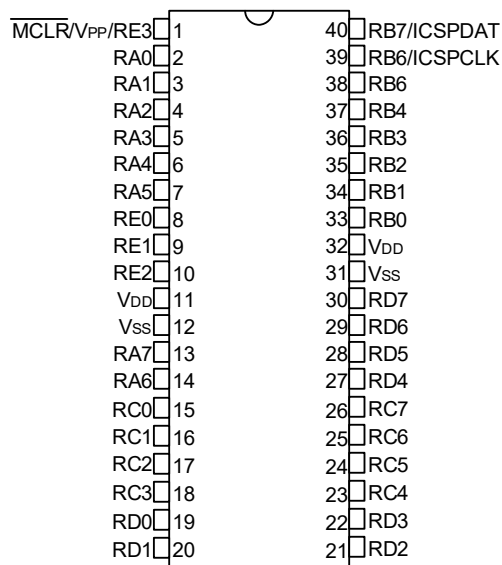
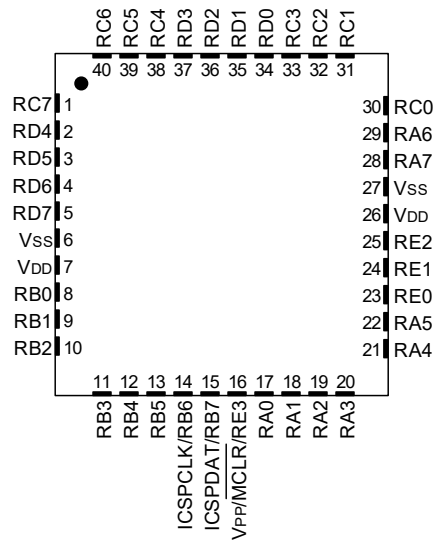


**Figure 4. 40-pinVQFN**

Rev. 00-000040B  
11/6/2017



**Note:** It is recommended that the exposed bottom pad be connected to  $V_{SS}$ , however it must not be the only  $V_{SS}$  connection to the device.

**Figure 5. 44-pin TQFP**

Rev. 00-000044A  
11/6/2017

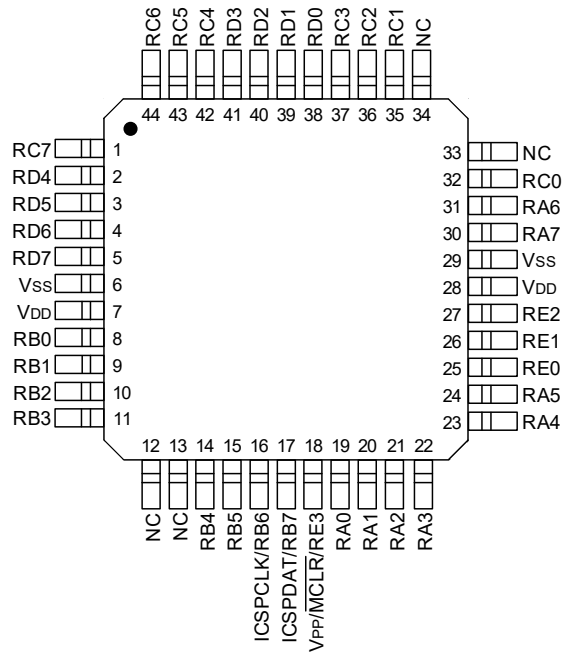
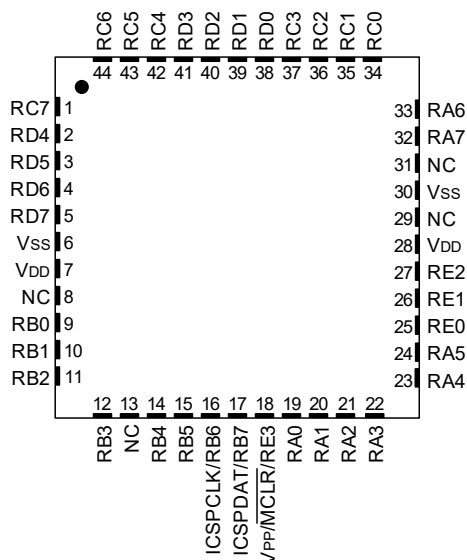


**Figure 6. 44-pin QFN**



**Note:** It is recommended that the exposed bottom pad be connected to  $V_{SS}$ , however it must not be the only  $V_{SS}$  connection to the device.

## Pin Allocation Tables

**Table 1. 28-Pin Allocation Table**

| I/O(2) | 28-Pin<br>SPDIP,<br>SOIC,<br>SSOP | 28-Pin<br>(V)QFN | A/D  | Reference                              | Comparator       | Timers               | CCP | CWG                 | ZCD   | Interrupt                    | EUSART | DSM                   | MSSP               | Pull-<br>up | Basic          |
|--------|-----------------------------------|------------------|------|----------------------------------------|------------------|----------------------|-----|---------------------|-------|------------------------------|--------|-----------------------|--------------------|-------------|----------------|
| RA0    | 2                                 | 27               | ANA0 | —                                      | C1IN0-<br>C2IN0- | —                    | —   | —                   | —     | IOCA0                        | —      | —                     | —                  | Y           | —              |
| RA1    | 3                                 | 28               | ANA1 | —                                      | C1IN1-<br>C2IN1- | —                    | —   | —                   | —     | IOCA1                        | —      | —                     | —                  | Y           | —              |
| RA2    | 4                                 | 1                | ANA2 | DAC1OUT1<br>Vref- (DAC)<br>Vref- (ADC) | C1IN0+<br>C2IN0+ | —                    | —   | —                   | —     | IOCA2                        | —      | —                     | —                  | Y           | —              |
| RA3    | 5                                 | 2                | ANA3 | Vref+ (DAC)<br>Vref+ (ADC)             | C1IN1+           | —                    | —   | —                   | —     | IOCA3                        | —      | MDCARL <sup>(1)</sup> | —                  | Y           | —              |
| RA4    | 6                                 | 3                | ANA4 | —                                      | —                | TOCKI <sup>(1)</sup> | —   | —                   | —     | IOCA4                        | —      | MDCARH <sup>(1)</sup> | —                  | Y           | —              |
| RA5    | 7                                 | 4                | ANA5 | —                                      | —                | —                    | —   | —                   | —     | IOCA5                        | —      | MDSRC <sup>(1)</sup>  | SS1 <sup>(1)</sup> | Y           | —              |
| RA6    | 10                                | 7                | ANA6 | —                                      | —                | —                    | —   | —                   | —     | IOCA6                        | —      | —                     | —                  | Y           | CLKOUT<br>OSC2 |
| RA7    | 9                                 | 6                | ANA7 | —                                      | —                | —                    | —   | —                   | —     | IOCA7                        | —      | —                     | —                  | Y           | OSC1<br>CLKIN  |
| RB0    | 21                                | 18               | ANB0 | —                                      | C2IN1+           | —                    | —   | CWG1 <sup>(1)</sup> | ZCDIN | IOCB0<br>INT0 <sup>(1)</sup> | —      | —                     | —                  | Y           | —              |
| RB1    | 22                                | 19               | ANB1 | —                                      | C1IN3-<br>C2IN3- | —                    | —   | —                   | —     | IOCB1<br>INT1 <sup>(1)</sup> | —      | —                     | —                  | Y           | —              |
| RB2    | 23                                | 20               | ANB2 | —                                      | —                | —                    | —   | —                   | —     | IOCB2<br>INT2 <sup>(1)</sup> | —      | —                     | —                  | Y           | —              |

| I/O <sup>(2)</sup> | 28-Pin<br>SPDIP,<br>SOIC,<br>SSOP | 28-Pin<br>(V)QFN | A/D              | Reference | Comparator       | Timers                                                             | CCP                          | CWG                              | ZCD | Interrupt | EUSART                                           | DSM | MSSP                                         | Pull-<br>up | Basic           |
|--------------------|-----------------------------------|------------------|------------------|-----------|------------------|--------------------------------------------------------------------|------------------------------|----------------------------------|-----|-----------|--------------------------------------------------|-----|----------------------------------------------|-------------|-----------------|
| RB3                | 24                                | 21               | ANB3             | —         | C1IN2-<br>C2IN2- | —                                                                  | —                            | —                                | —   | IOCB3     | —                                                | —   | —                                            | Y           | —               |
| RB4                | 25                                | 22               | ANB4             | —         | —                | T5G <sup>(1)</sup>                                                 | —                            | —                                | —   | IOCB4     | —                                                | —   | —                                            | Y           | —               |
| RB5                | 26                                | 23               | ANB5             | —         | —                | T1G <sup>(1)</sup>                                                 | —                            | —                                | —   | IOCB5     | —                                                | —   | —                                            | Y           | —               |
| RB6                | 27                                | 24               | ANB6             | —         | —                | —                                                                  | —                            | —                                | —   | IOCB6     | —                                                | —   | —                                            | Y           | ICSPCLK         |
| RB7                | 28                                | 25               | ANB7             | DAC1OUT2  | —                | T6IN <sup>(1)</sup>                                                | —                            | —                                | —   | IOCB7     | —                                                | —   | —                                            | Y           | ICSPDAT         |
| RC0                | 11                                | 8                | ANC0             | —         | —                | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup> | —                            | —                                | —   | IOCC0     | —                                                | —   | —                                            | Y           | SOSCO           |
| RC1                | 12                                | 9                | ANC1             | —         | —                | —                                                                  | CCP2 <sup>(1)</sup>          | —                                | —   | IOCC1     | —                                                | —   | —                                            | Y           | SOSCIN<br>SOSCI |
| RC2                | 13                                | 10               | ANC2             | —         | —                | T5CKI <sup>(1)</sup>                                               | CCP1 <sup>(1)</sup>          | —                                | —   | IOCC2     | —                                                | —   | —                                            | Y           | —               |
| RC3                | 14                                | 11               | ANC3             | —         | —                | T2IN <sup>(1)</sup>                                                | —                            | —                                | —   | IOCC3     | —                                                | —   | SCK1 <sup>(1)</sup><br>SCL1 <sup>(3,4)</sup> | Y           | —               |
| RC4                | 15                                | 12               | ANC4             | —         | —                | —                                                                  | —                            | —                                | —   | IOCC4     | —                                                | —   | SDI1 <sup>(1)</sup><br>SDA1 <sup>(3,4)</sup> | Y           | —               |
| RC5                | 16                                | 13               | ANC5             | —         | —                | T4IN <sup>(1)</sup>                                                | —                            | —                                | —   | IOCC5     | —                                                | —   | —                                            | Y           | —               |
| RC6                | 17                                | 14               | ANC6             | —         | —                | —                                                                  | —                            | —                                | —   | IOCC6     | CK1 <sup>(1,3)</sup>                             | —   | —                                            | Y           | —               |
| RC7                | 18                                | 15               | ANC7             | —         | —                | —                                                                  | —                            | —                                | —   | IOCC7     | RX1/<br>DT1 <sup>(1,3)</sup>                     | —   | —                                            | Y           | —               |
| RE3                | 1                                 | 26               | —                | —         | —                | —                                                                  | —                            | —                                | —   | IOCE3     | —                                                | —   | —                                            | Y           | Vpp/MCLR        |
| VSS                | 19                                | 16               | —                | —         | —                | —                                                                  | —                            | —                                | —   | —         | —                                                | —   | —                                            | —           | VSS             |
| VDD                | 20                                | 17               | —                | —         | —                | —                                                                  | —                            | —                                | —   | —         | —                                                | —   | —                                            | —           | VDD             |
| VSS                | 8                                 | 5                | —                | —         | —                | —                                                                  | —                            | —                                | —   | —         | —                                                | —   | —                                            | —           | VSS             |
| OUT <sup>(2)</sup> | —                                 | —                | ADGRDA<br>ADGRDB | —         | C1OUT<br>C2OUT   | TMR0                                                               | CCP1<br>CCP2<br>PWM3<br>PWM4 | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D | —   | —         | TX1/<br>CK1 <sup>(3)</sup><br>DT1 <sup>(3)</sup> | DSM | SDO1<br>SCK1                                 | —           | —               |

**Note:**

- This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
- All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
- This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- These pins are configured for I<sup>2</sup>C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

**Table 2. 40/44-Pin Allocation Table**

| I/O <sup>(2)</sup> | 40-Pin<br>PDIP | 40-Pin<br>VQFN | 44-Pin<br>QFN | 44-Pin<br>TQFP | A/D  | Reference                                  | Comparator       | Timers | CCP | CWG | ZCD | Interrupt | EUSART | DSM                   | MSSP | Pull-<br>up | Basic |
|--------------------|----------------|----------------|---------------|----------------|------|--------------------------------------------|------------------|--------|-----|-----|-----|-----------|--------|-----------------------|------|-------------|-------|
| RA0                | 2              | 17             | 19            | 19             | ANA0 | —                                          | C1IN0-<br>C2IN0- | —      | —   | —   | —   | IOCA0     | —      | —                     | —    | Y           | —     |
| RA1                | 3              | 18             | 20            | 20             | ANA1 | —                                          | C1IN1-<br>C2IN1- | —      | —   | —   | —   | IOCA1     | —      | —                     | —    | Y           | —     |
| RA2                | 4              | 19             | 21            | 21             | ANA2 | DAC1OUT1<br>Vref-<br>(DAC5)<br>Vref- (ADC) | C1IN0+<br>C2IN0+ | —      | —   | —   | —   | IOCA2     | —      | —                     | —    | Y           | —     |
| RA3                | 5              | 20             | 22            | 22             | ANA3 | Vref+<br>(DAC5)                            | C1IN1+           | —      | —   | —   | —   | IOCA3     | —      | MDCARL <sup>(1)</sup> | —    | Y           | —     |

# PIC18F2X/4XQ10

| I/O <sup>(2)</sup> | 40-Pin<br>PDIP | 40-Pin<br>VQFN | 44-Pin<br>QFN | 44-Pin<br>TQFP | A/D  | Reference      | Comparator       | Timers                                                             | CCP                 | CWG                 | ZCD   | Interrupt                    | EUSART                       | DSM                   | MSSP                                         | Pull-up | Basic           |
|--------------------|----------------|----------------|---------------|----------------|------|----------------|------------------|--------------------------------------------------------------------|---------------------|---------------------|-------|------------------------------|------------------------------|-----------------------|----------------------------------------------|---------|-----------------|
|                    |                |                |               |                |      | Vref+<br>(ADC) |                  |                                                                    |                     |                     |       |                              |                              |                       |                                              |         |                 |
| RA4                | 6              | 21             | 23            | 23             | ANA4 | —              | —                | T0CKI <sup>(1)</sup>                                               | —                   | —                   | —     | IOCA4                        | —                            | MDCARH <sup>(1)</sup> | —                                            | Y       | —               |
| RA5                | 7              | 22             | 24            | 24             | ANA5 | —              | —                | —                                                                  | —                   | —                   | —     | IOCA5                        | —                            | MDSRC <sup>(1)</sup>  | SS1 <sup>(1)</sup>                           | Y       | —               |
| RA6                | 14             | 29             | 33            | 31             | ANA6 | —              | —                | —                                                                  | —                   | —                   | —     | IOCA6                        | —                            | —                     | —                                            | Y       | CLKOUT<br>OSC2  |
| RA7                | 13             | 28             | 32            | 30             | ANA7 | —              | —                | —                                                                  | —                   | —                   | —     | IOCA7                        | —                            | —                     | —                                            | Y       | OSC1<br>CLKIN   |
| RB0                | 33             | 8              | 9             | 8              | ANB0 | —              | C2IN1+           | —                                                                  | —                   | CWG1 <sup>(1)</sup> | ZCDIN | IOCB0<br>INT0 <sup>(1)</sup> | —                            | —                     | SS2 <sup>(1)</sup>                           | Y       | —               |
| RB1                | 34             | 9              | 10            | 9              | ANB1 | —              | C1IN3-<br>C2IN3- | —                                                                  | —                   | —                   | —     | IOCB1<br>INT1 <sup>(1)</sup> | —                            | —                     | SCK2 <sup>(1)</sup><br>SCL2 <sup>(3,4)</sup> | Y       | —               |
| RB2                | 35             | 10             | 11            | 10             | ANB2 | —              | —                | —                                                                  | —                   | —                   | —     | IOCB2<br>INT2 <sup>(1)</sup> | —                            | —                     | SDI2 <sup>(1)</sup><br>SDA2 <sup>(3,4)</sup> | Y       | —               |
| RB3                | 36             | 11             | 12            | 11             | ANB3 | —              | C1IN2-<br>C2IN2- | —                                                                  | —                   | —                   | —     | IOCB3                        | —                            | —                     | —                                            | Y       | —               |
| RB4                | 37             | 12             | 14            | 14             | ANB4 | —              | —                | T5G <sup>(1)</sup>                                                 | —                   | —                   | —     | IOCB4                        | —                            | —                     | —                                            | Y       | —               |
| RB5                | 38             | 13             | 15            | 15             | ANB5 | —              | —                | T1G <sup>(1)</sup>                                                 | —                   | —                   | —     | IOCB5                        | —                            | —                     | —                                            | Y       | —               |
| RB6                | 39             | 14             | 16            | 16             | ANB6 | —              | —                | —                                                                  | —                   | —                   | —     | IOCB6                        | CK2 <sup>(1,3)</sup>         | —                     | —                                            | Y       | ICSPCLK         |
| RB7                | 40             | 15             | 17            | 17             | ANB7 | DAC1OUT2       | —                | T6IN <sup>(1)</sup>                                                | —                   | —                   | —     | IOCB7                        | RX2/<br>DT2 <sup>(1,3)</sup> | —                     | —                                            | Y       | ICSPDAT         |
| RC0                | 15             | 30             | 34            | 32             | ANC0 | —              | —                | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup> | —                   | —                   | —     | IOCC0                        | —                            | —                     | —                                            | Y       | SOSCO           |
| RC1                | 16             | 31             | 35            | 35             | ANC1 | —              | —                | —                                                                  | CCP2 <sup>(1)</sup> | —                   | —     | IOCC1                        | —                            | —                     | —                                            | Y       | SOSCIN<br>SOSCI |
| RC2                | 17             | 32             | 36            | 36             | ANC2 | —              | —                | T5CKI <sup>(1)</sup>                                               | CCP1 <sup>(1)</sup> | —                   | —     | IOCC2                        | —                            | —                     | —                                            | Y       | —               |
| RC3                | 18             | 33             | 37            | 37             | ANC3 | —              | —                | T2IN <sup>(1)</sup>                                                | —                   | —                   | —     | IOCC3                        | —                            | —                     | SCK1 <sup>(1)</sup><br>SCL1 <sup>(3,4)</sup> | Y       | —               |
| RC4                | 23             | 38             | 42            | 42             | ANC4 | —              | —                | —                                                                  | —                   | —                   | —     | IOCC4                        | —                            | —                     | SDI1 <sup>(1)</sup><br>SDA1 <sup>(3,4)</sup> | —       | —               |
| RC5                | 24             | 39             | 43            | 43             | ANC5 | —              | —                | T4IN <sup>(1)</sup>                                                | —                   | —                   | —     | IOCC5                        | —                            | —                     | —                                            | Y       | —               |
| RC6                | 25             | 40             | 44            | 44             | ANC6 | —              | —                | —                                                                  | —                   | —                   | —     | IOCC6                        | CK1 <sup>(1,3)</sup>         | —                     | —                                            | Y       | —               |
| RC7                | 26             | 1              | 1             | 1              | ANC7 | —              | —                | —                                                                  | —                   | —                   | —     | IOCC7                        | RX1/<br>DT1 <sup>(1,3)</sup> | —                     | —                                            | Y       | —               |
| RD0                | 19             | 34             | 38            | 38             | AND0 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD1                | 20             | 35             | 39            | 39             | AND1 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD2                | 21             | 36             | 40            | 40             | AND2 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD3                | 22             | 37             | 41            | 41             | AND3 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD4                | 27             | 2              | 2             | 2              | AND4 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD5                | 28             | 3              | 3             | 3              | AND5 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD6                | 29             | 4              | 4             | 4              | AND6 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RD7                | 30             | 5              | 5             | 5              | AND7 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RE0                | 8              | 23             | 25            | 25             | ANE0 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |
| RE1                | 9              | 24             | 26            | 26             | ANE1 | —              | —                | —                                                                  | —                   | —                   | —     | —                            | —                            | —                     | —                                            | Y       | —               |

# PIC18F2X/4XQ10

| I/O <sup>(2)</sup> | 40-Pin<br>PDIP | 40-Pin<br>VQFN | 44-Pin<br>QFN | 44-Pin<br>TQFP | A/D              | Reference | Comparator     | Timers | CCP                          | CWG                              | ZCD | Interrupt | EUSART                                                                                               | DSM | MSSP                         | Pull-up | Basic        |
|--------------------|----------------|----------------|---------------|----------------|------------------|-----------|----------------|--------|------------------------------|----------------------------------|-----|-----------|------------------------------------------------------------------------------------------------------|-----|------------------------------|---------|--------------|
| RE2                | 10             | 25             | 27            | 27             | ANE2             | —         | —              | —      | —                            | —                                | —   | —         | —                                                                                                    | —   | —                            | Y       | —            |
| RE3                | 1              | 16             | 18            | 18             | —                | —         | —              | —      | —                            | —                                | —   | IOCE3     | —                                                                                                    | —   | —                            | Y       | Vpp/<br>MCLR |
| VSS                | 12             | 6              | 6             | 6              | —                | —         | —              | —      | —                            | —                                | —   | —         | —                                                                                                    | —   | —                            | —       | VSS          |
| VDD                | 11             | 7              | 7             | 7              | —                | —         | —              | —      | —                            | —                                | —   | —         | —                                                                                                    | —   | —                            | —       | VDD          |
| VDD                | 32             | 26             | 28            | 28             | —                | —         | —              | —      | —                            | —                                | —   | —         | —                                                                                                    | —   | —                            | —       | VSS          |
| VSS                | 31             | 27             | 30            | 29             | —                | —         | —              | —      | —                            | —                                | —   | —         | —                                                                                                    | —   | —                            | —       | VSS          |
| OUT <sup>(2)</sup> | —              | —              | —             | —              | ADGRDA<br>ADGRDB | —         | C1OUT<br>C2OUT | TMR0   | CCP1<br>CCP2<br>PWM3<br>PWM4 | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D | —   | —         | TX1/<br>CK1 <sup>(3)</sup><br>DT1 <sup>(3)</sup><br>TX2/<br>CK2 <sup>(3)</sup><br>DT2 <sup>(3)</sup> | DSM | SDO1<br>SCK1<br>SDO2<br>SCK2 | —       | —            |

## Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
2. All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I<sup>2</sup>C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

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