



CMOS Static RAM 16K (4K x 4-Bit)

IDT6168SA
IDT6168LA

Features

- ♦ High-speed (equal access and cycle time)
 - Military: 25/45ns (max.)
 - Industrial: 25ns (max.)
 - Commercial: 15/20/25ns (max.)
- ♦ Low power consumption
- ♦ Battery backup operation—2V data retention voltage (IDT6168LA only)
- ♦ Available in high-density 20-pin ceramic or plastic DIP and 20-pin leadless chip carrier (LCC)
- ♦ Produced with advanced CMOS high-performance technology
- ♦ CMOS process virtually eliminates alpha particle soft-error rates
- ♦ Bidirectional data input and output
- ♦ Military product compliant to MIL-STD-883, Class B

Description

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability

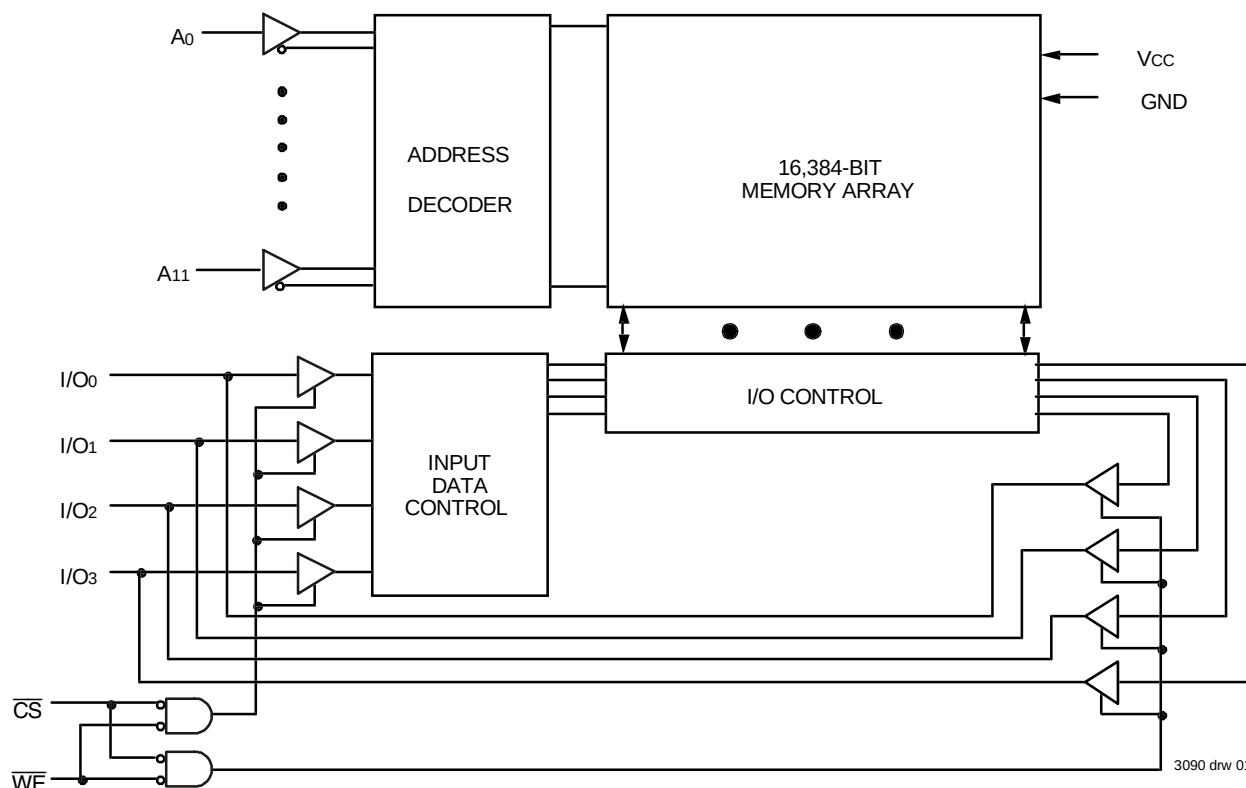
CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 μ W operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP or a 20-pin LCC providing high board-level packing densities.

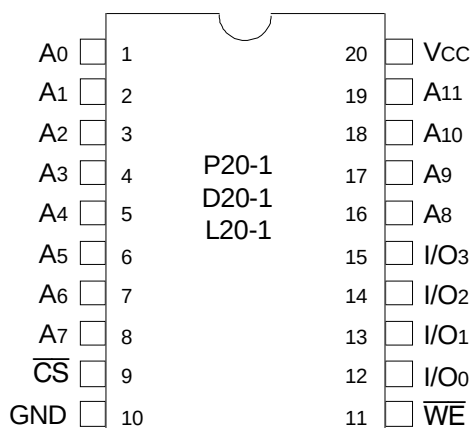
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



FEBRUARY 2001

Pin Configurations



3090 drw 02

DIP/LCC Top View

Pin Descriptions

Name	Description
A ₀ - A ₁₁	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O ₀ - I/O ₃	Data Input/Output
V _{CC}	Power
GND	Ground

3090 tbl 01

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	7	pF
C _{IO}	I/O Capacitance	V _{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

3090 tbl 02

Truth Table⁽¹⁾

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	D _{IN}	Active

3090 tbl 03

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

3090 tbl 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

3090 tbl 05

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-45°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

DC Electrical Characteristics⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA15		6168SA20 6168LA20		6168SA25 6168LA25		6168SA45 6168LA45		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l. & Ind.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = 0 ⁽²⁾	SA	110	—	90	—	90	100	—	100	mA
		LA	—	—	70	—	70	80	—	80	
I _{CC2}	Dynamic Operating Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	SA	145	—	120	—	110	120	—	110	mA
		LA	—	—	100	—	90	100	—	80	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	SA	55	—	45	—	35	45	—	35	mA
		LA	—	—	30	—	25	30	—	25	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} , f = 0 ⁽²⁾	SA	20	—	20	—	3	10	—	10	mA
		LA	—	—	0.5	—	0.5	0.3	—	0.3	

3090 tbl 07

NOTES:

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/trc, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.

DC Electrical Characteristics

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6168SA		IDT6168LA		Unit
				Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL. COM'L.	— —	10 2	— —	5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., CS = V _{IH} , V _{OUT} = GND to V _{CC}	MIL. COM'L.	— —	10 2	— —	5 2	μA
V _{OL}	Output LOW Voltage	I _{OL} = 10mA, V _{CC} = Min.		—	0.5	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.		—	0.4	—	0.4	
V _{OH}	Output HIGH Voltage	I _{OH} = -4mA, V _{CC} = Min.		2.4	—	2.4	—	V

3090 tbl 09

Data Retention Characteristics (LA Version Only)

$V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

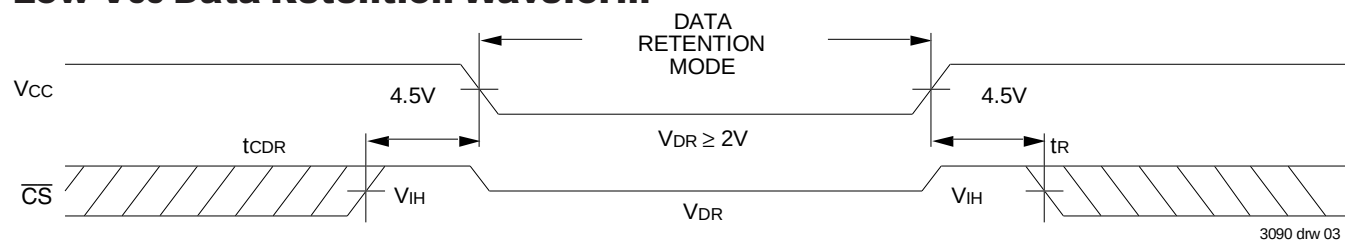
Symbol	Parameter	Test Condition	IDT6168LA			Unit
			Min.	Typ. ⁽¹⁾	Max.	
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ $or \leq V_{LC}$	2.0	—	—	V
I_{CDR}	Data Retention Current		—	0.5 ⁽²⁾ 1.0 ⁽³⁾	100 ⁽²⁾ 150 ⁽³⁾	μA
$t_{CDR}^{(5)}$	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(6)}$	Operation Recovery Time		$t_{RC}^{(4)}$	—	—	ns

3090 tbl 10

NOTES:

1. $T_A = +25^\circ C$.
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3090 tbl 11

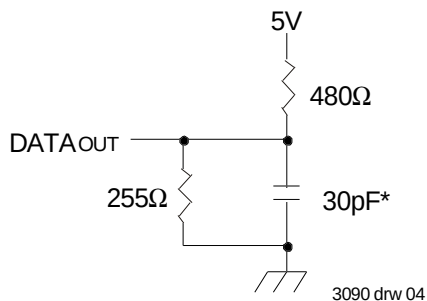


Figure 1. AC Test Load

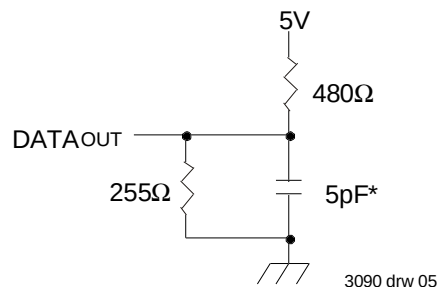


Figure 2. AC Test Load
(for tCHZ, tCLZ, tWHZ and tOW)

*Includes scope and jig capacitances

AC Electrical Characteristics (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

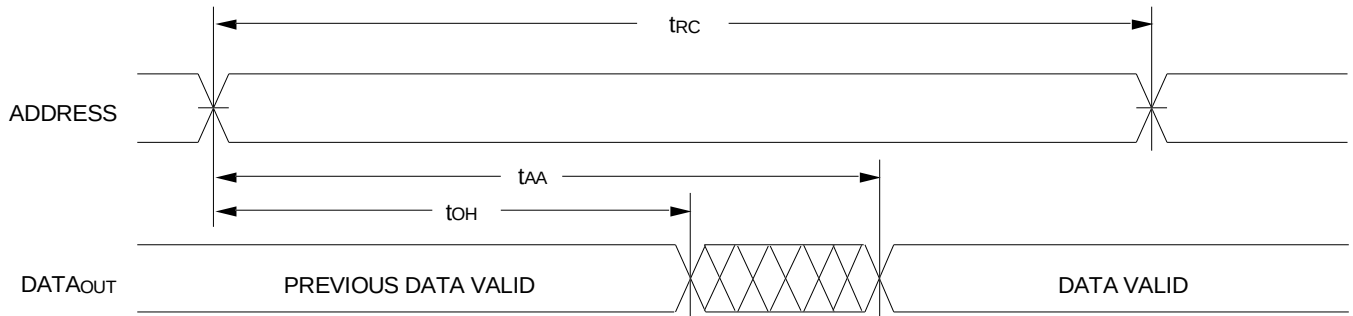
Symbol	Parameter	6168SA15 ⁽¹⁾		6168SA20 ⁽¹⁾ 6168LA20 ⁽¹⁾		6168SA25 6168LA25		6168SA45 ⁽²⁾ 6168LA45 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	15	—	20	—	25	—	45	—	ns
t _{AA}	Address Access Time	—	15	—	20	—	25	—	45	ns
t _{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	45	ns
t _{OLZ} ⁽³⁾	Chip Select to Output in Low-Z	3	—	5	—	5	—	5	—	ns
t _{CHZ} ⁽³⁾	Chip Deselect to Output in High-Z	—	8	—	10	—	10	—	25	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t _{PU} ⁽³⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽³⁾	Chip Deselect to Power Down Time	—	35	—	20	—	25	—	40	ns

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NOTES:

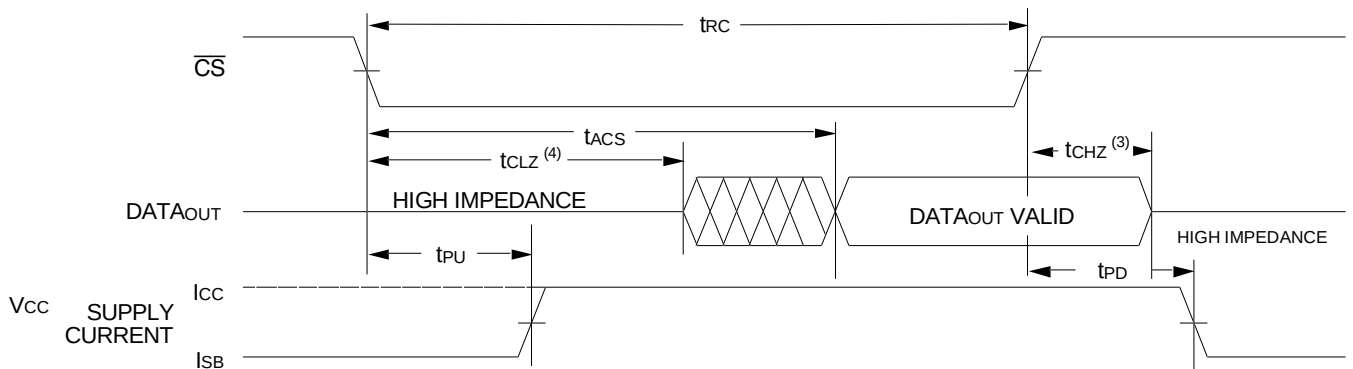
- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1^(1, 2)



3090 drw 06

Timing Waveform of Read Cycle No. 2^(1, 3)



3090 drw 07

NOTES:

- $\overline{WE}$ is HIGH for Read cycle.
- $\overline{CS}$ is LOW for Read cycle.
- Device is continuously selected, $\overline{CS}$ is LOW.
- Address valid prior to or coincident with $\overline{CS}$ transition LOW.
- Transition is measured ±200mV from steady state.

AC Electrical Characteristics (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

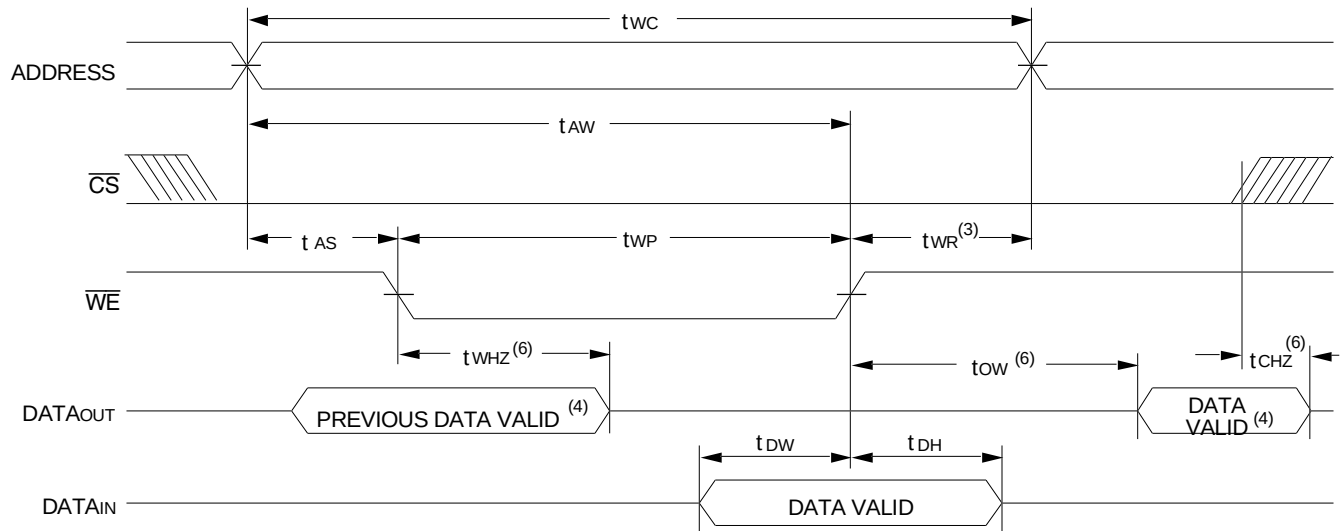
Symbol	Parameter	6168SA15 ⁽¹⁾		6168SA20 ⁽¹⁾ 6168LA20 ⁽¹⁾		6168SA25 6168LA25		6168SA45 ⁽²⁾ 6168LA45 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	15	—	20	—	20	—	40	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	20	—	40	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	20	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	20	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tdW	Data to Valid to End-of-Write	9	—	10	—	10	—	20	—	ns
tdH	Data Hold Time	0	—	0	—	0	—	3	—	ns
tWHZ ⁽³⁾	Write Enable to Output in High-Z	—	6	—	7	—	7	—	20	ns
tOW ⁽³⁾	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

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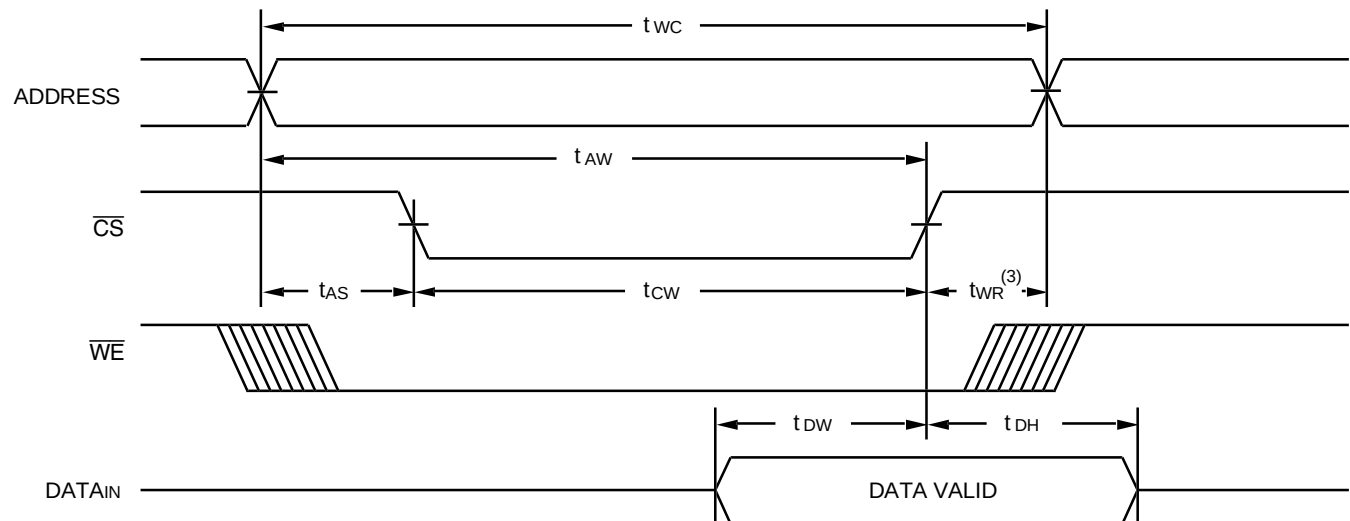
NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)^(1,2,5)



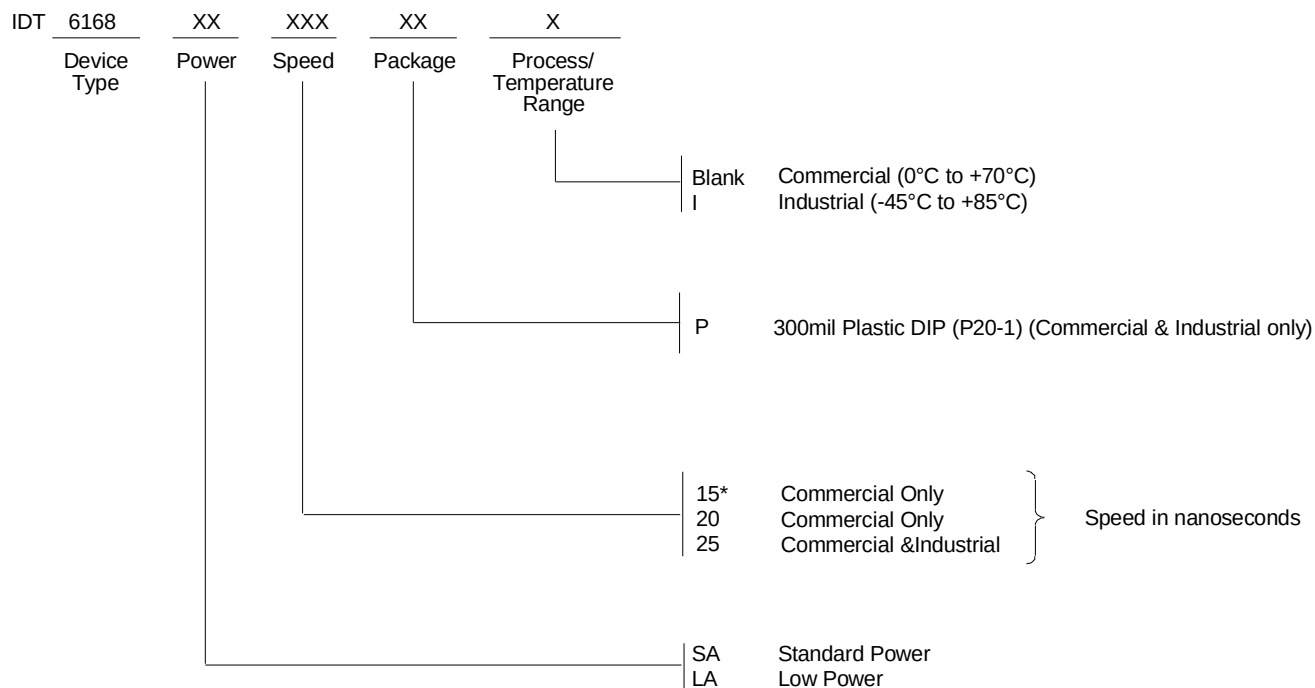
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)^(1,2,5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

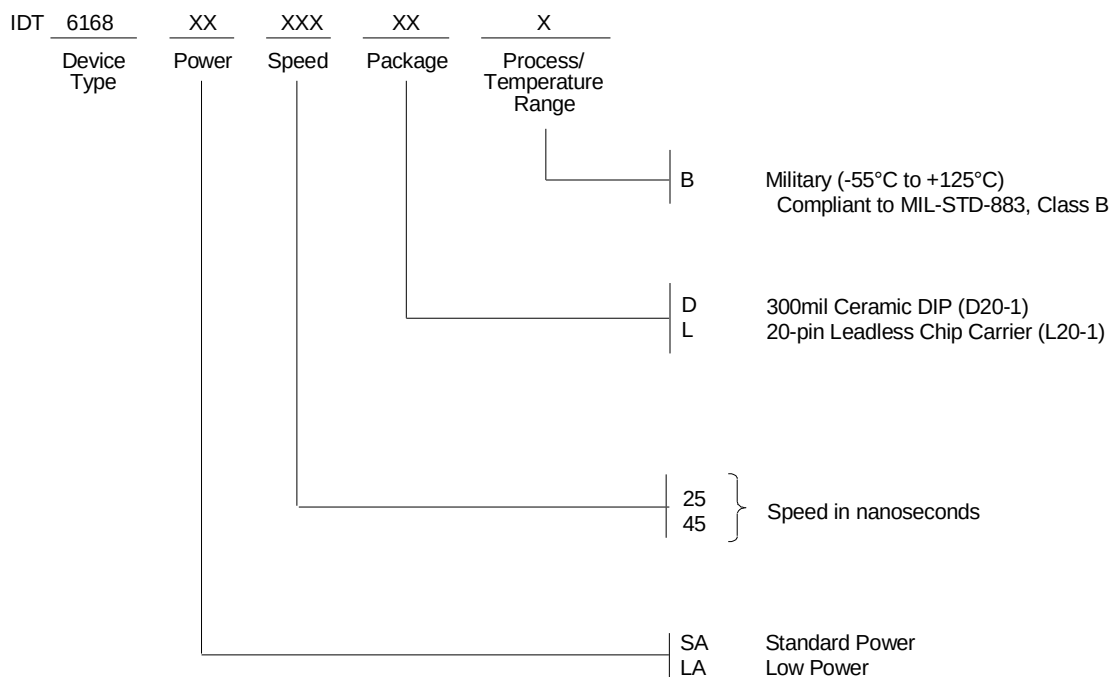
Ordering Information -- Commercial & Industrial



*Standard power only.

3090 drw 10

Ordering Information -- Military



*Standard power only.

3090 drw 10a

Datasheet Document History

11/22/99		Updated to new format
	Pg. 8	Added Datasheet Document History
	Pg. 1, 2, 3, 5, 6, 8	Added Industrial Temperature range offerings
01/07/00		Revised package offerings
08/09/00	Pg. 1, 2, 8	Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"



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