



General Description

The 954206B is a CK410M Compliant clock synthesizer. 954206B provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. 954206B is driven with a 14.318MHz crystal and generates CPU outputs up to 400MHz. It provides the tight ppm accuracy required by Serial ATA and PCI Express.

Recommended Application

- CK410M Compliant Main Clock

Output Features

- 2 - 0.7V current-mode differential CPU pairs
- 4 - 0.7V current-mode differential PCI Express*pairs
- 1 - 0.7V current-mode differential CPU/PCI Express selectable pair
- 1 - 0.7V current-mode differential SATA pair
- 1 - 0.7V current-mode differential LCDCLK/PCI Express selectable pair
- 1 - 0.7V current-mode differential PCI Express/Clock Request pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 2 - REF, 14.318MHz

Features/Benefits

- Supports tight ppm accuracy clocks for Serial-ATA and PCI Express
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, PCI Express pair in PD for power management.
- PEREQ# pins to support PCI Express and SATA power management.

Key Specifications

- CPU outputs cycle-cycle jitter < 85ps
- PCI Express outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- ± 300ppm frequency accuracy on CPU, PCI Express and SATA clocks
- ± 100ppm frequency accuracy on USB clocks

Pin Assignment

| | | |
|-------------------------------|----|----------------------|
| VDDPCI1 | 56 | PCICLK2/REQ_SEL** |
| GND 2 | 55 | PCI/SRC_STOP# |
| PCICLK3 3 | 54 | CPU_STOP# |
| PCICLK4 4 | 53 | REF1/FS_C/TEST_SEL |
| PCICLK5 5 | 52 | REF0 |
| GND 6 | 51 | GND |
| VDDPCI 7 | 50 | X1 |
| ITP_EN/PCICLK_F0 8 | 49 | X2 |
| *SELPCIEX_LCDCLK#/PCICLK_F1 9 | 48 | VDDREF |
| Vtt_PwrGd#/PD 10 | 47 | SDATA |
| VDD48 11 | 46 | SCLK |
| FS_A/USB_48MHz 12 | 45 | GND |
| GND 13 | 44 | CPUCLKT0 |
| DOTT_96MHz 14 | 43 | CPUCLKC0 |
| DOTC_96MHz 15 | 42 | VDDCPU |
| FS_B/TEST_MODE 16 | 41 | CPUCLKT1 |
| LCDCLK_SS/PCIEX0T 17 | 40 | CPUCLKC1 |
| LCDCLK_SS/PCIEX0C 18 | 39 | IREF |
| PCIEXT1 19 | 38 | GNDA |
| PCIEXC1 20 | 37 | VDDA |
| VDDPCIEX 21 | 36 | CPUCLKT2_ITP/PCIEXT6 |
| PCIEXT2 22 | 35 | CPUCLKC2_ITP/PCIEXC6 |
| PCIEXC2 23 | 34 | VDDPCIEX |
| PCIEXT3 24 | 33 | PEREQ1#/PCIEXT5 |
| PCIEXC3 25 | 32 | PEREQ2#/PCIEXC5 |
| SATACLKT 26 | 31 | PCIEXT4 |
| SATACLKC 27 | 30 | PCIEXC4 |
| VDDPCIEX 28 | 29 | GND |

56-pin TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Functional Block Diagram

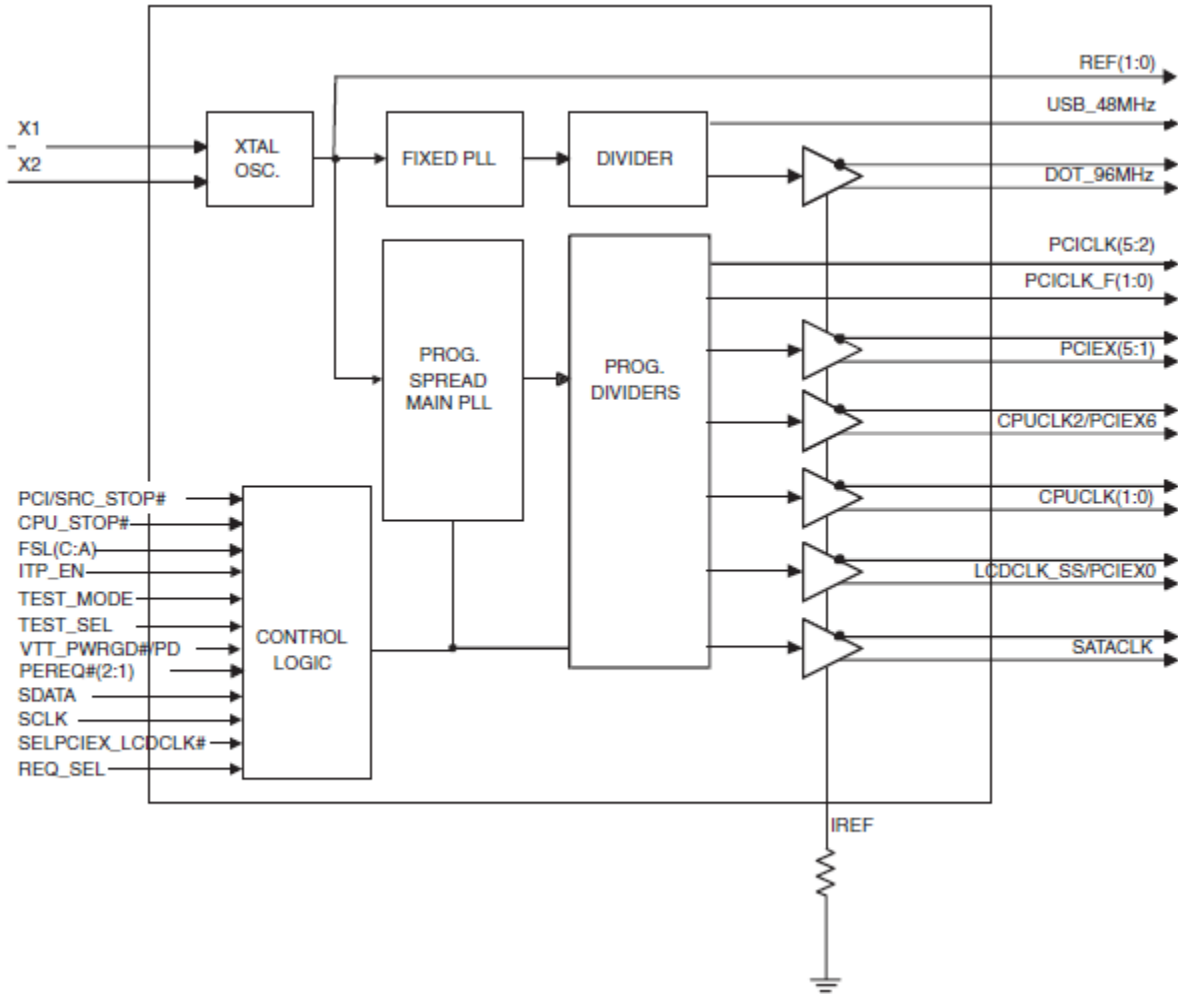


Table 1: Frequency Selection Table

| FS _L C B6b2 | FS _L B B6b1 | FS _L A B6b0 | CPU MHz | PCIEX MHz | PCI MHz | REF MHz | USB MHz | DOT MHz | Spread % |
|------------------------|------------------------|------------------------|---------|-----------|---------|---------|---------|---------|-----------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 0 | 0 | 1 | 133.33 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 0 | 1 | 0 | 200.00 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 0 | 1 | 1 | 166.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 1 | 0 | 0 | 333.33 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 1 | 0 | 1 | 100.00 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 1 | 1 | 0 | 400.00 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |
| 1 | 1 | 1 | 200.00 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 | 0.5% Down |

Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|------------------------------|------|--|
| 1 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 2 | GND | PWR | Ground pin. |
| 3 | PCICLK3 | OUT | PCI clock output. |
| 4 | PCICLK4 | OUT | PCI clock output. |
| 5 | PCICLK5 | OUT | PCI clock output. |
| 6 | GND | PWR | Ground pin. |
| 7 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 8 | ITP_EN/PCICLK_F0 | I/O | Free running PCI clock not affected by PCI_STOP# through I2C . ITP_EN: latched input to select pin functionality 1 = CPU_2_ITP pair 0 = PCIE_X_6 pair |
| 9 | *SELPCIE_X_LCDCLK#/PCICLK_F1 | I/O | Latched select input for LCDCLK/PCIE_X output 0 = LCDCLK, 1 = PCIE_X / Free running 3.3V PCI clock output. |
| 10 | Vtt_PwrGd#/PD | IN | Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped. |
| 11 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 12 | FSLA/USB_48MHz | I/O | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V. |
| 13 | GND | PWR | Ground pin. |
| 14 | DOTT_96MHz | OUT | True clock of differential pair for 96.00MHz DOT clock. |
| 15 | DOTC_96MHz | OUT | Complement clock of differential pair for 96.00MHz DOT clock. |
| 16 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 17 | LCDCLK_SS/PCIE_X0T | OUT | True clock of LCDCLK_SS output / True clock of PCI Express differential pair. Selected by SELPCIE_X_LCDCLK# |
| 18 | LCDCLK_SS/PCIE_X0C | OUT | Complementary clock of LCDCLK_SS output / Complementary clock of PCI Express differential pair. Selected by SELPCIE_X_LCDCLK# |
| 19 | PCIE_XT1 | OUT | True clock of differential PCI_Express pair. |
| 20 | PCIE_XC1 | OUT | Complement clock of differential PCI_Express pair. |
| 21 | VDDPCIE_X | PWR | Power supply for PCI Express clocks, nominal 3.3V |
| 22 | PCIE_XT2 | OUT | True clock of differential PCI_Express pair. |
| 23 | PCIE_XC2 | OUT | Complement clock of differential PCI_Express pair. |
| 24 | PCIE_XT3 | OUT | True clock of differential PCI_Express pair. |
| 25 | PCIE_XC3 | OUT | Complement clock of differential PCI_Express pair. |
| 26 | SATACLKT | OUT | True clock of differential SATA pair. |
| 27 | SATACLKC | OUT | Complement clock of differential SATA pair. |
| 28 | VDDPCIE_X | PWR | Power supply for PCI Express clocks, nominal 3.3V |

Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|----------------------|------|---|
| 29 | GND | PWR | Ground pin. |
| 30 | PCIEXC4 | OUT | Complement clock of differential PCI_Express pair. |
| 31 | PCIEXT4 | OUT | True clock of differential PCI_Express pair. |
| 32 | PEREQ2#*/PCIEXC5 | I/O | Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / Complement clock of differential PCI Express output. |
| 33 | PEREQ1#*/PCIEXT5 | I/O | Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / True clock of differential PCI Express output. |
| 34 | VDDPCIEX | PWR | Power supply for PCI Express clocks, nominal 3.3V |
| 35 | CPUCLKC2_ITP/PCIEXC6 | OUT | Complementary clock of CPU_ITP/PCIEX differential pair CPU_ITP/PCIEX output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input. |
| 36 | CPUCLKT2_ITP/PCIEXT6 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair |
| 37 | VDDA | PWR | 3.3V power for the PLL core. |
| 38 | GND A | PWR | Ground pin for the PLL core. |
| 39 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 40 | CPUCLKC1 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 41 | CPUCLKT1 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 42 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 43 | CPUCLKC0 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 44 | CPUCLKT0 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 45 | GND | PWR | Ground pin. |
| 46 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 47 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 48 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 49 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 50 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 51 | GND | PWR | Ground pin. |
| 52 | REF0 | OUT | 14.318 MHz reference clock. |
| 53 | REF1/FSLC/TEST_SEL | I/O | 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table |
| 54 | CPU_STOP# | IN | Stops all CPUCLK, except those set to be free running clocks |
| 55 | PCI/SRC_STOP# | IN | Stops all PCICLKs and SRCCLKs besides the free-running clocks at logic 0 level, when input low |
| 56 | PCICLK2/REQ_SEL** | I/O | 3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ# |

Table2: LCDCLK Spread and Frequency Selection Table

| Byte 6b7 | Byte 6b6 | Byte 6b5 | Byte 6b4 | Byte 6b3 | Pin 17/18 | Spread |
|----------|----------|----------|----------|----------|-----------|----------------|
| | | | | | MHz | % |
| 0 | 0 | 0 | 0 | 0 | 96.00 | 0.8 Down |
| 0 | 0 | 0 | 0 | 1 | 96.00 | 1 Down |
| 0 | 0 | 0 | 1 | 0 | 96.00 | 1.25 Down |
| 0 | 0 | 0 | 1 | 1 | 96.00 | 1.5 Down |
| 0 | 0 | 1 | 0 | 0 | 96.00 | 1.75 Down |
| 0 | 0 | 1 | 0 | 1 | 96.00 | 2 Down |
| 0 | 0 | 1 | 1 | 0 | 96.00 | 2.5 Down |
| 0 | 0 | 1 | 1 | 1 | 96.00 | 3 Down |
| 0 | 1 | 0 | 0 | 0 | 96.00 | +/-0.3 Center |
| 0 | 1 | 0 | 0 | 1 | 96.00 | +/-0.4 Center |
| 0 | 1 | 0 | 1 | 0 | 96.00 | +/-0.5 Center |
| 0 | 1 | 0 | 1 | 1 | 96.00 | +/-0.6 Center |
| 0 | 1 | 1 | 0 | 0 | 96.00 | +/-0.8 Center |
| 0 | 1 | 1 | 0 | 1 | 96.00 | +/-1.0 Center |
| 0 | 1 | 1 | 1 | 0 | 96.00 | +/-1.25 Center |
| 0 | 1 | 1 | 1 | 1 | 96.00 | +/-1.5 Center |
| 1 | 0 | 0 | 0 | 0 | 100.00 | 0.8 Down |
| 1 | 0 | 0 | 0 | 1 | 100.00 | 1 Down |
| 1 | 0 | 0 | 1 | 0 | 100.00 | 1.25 Down |
| 1 | 0 | 0 | 1 | 1 | 100.00 | 1.5 Down |
| 1 | 0 | 1 | 0 | 0 | 100.00 | 1.75 Down |
| 1 | 0 | 1 | 0 | 1 | 100.00 | 2 Down |
| 1 | 0 | 1 | 1 | 0 | 100.00 | 2.5 Down |
| 1 | 0 | 1 | 1 | 1 | 100.00 | 3 Down |
| 1 | 1 | 0 | 0 | 0 | 100.00 | +/-0.3 Center |
| 1 | 1 | 0 | 0 | 1 | 100.00 | +/-0.4 Center |
| 1 | 1 | 0 | 1 | 0 | 100.00 | +/-0.5 Center |
| 1 | 1 | 0 | 1 | 1 | 100.00 | +/-0.6 Center |
| 1 | 1 | 1 | 0 | 0 | 100.00 | +/-0.8 Center |
| 1 | 1 | 1 | 0 | 1 | 100.00 | +/-1.0 Center |
| 1 | 1 | 1 | 1 | 0 | 100.00 | +/-1.25 Center |
| 1 | 1 | 1 | 1 | 1 | 100.00 | +/-1.5 Center |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 954206B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------|----------|------------|-----------|-----|------------------------|-------|-------|
| 3.3V Core Supply Voltage | VDD_A | - | | | V _{DD} + 0.5V | V | 1 |
| 3.3V Logic Input Supply Voltage | VDD_In | - | GND - 0.5 | | V _{DD} + 0.5V | V | 1 |
| Storage Temperature | Ts | - | -65 | | 150 | °C | 1 |
| Ambient Operating Temp | Tambient | - | 0 | | 70 | °C | 1 |
| Case Temperature | Tcase | - | | | 115 | °C | 1 |
| Input ESD protection HBM | ESD prot | - | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics – Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|-------------------------------------|---------------|--|----------------|----------|----------------|-------|-------|
| Input High Voltage | V_{IH} | 3.3 V +/-5% | 2 | | $V_{DD} + 0.3$ | V | 1 |
| Input Low Voltage | V_{IL} | 3.3 V +/-5% | $V_{SS} - 0.3$ | | 0.8 | V | 1 |
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | -5 | | 5 | uA | 1 |
| Input Low Current | I_{IL1} | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I_{IL2} | $V_{IN} = 0$ V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Low Threshold Input-High Voltage | V_{IH_FS} | 3.3 V +/-5% | 0.7 | | $V_{DD} + 0.3$ | V | 1 |
| Low Threshold Input-Low Voltage | V_{IL_FS} | 3.3 V +/-5% | $V_{SS} - 0.3$ | | 0.35 | V | 1 |
| Operating Supply Current | $I_{DD3.3OP}$ | Full Active, $C_L =$ Full load; | | 300 | 350 | mA | 1 |
| Powerdown Current | $I_{DD3.3PD}$ | all diff pairs driven | | 56 | 70 | mA | 1 |
| | | all differential pairs tri-stated | | 5 | 12 | mA | 1 |
| Input Frequency | F_I | $V_{DD} = 3.3$ V | | 14.31818 | | MHz | 2 |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Input Capacitance | C_{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C_{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| | C_{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | T_{STAB} | From VDD Power-Up or de-assertion of PD to 1st clock | | | 1.8 | ms | 1 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_PD | | CPU output enable after PD de-assertion | | | 300 | us | 1 |
| Tfall_PD | | PD fall time of | | | 5 | ns | 1 |
| Trise_PD | | PD rise time of | | | 5 | ns | 1 |
| SMBus Voltage | V_{DD} | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | V_{OL} | @ I_{PULLUP} | | | 0.4 | V | 1 |
| Current sinking at $V_{OL} = 0.4$ V | I_{PULLUP} | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | T_{RI2C} | (Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | T_{FI2C} | (Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$) | | | 300 | ns | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

² Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics – CPU 0.7V Current Mode Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|----------------------|--|--------|-----|---------|-------|-------|
| Current Source Output Impedance | Z _o | V _o = V _x | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal | 660 | 766 | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | 21 | 150 | mV | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | Vx(abs) | | 250 | 370 | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vx | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 400MHz nominal | 2.4993 | | 2.5008 | ns | 2 |
| | | 400MHz spread | 2.4993 | | 2.5133 | ns | 2 |
| | | 333.33MHz nominal | 2.9991 | | 3.0009 | ns | 2 |
| | | 333.33MHz spread | 2.9991 | | 3.016 | ns | 2 |
| | | 266.66MHz nominal | 3.7489 | | 3.7511 | ns | 2 |
| | | 266.66MHz spread | 3.7489 | | 3.77 | ns | 2 |
| | | 200MHz nominal | 4.9985 | | 5.0015 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2 |
| | | 166.66MHz nominal | 5.9982 | | 6.0018 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2 |
| | | 133.33MHz nominal | 7.4978 | | 7.5023 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 7.5400 | ns | 2 |
| | | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | T _{absmin} | 400MHz nominal/spread | 2.4143 | | | ns | 1,2 |
| | | 333.33MHz nominal/spread | 2.9141 | | | ns | 1,2 |
| | | 266.66MHz nominal/spread | 3.6639 | | | ns | 1,2 |
| | | 200MHz nominal/spread | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | 175 | 227 | 700 | ps | 1 |
| Fall Time | t _f | V _{OH} = 0.525V V _{OL} = 0.175V | 175 | 227 | 700 | ps | 1 |
| Rise Time Variation | d-t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | | 32 | 125 | ps | 1 |
| Fall Time Variation | d-t _f | V _{OH} = 0.525V V _{OL} = 0.175V | | 37 | 125 | ps | 1 |
| Duty Cycle | d ₁₃ | Measurement from differential waveform | 45 | 51 | 55 | % | 1 |
| Skew | t _{sk3} | CPU(1:0), V _T = 50% | | 28 | 100 | ps | 1 |
| Skew | t _{sk4} | CPU(1:0) to CPU2_ITP, V _T = 50% | | 105 | 150 | ps | 1 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | Measurement from differential waveform (CPU2_ITP) | | 65 | 125 | ps | 1 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | Measurement from differential waveform, (CPU(1:0)) | | 50 | 85 | ps | 1 |

*TA - 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF}=475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics – SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------|----------------------|--|--------|-----|---------|-------|-------|
| Current Source Output Impedance | Z _o | V _O = V _x | 3000 | | | Ω | 1 |
| Voltage High | V _{High} | Statistical measurement on single ended signal | 660 | 780 | 850 | mV | 1,3 |
| Voltage Low | V _{Low} | | -150 | -15 | 150 | mV | 1,3 |
| Max Voltage | V _{ovs} | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | V _{uds} | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | V _{x(abs)} | | 250 | 360 | 550 | mV | 1 |
| Crossing Voltage (var) | d-V _x | Variation of crossing over all edges | | 50 | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | T _{absmin} | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | 175 | 228 | 700 | ps | 1 |
| Fall Time | t _f | V _{OH} = 0.525V V _{OL} = 0.175V | 175 | 221 | 700 | ps | 1 |
| Rise Time Variation | d-t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | | 18 | 125 | ps | 1 |
| Fall Time Variation | d-t _f | V _{OH} = 0.525V V _{OL} = 0.175V | | 41 | 125 | ps | 1 |
| Duty Cycle | d _{t3} | Measurement from differential waveform | 45 | 51 | 55 | % | 1 |
| Skew | t _{sk3} | V _T = 50% | | 135 | 250 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | Measurement from differential waveform | | 55 | 125 | ps | 1 |

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 2pF, R_S = 33.2Ω, R_P = 49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O = 50Ω.

Electrical Characteristics – PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|--|-----|------|------|-------|-------|
| Output Impedance | R _{DSP} | V _O = V _{DD} *(0.5) | 12 | | 55 | Ω | 1 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | | 38 | mA | 1 |
| Edge Rate | t _{slewr/f} | Rising/Falling edge rate | 1 | 1.5 | 4 | V/ns | 1 |
| Rise Time | t _r | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.5 | 1.26 | 2 | ns | 1 |
| Fall Time | t _f | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.5 | 1.34 | 2 | ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | 50 | 55 | % | 1 |
| Group Skew | t _{skew} | V _T = 1.5 V | | 25 | 250 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | V _T = 1.5 V | | 112 | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with R_s = 7Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

³Spread Spectrum is off

Electrical Characteristics – USB48MHz

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|--------------------------|--|---------|------|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Clock period | T _{period} | 48.00MHz output nominal | 20.8313 | | 20.8354 | ns | 2 |
| Output Impedance | R _{DSP} | V _O = V _{DD} *(0.5) | 12 | | 55 | Ω | 1 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | | 38 | mA | 1 |
| Edge Rate | t _{slewr/f_USB} | USB48 Rising/Falling edge rate | 1 | 1.5 | 2 | V/ns | 1 |
| Rise Time | t _{r_USB} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 1 | 1.26 | 2 | ns | 1 |
| Fall Time | t _{f_USB} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 1 | 1.34 | 2 | ns | 1 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 51.6 | 55 | % | 1 |
| Group Skew | t _{skew} | V _T = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | V _T = 1.5 V | | 228 | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics – DOT_96MHz 0.7V Current Mode Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------|----------------------|--|---------|------|---------|-------|-------|
| Current Source Output Impedance | Z _o | V _O = V _x | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal | 660 | 780 | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | 0 | 150 | mV | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | Vx(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Average period | Tperiod | 96.00MHz nominal | 10.4135 | | 10.4198 | ns | 2 |
| Absolute min period | Tabsmn | 96.00MHz nominal | 10.1635 | | | ns | 1,2 |
| Rise Time | t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | 175 | 228 | 700 | ps | 1 |
| Fall Time | t _f | V _{OH} = 0.525V V _{OL} = 0.175V | 175 | 221 | 700 | ps | 1 |
| Rise Time Variation | d-t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | | 21 | 125 | ps | 1 |
| Fall Time Variation | d-t _f | V _{OH} = 0.525V V _{OL} = 0.175V | | 18 | 125 | ps | 1 |
| Duty Cycle | d _{t3} | Measurement from differential waveform | 45 | 49.8 | 55 | % | 1 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | Measurement from differential waveform | | 120 | 250 | ps | 1 |

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 2pF, R_S = 33.2Ω, R_P = 49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O = 50Ω.

Electrical Characteristics – REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------|----------------------|---|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | T_{period} | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{\text{OH}} = -1 \text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{\text{OL}} = 1 \text{ mA}$ | | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{\text{OH}} @ \text{MIN} = 1.0 \text{ V},$ $V_{\text{OH}} @ \text{MAX} = 3.135 \text{ V}$ | -29 | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{\text{OL}} @ \text{MIN} = 1.95 \text{ V},$ $V_{\text{OL}} @ \text{MAX} = 0.4 \text{ V}$ | 29 | | 27 | mA | 1 |
| Edge Rate | $t_{\text{slewr/f}}$ | Rising/Falling edge rate | 1 | 2 | 4 | V/ns | 1 |
| Rise Time | t_{r1} | $V_{\text{OL}} = 0.4 \text{ V}, V_{\text{OH}} = 2.4 \text{ V}$ | 0.5 | 1.6 | 2 | ns | 1 |
| Fall Time | t_{f1} | $V_{\text{OH}} = 2.4 \text{ V}, V_{\text{OL}} = 0.4 \text{ V}$ | 0.5 | 2 | 2 | ns | 1 |
| Skew | t_{sk1} | $V_{\text{T}} = 1.5 \text{ V}$ | | | 500 | ps | 1 |
| Duty Cycle | d_{t1} | $V_{\text{T}} = 1.5 \text{ V}$ | 45 | 53 | 55 | % | 1 |
| Jitter | $t_{\text{jvc-cvc}}$ | $V_{\text{T}} = 1.5 \text{ V}$ | | 750 | 1000 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

General SMBus Serial Interface Information for 954206B

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | |
| | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Read Address | Write Address |
|-------------------|-------------------|
| D3 _(H) | D2 _(H) |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | |
| | | Beginning Byte N |
| ACK | | |
| O | X Byte | O |
| O | | O |
| O | | O |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

I²C Table: Output Control Register

| Byte 0 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|---|-------|---------------------------|------------------|------|---------|--------|-----|
| Bit 7 | - | | CPUCLK2_ITP/PCIEX6 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | - | | PCIEX5 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | - | | PCIEX4 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | | SATACLK Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | - | | PCIEX3 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | - | | PCIEX2 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | - | | PCIEX1 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | | LCDCLK/PCIEX0 Enable | Output Enable | RW | Disable | Enable | 1 |

I²C Table: Spread and Output Control Register

| Byte 1 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|---|-------|-----------------------------|-------------------------|------|---------|--------|-----|
| Bit 7 | - | | Test Clock Mode Entry | Test Mode | RW | Disable | Enable | 0 |
| Bit 6 | - | | DOT_96MHz Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | - | | USB_48MHz Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | | REF_0 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | - | | LCDCLK/PCIEX0 Spectrum Mode | Spread Control | RW | OFF | ON | 1 |
| Bit 2 | - | | CPUCLK1 | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | - | | CPUCLK0 | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | | Spread Spectrum Mode | Spread Control for PLL1 | RW | OFF | ON | 0 |

I²C Table: Output Control Register

| Byte 2 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|---|-------|---------------------|-------------------------------------|------|---------|---------|-----|
| Bit 7 | - | | PCICLK5 | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | - | | PCICLK4 | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | - | | PCICLK3 | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | | PCICLK2 | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | - | | Test Mode Selection | Test Mode Selection | RW | Hi-Z | REF/N | 0 |
| Bit 2 | - | | PCI_STOP | Stop all PCI, PCIEX and SATA clocks | RW | Enable | Disable | 1 |
| Bit 1 | - | | PCI_F0 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | | PCI_F1 Enable | Output Enable | RW | Disable | Enable | 1 |

I²C Table: Output Control Register

| Byte 3 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|---|-------|---------|--|------|--------------|-----------|-----|
| Bit 7 | - | | PCIEX6 | Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCIEX clocks | RW | Free Running | Stoppable | 0 |
| Bit 6 | - | | PCIEX5 | | RW | Free Running | Stoppable | 0 |
| Bit 5 | - | | PCIEX4 | | RW | Free Running | Stoppable | 0 |
| Bit 4 | - | | SATACLK | | RW | Free Running | Stoppable | 0 |
| Bit 3 | - | | PCIEX3 | | RW | Free Running | Stoppable | 0 |
| Bit 2 | - | | PCIEX2 | | RW | Free Running | Stoppable | 1 |
| Bit 1 | - | | PCIEX1 | | RW | Free Running | Stoppable | 1 |
| Bit 0 | - | | PCIEX0 | | RW | Free Running | Stoppable | 1 |

I²C Table: Output Control Register

| Byte 4 | Pin # | Name | Control | Type | 0 | 1 | PWD |
|--------|-------|----------------|---|------|--------------|-----------|-----|
| | | | Function | | | | |
| Bit 7 | - | REF_1 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | - | 96MHz | Driven in PD | RW | Driven | Hi-Z | 1 |
| Bit 5 | - | REF_0 STRENGTH | Strength Programming | RW | 1X | 2X | 1 |
| Bit 4 | - | PCL_F1 | Allow assertion of PCL_STOP# or setting of | RW | Free Running | Stoppable | 1 |
| Bit 3 | - | PCL_F0 | | RW | Free Running | Stoppable | 1 |
| Bit 2 | - | CPUCLK2_ITP | Allow assertion of CPU_STOP# to stop CPUCLK outputs | RW | Free Running | Stoppable | 1 |
| Bit 1 | - | CPUCLK1 | | RW | Free Running | Stoppable | 1 |
| Bit 0 | - | CPUCLK0 | | RW | Free Running | Stoppable | 1 |

I²C Table: Output Control Register

| Byte 5 | Pin # | Name | Control | Type | 0 | 1 | PWD |
|--------|-------|-----------------------------|--------------------------|------|--------|---------|-------|
| | | | Function | | | | |
| Bit 7 | - | PCI_STOP Drive Mode | Driven in PCI_STOP# | RW | Driven | Hi-Z | 0 |
| Bit 6 | - | CPUCLK2_ITP_STOP Drive Mode | Driven in CPU_STOP# | RW | Driven | Hi-Z | 0 |
| Bit 5 | - | CPUCLK1_STOP Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 4 | - | CPUCLK0_STOP Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 3 | - | PCIEX (6:0) Drive Mode | Driven in Powerdown (PD) | RW | Driven | Hi-Z | 0 |
| Bit 2 | - | CPUCLK2_ITP_PD Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 1 | - | CPUCLK[1:0] PD Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 0 | - | ITP_EN | PCIEX/CPU_ITP select | RW | PCIEX | CPU_ITP | latch |

I²C Table: Output Control Register

| Byte 6 | Pin # | Name | Control | Type | 0 | 1 | PWD |
|--------|-------|------|--------------------------|------|---|--------|---------|
| | | | Function | | | | |
| Bit 7 | - | SS4 | LCDCLK Spread Prog Bit 4 | RW | 96Mhz | 100Mhz | 0 |
| Bit 6 | - | SS3 | LCDCLK Spread Prog Bit 3 | RW | See Table 2: LCDCLK Freq Sel | | 1 |
| Bit 5 | - | SS2 | LCDCLK Spread Prog Bit 2 | RW | | | 0 |
| Bit 4 | - | SS1 | LCDCLK Spread Prog Bit 1 | RW | | | 0 |
| Bit 3 | - | SS0 | LCDCLK Spread Prog Bit 0 | RW | | | 0 |
| Bit 2 | - | FSLC | Freq Select Bit 2 | RW | See Table 1: PLL1 Frequency Selection Table | | Latched |
| Bit 1 | - | FSLB | Freq Select Bit 1 | RW | | | Latched |
| Bit 0 | - | FSLA | Freq Select Bit 0 | RW | | | Latched |

I²C Table: Vendor & Revision ID Register

| Byte 7 | Pin # | Name | Control | Type | 0 | 1 | PWD |
|--------|-------|------|-------------|------|---|---|-----|
| | | | Function | | | | |
| Bit 7 | - | RID3 | REVISION ID | R | - | - | x |
| Bit 6 | - | RID2 | | R | - | - | x |
| Bit 5 | - | RID1 | | R | - | - | x |
| Bit 4 | - | RID0 | | R | - | - | x |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

I²C Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|----------------------------------|------|---|---|-----|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes. | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 1 |
| Bit 1 | - | BC1 | | RW | | | 1 |
| Bit 0 | - | BC0 | | RW | | | 1 |

I²C Table: Watchdog Timer Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------------|-----------------------------|------|---|-------------|-----|
| Bit 7 | - | WDH_EN | Watchdog Hard Alarm Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | WDS_EN | Watchdog Soft Alarm Enable | RW | Disable | Enable | 0 |
| Bit 5 | - | WD Hard Status | WD Hard Alarm Status | R | Normal | Alarm | X |
| Bit 4 | - | WD Soft Status | WD Soft Alarm Status | R | Normal | Alarm | X |
| Bit 3 | - | WDTCtrl | Watch Dog Time base Control | RW | 290ms Base | 1160ms Base | 0 |
| Bit 2 | - | WD2 | WD Timer Bit 2 | RW | These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s. | | 1 |
| Bit 1 | - | WD1 | WD Timer Bit 1 | RW | | | 1 |
| Bit 0 | - | WD0 | WD Timer Bit 0 | RW | | | 1 |

I²C Table: VCO Control Select Bit & WD Timer Control Register

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|---------------------|--------------------------------------|------|--|-----------|-------|
| Bit 7 | - | M/N_EN | PLL/M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | LCDCLK/PCIEX0 SEL | SELPCIEX0/LCDCLK# | RW | LCDCLK | PCIEX0 | latch |
| Bit 5 | - | REQ_SEL | REQ_SEL | RW | PCIEX5 | PEREQ | latch |
| Bit 4 | - | LCDCLK/PCIEX0 | Driven in PD | RW | Driven | Hi-Z | 0 |
| Bit 3 | - | WD Safe Freq Source | WD Safe Freq Source | RW | Latch Inputs/Byte6[2:0] | B10b(2:0) | 0 |
| Bit 2 | - | WD SFC | Watch Dog Safe Freq Programming bits | RW | Writing to these bit will configure the safe frequency as Byte0 bit (4:0). | | 0 |
| Bit 1 | - | WD SFB | | RW | | | 0 |
| Bit 0 | - | WD SFA | | RW | | | 0 |

I²C Table: VCO Frequency Control Register

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|---------|----------------------------|------|---|---|-----|
| Bit 7 | - | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$ | | X |
| Bit 6 | - | N Div 9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | - | M Div4 | | RW | | | X |
| Bit 3 | - | M Div3 | | RW | | | X |
| Bit 2 | - | M Div2 | | RW | | | X |
| Bit 1 | - | M Div1 | | RW | | | X |
| Bit 0 | - | M Div0 | | RW | | | X |

I²C Table: VCO Frequency Control Register

| Byte 12 | | Pin # | Name | Control Function | Type | 0 | | 1 | | PWD |
|---------|---|-------|--------|---------------------------------|------|---|--|---|--|-----|
| Bit 7 | - | - | N Div7 | N Divider Programming b(8:0) | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$ | | | | X |
| Bit 6 | - | - | N Div6 | | RW | | | | | X |
| Bit 5 | - | - | N Div5 | | RW | | | | | X |
| Bit 4 | - | - | N Div4 | | RW | | | | | X |
| Bit 3 | - | - | N Div3 | | RW | | | | | X |
| Bit 2 | - | - | N Div2 | | RW | | | | | X |
| Bit 1 | - | - | N Div1 | | RW | | | | | X |
| Bit 0 | - | - | N Div0 | | RW | | | | | X |

I²C Table: Spread Spectrum Control Register

| Byte 13 | | Pin # | Name | Control Function | Type | 0 | | 1 | | PWD |
|---------|---|-------|------|---------------------------------------|------|--|--|---|--|-----|
| Bit 7 | - | - | SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming. | | | | X |
| Bit 6 | - | - | SSP6 | | RW | | | | | X |
| Bit 5 | - | - | SSP5 | | RW | | | | | X |
| Bit 4 | - | - | SSP4 | | RW | | | | | X |
| Bit 3 | - | - | SSP3 | | RW | | | | | X |
| Bit 2 | - | - | SSP2 | | RW | | | | | X |
| Bit 1 | - | - | SSP1 | | RW | | | | | X |
| Bit 0 | - | - | SSP0 | | RW | | | | | X |

I²C Table: Spread Spectrum Control Register

| Byte 14 | | Pin # | Name | Control Function | Type | 0 | | 1 | | PWD |
|---------|---|-------|----------|--|------|--|---|---|---|-----|
| Bit 7 | - | - | Reserved | Reserved | R | - | - | - | - | 0 |
| Bit 6 | - | - | SSP14 | Spread Spectrum Programming b(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming. | | | | X |
| Bit 5 | - | - | SSP13 | | RW | | | | | X |
| Bit 4 | - | - | SSP12 | | RW | | | | | X |
| Bit 3 | - | - | SSP11 | | RW | | | | | X |
| Bit 2 | - | - | SSP10 | | RW | | | | | X |
| Bit 1 | - | - | SSP9 | | RW | | | | | X |
| Bit 0 | - | - | SSP8 | | RW | | | | | X |

I²C Table: Output Divider Control Register

| Byte 15 | | Pin # | Name | Control Function | Type | 0 | | 1 | | PWD |
|---------|---|-------|------------|--------------------------------------|------|----------|----------|----------|-----------|-----|
| Bit 7 | - | - | PCIEX Div3 | PCIEX Divider Ratio Programming Bits | RW | 0000:/2 | 0100:/4 | 1000:/8 | 1100:/16 | X |
| Bit 6 | - | - | PCIEX Div2 | | RW | 0001:/3 | 0101:/6 | 1001:/12 | 1101:/24 | X |
| Bit 5 | - | - | PCIEX Div1 | | RW | 0010:/5 | 0110:/10 | 1010:/20 | 1110:/40 | X |
| Bit 4 | - | - | PCIEX Div0 | | RW | 0011:/15 | 0111:/30 | 1011:/60 | 1111:/120 | X |
| Bit 3 | - | - | CPU Div3 | CPUDivider Ratio Programming Bits | RW | 0000:/2 | 0100:/4 | 1000:/8 | 1100:/16 | X |
| Bit 2 | - | - | CPU Div2 | | RW | 0001:/3 | 0101:/6 | 1001:/12 | 1101:/24 | X |
| Bit 1 | - | - | CPU Div1 | | RW | 0010:/5 | 0110:/10 | 1010:/20 | 1110:/40 | X |
| Bit 0 | - | - | CPU Div0 | | RW | 0011:/15 | 0111:/30 | 1011:/60 | 1111:/120 | X |

I²C Table: PEREQ# Control Register

| Byte 16 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|---|-------|--|-----------------------|------|----------------|------------|-----|
| Bit 7 | - | | Reserved | Reserved | RW | - | - | 0 |
| Bit 6 | - | | PEREQ2# controls selected outputs. Outputs controlled by this pin will be Hi-Z when PEREQ2# is high. | PCIEX4 is controlled | RW | Not Controlled | Controlled | 1 |
| Bit 5 | - | | | PCIEX3 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 4 | - | | | PCIEX1 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 3 | - | | Reserved | Reserved | RW | - | - | 0 |
| Bit 2 | - | | PEREQ1# controls selected outputs. Outputs controlled by this pin will be Hi-Z when PEREQ1# is high. | SATACLK is controlled | RW | Not Controlled | Controlled | 1 |
| Bit 1 | - | | | PCIEX2 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 0 | - | | | PCIEX0 is controlled | RW | Not Controlled | Controlled | 0 |

I²C Table: PLL 2 VCO Frequency Control Register

| Byte 17 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|---|-------|--------|----------------------------|------|---|---|-----|
| Bit 7 | - | | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$ | | X |
| Bit 6 | - | | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | - | | M Div4 | | RW | | | X |
| Bit 3 | - | | M Div3 | | RW | | | X |
| Bit 2 | - | | M Div2 | | RW | | | X |
| Bit 1 | - | | M Div1 | | RW | | | X |
| Bit 0 | - | | M Div0 | | RW | | | X |

I²C Table: PLL 2 VCO Frequency Control Register

| Byte 18 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|---|-------|--------|------------------------------|------|---|---|-----|
| Bit 7 | - | | N Div7 | N Divider Programming b(8:0) | RW | The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$ | | X |
| Bit 6 | - | | N Div6 | | RW | | | X |
| Bit 5 | - | | N Div5 | | RW | | | X |
| Bit 4 | - | | N Div4 | | RW | | | X |
| Bit 3 | - | | N Div3 | | RW | | | X |
| Bit 2 | - | | N Div2 | | RW | | | X |
| Bit 1 | - | | N Div1 | | RW | | | X |
| Bit 0 | - | | N Div0 | | RW | | | X |

I²C Table: PLL 2 Spread Spectrum Control Register

| Byte 19 | | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|---|-------|------|------------------------------------|------|--|---|-----|
| Bit 7 | - | | SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming. | | X |
| Bit 6 | - | | SSP6 | | RW | | | X |
| Bit 5 | - | | SSP5 | | RW | | | X |
| Bit 4 | - | | SSP4 | | RW | | | X |
| Bit 3 | - | | SSP3 | | RW | | | X |
| Bit 2 | - | | SSP2 | | RW | | | X |
| Bit 1 | - | | SSP1 | | RW | | | X |
| Bit 0 | - | | SSP0 | | RW | | | X |

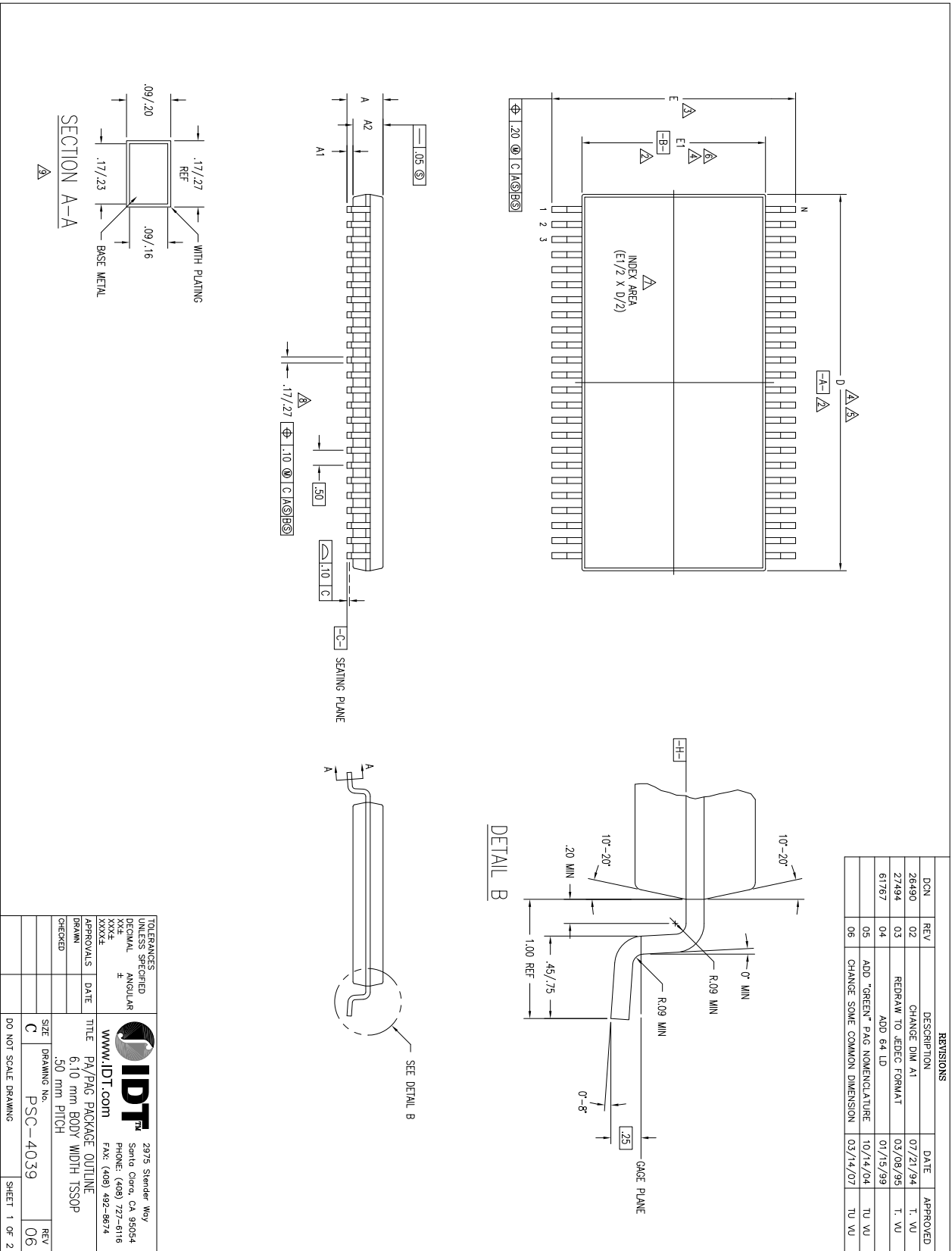
I²C Table: PLL2 Spread Spectrum Control Register

| Byte 20 | Pin # | Name | Control | Type | 0 | 1 | PWD |
|---------|-------|----------|-------------------------------------|------|--|---|-----|
| | | | Function | | | | |
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | SSP14 | Spread Spectrum Programming b(14:8) | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming. | | X |
| Bit 5 | - | SSP13 | | RW | | | X |
| Bit 4 | - | SSP12 | | RW | | | X |
| Bit 3 | - | SSP11 | | RW | | | X |
| Bit 2 | - | SSP10 | | RW | | | X |
| Bit 1 | - | SSP9 | | RW | | | X |
| Bit 0 | - | SSP8 | | RW | | | X |

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|---|----------------------|-----------------------|---------------------|--------------------|--------|
| | FSLC/TEST_SEL HW PIN | FSLB/TEST_MODE HW PIN | TEST ENTRY BIT W1b7 | REF/N or HI-Z W2b3 | |
| | | 0 | X | 0 | |
| Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If power-up w/ V>2.0V (-0.3V) then use TEST_SEL If power-up w/ V<2.0V (-0.3V) then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a | 1 | 0 | X | 0 | HI-Z |
| | 1 | 0 | X | 1 | REF/N |
| | 1 | 1 | X | 0 | REF/N |
| If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through W1b7. If test mode is invoked by W1b7, only W2b3 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control | 1 | 1 | X | 1 | REF/N |
| | 0 | X | 1 | 0 | HI-Z |
| | 0 | X | 1 | 1 | REF/N |
| W1b7: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION) | | | | | |
| W2b3: 1= REF/N, Default = 0 (HI-Z) | | | | | |

Package Outline and Dimensions (56-pin TSSOP)



| REVISIONS | | | | |
|-----------|-----|------------------------------|----------|----------|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 26490 | 02 | CHANGE DIM A1 | 07/21/94 | T. WU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | T. WU |
| 61767 | 04 | ADD 64 LD | 07/15/99 | TU WU |
| | 05 | ADD "GREEN" PAG NOMENCLATURE | 10/14/04 | TU WU |
| | 06 | CHANGE SOME COMMON DIMENSION | 03/14/07 | TU WU |

| | | |
|-----------------------------|-------------|--|
| TOLERANCES UNLESS SPECIFIED | | <p>2975 Sander Way Santa Clara, CA 95054 Phone: (408) 727-6116 Fax: (408) 492-8674</p> |
| DECIMAL | ANGULAR | |
| XXX | ± | |
| XXXX | | |
| APPROVALS | DATE | TITLE |
| DESIGNED | | PA/PKG PACKAGE OUTLINE |
| CHECKED | | 6.10 mm BODY WIDTH TSSOP |
| | | .50 mm PITCH |
| SIZE | DRAWING No. | PSC-4039 |
| C | | |
| DO NOT SCALE DRAWING | | SHEET 1 OF 2 |

Package Outline and Dimensions, cont. (56-pin TSSOP)

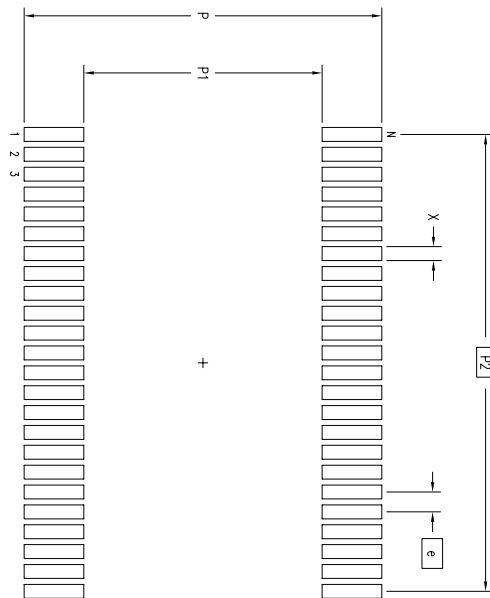
| SYMBOL | JEDEC VARIATION | | | N D T E | JEDEC VARIATION | | | N D T E | JEDEC VARIATION | | | N D T E |
|--------|-----------------|-------|-------|---------|-----------------|-------|-------|---------|-----------------|-------|-------|---------|
| | ED | NOM | MAX | | EE | NOM | MAX | | EF | NOM | MAX | |
| A | — | 1.20 | — | — | — | 1.20 | — | — | — | 1.20 | — | |
| A1 | .05 | .15 | — | .05 | .15 | — | .05 | .15 | — | .15 | — | |
| A2 | .80 | 1.05 | — | .80 | 1.05 | — | .80 | 1.05 | — | 1.05 | — | |
| D | 12.40 | 12.50 | 12.60 | 4.5 | 13.90 | 14.00 | 14.10 | 4.5 | 16.90 | 17.00 | 17.10 | 4.5 |
| E | 7.95 | 8.10 | 8.25 | 3 | 7.95 | 8.10 | 8.25 | 3 | 7.95 | 8.10 | 8.25 | 3 |
| E1 | 6.00 | 6.10 | 6.20 | 4.6 | 6.00 | 6.10 | 6.20 | 4.6 | 6.00 | 6.10 | 6.20 | 4.6 |
| N | 48 | | | 56 | | | 64 | | | 4.6 | | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION ED, EE & EF

| REVISIONS | | | | |
|-----------|-----|------------------------------|----------|----------|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 26490 | 02 | CHANGE DIM A1 | 07/21/94 | T. VU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | T. VU |
| 61767 | 04 | ADD 64 LD | 01/15/99 | TU VU |
| 05 | 05 | ADD "GREEN" PAG NOMENCLATURE | 10/14/04 | TU VU |
| 06 | 06 | CHANGE SOME COMMON DIMENSION | 03/14/07 | TU VU |

LAND PATTERN DIMENSIONS



| | MIN | MAX | MIN | MAX | MIN | MAX |
|----|-----------|------|-----------|------|-----------|------|
| P | 8.90 | 9.10 | 8.90 | 9.10 | 8.90 | 9.10 |
| P1 | 5.90 | 6.10 | 5.90 | 6.10 | 5.90 | 6.10 |
| P2 | 11.50 BSC | | 13.50 BSC | | 15.50 BSC | |
| X | .30 | .40 | .30 | .40 | .30 | .40 |
| e | .50 BSC | | .50 BSC | | .50 BSC | |
| N | 48 | | 56 | | 64 | |

| TOLERANCES UNLESS SPECIFIED | | 2975 Steiner Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 | |
|-----------------------------|------|---|--------------|
| DECIMAL | ± | www.IDT.com | |
| XXX.X | | TITLE: P4/P4G PACKAGE OUTLINE | |
| XXXX.X | | 6.10 mm BODY WIDTH TSSOP | |
| APPROVALS | DATE | SIZE | DRAWING No. |
| DRAWN | | C | PSC-4039 |
| CHECKED | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |
| REV | | | REV |
| | | | 06 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|--------------|-------------|
| 954206BGLF | Tubes | 56-pin TSSOP | 0 to +70° C |
| 954206BGLFT | Tape and Reel | 56-pin TSSOP | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"C" is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|---------|
| A | 2/22/2016 | <ol style="list-style-type: none"> 1. Updated Output Features 2. Updated Electrical tables 3. Reformatted datasheet to latest template. 4. Updated POD drawings. | Various |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
www.idt.com/go/support

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2016 Integrated Device Technology, Inc.. All rights reserved.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.