Single chip 2.4 GHz Transmitter

nRF2402
nRF2402G

FEATURES

- True single chip GFSK transmitter in a small 16-pin package (QFN16 4x4)
- Adjustable output power up to 0dBm
- Data rate 0 to 1Mbps
- Low Bill of Material
- Multi Channel operation
  - 128 channels
  - Support frequency hopping
  - Channel switching time <200µs.
- Power supply range: 1.9 to 3.6 V
- CRC computation
- ShockBurst™ mode for ultra-low power operation
- Low supply current, typical 10mA peak @ -5dBm output power
- 100% RF tested
- World wide use

APPLICATIONS

- Wireless mouse, keyboard, joystick
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Intelligent sports equipment
- Industrial sensors
- Toys

GENERAL DESCRIPTION

nRF2402/nRF2402G is a single-chip radio transmitter for the world wide 2.4 - 2.5 GHz ISM band. The transmitter consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channel is easily programmable by use of the 3-wire interface. Current consumption is very low, only 10 mA at an output power of -5dBm. Built-in ShockBurst™ and Power Down modes makes power saving easily realizable.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum GFSK data rate	1000	kbps
Supply current GFSK transmitter @ -5dBm output power	10	mA
Supply current in Power Down mode	200	nA

Table 1 nRF2402/nRF2402G quick reference data

Type Number	Description	Version
NRF2402	16 pin QFN 4x4, punch/saw	A
NRF2402G	16 pin QFN 4x4, punch, green	A

Table 2 nRF2402/nRF2402G ordering information

BLOCK DIAGRAM

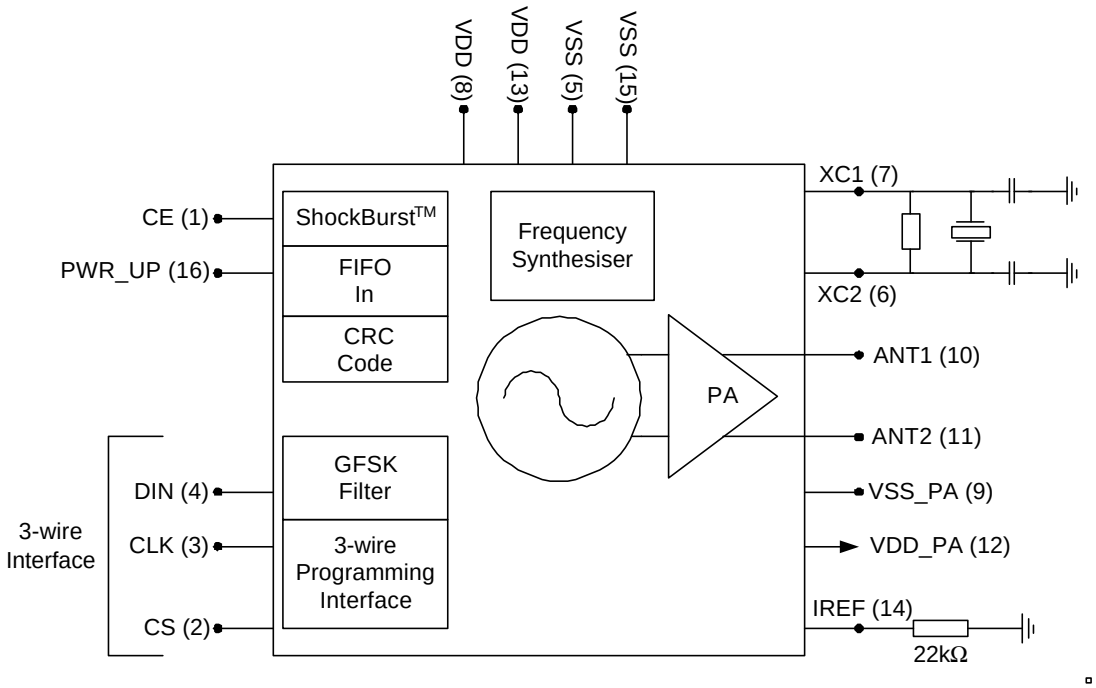


Figure 1 nRF2402/nRF2402G with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	CE	Input	Chip Enable Activates TX mode
2	CS	Input	Chip Select Activates Configuration Mode
3	CLK	Input	Clock Input TX Data and 3-wire Interface
4	DIN	Input	TX Data Input / Configuration Data Input
5	VSS	Power	Ground (0V)
6	XC2	Output	Crystal pin 2
7	XC1	Input	Crystal pin 1
8	VDD	Power	Power Supply (1.9-3.6V)
9	VSS_PA	Power	Ground (0V)
10	ANT1	Power/RF	Antenna output 1
11	ANT2	Power/RF	Antenna output 2
12	VDD_PA	Power Output	Power Supply (+1.8V) output to internal Power Amplifier
13	VDD	Power	Power Supply (1.9-3.6V)
14	IREF	Input	Reference current
15	VSS	Power	Ground (0V)
16	PWR_UP	Input	Power Up

Table 3 nRF2402/nRF2402G pin functions

PIN ASSIGNMENT

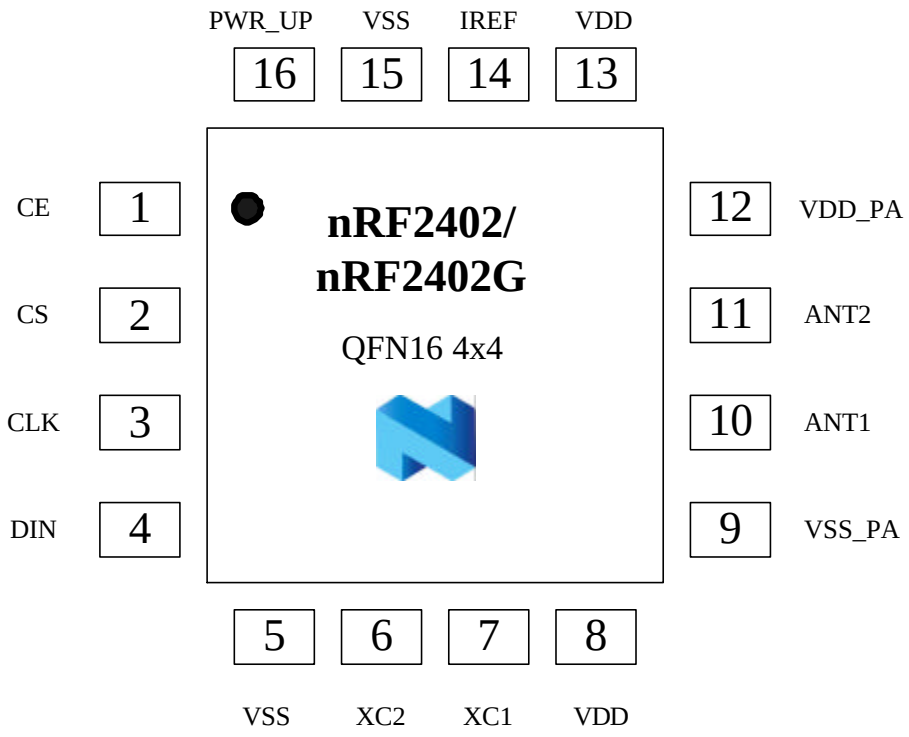


Figure 2. nRF2402/nRF2402G pin assignment (top view).

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, T_A = - 40ºC to + 85ºC

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		0.7·VDD		VDD	V
V_{IL}	LOW level input voltage		Vss		0.3·VDD	V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD- 0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		Vss		0.3	V
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2527	MHz
f_{XTAL}	Crystal frequency	2)	4		20	MHz
Δf	Frequency deviation			±156		kHz
R_{GFSK}	GFSK data rate ShockBurst™		>0		1000	kbps
R_{GFSK}	GFSK data rate Direct Mode	3)	250		1000	kbps
$F_{CHANNEL}$	Channel spacing			1		MHz
	Transmitter operation					
P_{RF}	Maximum Output Power	4)		0	+4	dBm
P_{RFC}	RF Power Control Range		16	20		dB
P_{RFCR}	RF Power Range Control Resolution				±3	dB
P_{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P_{RF2}	2nd Adjacent Channel Transmit Power 2MHz				-20	dBc
P_{RF3}	3rd Adjacent Channel Transmit Power 3MHz				-40	dBc
I_{VDD}	Supply current @ 0dBm output power	5)		11.5		mA
I_{VDD}	Supply current @ -5dBm output power	5)		10.0		mA
I_{VDD}	Supply current @ -10dBm output power	5)		8.5		mA
I_{VDD}	Supply current @ -20dBm output power	5)		7.0		mA
I_{VDD}	Average Supply current @ -5dBm output power, ShockBurst™	6)		500		µA
I_{VDD}	Supply current in stand-by mode			12		µA
I_{VDD}	Supply current in power down			200		nA

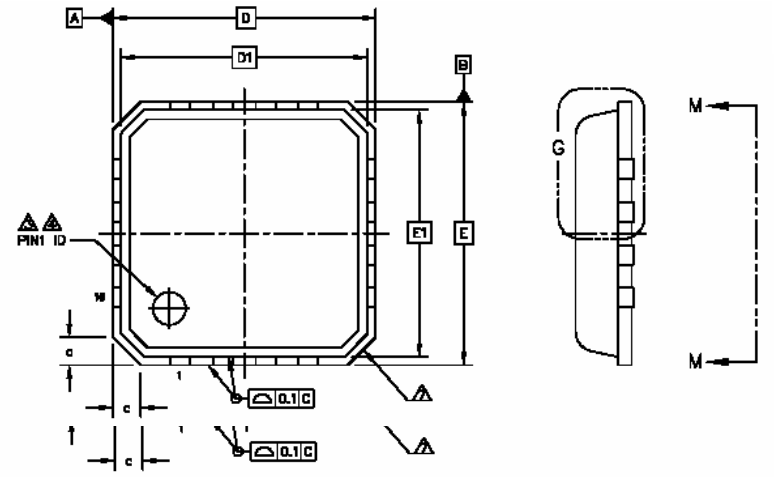
NOTES:

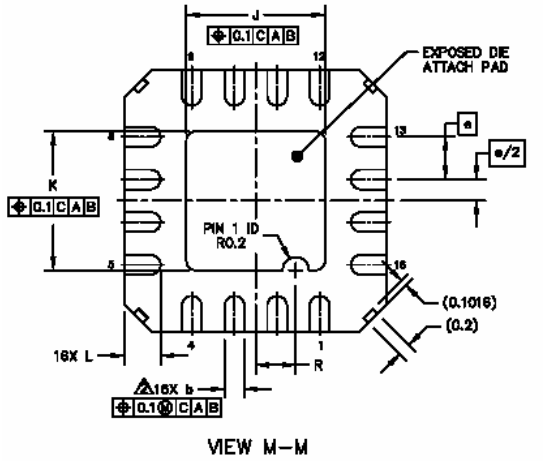
1) Usable band is determined by local regulations
2) The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word, see Table 8. 16MHz is required for 1Mbps operation.
3) Data rate must be either 250kbps or 1000kbps.
4) Antenna load impedance = 100Ω+j175Ω
5) Antenna load impedance = 100Ω+j175Ω. Effective data rate 250kbps or 1Mbps.
6) Antenna load impedance = 100Ω+j175Ω. Effective data rate 10kbps.

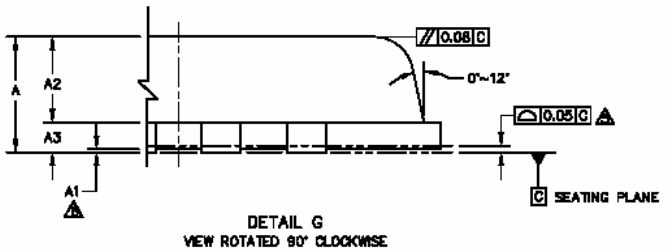
Table 4 nRF2402/nRF2402G electrical specifications

PACKAGE OUTLINE, PUNCH TYPE

nRF2402G uses the GREEN QFN16 4x4 package, with matt tin plating.





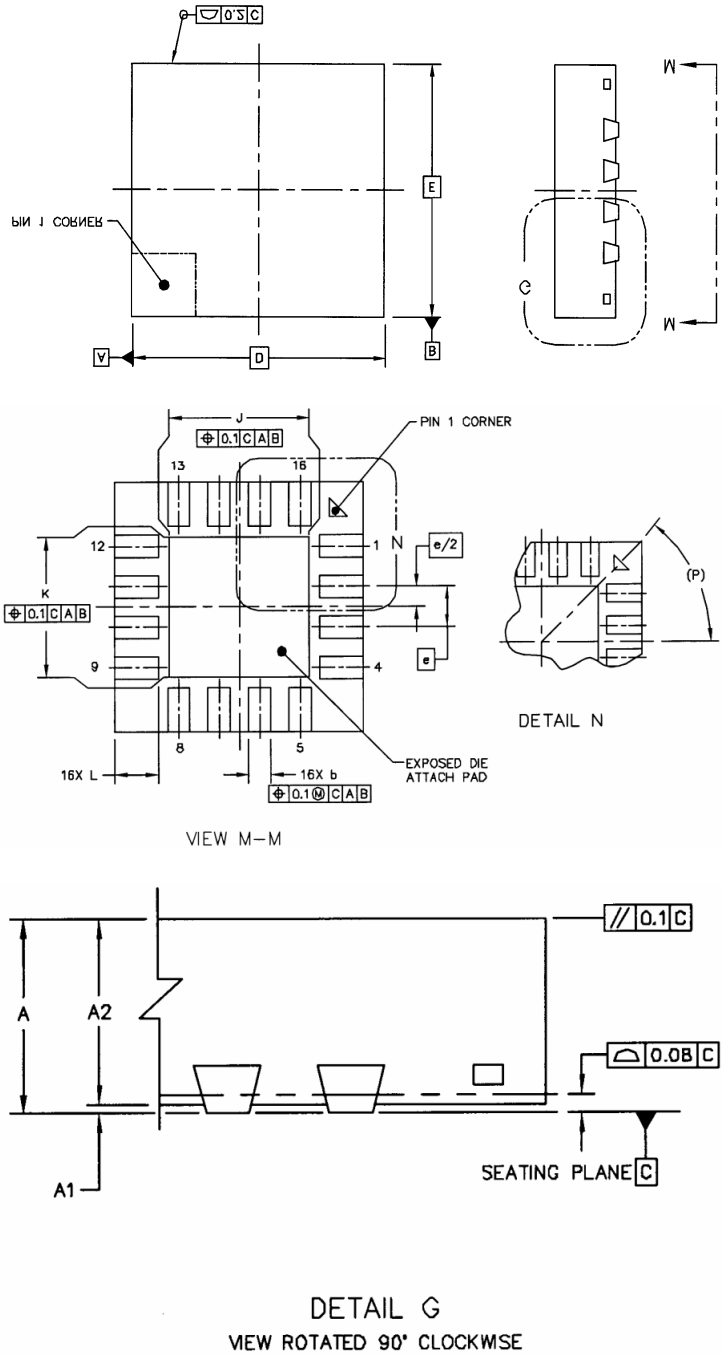


Package Type		A	A_1	A2	b	D/E	D1/E1	e	J	K	L	R
Green QFN16 (4x4 mm)	**Min**	0.8	0.0	0.65	0.25				2.02	2.02	0.45	0.51
	typ.		0.02		0.3	4 BSC	3.75	0.65 BSC	2.12	2.12	0.55	0.61
	Max	0.9	0.05	0.69	0.35		BSC		2.22	2.22	0.65	0.71

Figure 3 nRF2402G Punch package outline.

PACKAGE OUTLINE, SAW TYPE

nRF2402, uses the QFN16 4x4 package, only available with SnPb plating. Dimensions are in mm.



Package Type		A	A_1	A2	b	D	E	e	J	K	L	P
QFN16 (4x4 mm)	**Min**	0.8	0.0	0.75	0.23				0.75	0.7	0.45	45°
	typ.				0.3	4 BSC	4 BSC	0.65 BSC			0.55	REF
	Max	1	0.05	1	0.38				2.25	2.25	0.75	

Figure 4 nRF2402 Saw package outline, dimensions in mm.

ABSOLUTE MAXIMUM RATINGS

Supply voltages
VDD ..... - 0.3V to + 3.6V
VSS 0V

Input voltage
V_I..... - 0.3V to VDD + 0.3V

Output voltage
V_O..... - 0.3V to VDD + 0.3V

Total Power Dissipation
P_D (T_A=85°C) 35mW

Temperatures
Operating Temperature…. - 40°C to + 85°C
Storage Temperature…... - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling.

GLOSSARY OF TERMS

Term	Description
CLK	Clock
CRC	Cyclic Redundancy Check
CS	Chip Select
CE	Chip Enable
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
MCU	Micro Controller Unit
OD	Overdrive
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
ST_BY	Standby
TX	Transmit

Table 5 Glossary

MODES OF OPERATION

Overview of Operational Modes

The nRF2402/nRF2402G can be set in the following main modes depending on three control pins:

Mode	PWR_UP	CE	CS
Active	1	1	0
Configuration	1	0	1
Stand By	1	0	0
Power Down	0	X	X

Table 6 Overview of Operational Modes of nRF2402/nRF2402G.

Active Modes

The nRF2402/nRF2402G has two transmit modes:

- ShockBurst™
- Direct Mode

The device functionality in these modes is determined by the content of a configuration word. This configuration word is presented in the configuration section.

ShockBurst™

The ShockBurst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling extreme reduction in power consumption.
When operating the nRF2402/nRF2402G (in co-operation with nRF2401/nRF24E1) in ShockBurst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.
By putting all high speed signal processing related to RF protocol on-chip, the nRF2402/nRF2402G offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly reduced risk of ‘on-air’ collisions due to short transmission time

The nRF2402/nRF2402G can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.
By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the nRF ShockBurst™ mode reduces the average current consumption in applications considerably.

ShockBurst™ principle

When the nRF2402/nRF2402G is configured in ShockBurst™, TX operation is conducted in the following way (10 kbps for this example only).

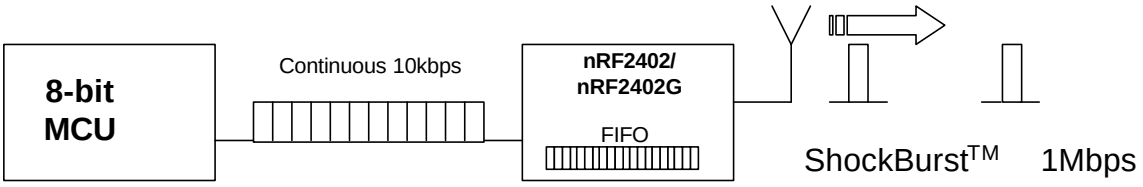


Figure 5 Clocking in data with MCU and sending with ShockBurst™ technology

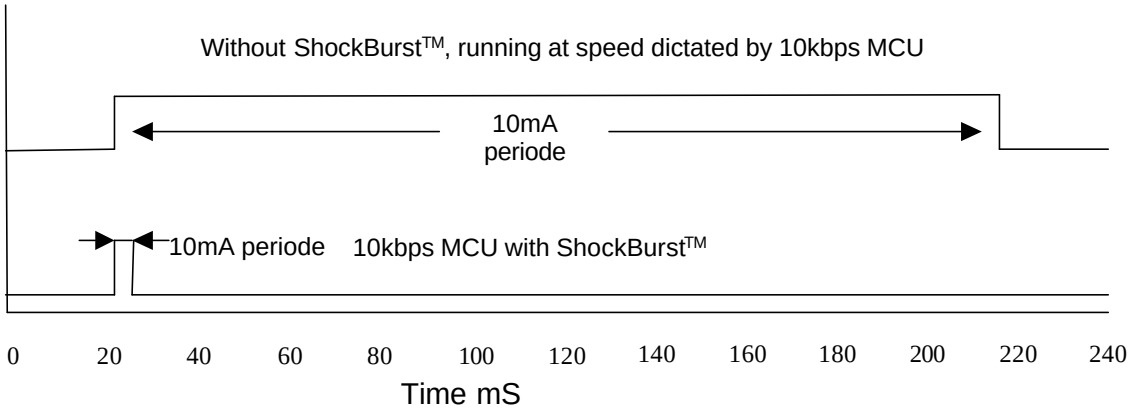


Figure 6 Current consumption with and without ShockBurst™ technology

nRF2402/nRF2402G ShockBurst™ Transmit:

MCU interface pins: CE, CLK, DIN

1. When the application MCU has data to send, set CE high. This activates RF2402 on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the nRF2402/nRF2402G. The application protocol or MCU sets the speed (ex: 10kbps).
3. MCU sets CE low, this activates a nRF2402/nRF2402G ShockBurst™ transmission.
4. nRF2402/nRF2402G ShockBurst™:
    - RF front end is powered up
    - RF package is completed (preamble added, CRC calculated)
    - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
    - nRF2402/nRF2402G returns to stand-by when finished

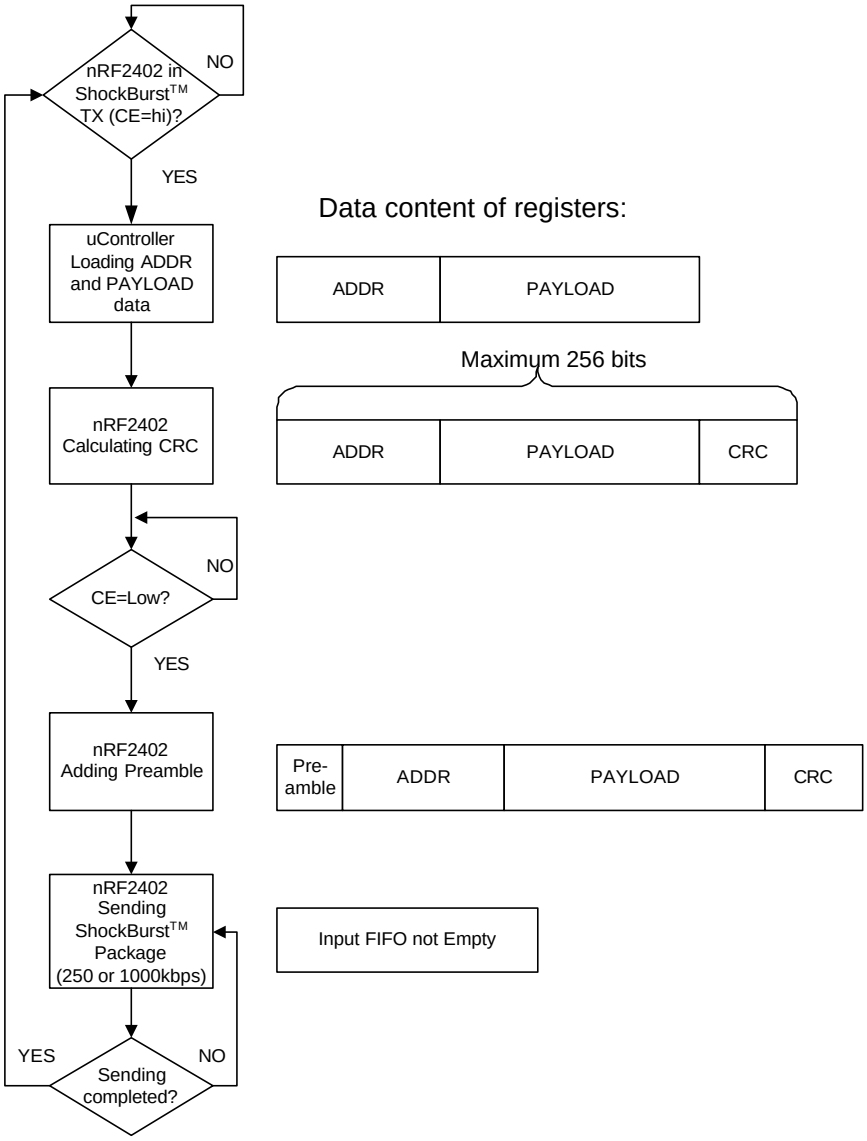


Figure 7 Flow Chart ShockBurst™ Transmit of nRF2402/nRF2402G with CRC and preamble.

Direct Mode

In direct mode the nRF2402/nRF2402G works like a traditional RF device. The data rate must be 1Mbps ±200ppm, or 250kbps ±200ppm at low data rate setting, for the receiver (nRF2402/nRF24E1) to detect the signals.

MCU interface pins: CE, DIN

1. When application MCU has data to send, set CE high
2. The nRF2402/nRF2402G RF front end is now immediately activated, and after 200 µs settling time, signal on the DIN pin will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

Configuration Mode

In configuration mode a configuration word of up to 20 bits is downloaded to nRF2402/nRF2402G. This is done through a simple 3-wire interface (CS, CLK and DIN). For more information on configuration please refer to the nRF2402/nRF2402G device configuration chapter, page13.

Power Down Mode

Power down mode is used to achieve very low current consumption. Effectively the chip is disabled with minimal leakage current consumption, typically less than 200nA. Operating in this mode when not transmitting data significantly increases battery lifetime.

Stand-By Mode

Stand by mode is used to achieve low current consumption. In this mode only a part of the crystal oscillator is running (12µA) to guarantee a short start-up time. Operating in this mode when not transmitting data increases battery lifetime while keeping start up delays short.

Pin configuration for the different modes of nRF2402/nRF2402G

nRF2402/nRF2402G MODES	**INPUT PINS**				
Pin Name	**PWR_UP**	**CE**	**CS**	**CLK**	**DIN**
Power down	0	0	X	X	X
Stand by	1	0	0	X	X
Configuration	1	0	1	CLK	CONFIG DATA
TX ShockBurst™	1	1	0	CLK	TX DATA
TX Direct	1	1	0	Set to 0*	TX DATA

Table 7 Pin configuration of nRF2402/nRF2402G.

* CLK not used in direct mode.

DEVICE CONFIGURATION

All configuration of the nRF2402/nRF2402G is done via a 3-wire interface to a single configuration register. The configuration word can be up to 20 bits long for ShockBurst™ use and up to 14 bits long for direct mode.

Configuration for ShockBurst™ operation

The configuration word in ShockBurst™ enables the nRF2402/nRF2402G to handle the RF protocol (in co-operation with nRF2401/nRF24E1). Once the protocol is completed and loaded into nRF2402/nRF2402G only seven bits, also used in direct mode, needs to be updated during operation.

The configuration bits dedicated to ShockBurst™ is as follows:

- Preamble: Generation of 8 bit preamble in transmitted data.
- CRC: Enables nRF2402/nRF2402G on-chip CRC generation.

NOTE:
The MCU must generate an address and a payload section that fits the configuration of the nRF2401/nRF24E1 that is to receive the data.
When using the nRF2402/nRF2402G on-chip CRC feature ensure that CRC is enabled and uses the same length for both the nRF2402/nRF2402G and the receiving nRF2401/nRF24E1 devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 8 Data packet set-up

Configuration for Direct Mode operation

For direct mode operation only the 14 first bits (bit[13:0]) of the configuring word is relevant.

Configuration Word overview

	Bit position	Number of bits	Name	Function
General device configuration				
	19	6	PLL Control	Close the PLL for test.
	18	1		UNUSED
	17	1	PREAMBLE	Enable on-chip PREAMBLE generation
	16	1	PREAMBLE	UNUSED, must be 1
	15	1	CRC	8 or 16 bit CRC
	14	1	CRC	Enable on-chip CRC generation
	13	1	CM	Communication mode (Direct or ShockBurst™)
	12	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	11:9	3	XO_F	Crystal frequency
	8:7	2	RF_PWR	RF output power
	6:0	7	RF_CH#	Frequency channel (0 to 127)

Table 8 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK edges. New configuration is enabled on the negative edge of CS.

NOTE!
On the negative edge of CS, the nRF2402/nRF2402G updates the number of bits actually shifted in during the last configuration.
Ex:
If the nRF2402/nRF2402G is to be configured for Preamble and CRC in ShockBurst™, a total of 17 bits must be shifted in during the first configuration after VDD is applied.
Once the wanted "protocol" and modus are set there is no need to update this part of the configuration during operation. If RF channel is to be changed, only the RF_CH# bits need to be updated.

Configuration Word Detailed Description

The following describes the function of the 32 bits (bit 31 = MSB) that is used to configure the nRF2402/nRF2402G.
General Device Configuration: bit[13:0]
ShockBurst™ Configuration: bit[17:14]
Test Configuration: bit[19:18]

TEST		ShockBurst				
D19	D18	D17	D16	D15	D14	
PLL		PRE_EN		CRC		
0	0	1	1	0	0	Default

RF-Programming													LSB	
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Burst	OD	XO Frequency			RF Power		Channel selection							
0	0	1	1	1	1	0	0	0	0	0	0	1	0	Default

The MSB bit should be loaded first into the configuration register.
Default configuration word: h30F02.

Test configuration

Bit 19:

PLL: For test purposes the PLL may be closed to send a constant carrier
Logic 0: Open loop (normal operation)
Logic 1: Closed loop (test only)

Bit: 18:

Not used, must be set to logic 1

ShockBurst™ configuration

The section bit[17:14] contains the segments of the configuration register dedicated to ShockBurst™ operation. After VDD is turned on ShockBurst™ configuration must be done once, but remains set whilst VDD is present. During operation only the 7 bits for frequency channel normally need to be changed.

PREAMBLE		CRC	
17	16	15	14

Table 9 Preamble and CRC settings.

Bit 17:

PRE_EN: Preamble to be generated by nRF2402/nRF2402G in ShockBurst™.
Logic 0: No generation of Preamble
Logic 1: Preamble generation enabled (default)

Bit: 16:

Not used, must be set to logic 1

Bit 15:

CRC_L: CRC length to be calculated by nRF2402/nRF2402G in ShockBurst™.
Logic 0: 8 bit CRC (default)
Logic 1: 16 bit CRC

Bit: 14:

CRC_EN: Enables on-chip CRC generation (TX)
Logic 0: On-chip CRC generation disabled (default)
Logic 1: On-chip CRC generation enabled

NOTE:
An 8 bit CRC (compared to 16 bit) will increase the number of payload bits possible in each ShockBurst™ data packet, but will also reduce the communication integrity.

General device configuration:

This section of the configuration word handles RF and device related parameters.

Burst	OD	XO_F			RF_PWR	
13	12	11	10	9	8	7

Table 10 RF operational settings.

Bit 13:

Burst: Logic 0: nRF2402/nRF2402G operates in direct mode (default)
Logic 1: nRF2402/nRF2402G operates in ShockBurst™ mode

Bit 12:

OD:

Logic 0: 250 kbps data rate
Logic 1: 1 Mbps data rate

NOTE:

1Mbps requires 16MHz crystal.

Bit 11-9:

XO_F: Selects the nRF2402/nRF2402G crystal frequency to be used:

XO FREQUENCY SELECTION			
D11	**D10**	**D9**	**Crystal Frequency [MHz]**
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20

Table 11 Crystal frequency setting.

Bit 8-7:

RF_PWR: Sets nRF2402/nRF2402G RF output power:

RF OUTPUT POWER		
D8	**D7**	**P [dBm]**
0	0	-20
0	1	-10
1	0	-5
1	1	0

Table 12 RF output power setting.

Conditions: Load impedance = 100+j175 Ω.

RF channel

RF_CH#						
6	5	4	3	2	1	0

Table 13 Frequency channel setting.

Bit 6 – 0:

RF_CH#: Sets the frequency channel the nRF2402/nRF2402G transmits in.

The channel frequency is given by:

$$Channel_{RF} = 2400\ MHz + RF_CH\# \cdot 1.0\ MHz$$

RF_CH #: Frequencies between 2400MHz and 2527MHz may be set.

DATA PACKAGE DESCRIPTION

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 9 Data Package Diagram

The data packet for both ShockBurst™ mode and direct mode communication is divided into 4 sections. These are:

1. PREAMBLE	• The preamble field is a requirement for ShockBurst™ and Direct modes • Preamble is 8 bits in length and is dependent on the 1st data bit. PREAMBLE — 1st Data Bit (Address) 01010101 — 0 10101010 — 1 • Preamble is automatically added to the data packet and thereby gives extra space for payload in ShockBurst™. Preamble must be added by MCU in Direct mode
2 ADDRESS	• The address field is required in ShockBurst™ mode.[1] • 8 to 40 bits length. • Address automatically removed from received packet in ShockBurst™ mode. In Direct mode MCU must handle address.
3 PAYLOAD	• The data to be transmitted • In ShockBurst™ mode payload size is 256 bits minus the following: (Address: 8 to 40 bits. + CRC 8 or 16 bits). • In Direct mode the maximum payload size is defined by 1Mbps for 4ms: 4000 bits minus the following: (Preamble: 8 bits. + Address: 0 to 40 bits. + CRC: 0, 8 or 16 bits).
4 CRC	• On chip CRC calculation is an option in ShockBurst™ mode, and is not used in Direct mode. • 8 or 16 bits length

Table 14 Data package

[1] Suggestions for the use of addresses in ShockBurst™: In general more bits in the address gives less false detection, which in the end may give lower data packet loss.

- The address made by (5, 4, 3, or 2) equal bytes are not recommended because it in general will make the packet-error-rate increase.
- Addresses where the level shift only one time (i.e. 000FFFFFFF) could often be detected in noise that may give a false detection, which again may give raised packet-error-rate.

Direct mode will be dependent on the software used in the MCU, but it is recommended to have the same restrictions on addresses for this mode.

IMPORTANT TIMING DATA

The following timing applies for operation of nRF2402/nRF2402G.

nRF2402/nRF2402G Timing Data

nRF2402/nRF2402G timing	Min.	Max.	Name
PWR_DWN ➔ Configuration mode		3ms	Tpd2cfgm
PWR_DWN➔ Active mode (TX)		3ms	Tpd2a
ST_BY ➔ TX ShockBurst™		195µs	Tsby2txSB
ST_BY ➔ TX Direct Mode		202µs	Tsby2txDM
Minimum delay from CS to data.	5µs		Tcs2data
Minimum delay from CE to data.	5µs		Tce2data
Delay between edges	50ns		Td
Setup time	500ns		Ts
Hold time	500ns		Th
Delay to finish internal GFSK data	1/data rate		Tfd
Minimum input clock high	500ns		Thmin
Time on air, TX Direct mode		4ms	ToaDM

Table 15 Switching times for nRF2402/nRF2402G

When the nRF2402/nRF2402G is powered up it must always settle in stand by for 3ms before it can enter configuration or active mode.

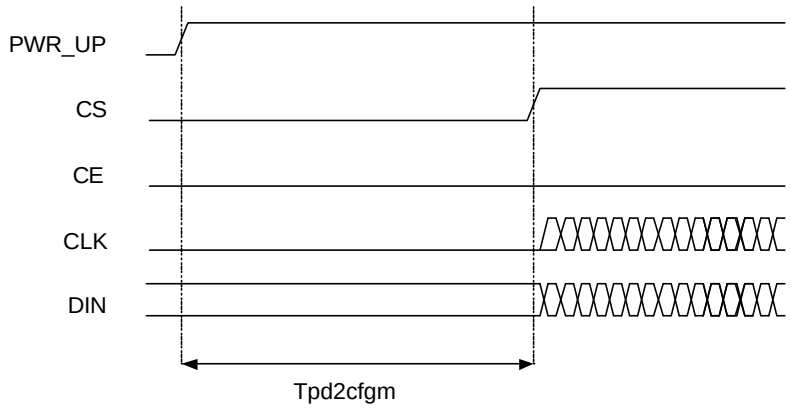


Figure 10 Timing diagram for power down (or VDD off) to configuration mode for nRF2402/nRF2402G.

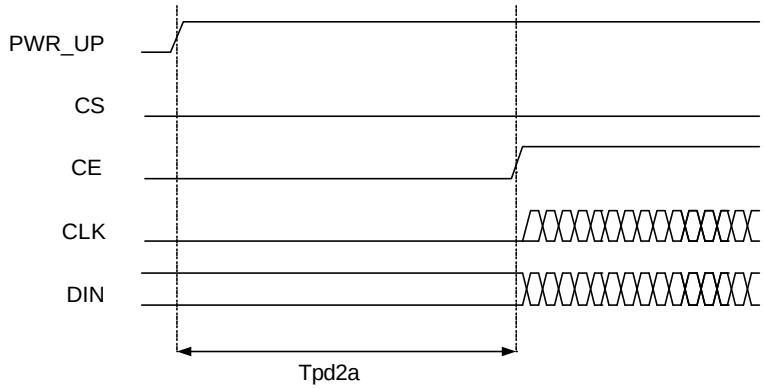


Figure 11 Power down (or VDD off) to active mode

Note that the configuration word will be lost when VDD is turned off and that the device then must be configured before going to active mode. If the device is configured one can go directly from power down to active mode.

Note:

CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.

Configuration Mode

In configuration mode the transmitters output power, transmit frequency, data rate, CRC, and preamble is set. The configuring data will be loaded during the Chip Select period (CS="1"). A random number of bits between 1 and 20 may be shifted in to the register to configure the transmitter, but normally you would at least shift in the seven channel frequency bits. The new configuration is activated on the negative edge of CS.

When one or more of the bits in the configuration word needs to be changed the following timing apply.

Configuration Mode Timing

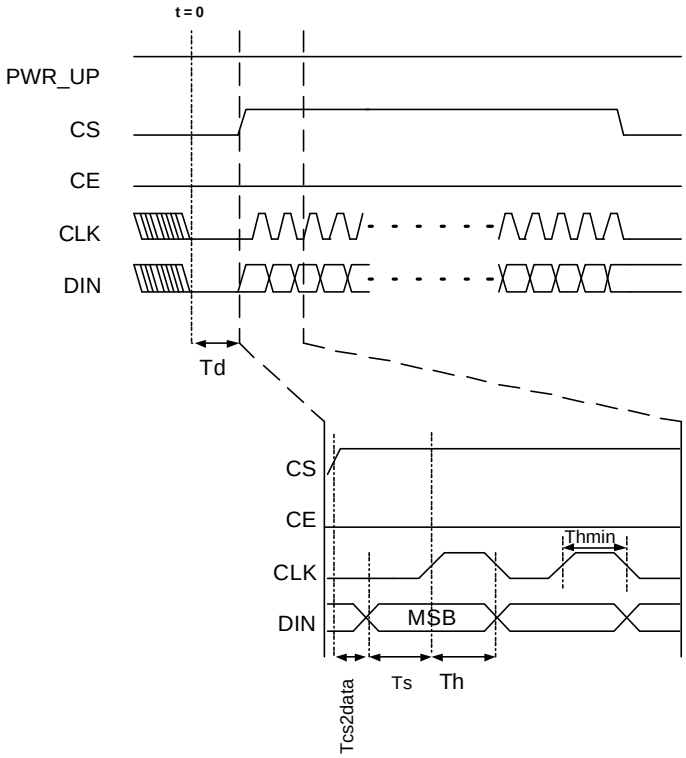


Figure 12 Timing Diagram of Configuration Mode

If configuration mode is entered from power down, CS can be set high after Tpd2sby as shown in Figure 10.

ShockBurst™ Mode Timing

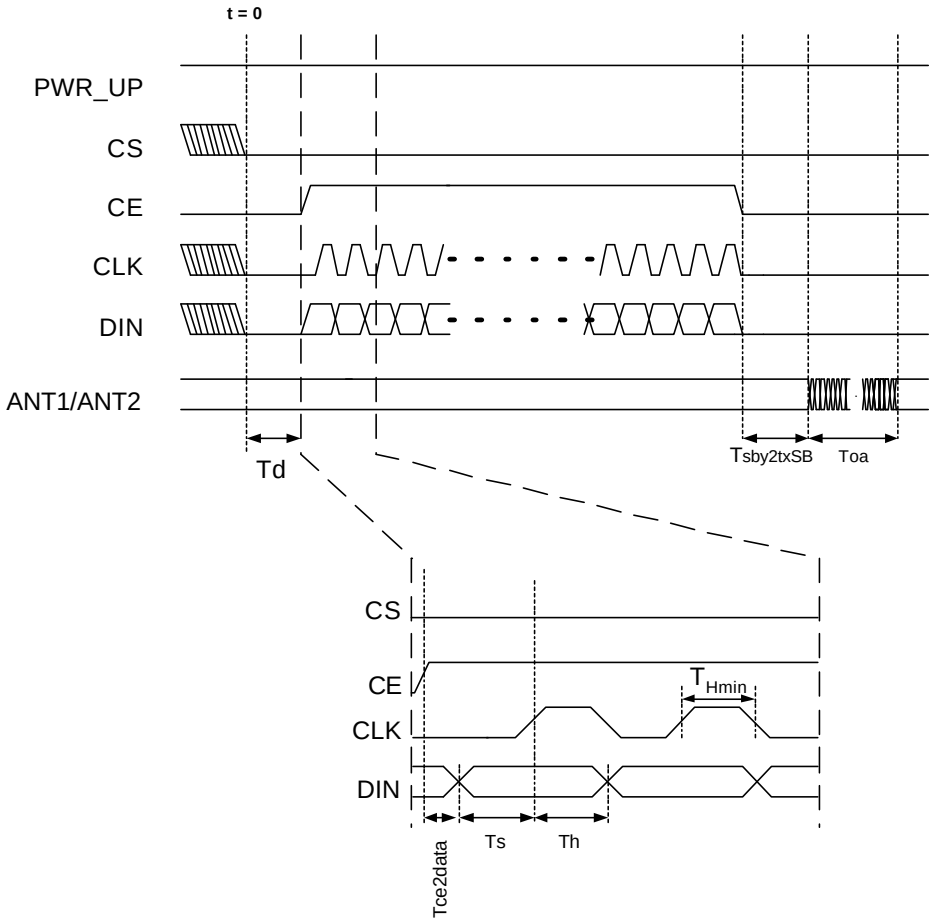


Figure 13 Timing of ShockBurst™ in nRF2402/nRF2402G.

The package length and the data rate give the delay Toa (time on air), as shown in the equation.

$$T_{OA} = 1/datarate \cdot (\#databits + 1)$$

Direct Mode Timing

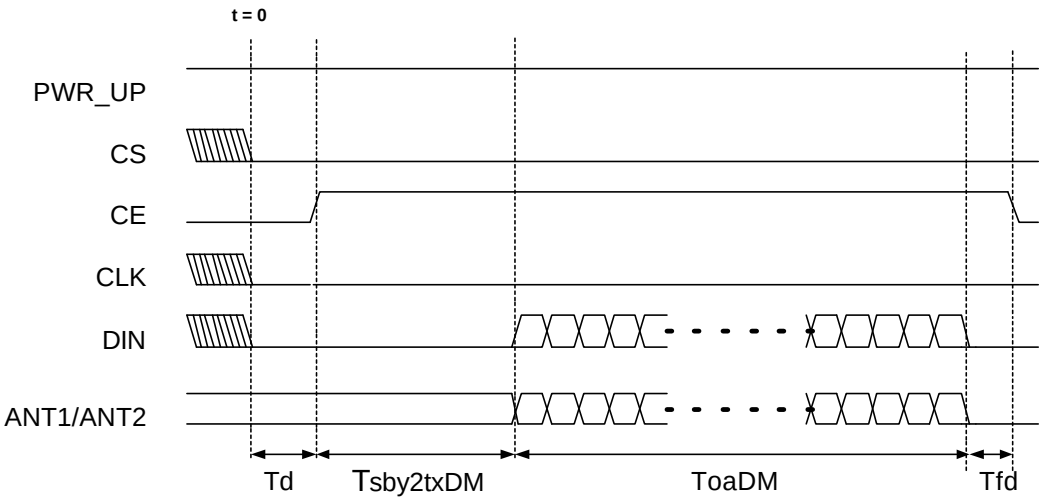


Figure 14 Timing Diagram of Direct Mode

In direct mode the input data will be sampled by nRF2402/nRF2402G and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay $T_{sby2txDM}$ is given by the equation:

$$T_{sby2txDM} = 194us + 1/F_{XO} \cdot 20 + 2.25us$$

The maximum length of a package (ToaDM) over all voltages and temperatures is 4ms. This is limited by frequency drift in the transmitter and is independent of data rate and frequency channel.

PERIPHERAL RF INFORMATION

Antenna output

The ANT1 and ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via a RF choke or via the center point in a balanced antenna. Differential load impedance between the ANT1 and ANT2 pins, 100Ω+j175Ω, is recommended for maximum output power. Antennas with lower load impedance (for example 50Ω) can be matched to nRF2402/nRF2402G by using a simple matching network.

Antenna matching networks

The recommended 50Ω matching network is shown in Figure 15. This is a low pass network improving higher harmonic suppression.

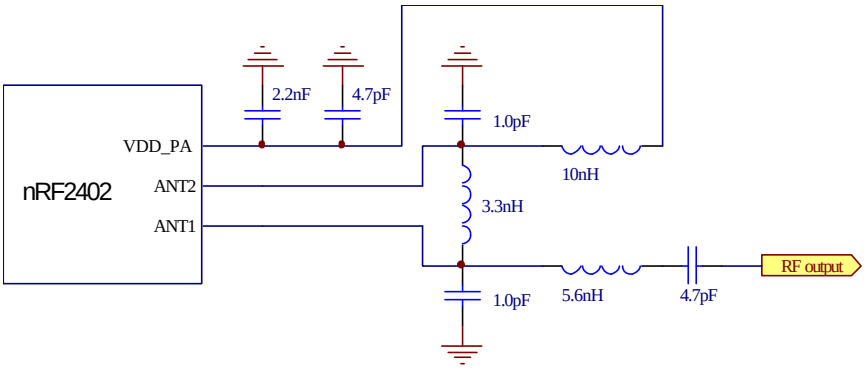


Figure 15 Low pass antenna matching network

A somewhat simpler matching network is shown in Figure 16.

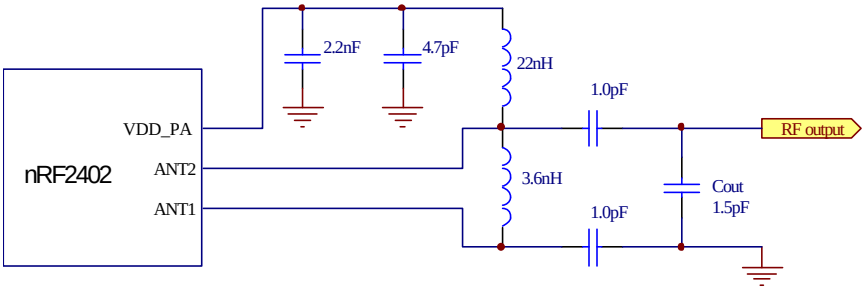


Figure 16 High pass antenna matching network

This network utilizes one component less and uses few inductors, but performance of this network requires very careful PCB ground plane layout. The value of capacitor C_{out} is dependent on PCB ground plane layout and parasitics in the layout, and must hence be matched to a given application layout. The value of C_{out} will typically be in the range 1.0pF – 1.8pF. C_{out} must be tuned while checking that the harmonics output is below frequency regulatory limits.

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	11.5 mA
10	-5 dBm ±3dB	10.0 mA
01	-10 dBm ±3dB	8.5 mA
00	-20 dBm ±3dB	7.0 mA

Conditions: Load impedance = 100+j175 Ω.

Table 16 RF output power setting for the nRF2402/nRF2402G.

Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
4MHz	8pF – 16pF	150Ω	7.0pF	±30ppm
8MHz	8pF – 16pF	100Ω	7.0pF	±30ppm
12MHz	8pF – 16pF	100Ω	7.0pF	±30ppm
16MHz	8pF – 16pF	100Ω	7.0pF	±30ppm
20MHz	8pF – 16pF	100Ω	7.0pF	±30ppm

Table 17 Crystal specification of the nRF2402/nRF2402G

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying a lower value of crystal parallel equivalent capacitance, Co=1.5pF is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.

The crystal load capacitance, C_L, is given by:

$$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}, \quad where\, C_1' = C_1 + C_{PCB1} + C_{I1}\ and\ C_2' = C_2 + C_{PCB2} + C_{I2}$$

C_1 and C_2 are 0603 SMD capacitors as shown in the application schematics. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the XC1 and XC2 pin respectively; the value is typical 1pF.

Sharing crystal with micro controller.

When using a micro controller to drive the crystal reference input XC1 of the nRF2402/nRF2402G transmitter some rules must be followed.

Crystal parameters:

When the micro controller drives the nRF2402/nRF2402G XC1 input, all crystal load parameters (C_L, C_0, ESR) are set by the micro controller specification. The frequency accuracy (±30 ppm) is still set by the nRF2402/nRF2402G specification. The nRF2402/nRF2402G will load the crystal circuitry of the micro controller by XC1 input capacitance (0.5pF) plus PBC routing paracitics.

External reference input amplitude & Current consumption

The reference input should never have signal levels exceeding rail voltages. Exceeding rail voltage will excite the ESD structure and the radio performance is degraded below specification. Applying reference sources without DC bias will bring the reference signal under GND level, and this is not acceptable.

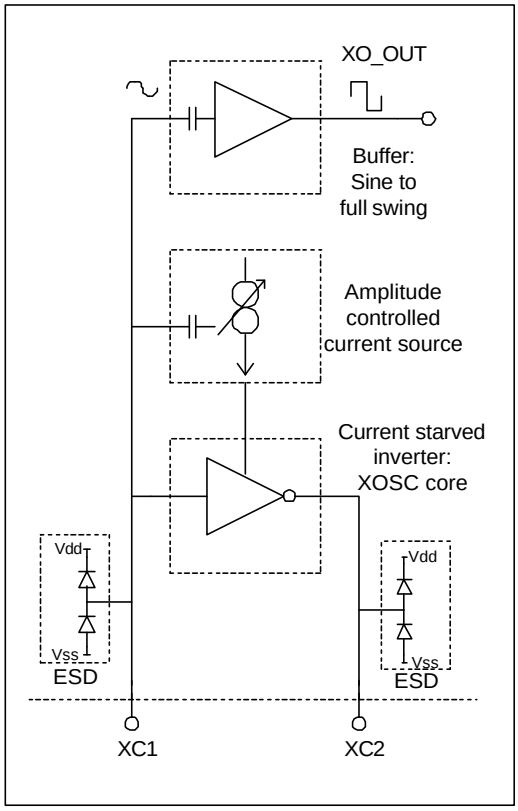


Figure 17 Principle of crystal oscillator

It is hence recommended to use a DC-block before the XC1 pin so that the internal ESD structures will self bias the XC1 voltage.

The nRF2402/nRF2402G crystal oscillator is amplitude regulated. To achieve low current consumption and also good signal-to-noise ratio, it is recommended to use an input signal

larger than 0.4 V-peak. The needed input swing is independent of the crystal frequency. When using external crystal refernce, XC2 is not used and can be left as an open pin.

Frequency Reference MCU

In direct mode there is a requirement on the accuracy of the data rate. For the receiver to detect the incoming data and recover the clock, the data rate must be within ±200ppm, given that the data is "random", i.e. there is a statistical calculation on how often a preamble like sequence is present in the data. The clock is synchronized for any preamble detection, be it a dedicated preamble or part of the data stream.

PCB layout and de-coupling guidelines

A well-designed PCB is necessary to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality, if due care is not taken. A fully qualified RF-layout for the nRF2402/nRF2402G and its surrounding components, including matching networks, can be downloaded from **www.nordicsemi.no**.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF2402/nRF2402G DC supply voltage should be de-coupled as close as possible to the VDD pins with high performance RF capacitors, see Table 18. It is preferable to mount a large surface mount capacitor (e.g. 4.7µF tantalum) in parallel with the smaller value capacitors. The nRF2402/nRF2402G supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF2402/nRF2402G IC. The VSS pins should be connected directly to the ground plane. One via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

APPLICATION EXAMPLE

nRF2402/nRF2402G with single ended matching network

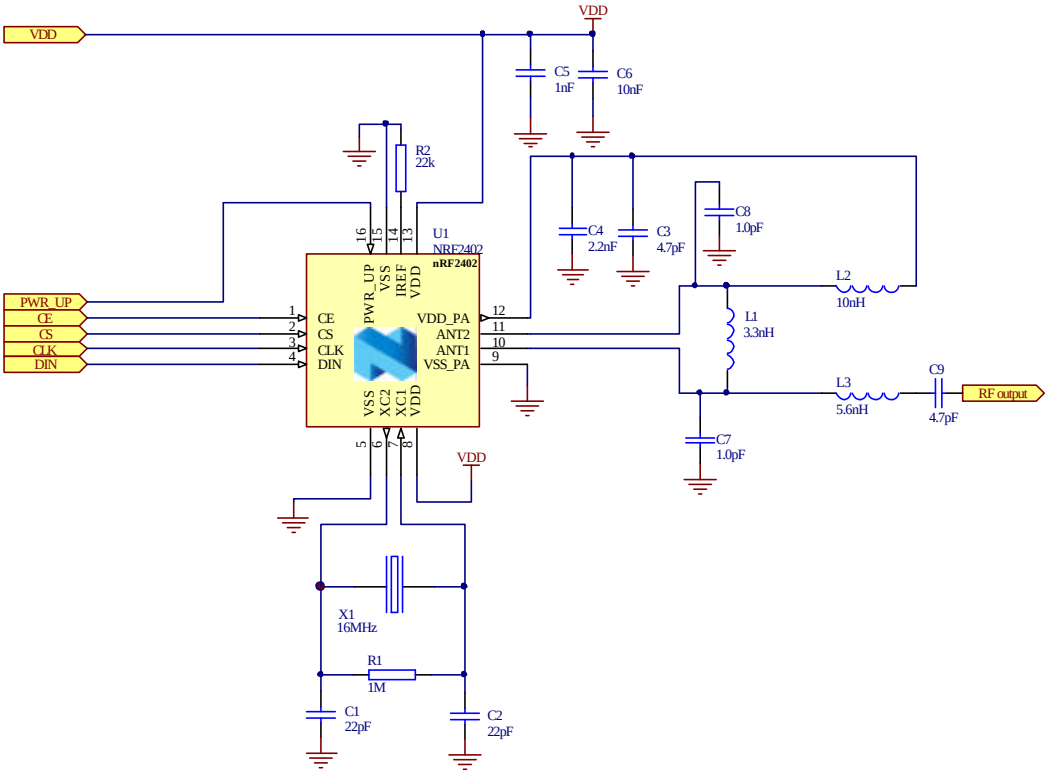


Figure 18 nRF2402/nRF2402G schematic for RF layouts with single ended 50Ω antenna

Component	Description	Size	Value	Tolerance	Units
C1	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C2	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C3	Capacitor ceramic, 50V, NPO	0603	4.7	±5%	pF
C4	Capacitor ceramic, 50V, X7R	0603	2.2	±10%	nF
C5	Capacitor ceramic, 50V, X7R	0603	1.0	±10%	nF
C6	Capacitor ceramic, 50V, X7R	0603	10	±10%	nF
R1	Resistor	0603	1.0	±10%	MΩ
R2	Resistor	0603	22	±1%	kΩ
U1	**nRF2402/nRF2402G** transmitter	QFN16 / 4x4	nRF2402/ nRF2402G		
X1	Crystal, CL = 12pF, ESR < 100 ohm	LxWxH = 4.0x2.5x0.8	16 [1]	+/- 30 ppm	MHz
L1	Inductor [2]	0603	3.3	± 5%	nH
L2	Inductor [2]	0603	10	± 5%	nH
L3	Inductor [2]	0603	5.6	± 5%	nH
C7	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C8	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C9	Ceramic capacitor, 50V, NP0	0603	4.7	± 0.25 pF	pF

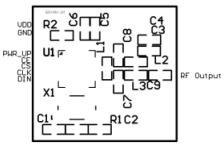
Table 18 Recommended components (BOM) in nRF2402/nRF2402G with antenna matching network

[1] **nRF2402/nRF2402G** can operate at several crystal frequencies, ref. the Crystal Spec. chapter.
[2] Self-resonant frequency (SFR) must be > 2.7 GHz

PCB layout example

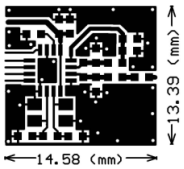
Figure 19 shows a PCB layout example for the application schematic in Figure 18.

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has ground planes on both bottom layer and top layer to ensure good grounding of critical component. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

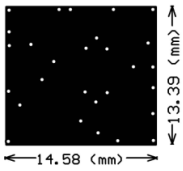


Top silk screen

No components in bottom layer



Top view



Bottom view

Figure 19 nRF2402/nRF2402G RF layout with single ended connection to 50Ω antenna and 0603 size passive components

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Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This datasheet contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Application information	
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Table 19. Definitions.

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Product Specification: Revision Date: 26/04/2005.

Datasheet order code: 260405-nRF2402/nRF2402G.

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