

Low Quiescent Current, Accurate Programmable-Delay Supervisory Circuit

FEATURES

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s
- Very Low Quiescent Current: 2.4µA typ
- High Threshold Accuracy: 0.5% typ
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V Are Available
- Manual Reset ($\overline{\text{MR}}$) Input
- Open-Drain $\overline{\text{RESET}}$ Output
- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Small SOT23 and 2mm x 2mm QFN Packages

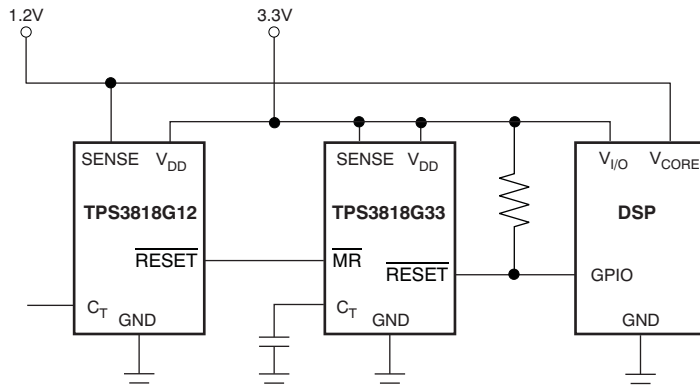
APPLICATIONS

- DSP or Microcontroller Applications
- Notebook/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

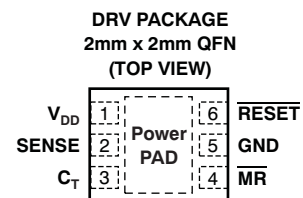
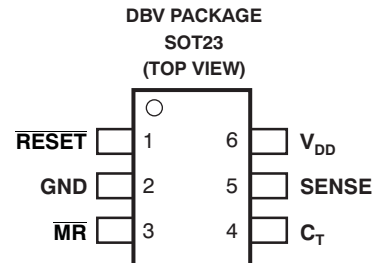
DESCRIPTION

The TPS3818xxx family of microprocessor supervisory circuits monitor system voltages from 0.4V to 5.0V, asserting an open-drain $\overline{\text{RESET}}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin drops to a logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ($\overline{\text{MR}}$) return above the respective thresholds.

The TPS3818 uses a precision reference to achieve 0.5% threshold accuracy for $V_{\text{IT}} \leq 3.3\text{V}$. The reset delay time can be set to 20ms by disconnecting the C_{T} pin, 300ms by connecting the C_{T} pin to V_{DD} using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the C_{T} pin to an external capacitor. When used with an external capacitor, the TPS3818xxx gives a more accurate delay time than the similar TPS3808xxx device. The TPS3818 has a very low typical quiescent current of 2.4µA so it is well-suited to battery-powered applications. It is available in either a small SOT23 and an ultra-small 2mm x 2mm QFN PowerPAD™ package, and is fully specified over a temperature range of -40°C to $+125^{\circ}\text{C}$ (T_{J}).



Typical Application Circuit



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | NOMINAL SUPPLY VOLTAGE ⁽²⁾ | THRESHOLD VOLTAGE (V_{IT}) |
|-------------|---------------------------------------|--------------------------------|
| TPS3818G01 | Adjustable | 0.405V |
| TPS3818G09 | 0.9V | 0.84V |
| TPS3818G12 | 1.2V | 1.12V |
| TPS3818G125 | 1.25V | 1.16V |
| TPS3818G15 | 1.5V | 1.40V |
| TPS3818G18 | 1.8V | 1.67V |
| TPS3818G25 | 2.5V | 2.33V |
| TPS3818G30 | 3.0V | 2.79V |
| TPS3818G33 | 3.3V | 3.07V |
| TPS3818G50 | 5.0V | 4.65V |

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Custom threshold voltages from 0.82V to 3.3V, 4.4V to 5.0V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating junction temperature range, unless otherwise noted.

| | TPS3818 | UNIT |
|--|------------------------|------|
| Input voltage range, V_{DD} | –0.3 to 7.0 | V |
| C_T voltage range, V_{CT} | –0.3 to $V_{DD} + 0.3$ | V |
| Other voltage ranges: V_{RESET} , V_{MR} , V_{SENSE} | –0.3 to 7 | V |
| \overline{RESET} pin current | 5 | mA |
| Operating junction temperature range, T_J ⁽²⁾ | –40 to +150 | °C |
| Storage temperature range, T_{STG} | –65 to +150 | °C |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 500 | V |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

ELECTRICAL CHARACTERISTICS

$1.7V \leq V_{DD} \leq 6.5V$, $R_{LRESET} = 100k\Omega$, $C_{LRESET} = 50pF$, over operating temperature range ($T_J = -40^\circ C$ to $+125^\circ C$), unless otherwise noted. Typical values are at $T_J = +25^\circ C$.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|---|--|---------------------|-------|---------------------|------------------|
| V _{DD} | Input supply range | | −40°C < T _J < +125°C | 1.7 | | 6.5 | V |
| | | | 0°C < T _J < +85°C | 1.65 | | 6.5 | |
| I _{DD} | Supply current (current into V _{DD} pin) | | V _{DD} = 3.3V, $\overline{\text{RESET}}$ not asserted $\overline{\text{MR}}$, $\overline{\text{RESET}}$, C _T open | | 2.4 | 5.0 | μA |
| | | | V _{DD} = 6.5V, $\overline{\text{RESET}}$ not asserted $\overline{\text{MR}}$, $\overline{\text{RESET}}$, C _T open | | 2.7 | 6.0 | μA |
| V _{OL} | Low-level output voltage | | 1.3V ≤ V _{DD} < 1.8V, I _{OL} = 0.4mA | | | 0.3 | V |
| | | | 1.8V ≤ V _{DD} ≤ 6.5V, I _{OL} = 1.0mA | | | 0.4 | V |
| | Power-up reset voltage ⁽¹⁾ | | V _{OL} (max) = 0.2V, I $\overline{\text{RESET}}$ = 15μA | | | 0.8 | V |
| V _{IT} | Negative-going input threshold accuracy | TPS3818G01 | | −2.0 | ±1.0 | +2.0 | % |
| | | V _{IT} ≤ 3.3V | | −1.5 | ±0.5 | +1.5 | |
| | | 3.3V < V _{IT} ≤ 5.0V | | −2.0 | ±1.0 | +2.0 | |
| | | V _{IT} ≤ 3.3V | −40°C < T _J < +85°C | −1.25 | ±0.5 | +1.25 | |
| | | 3.3V < V _{IT} ≤ 5.0V | −40°C < T _J < +85°C | −1.5 | ±0.5 | +1.5 | |
| V _{HYS} | Hysteresis on V _{IT} pin | TPS3818G01 | | | 1.5 | 3.0 | %V _{IT} |
| | | Fixed versions | −40°C < T _J < +85°C | | 1.0 | 2.0 | |
| | | | | | 1.0 | 2.5 | |
| R $\overline{\text{MR}}$ | $\overline{\text{MR}}$ Internal pull-up resistance | | | 70 | 90 | | kΩ |
| I _{SENSE} | Input current at SENSE pin | TPS3818G01 | V _{SENSE} = V _{IT} | −25 | | 25 | nA |
| | | Fixed versions | V _{SENSE} = 6.5V | | 1.7 | | μA |
| I _{OH} | $\overline{\text{RESET}}$ leakage current | | V $\overline{\text{RESET}}$ = 6.5V, $\overline{\text{RESET}}$ not asserted | | | 300 | nA |
| C _{IN} | Input capacitance, any pin | C _T pin | V _{IN} = 0V to V _{DD} | | 5 | | pF |
| | | Other pins | V _{IN} = 0V to 6.5V | | 5 | | |
| V _{IL} | $\overline{\text{MR}}$ logic low input | | | 0 | | 0.3 V _{DD} | V |
| V _{IH} | $\overline{\text{MR}}$ logic high input | | | 0.7 V _{DD} | | V _{DD} | |
| t _w | Input pulse width to $\overline{\text{RESET}}$ | SENSE | V _{IH} = 1.05V _{IT} , V _{IL} = 0.95V _{IT} | | 20 | | μs |
| | | $\overline{\text{MR}}$ | V _{IH} = 0.7V _{DD} , V _{IL} = 0.3V _{DD} | | 0.001 | | |
| t _d | $\overline{\text{RESET}}$ delay time ⁽²⁾ | C _T = Open | See Timing Diagram | 12 | 20 | 28 | ms |
| | | C _T = V _{DD} | | 180 | 300 | 420 | ms |
| V _{CT} | CT pin ($\overline{\text{RESET}}$ delay time) comparator threshold ⁽³⁾ | | | 1.211 | 1.23 | 1.249 | V |
| I _{CT} | CT pin ($\overline{\text{RESET}}$ delay time) charging current ⁽³⁾ | | R _{CT} = 2MΩ (resistor between C _T and GND) | 190 | 220 | 250 | nA |
| t _{pHL} | Propagation delay | $\overline{\text{MR}}$ to $\overline{\text{RESET}}$ | V _{IH} = 0.7V _{DD} , V _{IL} = 0.3V _{DD} | | 150 | | ns |
| | High to low level $\overline{\text{RESET}}$ delay | SENSE to $\overline{\text{RESET}}$ | V _{IH} = 1.05V _{IT} , V _{IL} = 0.95V _{IT} | | 20 | | μs |
| θ _{JA} | Thermal resistance, junction-to-ambient | | | | 290 | | °C/W |

(1) The lowest supply voltage (V_{DD}) at which \overline{RESET} becomes active. $T_{rise(V_{DD})} \geq 15\mu s/V$.

(2) The delay time accuracy without external capacitor is the same as that of the TPS3808xxx. This specification is included here for TPS3808xxx device comparison.

(3) The combined \overline{RESET} delay time accuracy from V_{CT} and I_{CT} is $\pm 15\%$.

FUNCTIONAL BLOCK DIAGRAMS

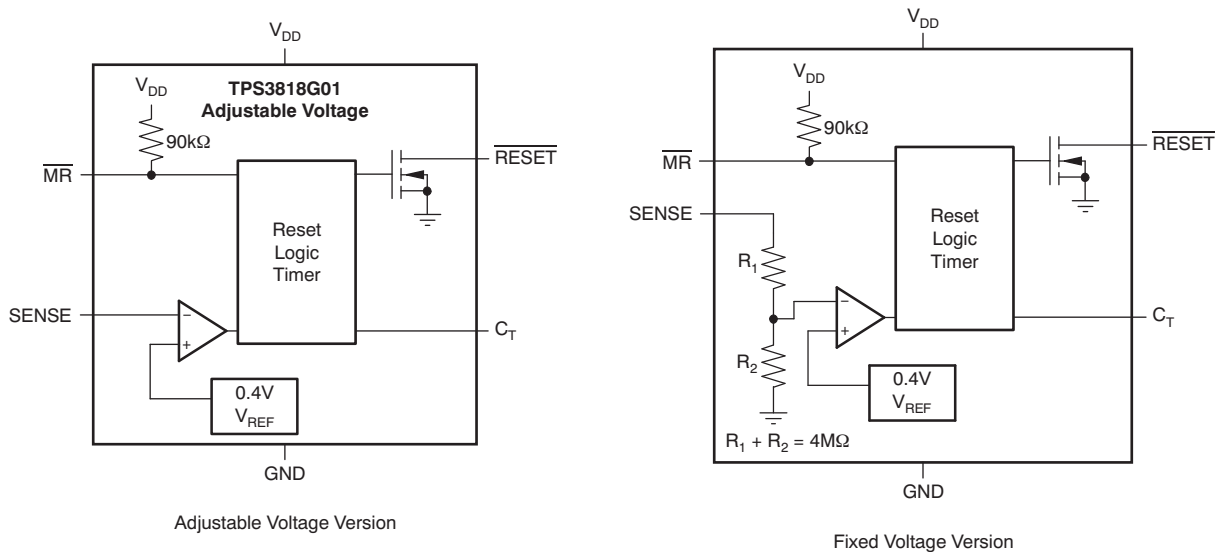


Figure 1. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS



Table 1. TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---------------------------|------------------------|--|
| NAME | SOT23 (DBV) PIN NO. | |
| $\overline{\text{RESET}}$ | 1 | $\overline{\text{RESET}}$ is an open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the MR pin is set to a logic low). $\overline{\text{RESET}}$ remains low (asserted) for the reset period after both SENSE is above V_{IT} and MR is set to a logic high. A pull-up resistor from 10k Ω to 1M Ω should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD} . |
| GND | 2 | Ground |
| $\overline{\text{MR}}$ | 3 | Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by a 90k Ω pull-up resistor. |
| C_T | 4 | Reset period programming pin. Connecting this pin to V_{DD} through a 40k Ω to 200k Ω resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor $\geq 100\text{pF}$ gives a user-programmable delay time. See the Selecting the Reset Delay Time section for more information. |
| SENSE | 5 | This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT} , then $\overline{\text{RESET}}$ is asserted. |
| V_{DD} | 6 | Supply voltage. It is good analog design practice to place a 0.1 μF ceramic capacitor close to this pin. |
| PowerPAD | | PowerPAD. Connect to ground plane to enhance thermal performance of package. |

TIMING DIAGRAM

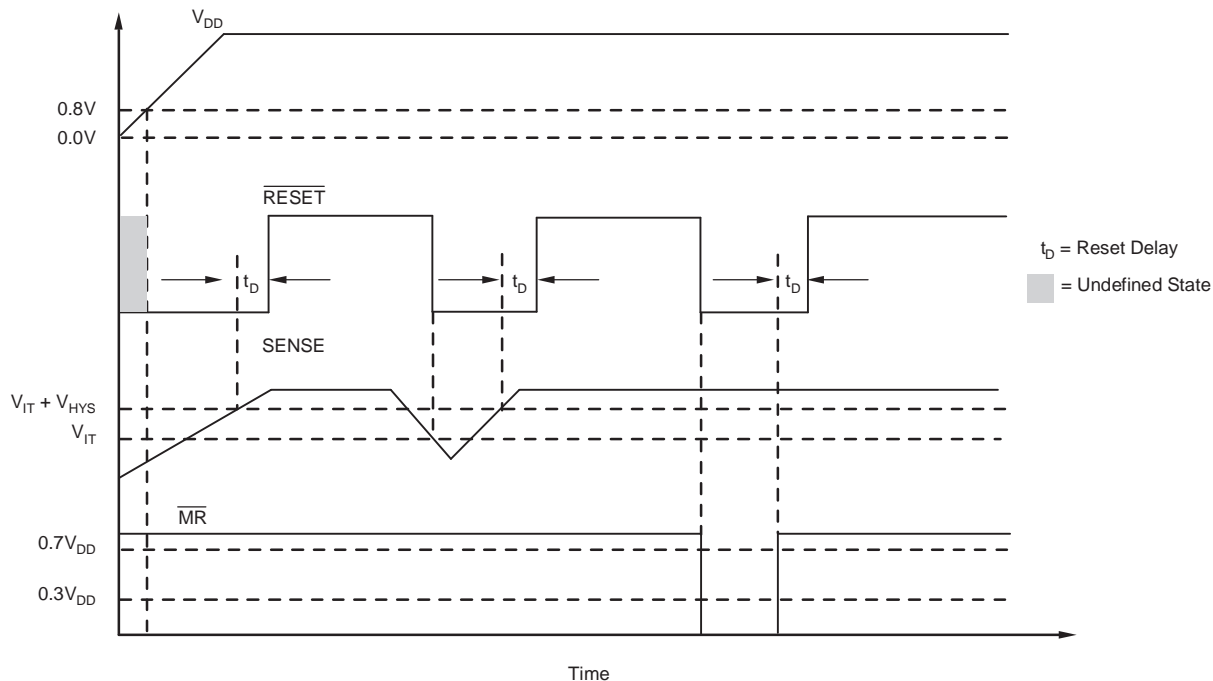


Figure 2. TPS3818 Timing Diagram Showing \overline{MR} and $SENSE$ Reset Timing

TRUTH TABLE

| \overline{MR} | $SENSE > V_{IT}$ | \overline{RESET} |
|-----------------|------------------|--------------------|
| L | 0 | L |
| L | 1 | L |
| H | 0 | L |
| H | 1 | H |

TYPICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $R_{L\text{RESET}} = 100\text{k}\Omega$, and $C_{L\text{RESET}} = 50\text{pF}$, unless otherwise noted.

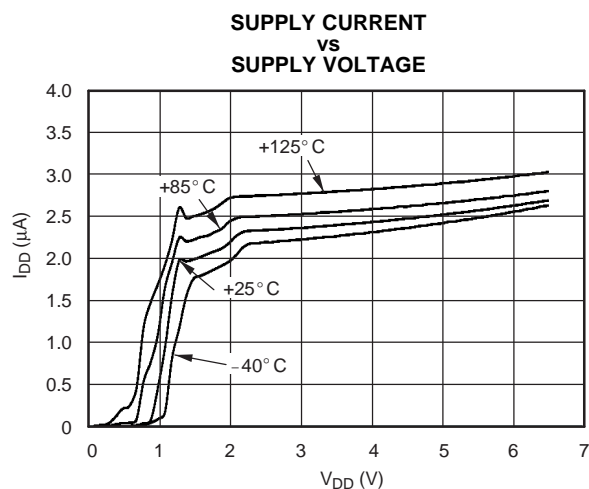


Figure 3.

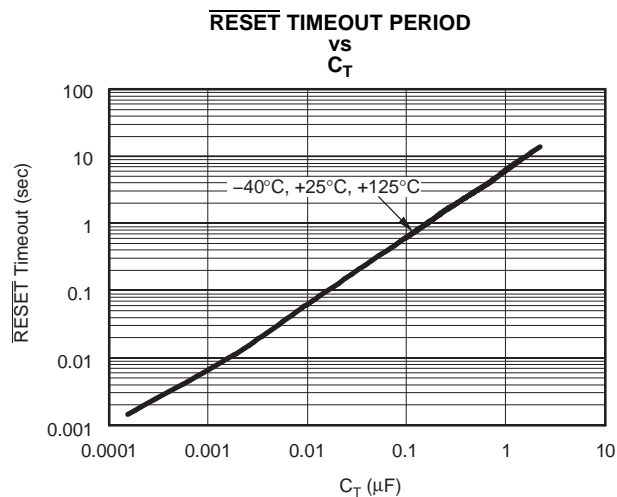


Figure 4.

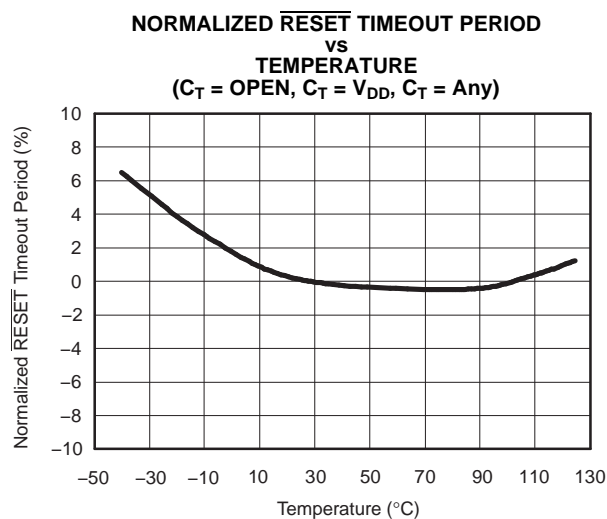


Figure 5.

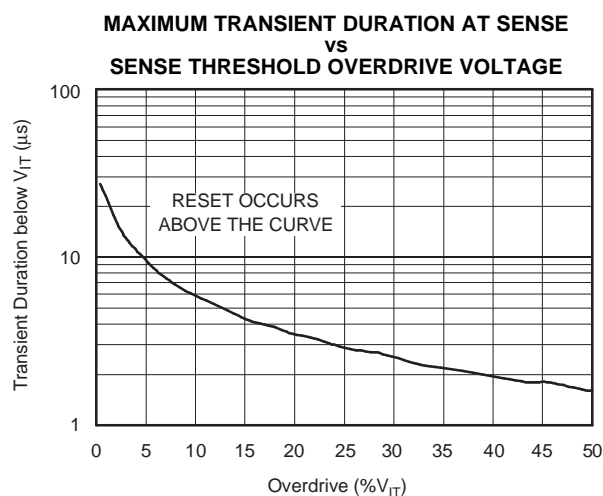


Figure 6.

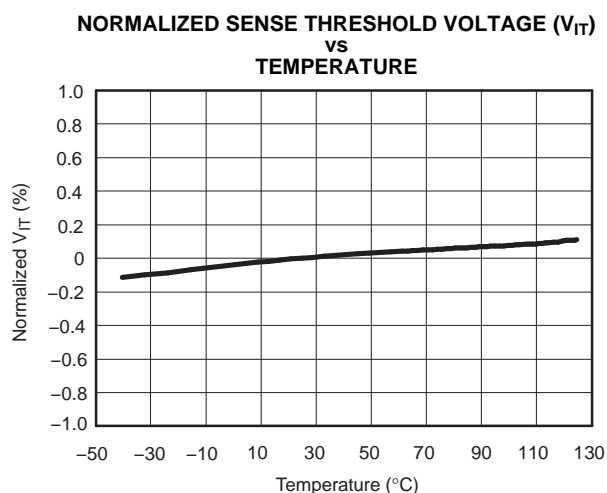


Figure 7.

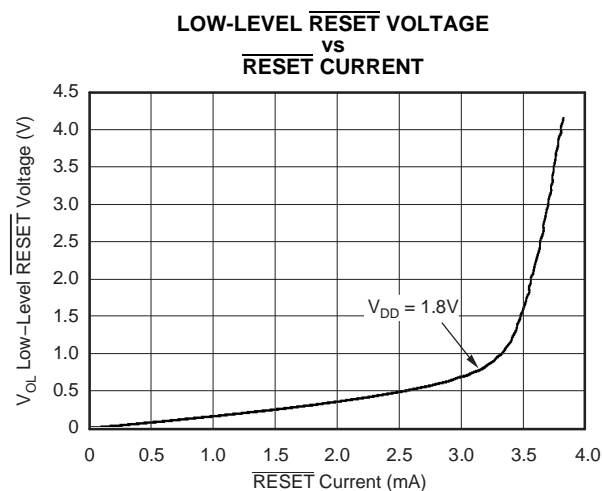


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $R_{LRESET} = 100\text{k}\Omega$, and $C_{LRESET} = 50\text{pF}$, unless otherwise noted.

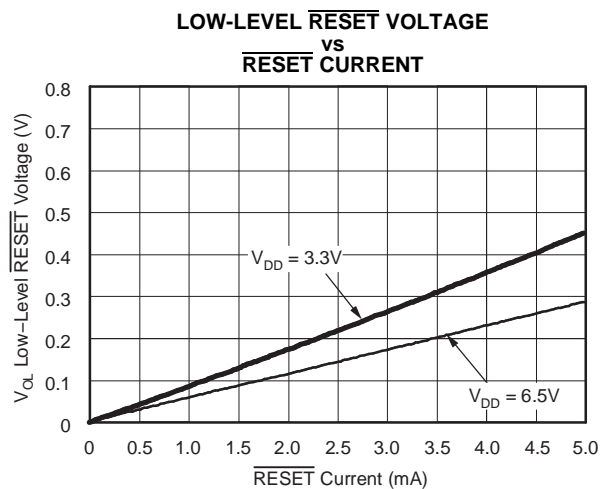


Figure 9.

DEVICE OPERATION

The TPS3818 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the TPS3818G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, while leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

RESET OUTPUT

A typical application of the TPS3818G25 used with the OMAP1510 processor is shown in Figure 10. The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pull-up resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 0.8V, but this is normally not a problem because most microprocessors do not function below this voltage. $\overline{\text{RESET}}$ remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset ($\overline{\text{MR}}$) is logic high. If either SENSE falls below V_{IT} or $\overline{\text{MR}}$ is driven low, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

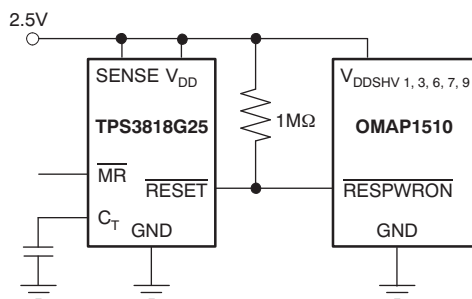


Figure 10. Typical Application of the TPS3818 with an OMAP Processor

Once $\overline{\text{MR}}$ is again logic high and SENSE is above $V_{IT} + V_{HYS}$ (the threshold hysteresis), a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state. The pull-up resistor from the open-drain $\overline{\text{RESET}}$ to the

supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the $\overline{\text{RESET}}$ line.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT} , then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3818G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 11.

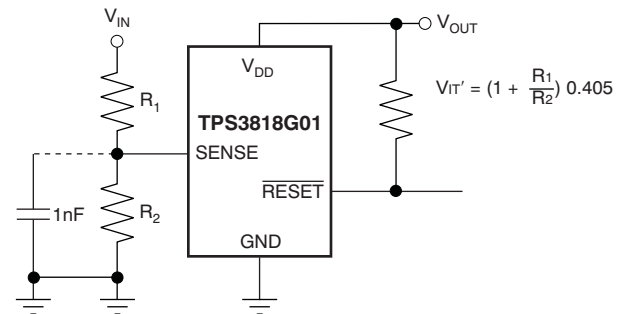


Figure 11. Using the TPS3818G01 to Monitor a User-Defined Threshold Voltage

MANUAL RESET ($\overline{\text{MR}}$) INPUT

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuit to initiate a reset. A logic low ($0.3V_{DD}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user-defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to V_{DD} using a 90kΩ resistor so this pin can be left unconnected if $\overline{\text{MR}}$ is not used.

See Figure 12 for how $\overline{\text{MR}}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to V_{DD} , there will be some additional current draw into V_{DD} as a result of the internal pull-up resistor on $\overline{\text{MR}}$. To minimize current draw, a logic-level FET can be used as illustrated in Figure 13.

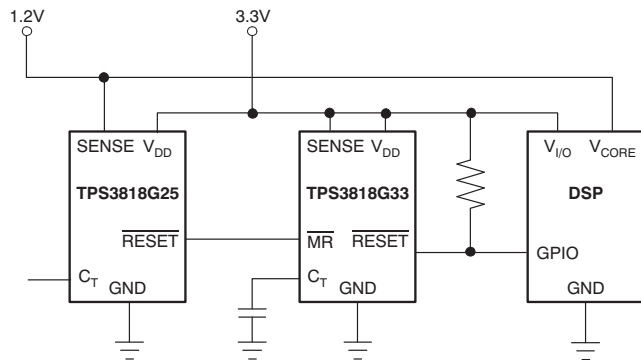


Figure 12. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages

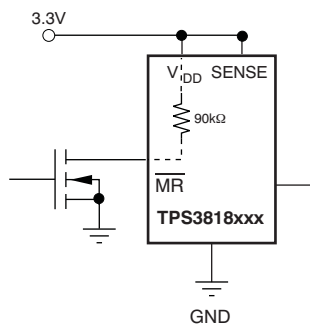


Figure 13. Using an External MOSFET to Minimize I_{DD} When $\overline{\text{MR}}$ Signal Does Not Go to V_{DD}

SELECTING THE RESET DELAY TIME

The TPS3818 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 14. Figure 14a shows the configuration for a fixed 300ms typical delay time by tying C_{T} to V_{DD} ; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected

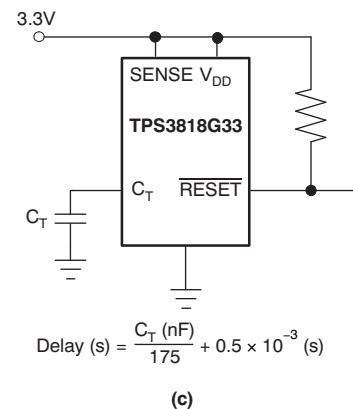
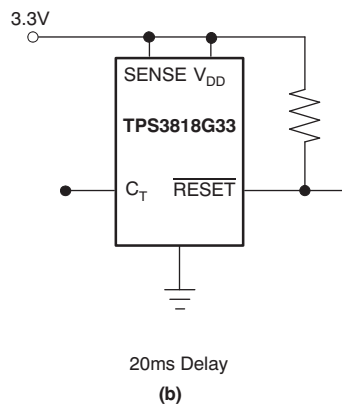
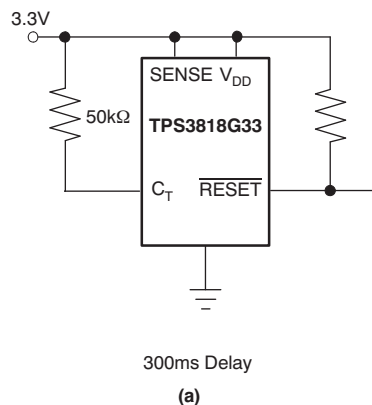


Figure 14. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

by the choice of resistor. Figure 14b shows a fixed 20ms delay time by leaving the C_{T} pin open. Figure 14c shows a ground referenced capacitor connected to C_{T} for a user-defined program time between 1.25ms and 10s.

The capacitor C_{T} should be $\geq 100\text{pF}$ nominal value in order for the TPS3818xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$\text{C}_{\text{T}} \text{ (nF)} = [\text{t}_{\text{D}} \text{ (s)} - 0.5 \times 10^{-3} \text{ (s)}] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, $\overline{\text{RESET}}$ is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS3818 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 6) in the *Typical Characteristics* section.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS3818G25DRVR | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CHJ | Samples |
| TPS3818G25DRVRG4 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CHJ | Samples |
| TPS3818G25DRVT | ACTIVE | SON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CHJ | Samples |
| TPS3818G25DRVTG4 | ACTIVE | SON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CHJ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

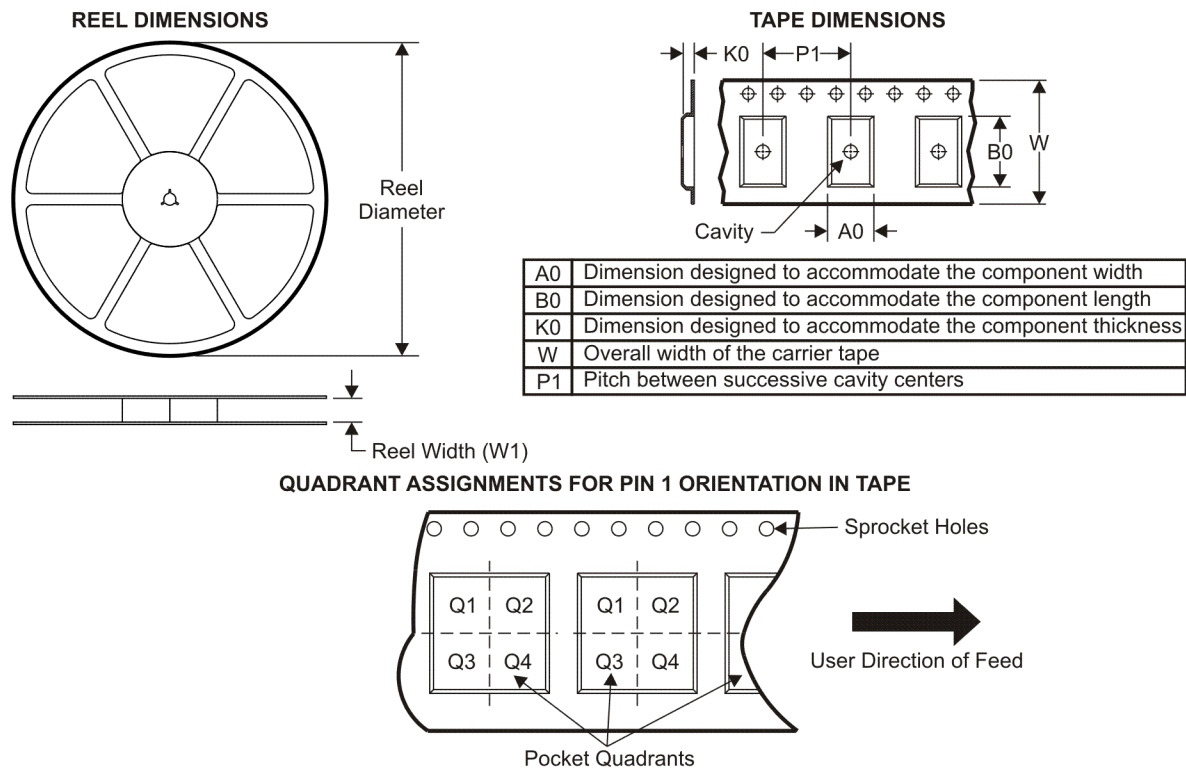
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3818G25DRVR | SON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS3818G25DRV | SON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS3818G25DRVR | SON | DRV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3818G25DRVT | SON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

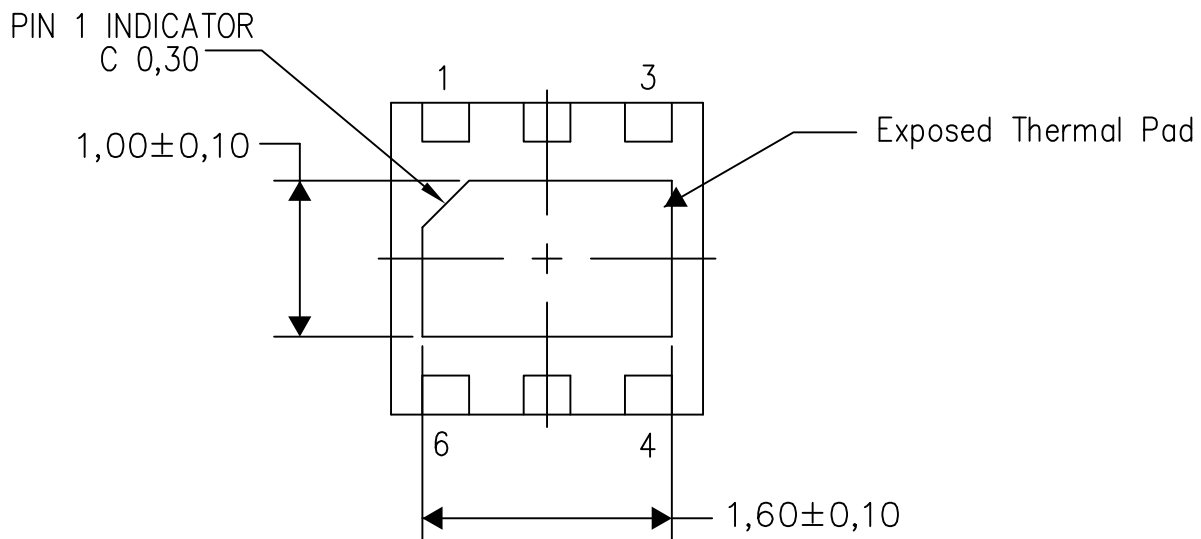
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

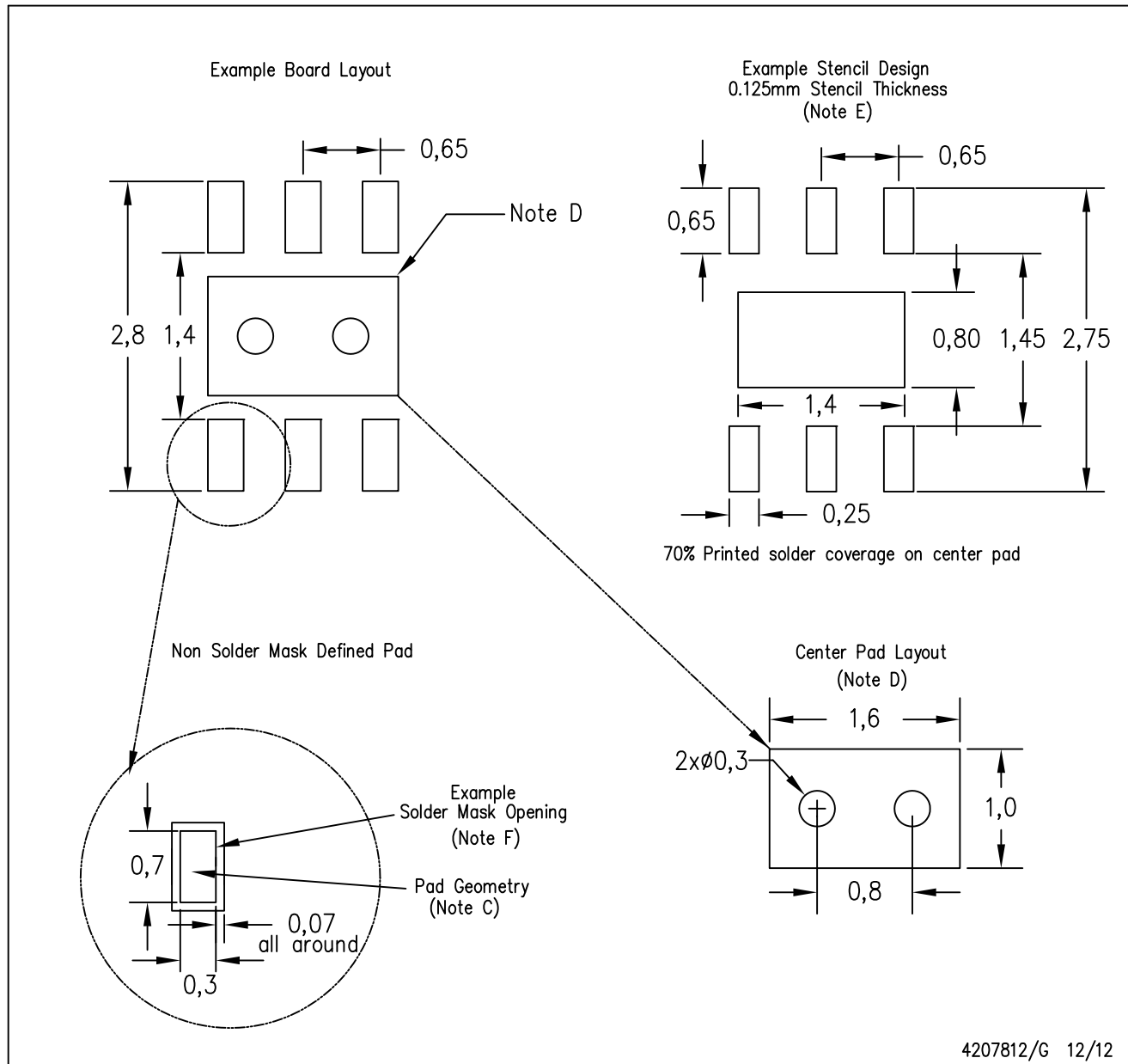
Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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