PmodCLP™
Parallel LCD Display Module
Reference Manual

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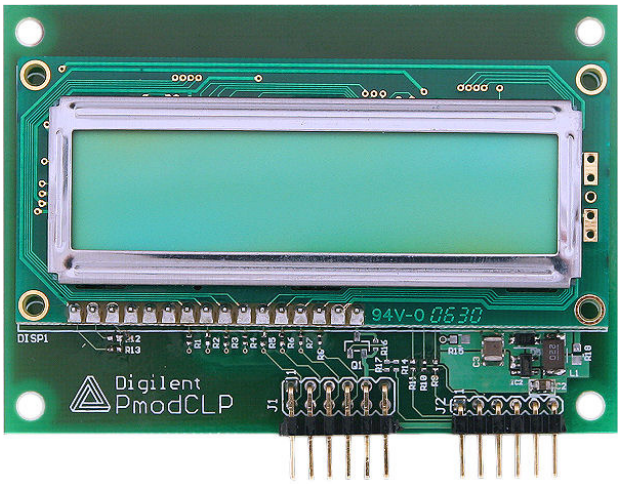
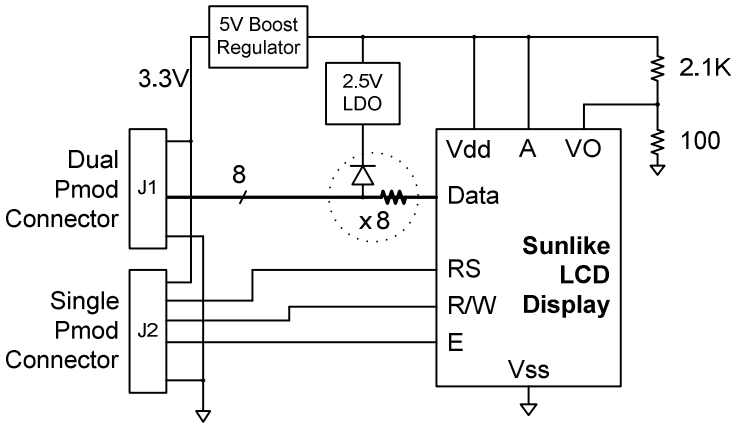
Overview

The PmodCLP is a 16x2 character LCD module that uses two Pmod connectors to present a 3.3V, 8-bit parallel data interface to system boards. It is based on a Sunlike LCD panel that uses a Samsung KS0066 (or equivalent) LCD controller. The module can be attached to any number of Digilent system boards to create a character LCD subsystem.



The PmodCLP can be supplied with 3.3V or 5V. Because the Sunlike LCD module requires a 5V supply, the PmodCLP includes a 3.3V-to-5V boost regulator and a 5V-to-3.3V voltage-translation circuit. The voltage translation circuit ensures that 3.3V data signals are returned to the system board whether 3.3V or 5V is used to supply the module (if 5V signal levels are desired, the 2.5V regulator can be removed).

A simple resistor-divider contrast-setting circuit is used to set the contrast voltage (VO) to about 200mV, ideal for temperatures around 20C. The divider circuit values can be changed to define other contrast voltage settings.



PmodCLP Block Diagram

The module is capable of displaying any one of more than 200 predefined characters in each of the 32 display locations (organized as 16 characters on two rows). Most characters use ASCII codes (see the Samsung KS0066 data sheet for a complete list of character codes). The module can also execute a variety of instructions, such as erasing specific characters, setting different display modes, scrolling, and displaying user-defined characters. These instructions are defined in table 3 below. Characters and instructions are written to the display using the 8-bit data bus as described below. Characters written to the display appear at the current location of the LCD panel's cursor.

This document contains much of the information required to drive the PmodCLP, but a good deal of the information presented in the LCD controller data sheet has not been reproduced here. Please refer to the Samsung manufacturer's data sheet for more information.

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LCD Controller

The LCD controller contains a character-generator ROM (CGROM) with 192 preset 5x8 character patterns (see table 4 below), a character-generator RAM (CGRAM) that can hold 8 user-defined 5x8 characters, and a display data RAM (DDRAM) that can hold 80 character codes. Character codes written into the DDRAM serve as indexes into the CGROM (or CGRAM). Writing a character code into a particular DDRAM location will cause the associated character to appear at the corresponding display location. Display positions can be shifted left or right by setting a bit in the instruction register (IR). The write-only IR directs display operations (such as clear display, shift left or right, set DDRAM address, etc). Available instructions (and the associated IR codes) are shown in the right-most column of table 3 below. A busy flag shows whether the display has competed the last requested operation; prior to initiating a new operation, the flag can be checked to see if the previous operation has been completed.

The display has more DDRAM locations than can be displayed at any given time. DDRAM locations 00H to 27H map to the first display row, and locations 40H to 67H map to the second row. Normally, DDRAM location 00H maps to the upper left display corner, and 40H to the lower left. Shifting the display left or right can change this mapping. The display uses a temporary data register (DR) to hold data during DDRAM /CGRAM reads or writes, and an internal address register to select the RAM location. Address register contents, set via the IR, are automatically incremented after each read or write operation. The LCD display uses ASCII character codes. Codes up through 7F are standard ASCII (which includes all “normal” alphanumeric characters). Codes above 7F produce various international characters – please see the manufacturer’s data sheet for more information on international codes.

The PmodCLP is connected to the system boards by one dual and one single Pmod connector. The interface includes eight data and three control signals that are routed from the Pmod connectors to the LCD controller IC via simple resistor-diode voltage translation circuits. Power (3.3V or 5V) and GND are routed to the LCD controller, and to a 3.3V-to-5V boost regulator that produces the 5VDC required by the LCD panel itself. The voltage translation circuit ensures the eight data signals are returned to the system board at 3.3V (as mentioned, if 5V signals are required, the regulator at IC1 can be removed). The three LCD control signals include RS (Register Strobe) that clocks data into registers, the R/W signal that determines bus direction, and the E signal that enables the bus for read or write operations. Pmod connector pin definitions are shown below, and following that is a figure showing LCD bus signals and timings.

Table 1. PmodCLP Connector Signals

Pin No.	Symbol	Signal Description
J1.5, J1.11, J2.5	Vss	Signal ground
J1.6, J1.12, J2.6	Vdd	Power supply (5V)
J2.1	RS	Register select: high for data transfer, low for instruction register
J2.2	R/W	Read/write signal: high for read mode, low for write mode
J2.3	E	Read/write strobe: high for read OE; falling edge writes data
J2.4	No Connect	Optional back-light enable (not connected on PmodCLP)
J1.1,2, 3, 4 J1.7,8,9,10	Data Bus	Bi-directional 8-bit data bus

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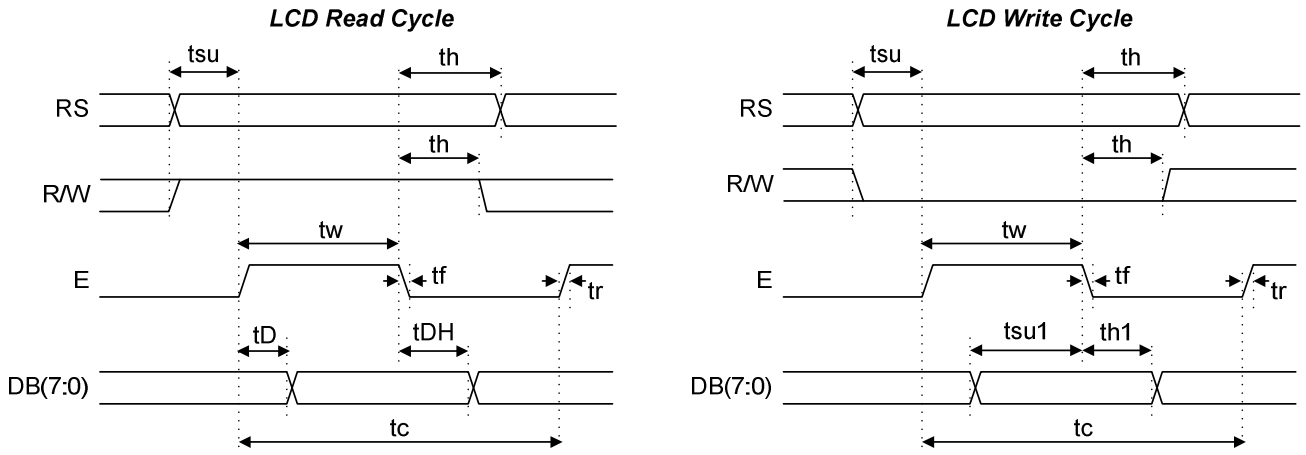
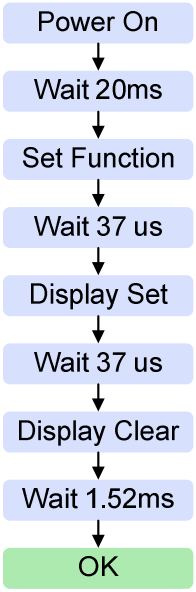


Table 2. LCD Bus Timings					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Pin**
Enable cycle time	tc	500		ns	E
Enable High pulse width	tw	220		ns	E
Enable rise/fall time	tr, tf		25	ns	E
RS, R/W setup time	tsu	40		ns	RS, R/W
RS, R/W hold time	th	10		ns	RS, R/W
Read data output delay	tD	60	120	ns	DB0-DB7
Read data hold time	tDH	20		ns	DB0-DB7
Write data setup time	tsu1	40		ns	DB0-DB7
Write data hold time	th1	10		ns	DB0-DB7

A startup sequence with specific timings is required to ensure proper LCD operation. This sequence is defined in detail in the Samsung KS0066U data sheet, and reproduced here for convenience.

After power-on, at least 20ms must elapse before the function-set instruction code can be written to set the bus width, number of lines, and character patterns (8-bit interface, 2 lines, and 5x8 dots are appropriate). After the function-set instruction, at least 37us must elapse before the display-control instruction can be written (to turn the display on, turn the cursor on or off, and set the cursor to blink or no blink). After another 37us, the display-clear instruction can be issued. After another 1.52ms, the entry-mode instruction can set address increment (or address decrement) mode, and display shift mode (on or off). After this sequence, data can be written into the DDRAM to cause information to appear on the display.

Note that other compatible LCD controllers use similar start-up sequences which may not use the same timings as the Samsung controller.



LCD startup sequence

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Table 3. LCD Instructions and Codes											
Instruction	**Instruction bit assignments**										**Description**
	RS	**R/W**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear display by writing a 20H to all DDRAM locations; set DDRAM address register to 00H; and return cursor to home.
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home (upper left corner), and set DDRAM address to 0H. DDRAM contents not changed.
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	I/D = '1' for right-moving cursor and address increment; SH = '1' for display shift (direction set by I/D bit).
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking cursor (B) on or off.
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C = '0' to shift cursor right or left, '1' to shift entire display right or left (R/L = '1' for right).
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL = '1' for 8 bit), number of display lines (N = '1' for 2 lines), display font (F = '0' for 5x 8 dots)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address counter AC5 – AC0
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address counter AC6 – AC0
Read busy flag/address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) and address counter AC6 – AC0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM or CGRAM, depending on which address was last set
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM or CGRAM, depending on which address was last set

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Table 4. LCD Character codes

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

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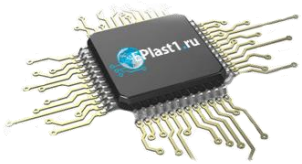

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