# PMN50XP

## P-channel TrenchMOS extremely low level FET

Rev. 02 — 2 October 2007 Product data sheet

## 1. Product profile

### 1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features

- Low on-state losses
- Low threshold voltage

### 1.3 Applications

- Battery management
- Load Switching
- Battery powered portable equipment
- Low power DC to DC converters

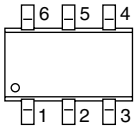
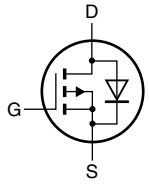
### 1.4 Quick reference data

**Table 1. Quick reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | - | -20 | V |
| $I_D$ | drain current | $V_{GS}$ = -4.5 V; $T_{sp}$ = 25 °C; see Figure 1 and 3 | - | - | -4.8 | A |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = -4.5 V; $I_D$ = -4.7 A; $V_{DS}$ = -10 V; $T_j$ = 25 °C; see Figure 9 and 10 | - | 1.3 | - | nC |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = -4.5 V; $I_D$ = -2.8 A; $T_j$ = 25 °C; see Figure 7 and 8 | - | 48 | 60 | mΩ |

## 2. Pinning information

**Table 2. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic Symbol |
|---|---|---|---|---|
| 1 | D | drain |  |  |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | source | | |
| 5 | D | drain | | |
| 6 | D | drain | | |



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## 3. Ordering information

**Table 3. Ordering information**

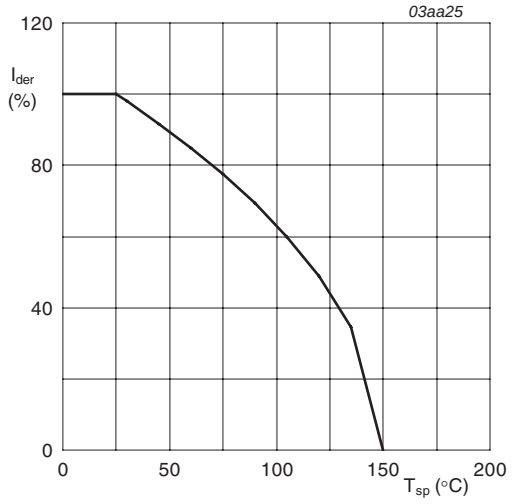
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PMN50XP | TSOP6 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

## 4. Limiting values

**Table 4. Limiting values**

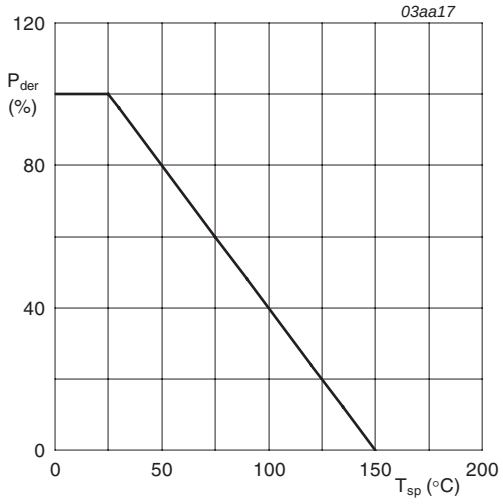
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | -20 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS}$ = 20 kΩ | - | -20 | V |
| $V_{GS}$ | gate-source voltage | | -12 | 12 | V |
| $I_D$ | drain current | $T_{sp}$ = 25 °C; $V_{GS}$ = -4.5 V; see Figure 1 and 3 | - | -4.8 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = -4.5 V | - | -3 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; $t_p$ < 10 μs; pulsed; see Figure 3 | - | -19.4 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; see Figure 2 | - | 2.2 | W |
| $T_{stg}$ | storage temperature | | -55 | 150 | °C |
| $T_j$ | junction temperature | | -55 | 150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source current | $T_{sp}$ = 25 °C | - | -1.9 | A |
| $I_{SM}$ | peak source current | $T_{sp}$ = 25 °C; $t_p \leq 10$ μs; pulsed | - | -7.5 | A |



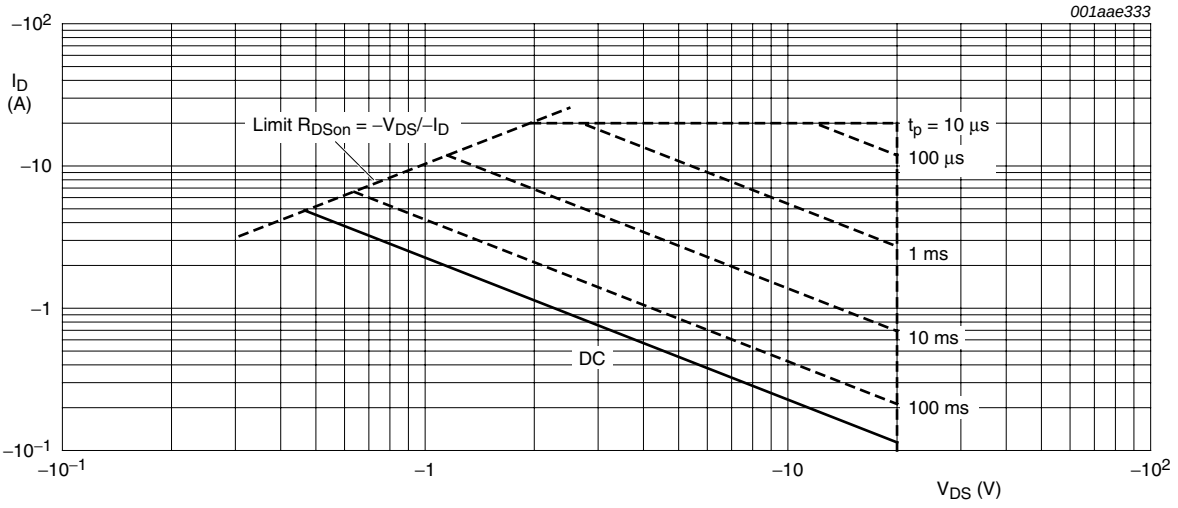

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**




$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see Figure 4 | - | - | 55 | K/W |

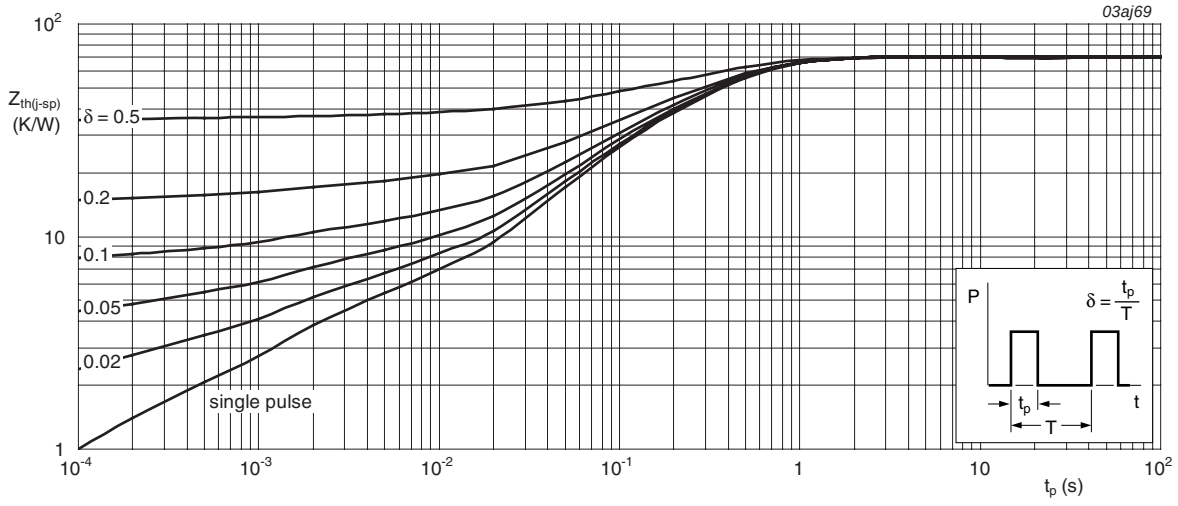



**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration**

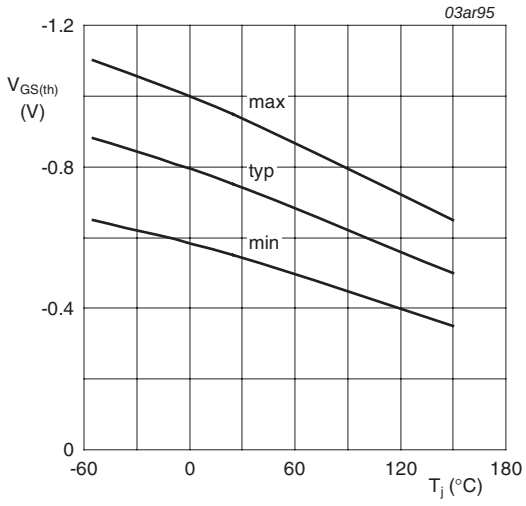
## 6. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = -250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | -20 | - | - | V |
| | | $I_D$ = -250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | -18 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = -0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 5 and 6 | -0.55 | -0.75 | -0.95 | V |
| | | $I_D$ = -0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C; see Figure 5 and 6 | -0.35 | - | - | V |
| | | $I_D$ = -0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 5 and 6 | - | - | -1.1 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = -20 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | - | -1 | µA |
| | | $V_{DS}$ = -20 V; $V_{GS}$ = 0 V; $T_j$ = 70 °C | - | - | -5 | µA |

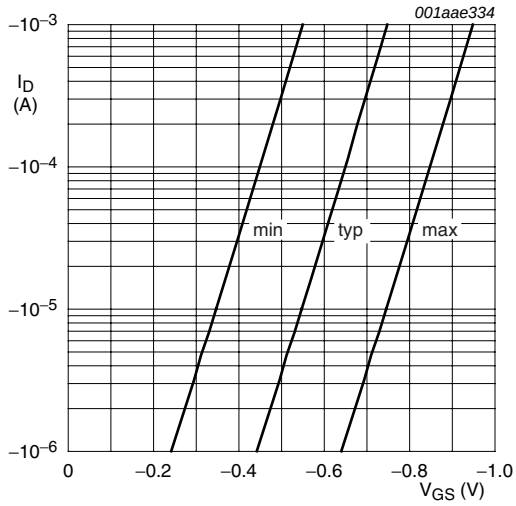
**Table 6. Characteristics** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{GSS}$ | gate leakage current | $V_{GS} \leq 12$ V; $V_{DS} = 0$ V; $T_j = 25$ °C | - | -10 | -100 | nA |
| | | $V_{GS} \geq 12$ V; $V_{DS} = 0$ V; $T_j = 25$ °C | - | -10 | -100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = -4.5$ V; $I_D = -2.8$ A; $T_j = 25$ °C; see Figure 7 and 8 | - | 48 | 60 | mΩ |
| | | $V_{GS} = -4.5$ V; $I_D = -2.8$ A; $T_j = 150$ °C; see Figure 7 and 8 | - | 77 | 96 | mΩ |
| | | $V_{GS} = -2.5$ V; $I_D = -2.3$ A; $T_j = 25$ °C; see Figure 7 and 8 | - | 65 | 80 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10 | - | 10 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10 | - | 2.2 | - | nC |
| $Q_{GD}$ | gate-drain charge | $I_D = -4.7$ A; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C; see Figure 9 and 10 | - | 1.3 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS} = -20$ V; $V_{GS} = 0$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11 | - | 1020 | - | pF |
| $C_{oss}$ | output capacitance | $V_{GS} = 0$ V; $V_{DS} = -20$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11 | - | 140 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | $V_{DS} = -20$ V; $V_{GS} = 0$ V; f = 1 MHz; $T_j = 25$ °C; see Figure 11 | - | 100 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $R_{G(ext)} = 6\ \Omega$; $R_L = 10\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C | - | 8.5 | - | ns |
| $t_r$ | rise time | $R_{G(ext)} = 6\ \Omega$; $R_L = 10\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C | - | 7.5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | $V_{DS} = -10$ V; $R_L = 10\ \Omega$; $V_{GS} = -4.5$ V; $R_{G(ext)} = 6\ \Omega$; $T_j = 25$ °C | - | 82 | - | ns |
| $t_f$ | fall time | $R_{G(ext)} = 6\ \Omega$; $R_L = 6\ \Omega$; $V_{DS} = -10$ V; $V_{GS} = -4.5$ V; $T_j = 25$ °C | - | 35 | - | ns |
| $V_{GS(pl)}$ | gate-source plateau voltage | $V_{DS} = -10$ V; $I_D = -4.7$ A; $T_j = 25$ °C; see Figure 9 and 10 | - | -1.6 | - | V |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S = -1.7$ A; $V_{GS} = 0$ V; $T_j = 25$ °C | - | -0.77 | -1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S = 3.5$ A; $dI_S/dt = -100$ A/µs; $V_{GS} = 0$ V; $V_{DS} = 20$ V; $T_j = 25$ °C | - | - | - | ns |



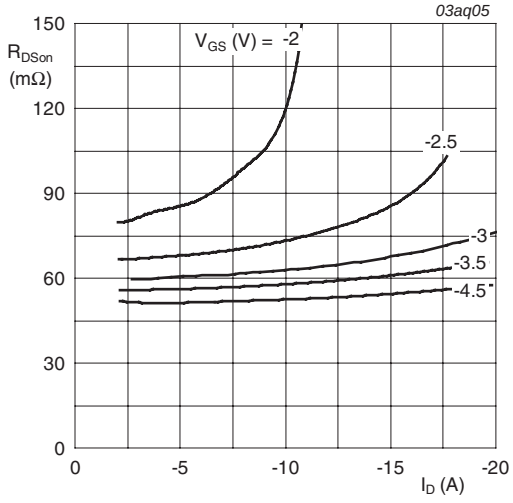

$I_D = -0.25\ mA; V_{DS} = V_{GS}$

**Fig 5. Gate-source threshold voltage as a function of junction temperature**



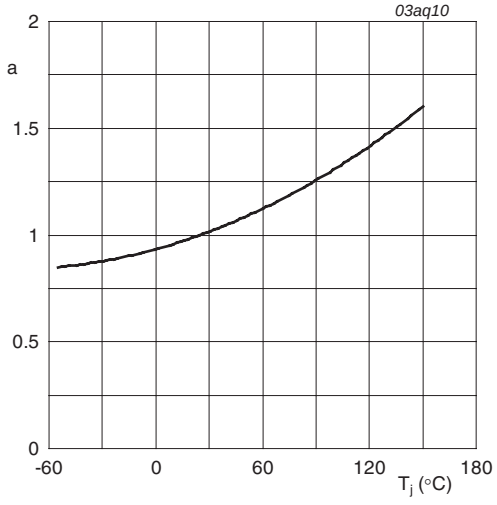

$T_j = 25\ °C; V_{DS} = -5\ V$

**Fig 6. Sub-threshold drain current as a function of gate-source voltage**



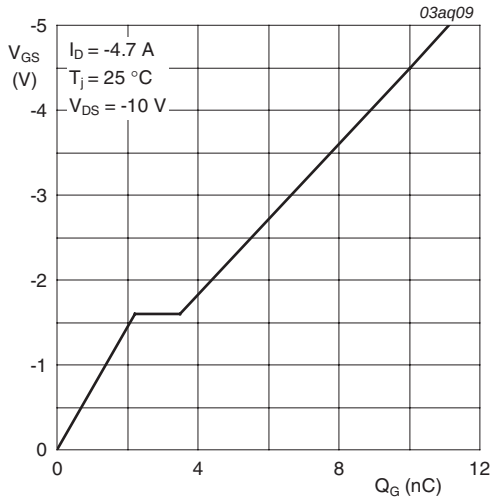

$T_j = 25\ °C$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**




$I_D = -4.7\ A; T_j = 25\ °C; V_{DS} = -10\ V$

**Fig 9. Gate-source voltage as a function of gate charge; typical values**

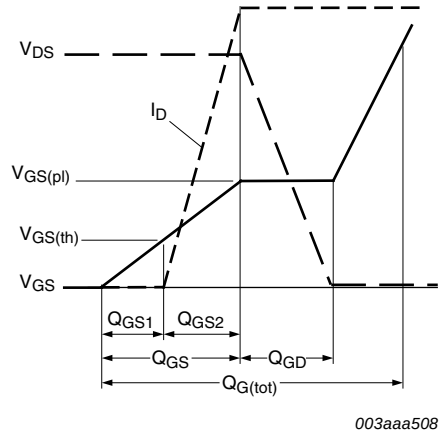
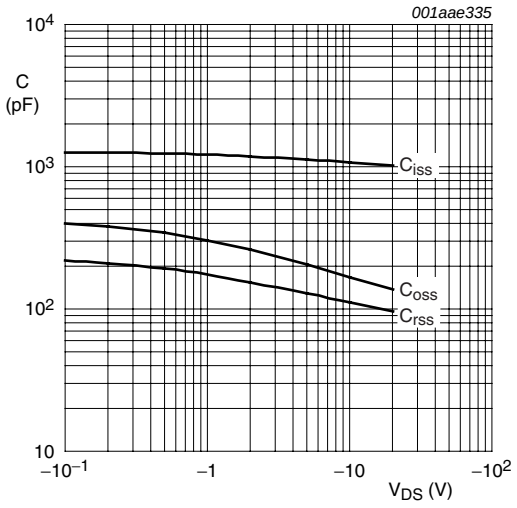



**Fig 10. Gate charge waveform definitions**

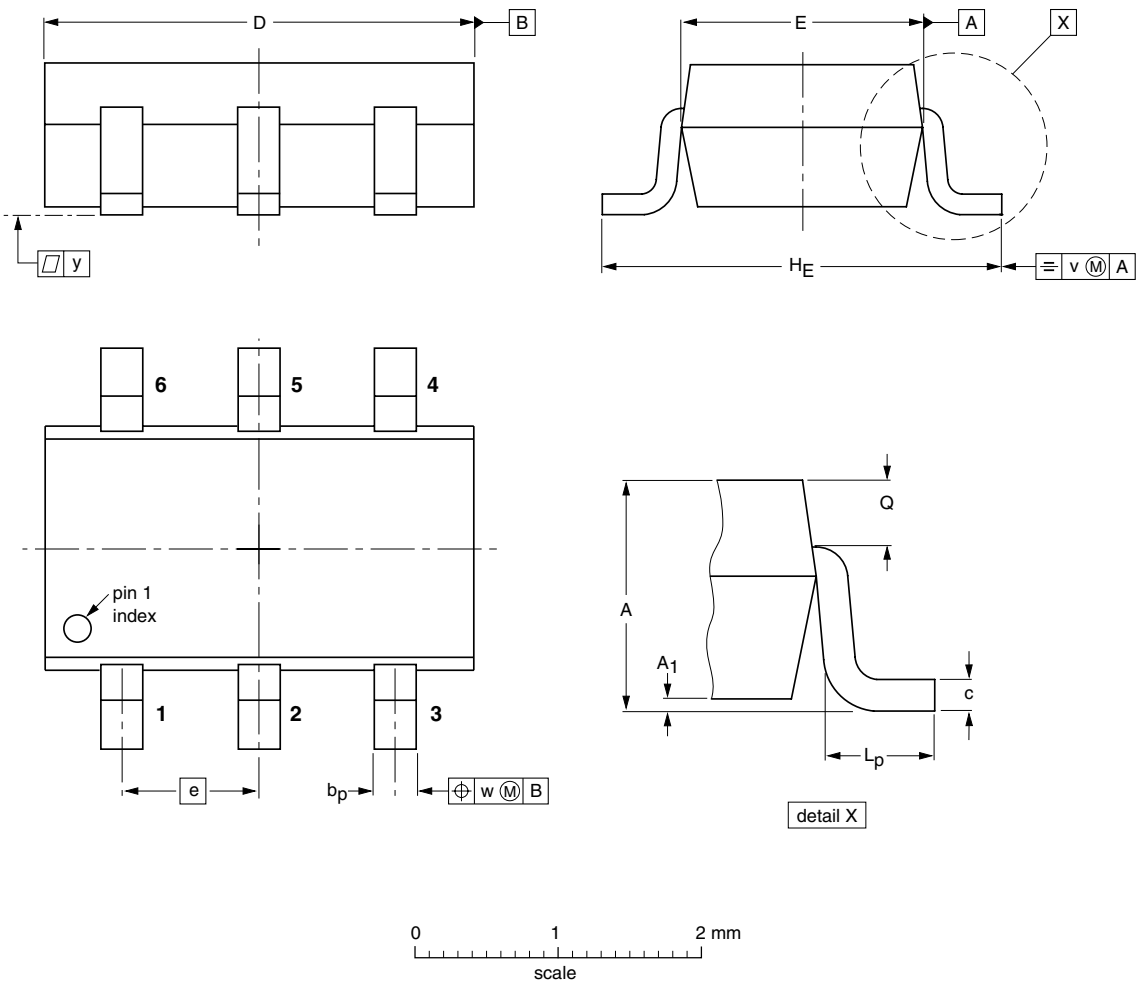



$V_{GS} = 0\ V;\ f = 1\ MHz$

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

## 7. Package outline

**Plastic surface-mounted package (TSOP6); 6 leads** **SOT457**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT457 | | | SC-74 | | | ~~05-11-07~~<br>06-03-16 |

**Fig 12. Package outline SOT457 (TSOP6)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PMN50XP_2 | 20071002 | Product data sheet | - | PMN50XP_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the company name where appropriate. | | | |
| PMN50XP_1 | 20060123 | Product data sheet | - | - |

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## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 11. Contents





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**Date of release: 2 October 2007**
**Document identifier: PMN50XP_2**

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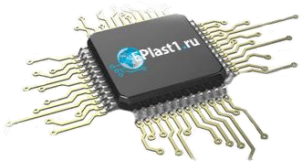
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

**Телефон:** 8 (812) 309 58 32 (многоканальный)
**Факс:** 8 (812) 320-02-42
**Электронная почта:** org@eplast1.ru
**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.