

N-channel 800 V, 0.37 Ω typ., 12 A MDmesh™ K5
Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

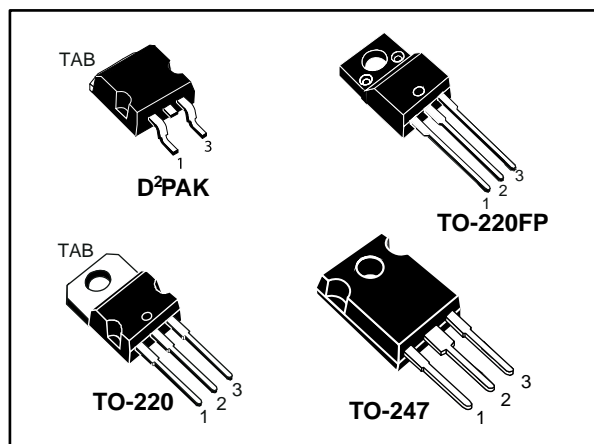
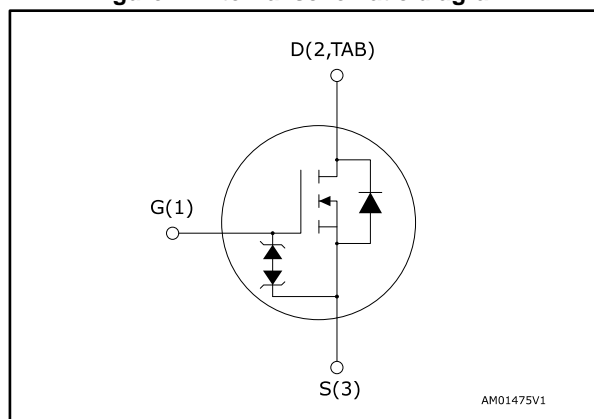


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB13N80K5	800 V	0.45 Ω	12 A	190 W
STF13N80K5				35 W
STP13N80K5				190 W
STW13N80K5				

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB13N80K5	13N80K5	D ² PAK	Tape and reel
STF13N80K5		TO-220FP	
STP13N80K5		TO-220	Tube
STW13N80K5		TO-247	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	10
4	Package information	11
	4.1 D ² PAK (TO-263) type A package information	11
	4.2 TO-220FP package information	14
	4.3 TO-220 type A packing information	16
	4.4 TO-247 package information	18
	4.5 D ² PAK type A packing information	20
5	Revision history	22

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	12	12 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	7.6	7.6 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	48	48 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	190	35	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T _C = 25 °C)		2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50		
T _j	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

Notes:

- ⁽¹⁾Limited by package.
- ⁽²⁾Pulse width limited by safe operating area.
- ⁽³⁾I_{SD} ≤ 12 A, di/dt = 100 A/μs; V_{DS} peak < V_{(BR)DSS}.
- ⁽⁴⁾V_{DS} ≤ 640 V.

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220	TO-220FP	TO-247	
R _{thj-case}	Thermal resistance junction-case	0.66		3.57	0.66	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5		50	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30				°C/W

Notes:

- ⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	4	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	148	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 800 V			1	µA
		V _{GS} = 0 V, V _{DS} = 800 V, T _C = 125 °C ⁽¹⁾			50	µA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	µA
V _{GS(th)}	Gate threshold voltage	V _{DD} = V _{GS} , I _D = 100 µA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 6 A		0.37	0.45	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	870	-	pF
C _{OSS}	Output capacitance		-	50	-	pF
C _{rss}	Reverse transfer capacitance		-	2	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0 V, V _{DS} = 0 to 640 V	-	110	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	43	-	pF
R _g	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	5	-	Ω
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 2.5 A V _{GS} = 0 to 10 V (see Figure 22: "Test circuit for gate charge behavior")	-	29	-	nC
Q _{gs}	Gate-source charge		-	7	-	nC
Q _{gd}	Gate-drain charge		-	18	-	nC

Notes:

⁽¹⁾C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}.

⁽²⁾C_{o(er)} is a constant capacitance value that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 21: "Test circuit for resistive load switching times" and Figure 26: "Switching time waveform")	-	16	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	16	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 23: "Test circuit for inductive load switching and diode recovery times")	-	406		ns
Q_{rr}	Reverse recovery charge		-	5.7		μC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 23: "Test circuit for inductive load switching and diode recovery times")	-	600		ns
Q_{rr}	Reverse recovery charge		-	7.9		μC
I_{RRM}	Reverse recovery current		-	26		A

Notes:

(1)Pulse width limited by safe operating area

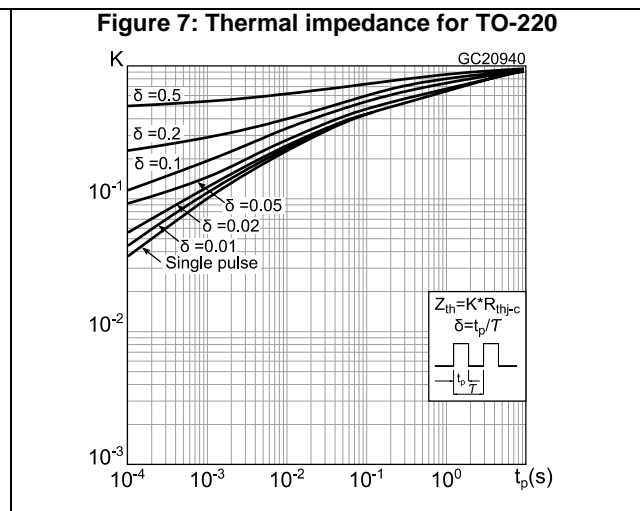
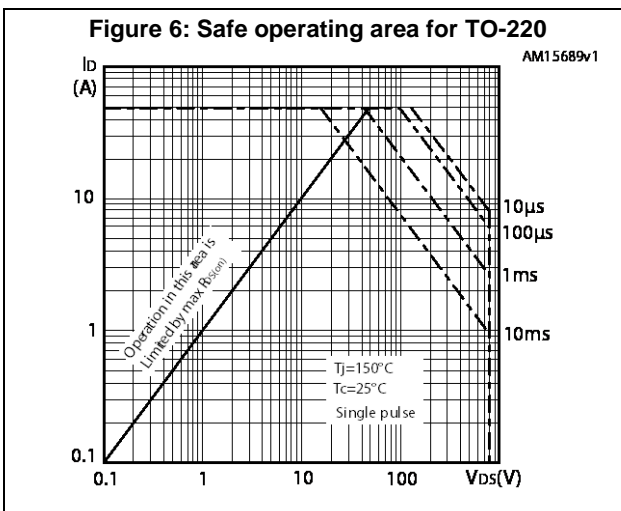
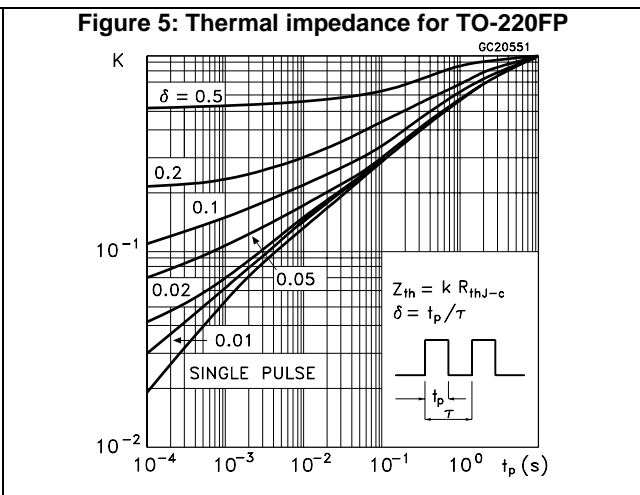
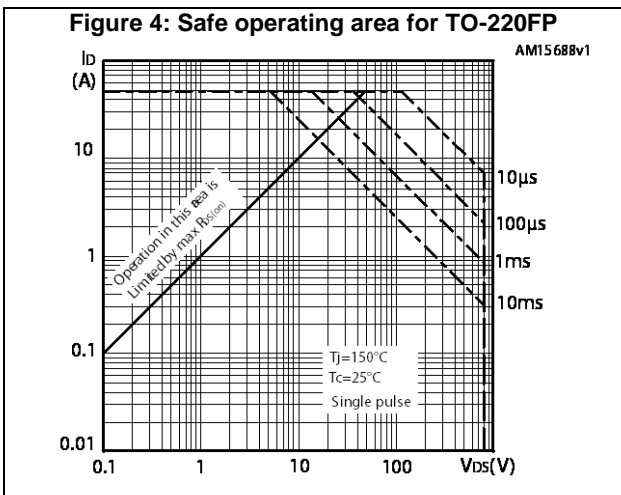
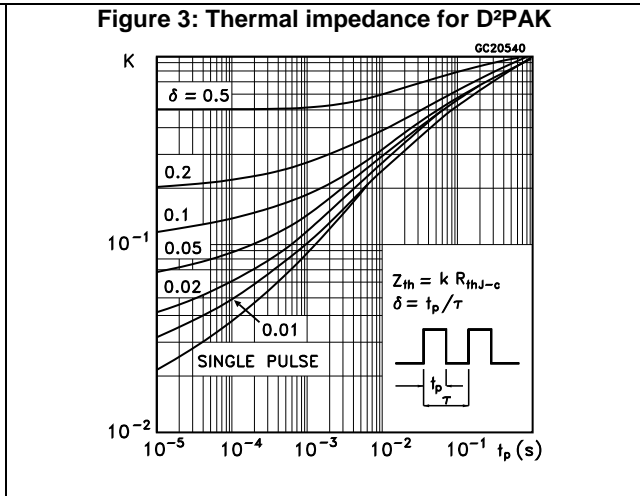
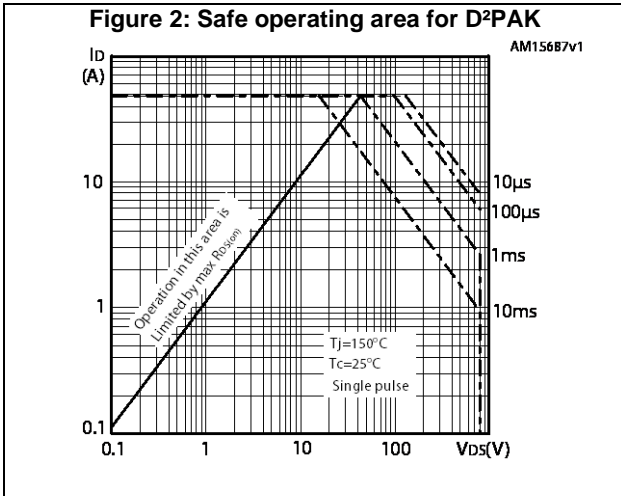
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

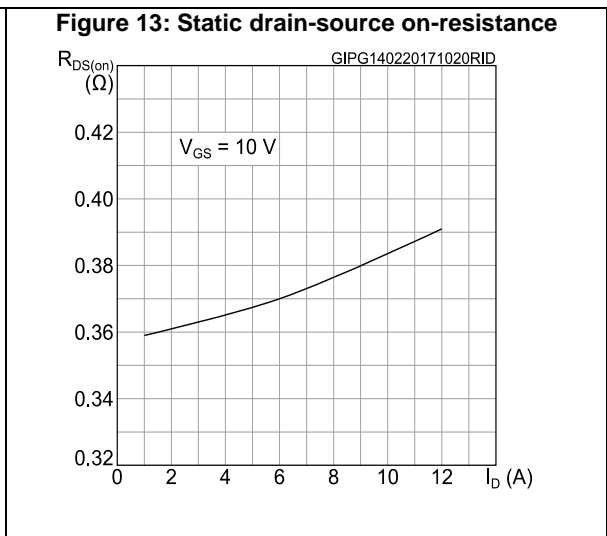
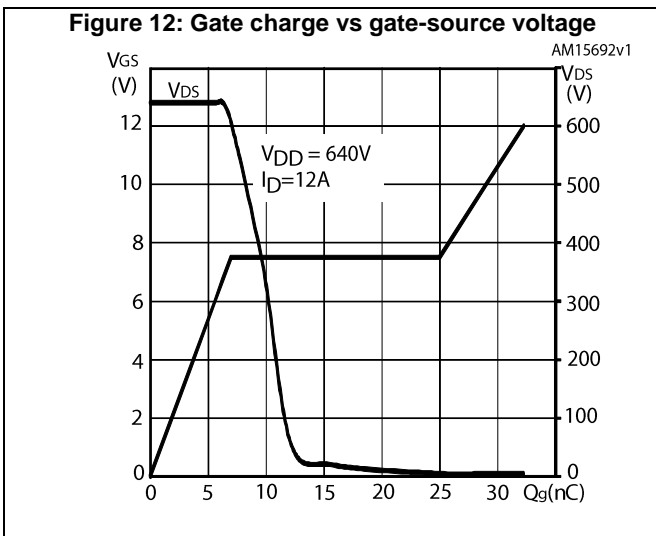
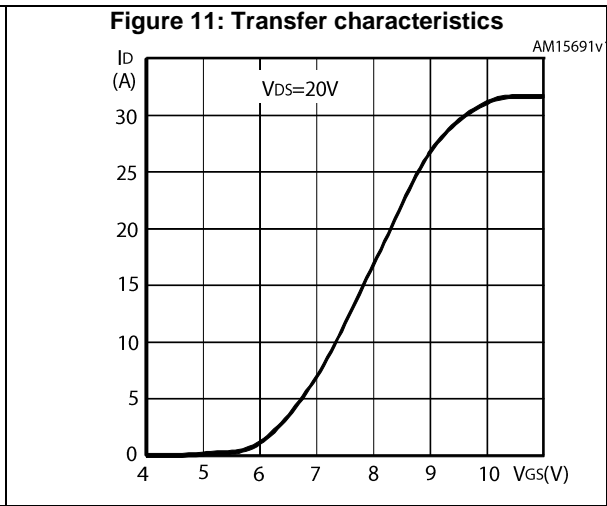
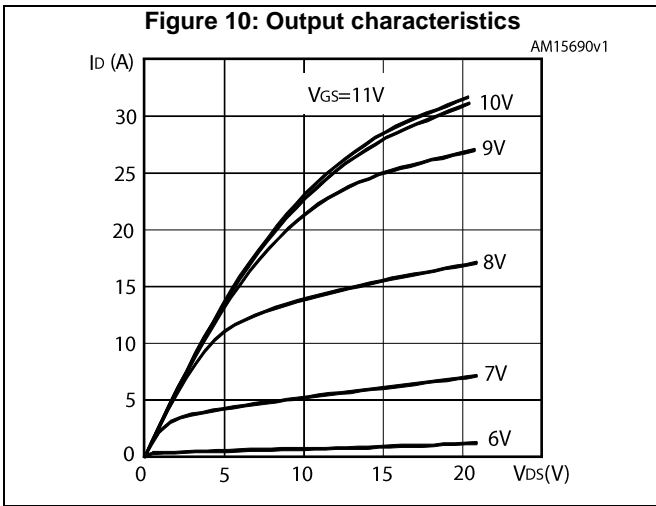
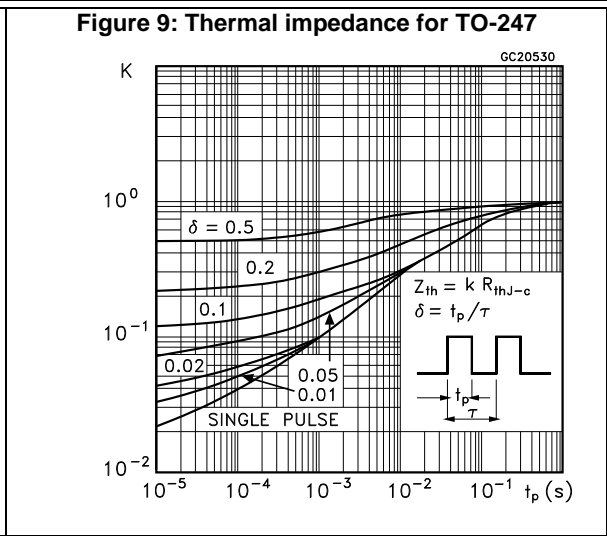
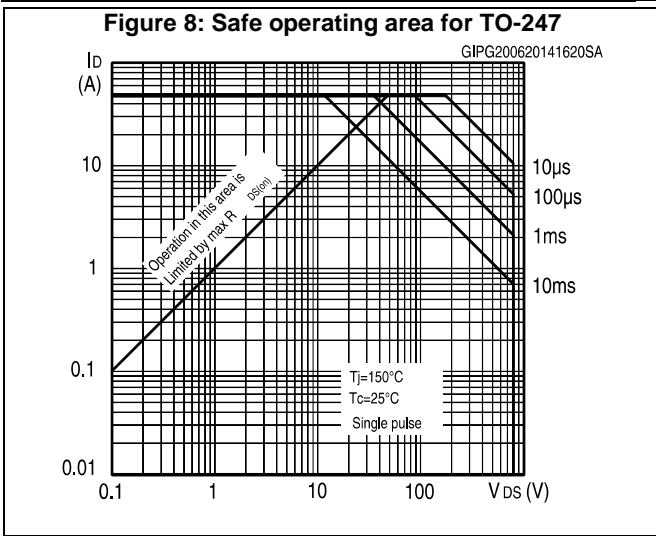
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)





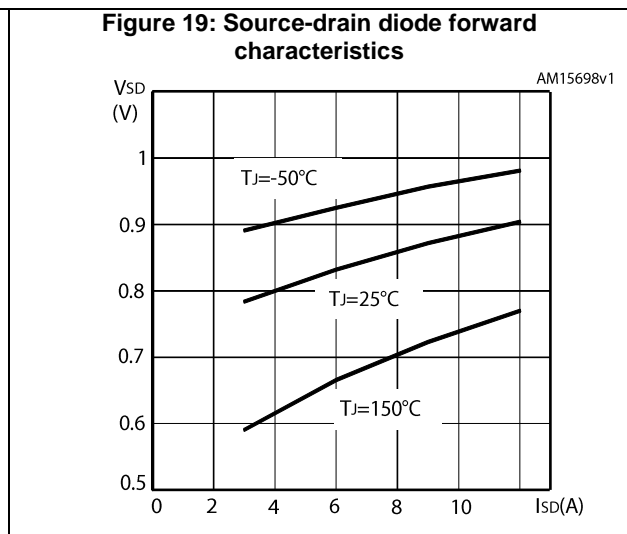
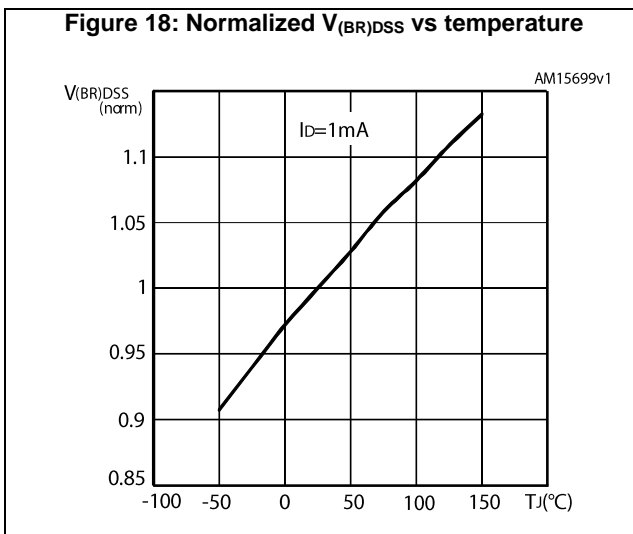
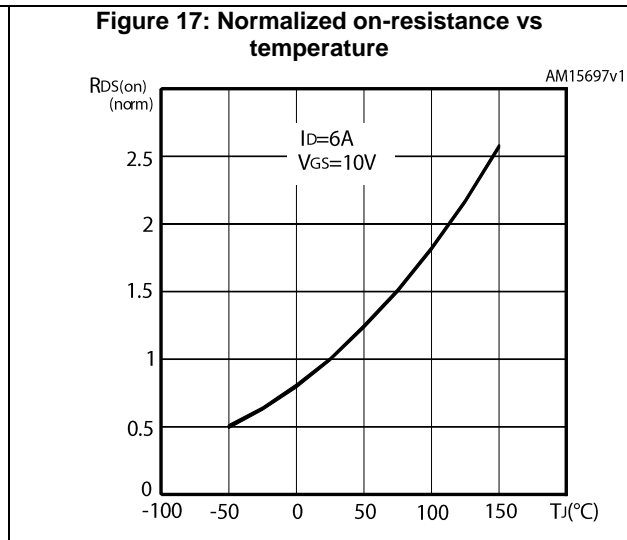
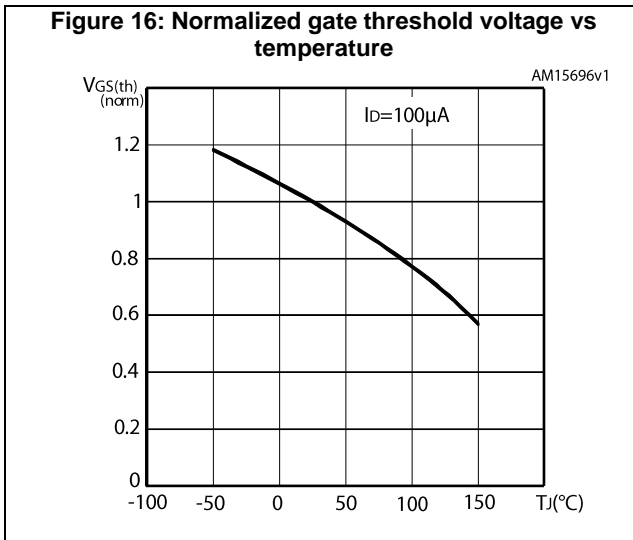
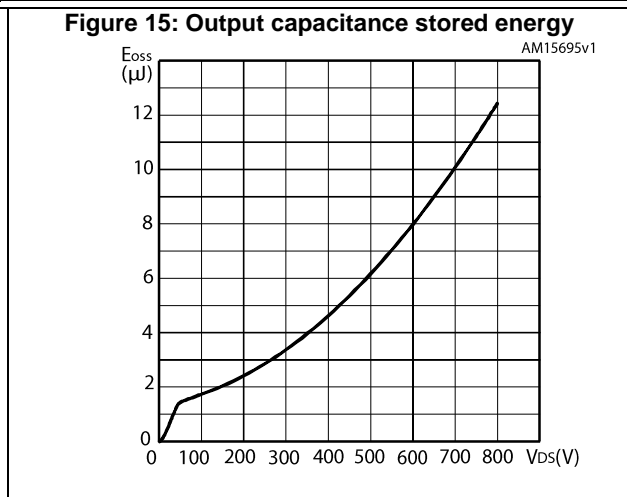
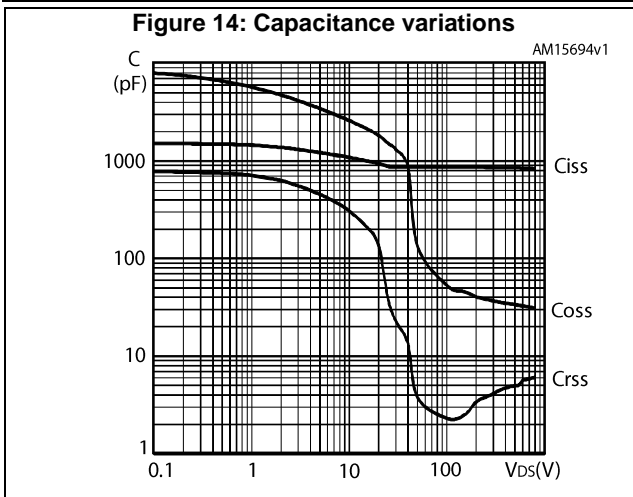
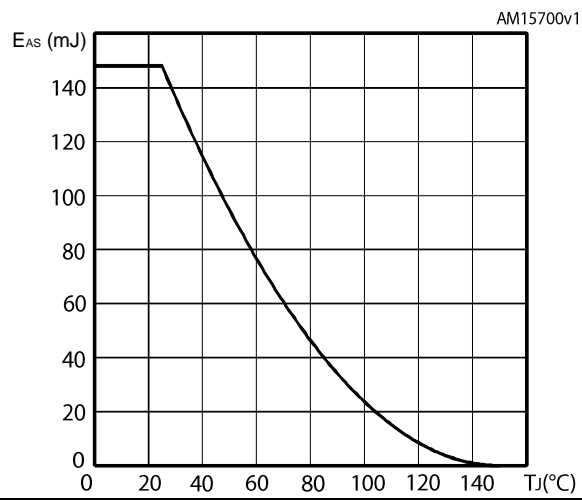
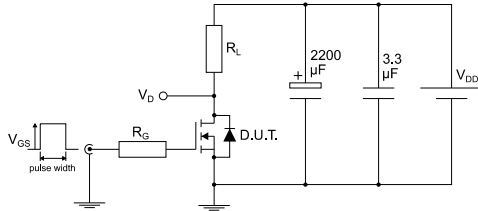


Figure 20: Maximum avalanche energy vs. starting T_j



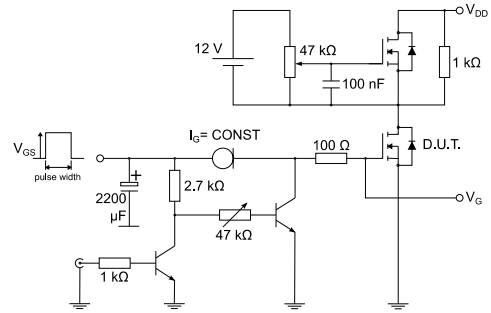
3 Test circuits

Figure 21: Test circuit for resistive load switching times



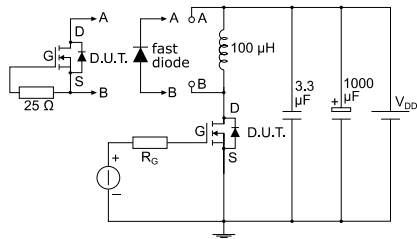
AM01468v1

Figure 22: Test circuit for gate charge behavior



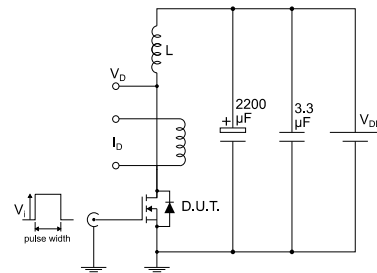
AM01469v1

Figure 23: Test circuit for inductive load switching and diode recovery times



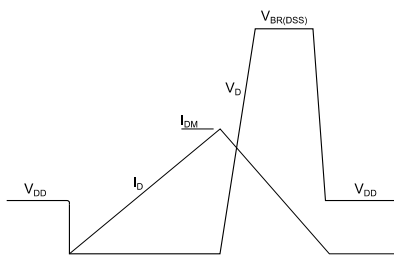
AM01470v1

Figure 24: Unclamped inductive load test circuit



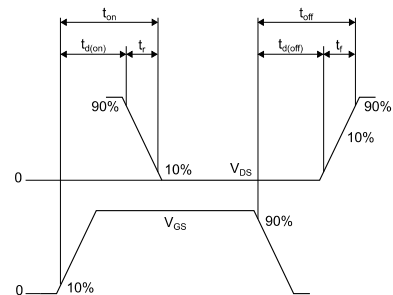
AM01471v1

Figure 25: Unclamped inductive waveform



AM01472v1

Figure 26: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 27: D²PAK (TO-263) type A package outline

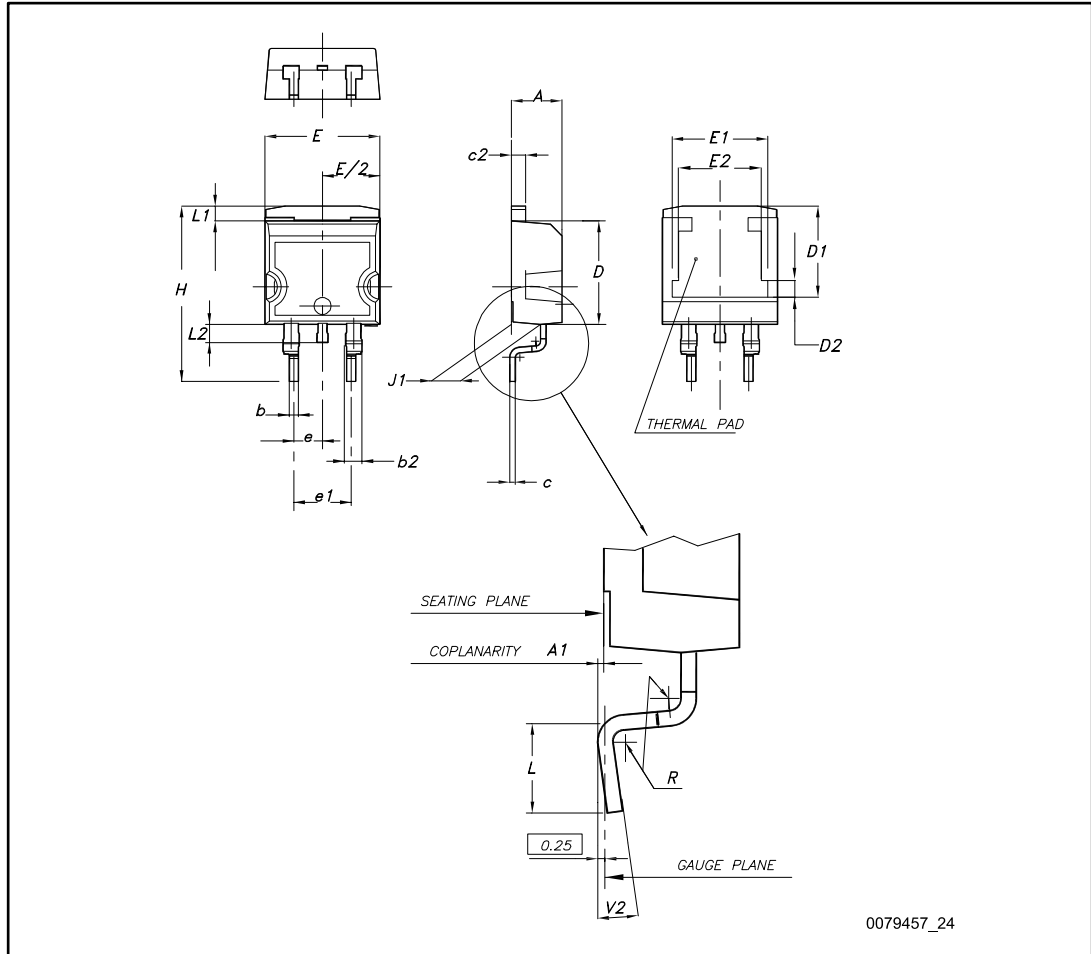
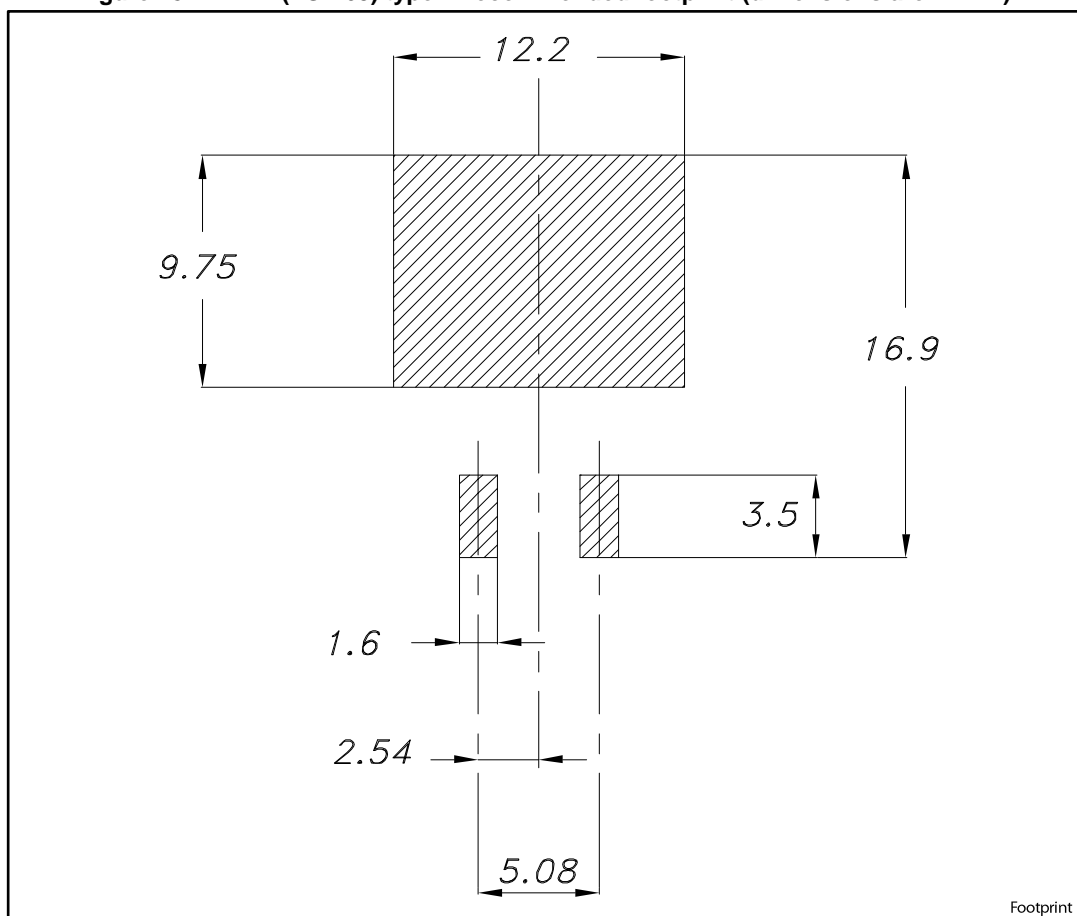


Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 28: D²PAK (TO-263) type A recommended footprint (dimensions are in mm)



4.2 TO-220FP package information

Figure 29: TO-220FP package outline



7012510_Rev_12_B

Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 TO-220 type A packing information

Figure 30: TO-220 type A package outline

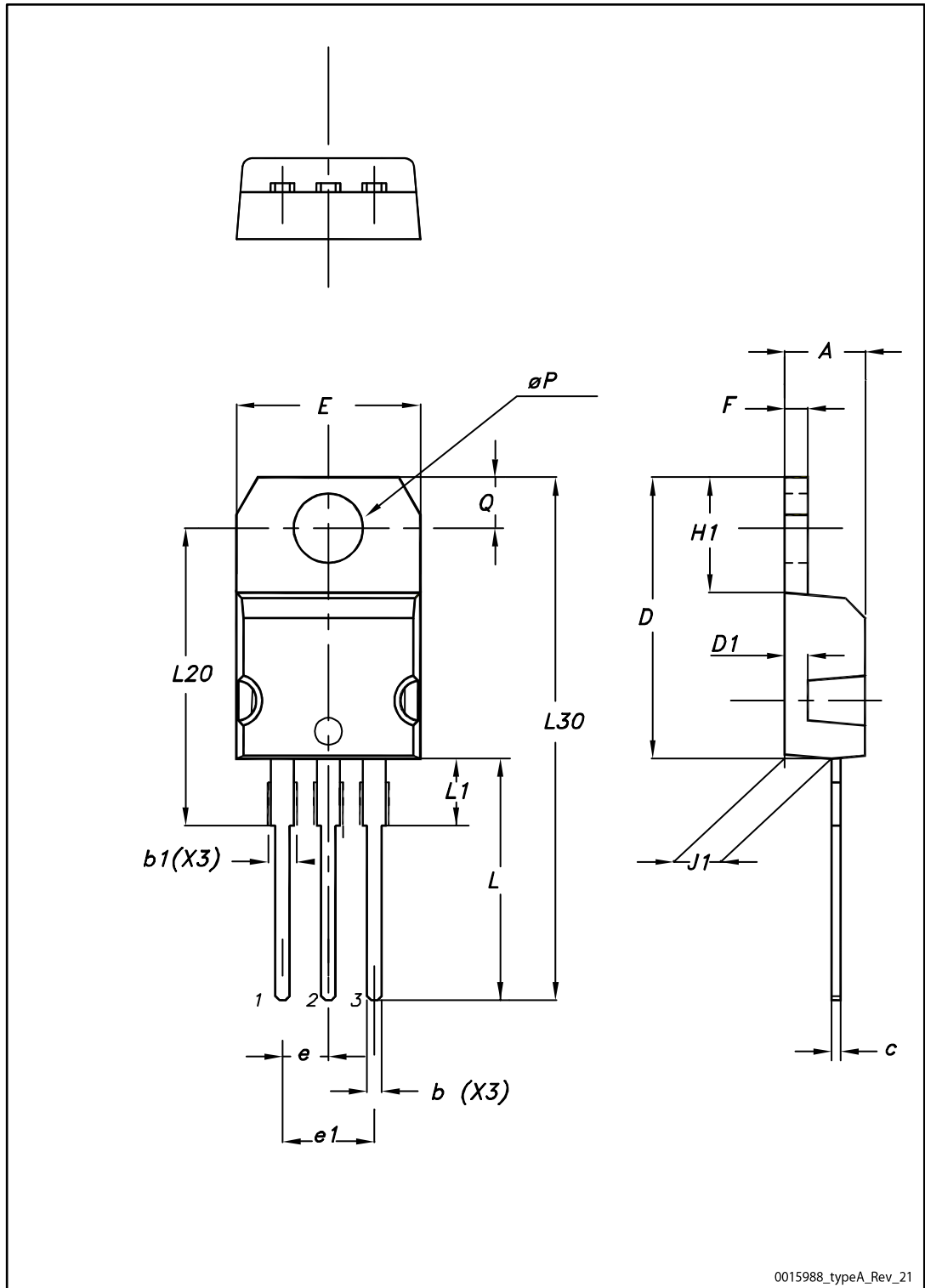


Table 12: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 31: TO-247 package outline

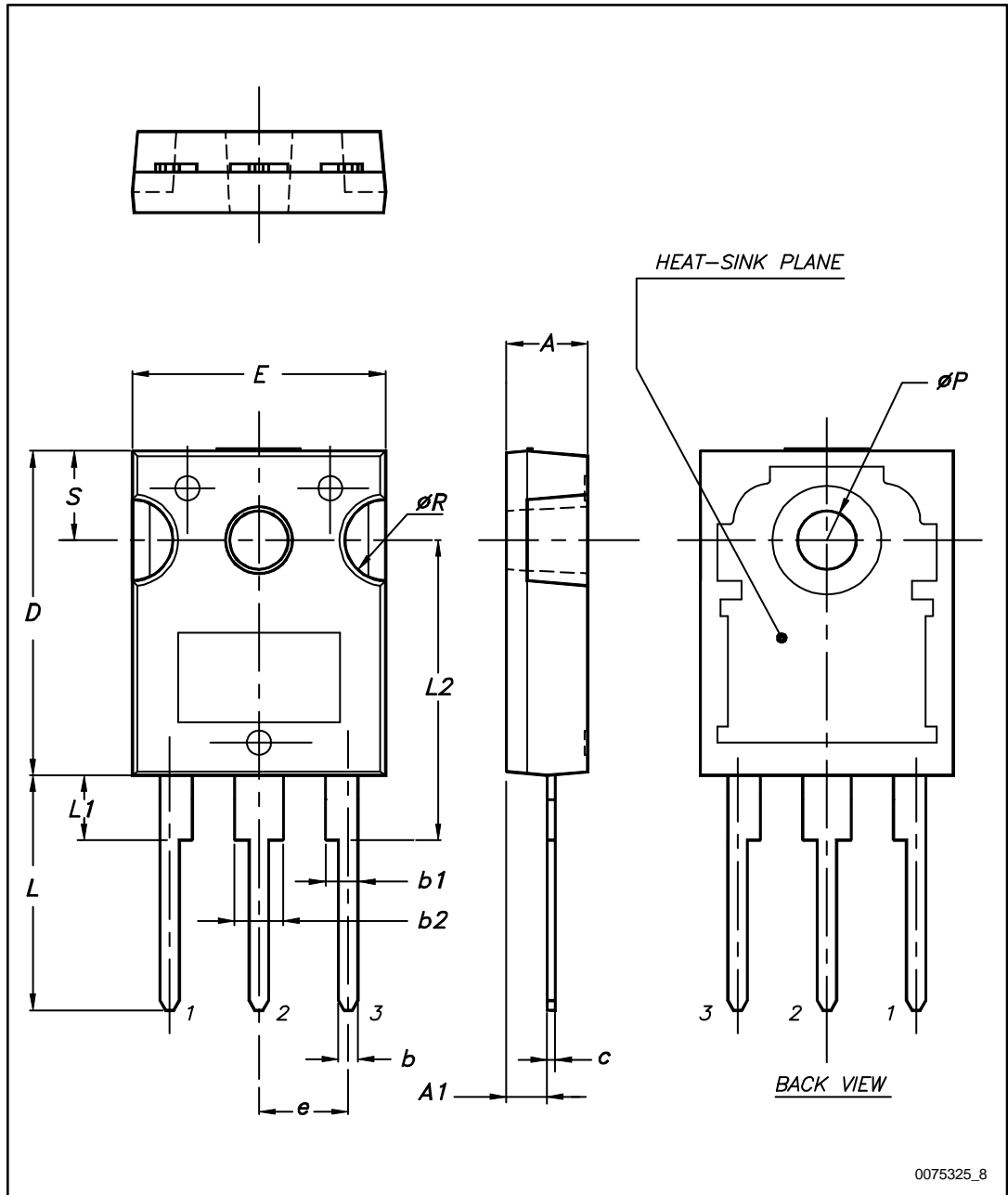


Table 13: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.5 D²PAK type A packing information

Figure 32: D²PAK type A tape outline

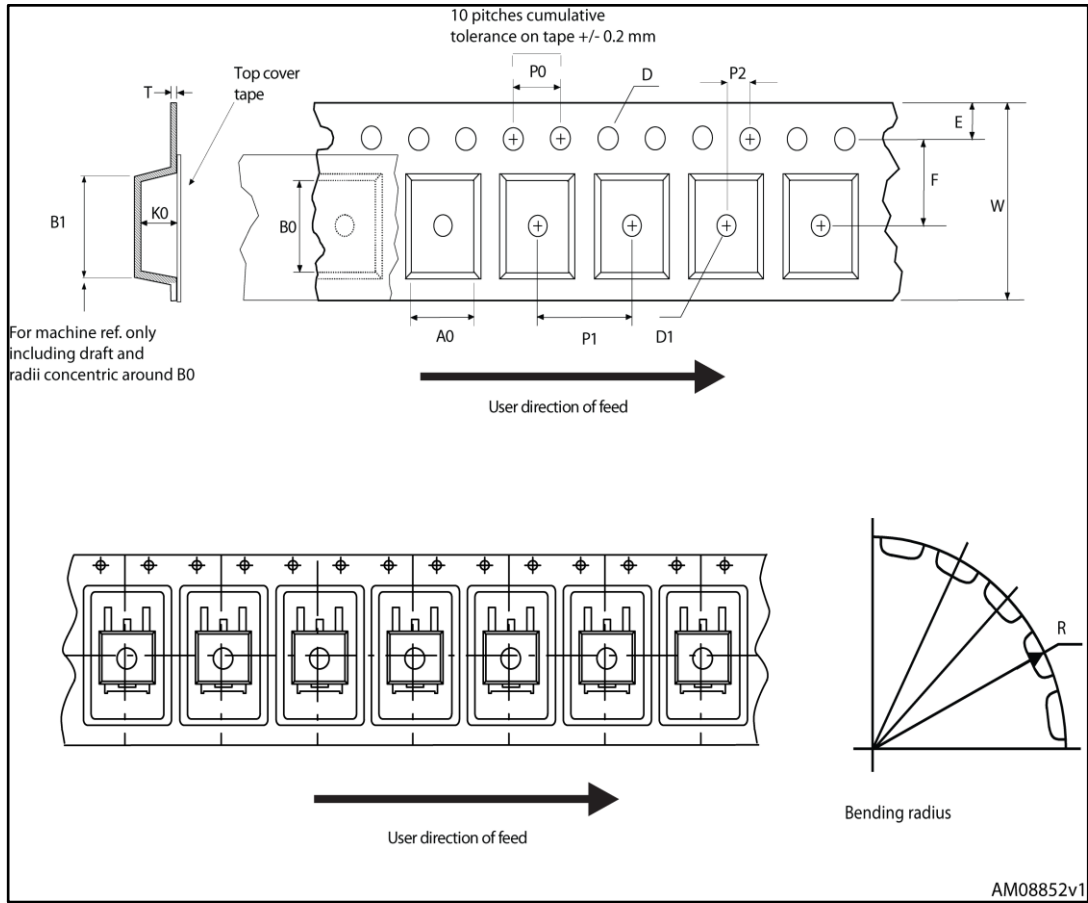


Figure 33: D²PAK type A reel outline

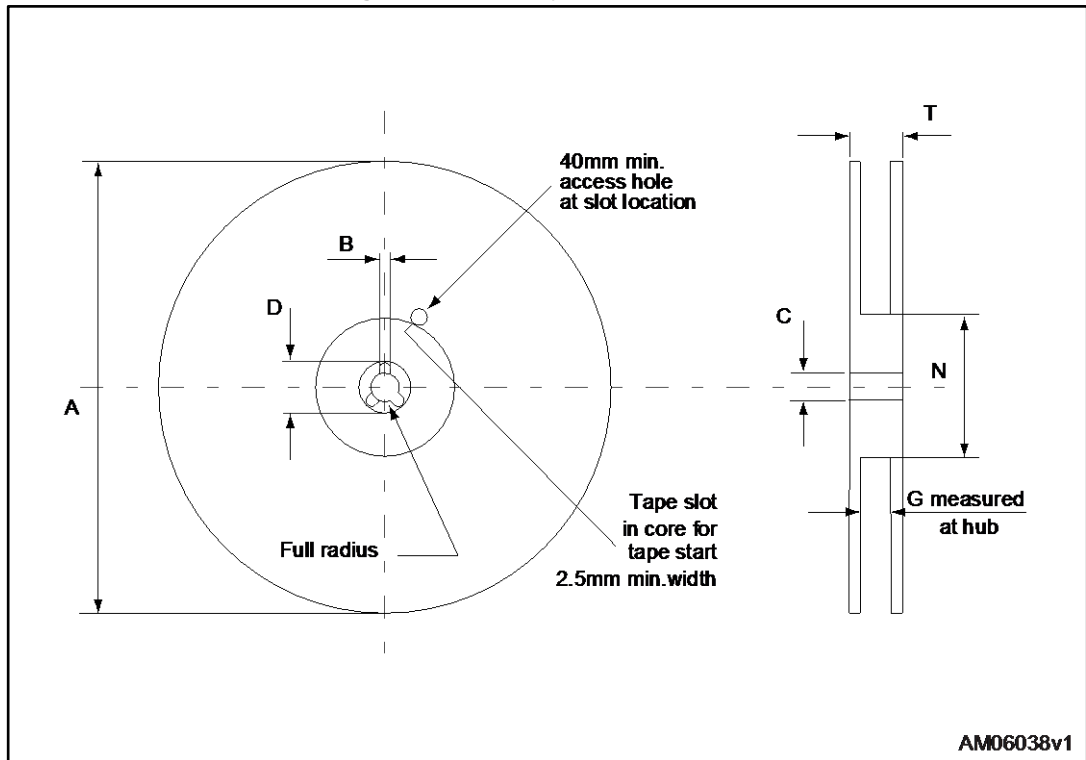


Table 14: D²PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 15: Document revision history

Date	Revision	Changes
07-Mar-2013	1	First release.
27-Mar-2013	2	Updated Figure 1: Internal schematic diagram. Minor text changes. Document status promoted from preliminary data to production data.
15-Apr-2013	3	– Modified: E _{AS} value, the entire typical values on <i>Table 5, 6 and 7</i> – Inserted: <i>Section 2.1: Electrical characteristics (curves)</i> – Minor text changes
25-Sep-2017	4	Added: TO-247 package. Updated title, features and description. Updated <i>Figure 13: "Static drain-source on-resistance"</i> . Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 5: "On/off-state"</i> , <i>Table 6: "Dynamic"</i> and <i>Table 8: "Source-drain diode"</i> . Added <i>Figure 8: "Safe operating area for TO-247"</i> and <i>Figure 9: "Thermal impedance for TO-247"</i> . Updated <i>Section 4.4: "TO-247 package information"</i> . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.