



CSD19533Q5A 100 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

2 Applications

- Primary Side Telecom
- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 100 V, 7.8 mΩ, SON 5 mm × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10 V)	27		nC
Q_{gd}	Gate Charge Gate to Drain	4.9		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	8.7	mΩ
		$V_{GS} = 10\text{ V}$	7.8	mΩ
$V_{GS(th)}$	Threshold Voltage	2.8		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD19533Q5A	13-Inch Reel	2500	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD19533Q5AT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

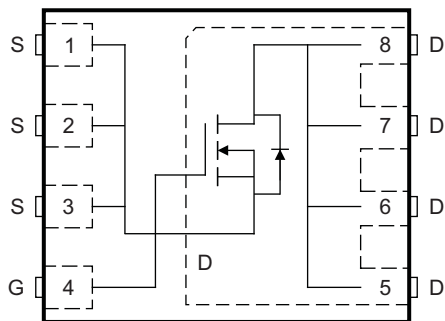
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	75	
	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	13	
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	231	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	96	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 46\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	106	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

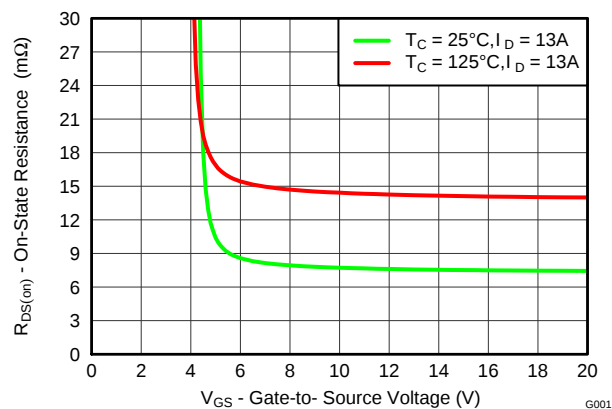
(2) Max $R_{\theta JC} = 1.3^\circ\text{C/W}$, pulse duration ≤100 μs, duty cycle ≤1%

Top View



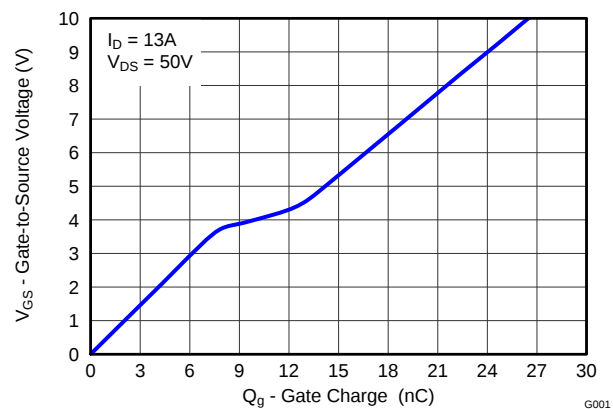
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$R_{DS(on)}$ vs V_{GS}



G001

Gate Charge



G001



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4 Revision History

Changes from Original (December 2013) to Revision A	Page
• Added small reel order number	1
• Increased pulsed drain current to 231A	1
• Added line for max power dissipation with case temperature held to 25°C	1
• Updated the pulsed drain current conditions	1
• Fixed y-axis on Figure 1 to state that it is a normalized $R_{\theta JC}$ curve	4
• Updated the safe operating area in Figure 10	6

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.2	2.8	3.4	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 6 V, I _D = 13 A		8.7	11.1	mΩ
		V _{GS} = 10 V, I _D = 13 A		7.8	9.4	mΩ
g _{fs}	Transconductance	V _{DS} = 10 V, I _D = 13 A		63		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		2050	2670	pF
C _{oss}	Output Capacitance			395	514	pF
C _{rss}	Reverse Transfer Capacitance			9.6	12.5	pF
R _G	Series Gate Resistance			1.2	2.4	Ω
Q _g	Gate Charge Total (10 V)	V _{DS} = 50 V, I _D = 13 A		27	35	nC
Q _{gd}	Gate Charge Gate to Drain			4.9		nC
Q _{gs}	Gate Charge Gate to Source			7.9		nC
Q _{g(th)}	Gate Charge at V _{th}			5.7		nC
Q _{oss}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		75		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 50 V, V _{GS} = 10 V, I _{DS} = 13 A, R _G = 0 Ω		6		ns
t _r	Rise Time			6		ns
t _{d(off)}	Turn Off Delay Time			16		ns
t _f	Fall Time			5		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 13 A, V _{GS} = 0 V		0.8	1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 50 V, I _F = 13 A, di/dt = 300 A/μs		163		nC
t _{rr}	Reverse Recovery Time			62		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			1.3	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

CSD19533Q5A

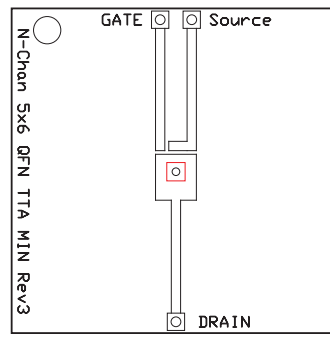
SLPS486A – DECEMBER 2013 – REVISED MAY 2014

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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

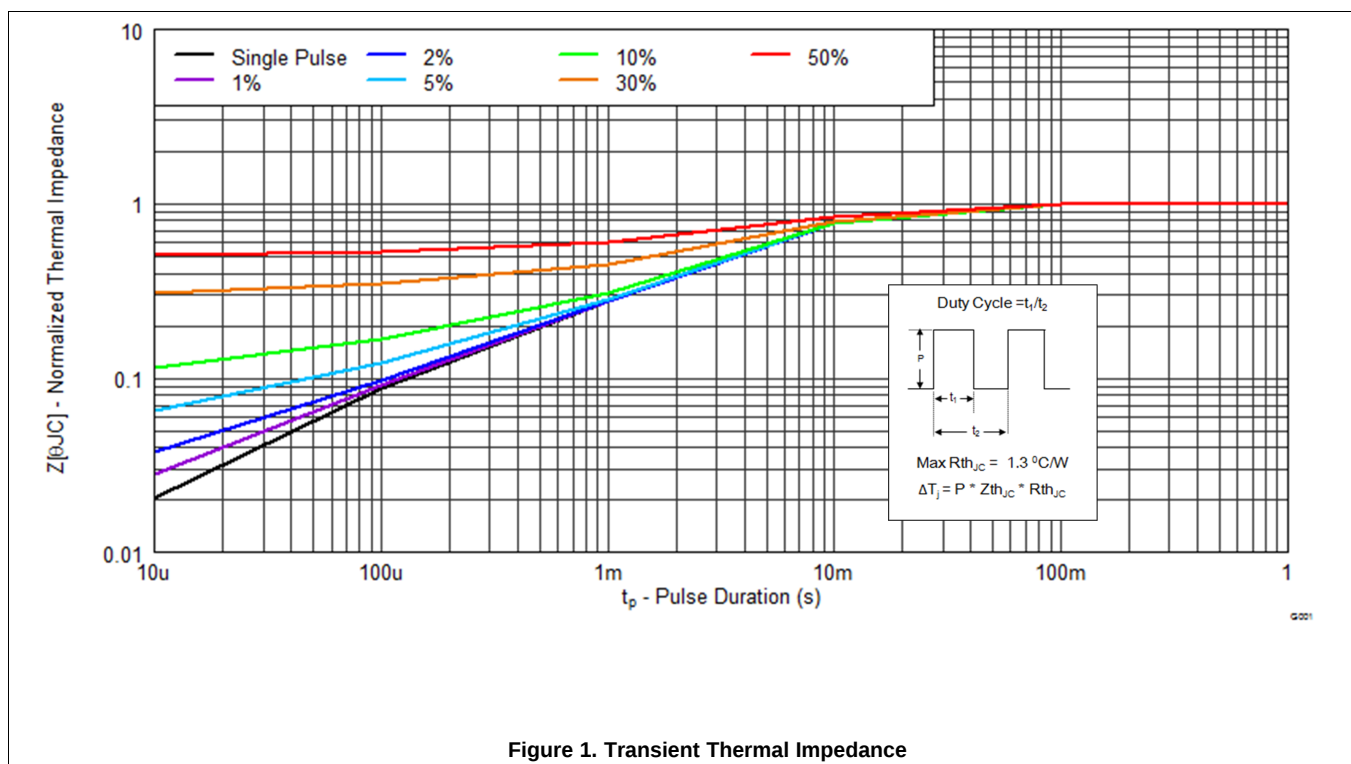


M0137-02

Max $R_{\theta JA} = 115^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

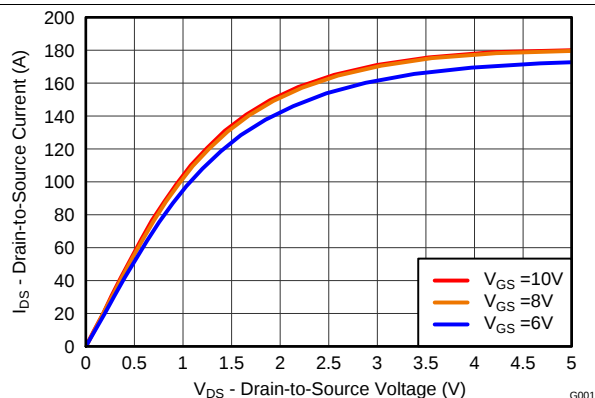


Figure 2. Saturation Characteristics

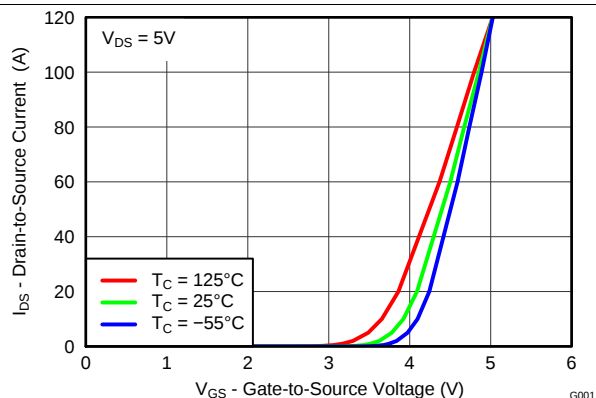


Figure 3. Transfer Characteristics

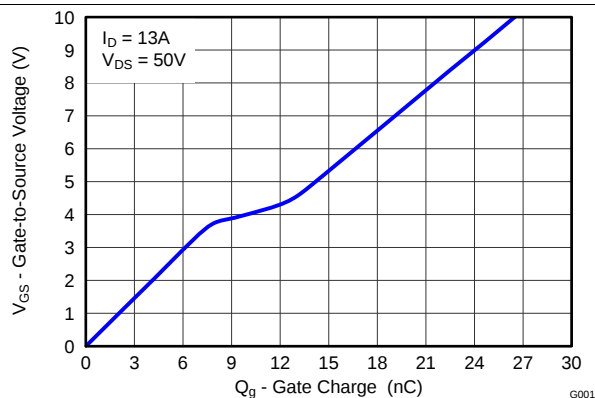


Figure 4. Gate Charge

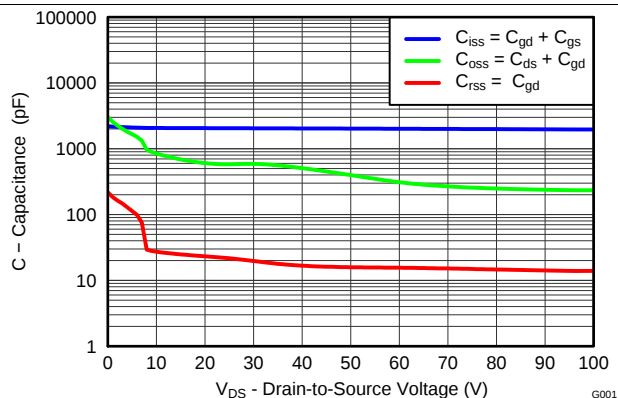


Figure 5. Capacitance

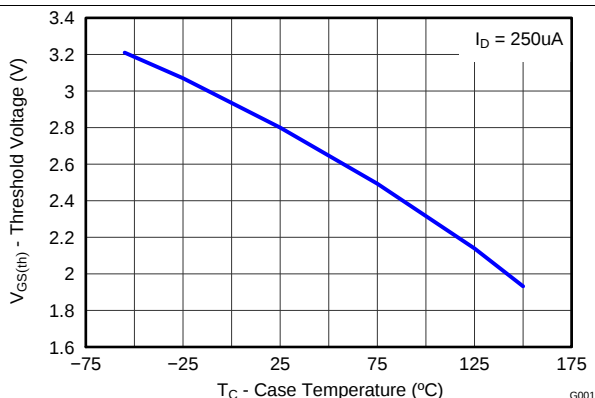


Figure 6. Threshold Voltage vs Temperature

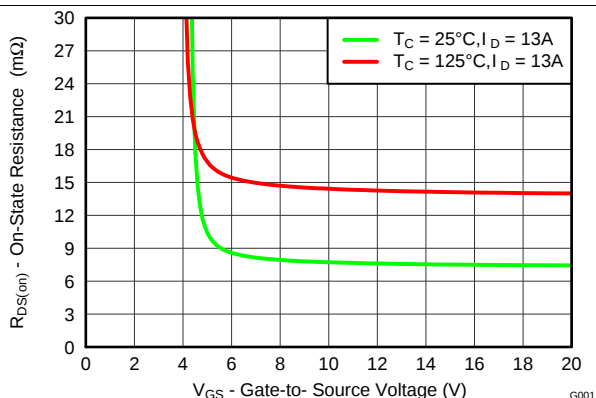


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

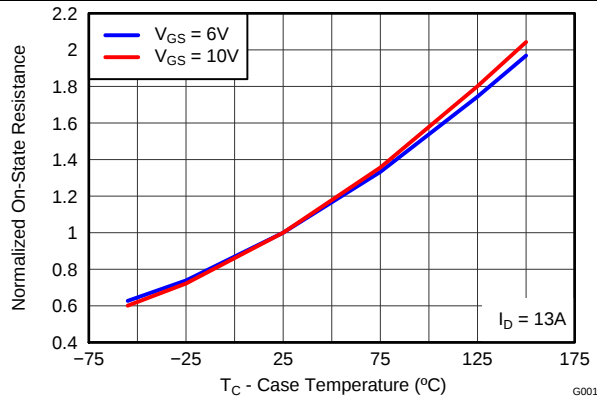


Figure 8. Normalized On-State Resistance vs Temperature

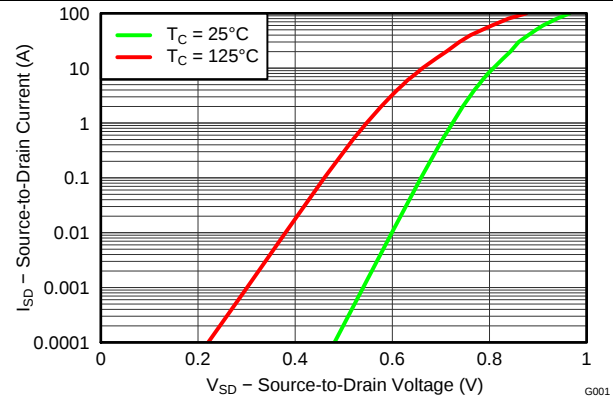


Figure 9. Typical Diode Forward Voltage

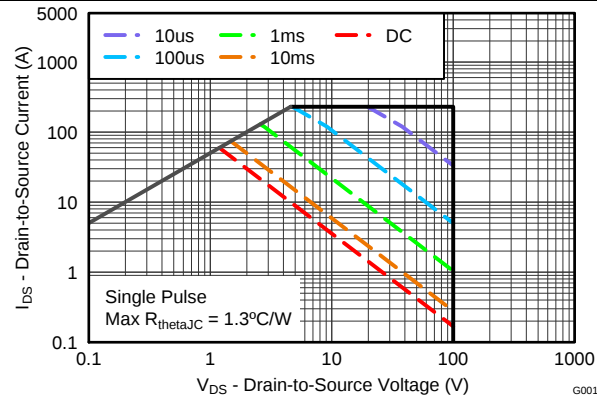


Figure 10. Maximum Safe Operating Area

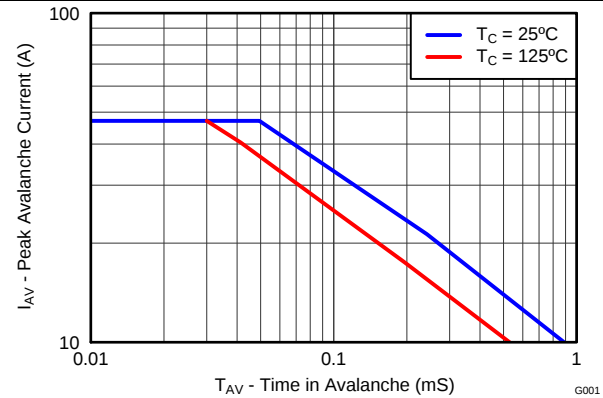


Figure 11. Single Pulse Unclamped Inductive Switching

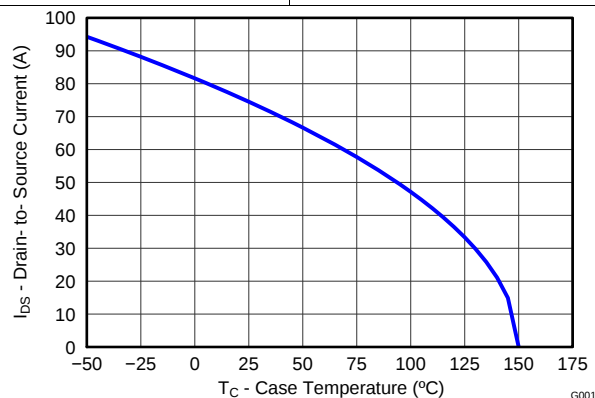


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

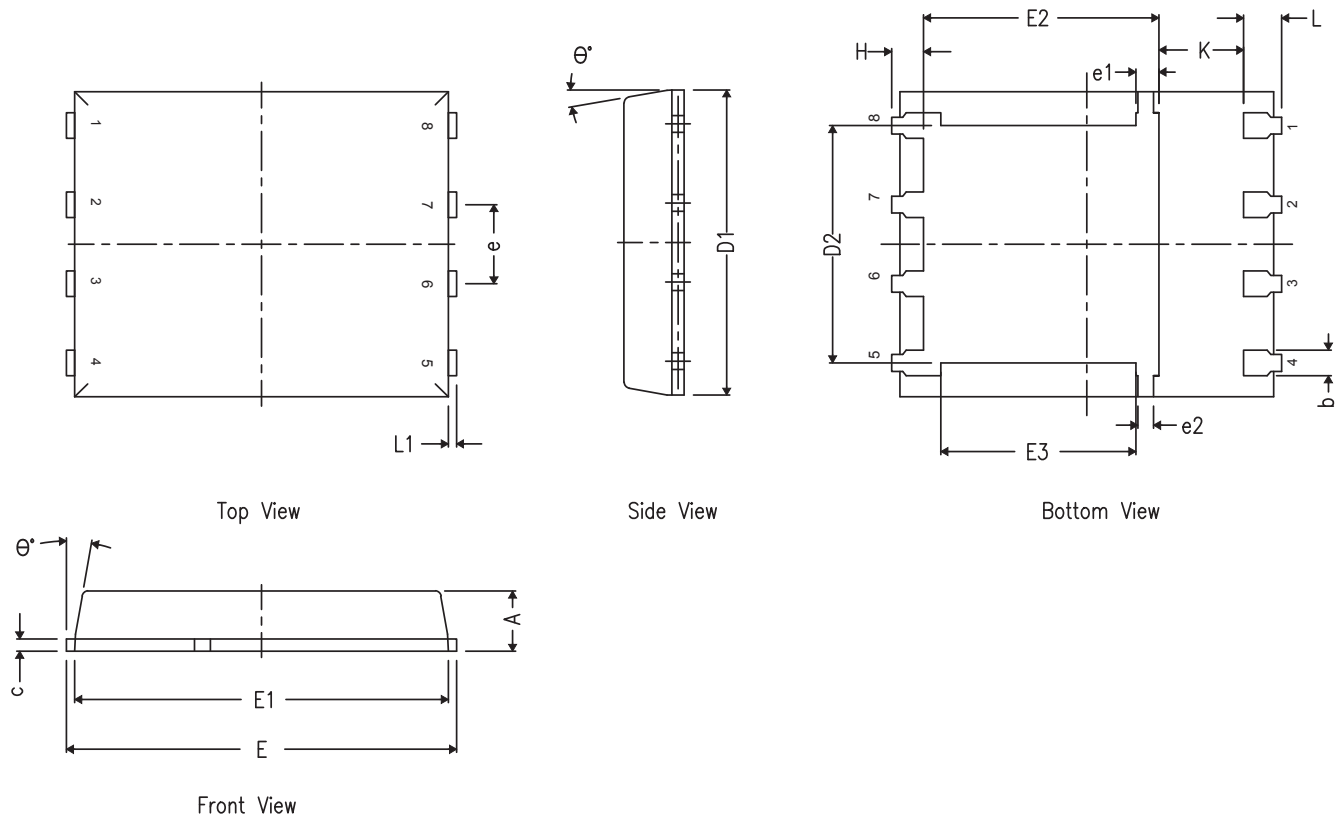
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

7 Mechanical, Packaging, and Orderable Information

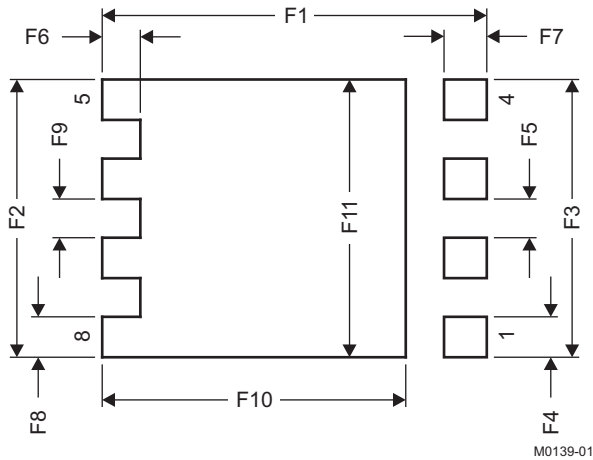
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	–	–
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	–	12°

7.2 Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19533Q5A	ACTIVE	VSON-FET	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD19533	Samples
CSD19533Q5AT	ACTIVE	VSON-FET	DQJ	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM		CSD19533	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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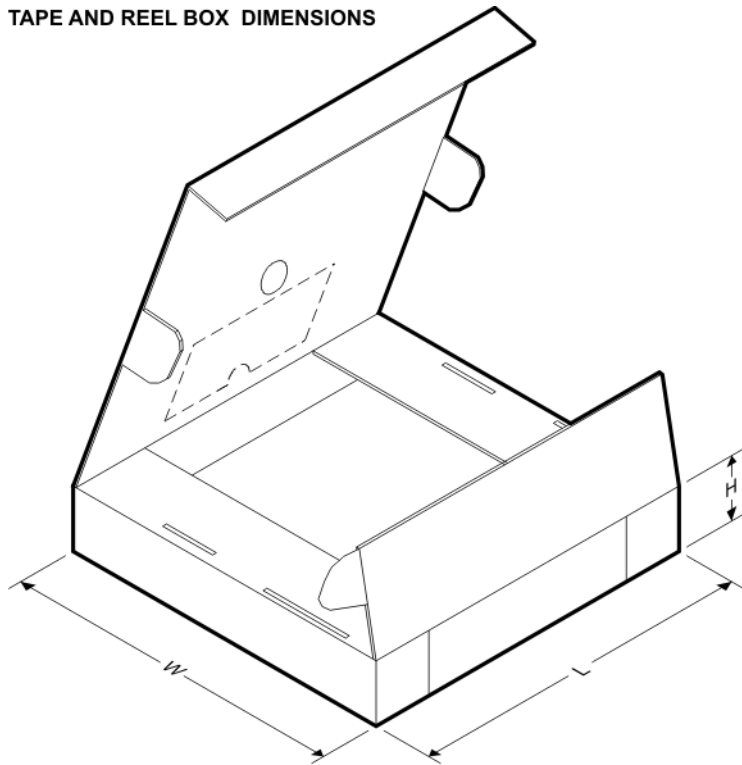
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19533Q5A	VSON-FET	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD19533Q5AT	VSON-FET	DQJ	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19533Q5A	VSON-FET	DQJ	8	2500	340.0	340.0	38.0
CSD19533Q5AT	VSON-FET	DQJ	8	250	340.0	340.0	38.0

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