

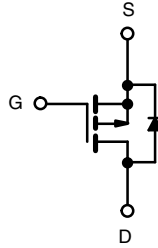
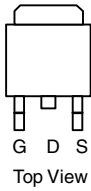
## Automotive P-Channel 80 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	- 80
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.025
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.031
$I_D$ (A)	- 50
Configuration	Single

### FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

**TO-263**


P-Channel MOSFET

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and Halogen-free	SQM50P08-25L-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 80	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$I_D$	$T_C = 25$ °C <sup>a</sup>	- 50	
		$T_C = 125$ °C	- 30	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	- 50	A	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	- 120		
Single Pulse Avalanche Current	$I_{AS}$	- 47		
Single Pulse Avalanche Energy	$E_{AS}$	L = 0.1 mH	110	mJ
Maximum Power Dissipation <sup>b</sup>			$P_D$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	$T_C = 25$ °C	50	W
		$T_C = 125$ °C		
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)			

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA		- 80	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA		- 1.5	- 2.0	- 2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V	-	-	- 1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V, T <sub>J</sub> = 125 °C	-	-	- 50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V, T <sub>J</sub> = 175 °C	-	-	- 250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> ≤ - 5 V	- 50	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A	-	0.020	0.025	Ω
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A, T <sub>J</sub> = 125 °C	-	-	0.044	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A, T <sub>J</sub> = 175 °C	-	-	0.055	
		V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 10.5 A	-	0.025	0.031	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 12.5 A		-	36	-	S
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 25 V, f = 1 MHz	-	4280	5350	pF
Output Capacitance	C <sub>oss</sub>			-	356	445	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	240	300	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 40 V, I <sub>D</sub> = - 12.5 A	-	91	137	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	8.2	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	24	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.4	2.99	4.5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = - 40 V, R <sub>L</sub> = 3.2 Ω I <sub>D</sub> ≅ - 12.5 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		-	11	17	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	11	17	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	71	107	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	16	24	
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 120	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = - 20 A, V <sub>GS</sub> = 0 V		-	- 0.86	- 1.5	V

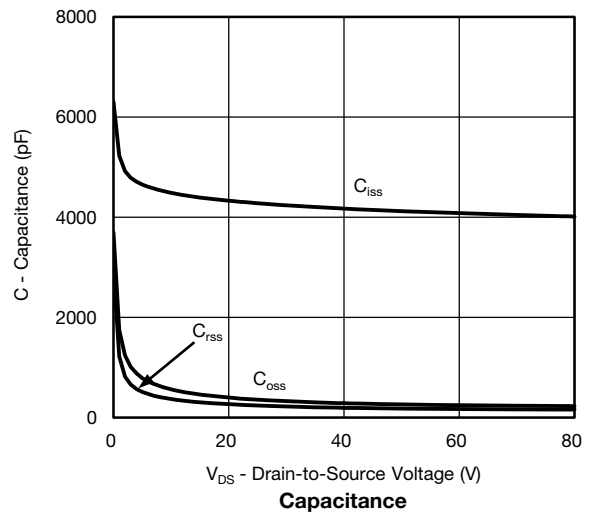
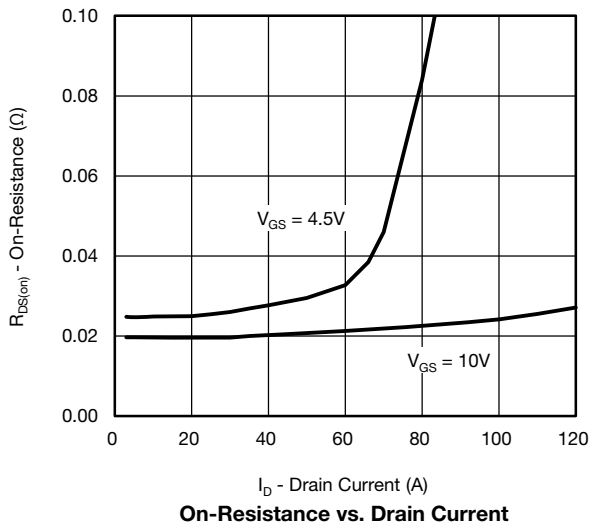
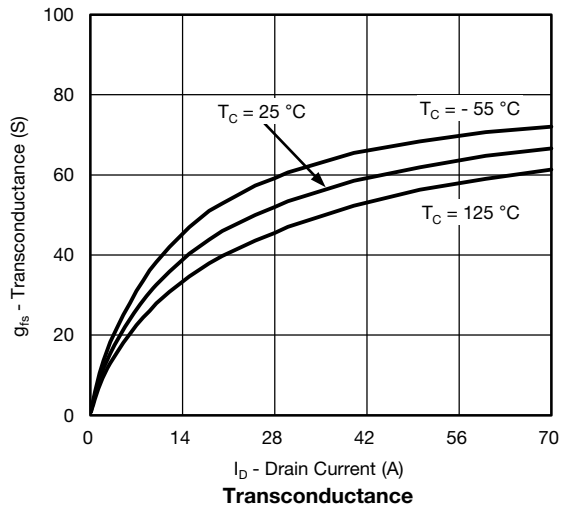
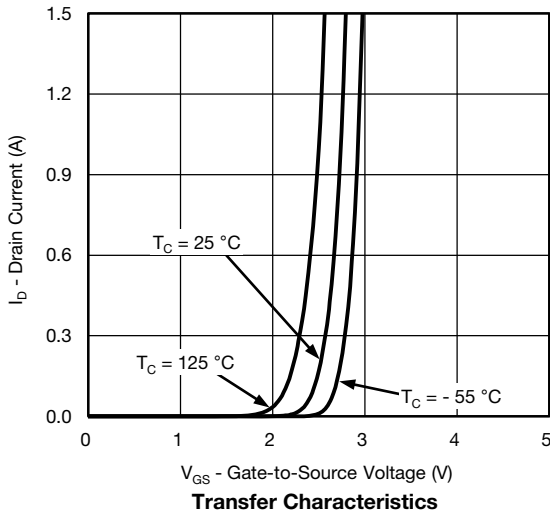
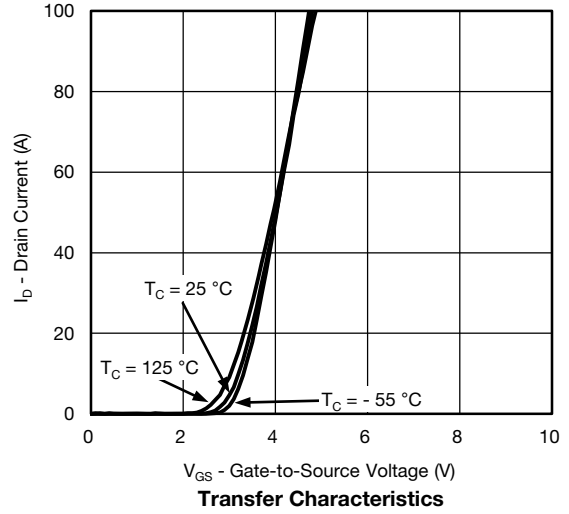
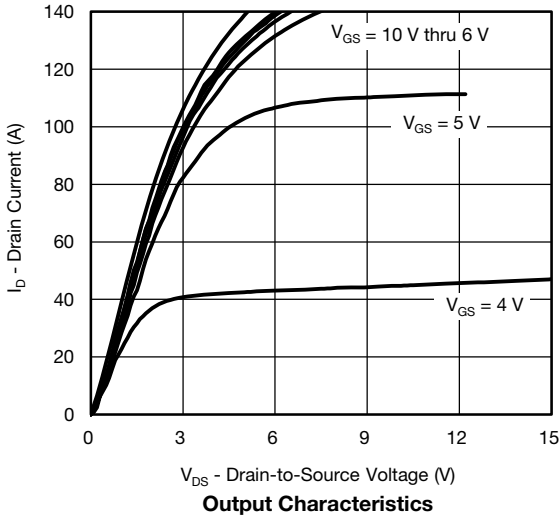
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

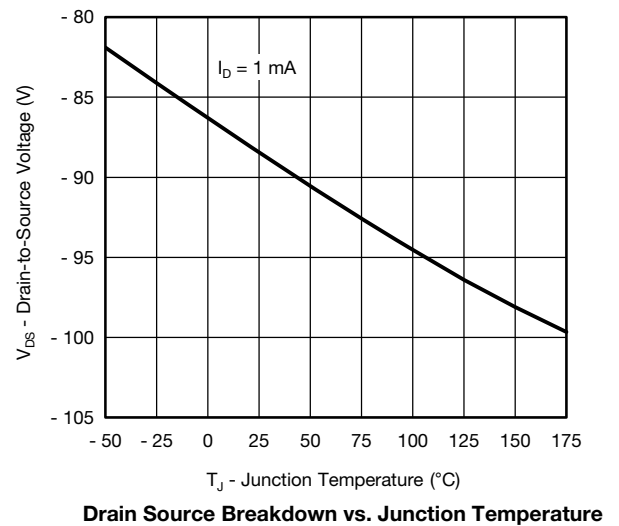
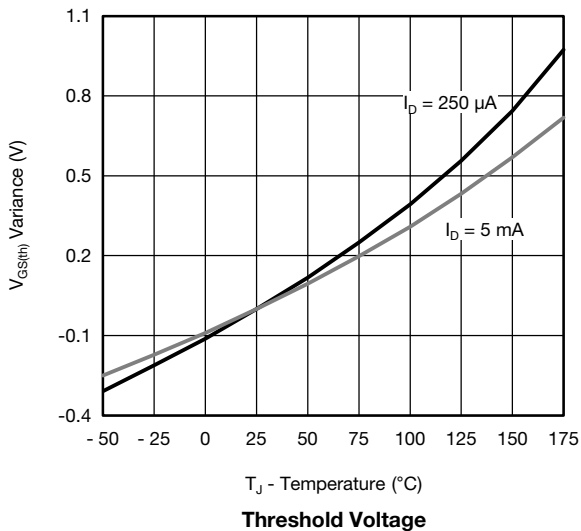
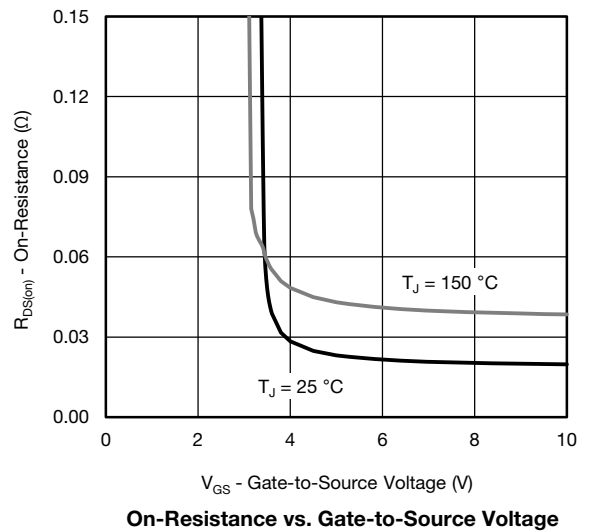
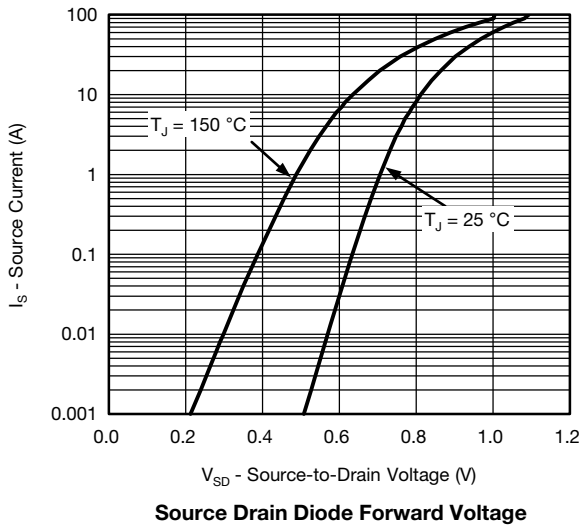
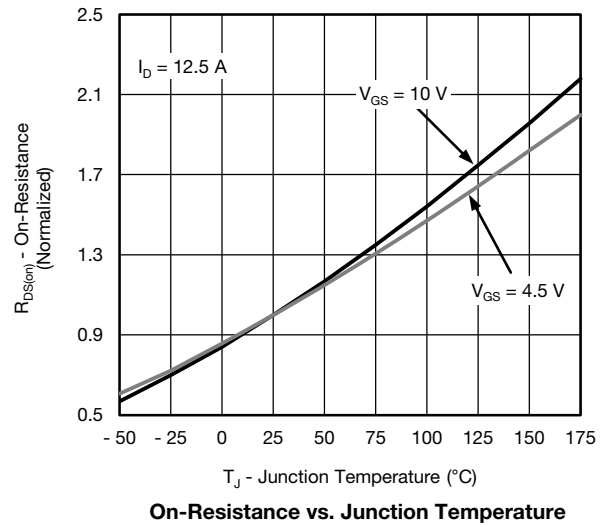
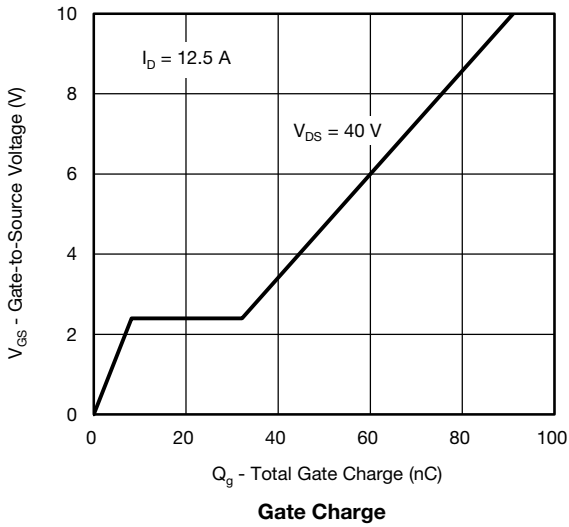


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



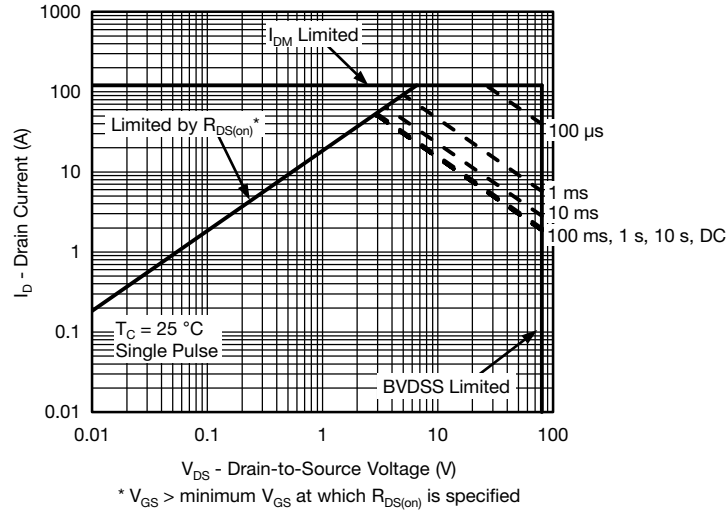


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)

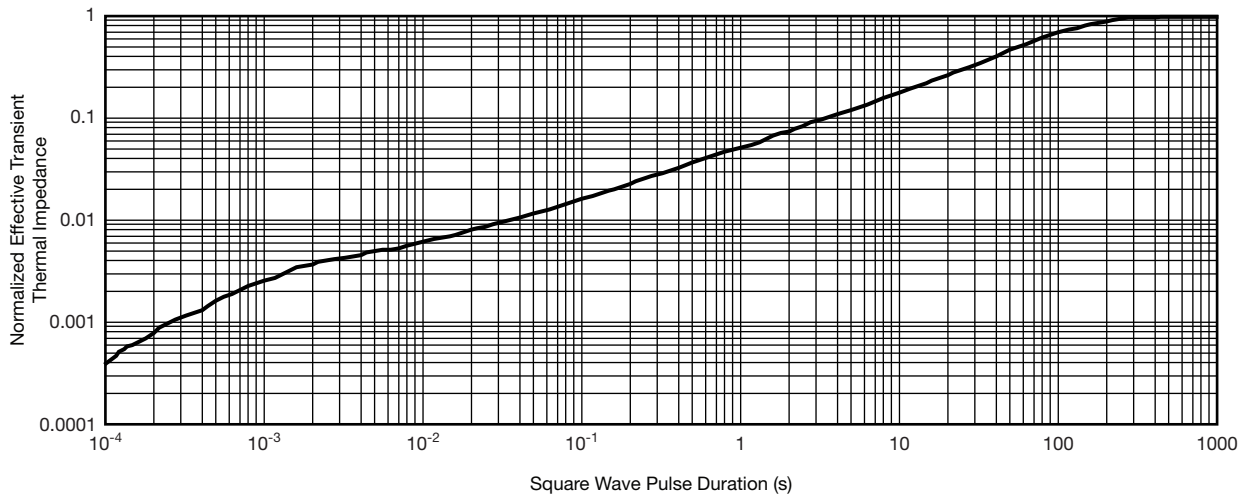




**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



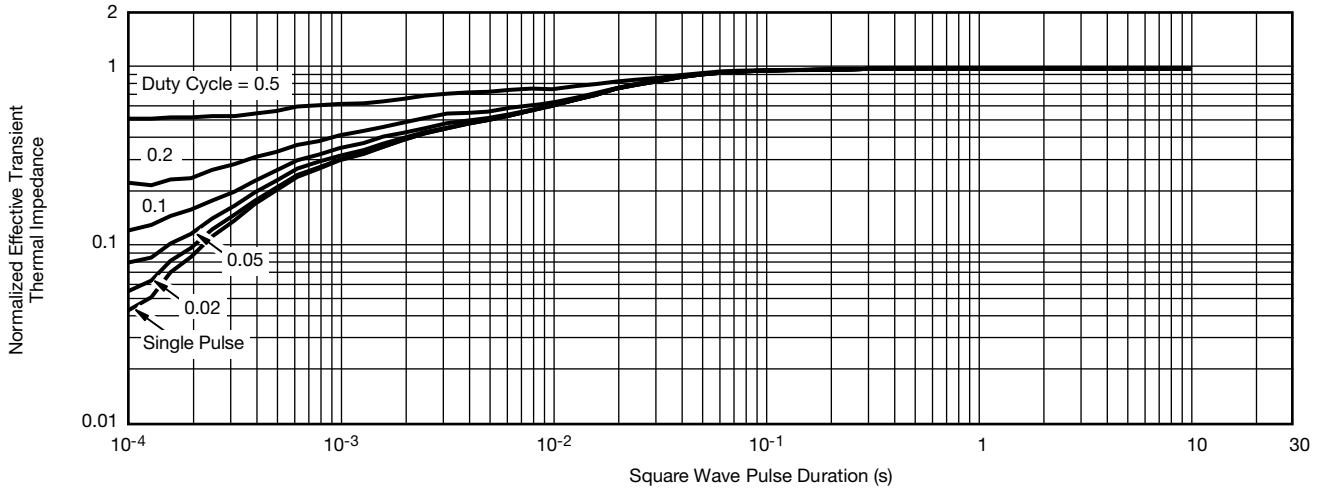
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67064](http://www.vishay.com/ppg?67064).

### TO-263 (D<sup>2</sup>PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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- Техническая поддержка проекта;
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#### Как с нами связаться

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