MicroConverter® Multichannel 24-/16-Bit ADCs with Embedded 62 kB Flash and Single-Cycle MCU

Data Sheet

ADuC845/ADuC847/ADuC848

FEATURES

- High resolution Σ-Δ ADCs
  - 2 independent 24-bit ADCs on the ADuC845
  - Single 24-bit ADC on the ADuC847 and single 16-bit ADC on the ADuC848
  - Up to 10 ADC input channels on all devices
  - 24-bit no missing codes
  - 22-bit rms (19.5 bit p-p) effective resolution
  - Offset drift 10 nV/°C, gain drift 0.5 ppm/°C chop enabled
- Memory
  - 62-kbyte on-chip Flash/EE program memory
  - 4-kbyte on-chip Flash/EE data memory
  - Flash/EE, 100-year retention, 100 kcycle endurance
  - 3 levels of Flash/EE program memory security
  - In-circuit serial download (no external hardware)
  - High speed user download (5 sec)
  - 2304 bytes on-chip data RAM
- 8051-based core
  - 8051-compatible instruction set
  - High performance single-cycle core
  - 32 kHz external crystal
  - On-chip programmable PLL (12.58 MHz max)
  - 3 × 16-bit timer/counter
  - 24 programmable I/O lines, plus 8 analog or digital input lines
  - 11 interrupt sources, two priority levels
  - Dual data pointer, extended 11-bit stack pointer
- On-chip peripherals
  - Internal power-on reset circuit
  - 12-bit voltage output DAC
  - Dual 16-bit Σ-Δ DACs
  - On-chip temperature sensor (ADuC845 only)
  - Dual excitation current sources (200 µA)
  - Time interval counter (wake-up/RTC timer)
  - UART, SPI®, and I²C® serial I/O
  - High speed dedicated baud rate generator (incl. 115,200)
  - Watchdog timer (WDT)
  - Power supply monitor (PSM)
- Power
  - Normal: 4.8 mA max at 3.6 V (core CLK = 1.57 MHz)
  - Power-down: 20 µA max with wake-up timer running
  - Specified for 3 V and 5 V operation
  - Package and temperature range:
  - 52-lead MQFP (14 mm × 14 mm), −40°C to +125°C
  - 56-lead LFCSP (8 mm × 8 mm), −40°C to +85°C

APPLICATIONS

Multichannel sensor monitoring
Industrial/environmental instrumentation
Weigh scales, pressure sensors, temperature monitoring
Portable instrumentation, battery-powered systems
Data logging, precision system monitoring

FUNCTIONAL BLOCK DIAGRAM

Figure 1. ADuC845 Functional Block Diagram

Rev. D

Document Feedback

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REVISION HISTORY

5/2016—Rev. C to Rev. D

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12/2012—Rev. B to Rev. C

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4/2004—Revision 0: Initial Version

SPECIFICATIONS[1]

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V, REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz crystal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Input buffer on for primary ADC, unless otherwise noted. Core speed = 1.57 MHz (default CD = 3), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY ADC					
Conversion Rate	5.4		105	Hz	Chop on (ADCMODE.3 = 0)
	16.06		1365	Hz	Chop off (ADCMODE.3 = 1)
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate with chop enabled
	24			Bits	≤80.3 Hz update rate with chop disabled
Resolution (ADuC845/ADuC847)	See Table 11 and Table 15				
Resolution (ADuC848)	See Table 13 and Table 17				
Output Noise (ADuC845/ADuC847)	See Table 10 and Table 14			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Output Noise (ADuC848)	See Table 12 and Table 16			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
					Chop off, offset error is in the order of the noise for the programmed gain and update rate following a calibration.
Offset Error Drift vs. Temperature[2]		±10		nV/°C	Chop on (ADCMODE.3 = 0)
		±200		nV/°C	Chop off (ADCMODE.3 = 1)
Full-Scale Error[4]					
ADuC845/ADuC847		±10		µV	±20 mV to ±2.56 V
ADuC848		±10		µV	±20 mV to ±640 mV
		±0.5		LSB_{16}	±1.28 V to ±2.56 V
Gain Error Drift vs. Temperature[4]		±0.5		ppm/°C	
Power Supply Rejection					
	80			dB	AIN = 1 V, ±2.56 V, chop enabled
		113		dB	AIN = 7.8 mV, ±20 mV, chop enabled
		80		dB	AIN = 1 V, ±2.56 V, chop disabled[2]
PRIMARY ADC ANALOG INPUTS					
Differential Input Voltage Ranges[5, 6]					Gain = 1 to 128
Bipolar Mode (ADC0CON1.5 = 0)		±1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
Unipolar Mode (ADC0CON1.5 = 1)		0 – 1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
ADC Range Matching		±2		µV	AIN = 18 mV, chop enabled
Common-Mode Rejection DC					Chop enabled, chop disabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
		113		dB	AIN = 1 V, range = ±2.56 V
Common-Mode Rejection 50 Hz/60 Hz[2]					50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop enabled, REJ60 enabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
	90			dB	AIN = 1 V, range = ±2.56 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
Analog Input Current[2]			±1	nA	T_{MAX} = 85°C, buffer on
			±5	nA	T_{MAX} = 125°C, buffer on
Analog Input Current Drift		±5		pA/°C	T_{MAX} = 85°C, buffer on
		±15		pA/°C	T_{MAX} = 125°C, buffer on
Average Input Current		±125		nA/V	±2.56 V range, buffer bypassed
Average Input Current Drift		±2		pA/V/°C	Buffer bypassed
Absolute AIN Voltage Limits[2]	A_{GND} + 0.1		AV_{DD} − 0.1	V	AIN1 … AIN10 and AINCOM with buffer enabled
Absolute AIN Voltage Limits[2]	A_{GND} − 0.03		AV_{DD} + 0.03	V	AIN1 … AIN10 and AINCOM with buffer bypassed
EXTERNAL REFERENCE INPUTS					
REFIN(+) to REFIN(−) Voltage		2.5		V	REFIN refers to both REFIN and REFIN2
REFIN(+) to REFIN(−) Range[2]	1		AV_{DD}	V	REFIN refers to both REFIN and REFIN2
Average Reference Input Current		±1		µA/V	Both ADCs enabled
Average Reference Input Current Drift		±0.1		nA/V/°C	
NOXREF Trigger Voltage	0.3		0.65	V	NOXREF (ADCSTAT.4) bit active if V_{REF} > 0.3 V, and inactive if V_{REF} > 0.65 V
Common-Mode Rejection					
DC Rejection		125		dB	AIN = 1 V, range = ±2.56 V
50 Hz/60 Hz Rejection[2]	90			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 82
Normal Mode Rejection 50 Hz/60 Hz[2]	75			dB	50 Hz/60 Hz ±1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off
AUXILIARY ADC (ADuC845 Only)					
Conversion Rate	5.4		105	Hz	Chop on
	16.06		1365	Hz	Chop off
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate, chop enabled
	24			Bits	80.3 Hz update rate, chop disabled
Resolution	See Table 19 and Table 21				
Output Noise	See Table 18 and Table 20				Output noise varies with selected update rates.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
		±0.25		LSB_{16}	Chop off
Offset Error Drift[2]		10		nV/°C	Chop on
		200		nV/°C	Chop off
Full-Scale Error[4]		±0.5		LSB_{16}	
Gain Error Drift[4]		±0.5		ppm/°C	
Power Supply Rejection	80			dB	AIN = 1 V, range = ±2.56 V, chop enabled
		80		dB	AIN = 1 V, range = ±2.56 V, chop disabled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY ADC ANALOG INPUTS (ADuC845 ONLY)					
Differential Input Voltage Ranges[5, 6]					
Bipolar Mode (ADC1CON.5 = 0)		$\pm V_{REF}$		V	REFIN = REFIN(+) – REFIN(–) (or Int 1.25 V_{REF})
Unipolar Mode (ADC1CON.5 = 1)		0 – V_{REF}		V	REFIN = REFIN(+) – REFIN(–) (or Int 1.25 V_{REF})
Average Analog Input Current		125		nA/V	
Analog Input Current Drift		±2		pA/V/°C	
Absolute AIN/AINCOM Voltage Limits[2, 7]	A_{GND} – 0.03		AV_{DD} + 0.03	V	
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN and REFIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
ADC SYSTEM CALIBRATION					
Full-Scale Calibration Limit			+1.05 × FS	V	
Zero-Scale Calibration Limit	–1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
DAC					
Voltage Range		0 – V_{REF}		V	DACCON.2 = 0
		0 – AV_{DD}		V	DACCON.2 = 1
Resistive Load		10		kΩ	From DAC output to AGND
Capactive Load		100		pF	From DAC output to AGND
Output Impedance		0.5		Ω	
I_{SINK}		50		µA	
DC Specifications[8]					
Resolution	12			Bits	
Relative Accuracy		±3		LSB	
Differential Nonlinearity			–1	LSB	Guaranteed 12-bit monotonic
Offset Error			±50	mV	
Gain Error			±1	%	AV_{DD} range
		±1		%	V_{REF} range
AC Specifications[2, 8]					
Voltage Output Settling Time		15		µs	Settling time to 1 LSB of final value
Digital-to-Analog Glitch Energy		10		nVs	1 LSB change at major carry
INTERNAL REFERENCE					
ADC Reference					Chop enabled
Reference Voltage	1.25 – 1%	1.25	1.25 + 1%	V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		45		dB	
Reference Tempco		100		ppm/°C	
DAC Reference					
Reference Voltage	2.5 – 1%	2.5	2.5 + 1%	±1% V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		50		dB	
Reference Tempco		±100		ppm/°C	
TEMPERATURE SENSOR (ADuC845 ONLY)					
Accuracy		±2		°C	
Thermal Impedance		90		°C/W	MQFP
		52		°C/W	LFCSP

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		−100		nA	AIN+ is the selected positive input (AIN4 or AIN6 only) to the primary ADC
AIN− Current		100		nA	AIN− is the selected negative input (AIN5 or AIN7 only) to the primary ADC
Initial Tolerance at 25°C		±10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		200		µA	Available from each current source
Initial Tolerance at 25°C		±10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		±1		%	Matching between both current sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD} = 5 V ± 5%
Load Regulation		0.1		µA/V	
Output Compliance[2]	AGND		AV_{DD} − 0.6	V	
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
AV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
DV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5 V
	2.5			V	DV_{DD} = 3 V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs Except SCLOCK, RESET, and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5 V
	0.95		2.5	V	DV_{DD} = 3 V
V_{T-}	0.8		1.4	V	DV_{DD} = 5 V
	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3		0.85	V	DV_{DD} = 5 V or 3 V
Input Currents					
Port 0, P1.0 to P1.7, $\overline{EA}$			±10	µA	V_{IN} = 0 V or V_{DD}
RESET			±10	µA	V_{IN} = 0 V, DV_{DD} = 5 V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V, internal pull-down
Port 2, Port 3			±10	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V
	−180		−660	µA	V_{IN} = 2 V, DV_{DD} = 5 V
	−20		−75	µA	V_{IN} = 0.45 V, DV_{DD} = 5 V
Input Capacitance		10		pF	All digital inputs

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (ALL DIGITAL OUTPUTS EXCEPT XTAL2)					
V_{OH}, Output High Voltage[2]	2.4			V	DV_{DD} = 5 V, I_{SOURCE} = 80 µA
	2.4			V	DV_{DD} = 3 V, I_{SOURCE} = 20 µA
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 8 mA, SCLOCK, SDATA
			0.4	V	I_{SINK} = 1.6 mA on P0, P1, P2
Floating State Leakage Current[2]			±10	µA	
Floating State Output Capacitance		10		pF	
START-UP TIME					
At Power-On		600		ms	
After Ext RESET in Normal Mode		3		ms	
After WDT RESET in Normal Mode		2		ms	Controlled via WDCON SFR
From Power-Down Mode					
Oscillator Running					PLLCON.7 = 0
Wake-Up with $\overline{INT0}$ Interrupt		20		µs	
Wake-Up with SPI Interrupt		20		µs	
Wake-Up with TIC Interrupt		20		µs	
Oscillator Powered Down					PLLCON.7 = 1
Wake-Up with $\overline{INT0}$ Interrupt		30		µs	
Wake-Up with SPI Interrupt		30		µs	
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS					
Endurance[9]	100,000			Cycles	
Data Retention[10]	100			Years	
POWER REQUIREMENTS					
Power Supply Voltages					
AV_{DD} 3 V Nominal	2.7		3.6	V	
AV_{DD} 5 V Nominal	4.75		5.25	V	
DV_{DD} 3 V Nominal	2.7		3.6	V	
DV_{DD} 5 V Nominal	4.75		5.25	V	
5 V Power Consumption					4.75 V < DV_{DD} < 5.25 V, AV_{DD} = 5.25 V
Normal Mode[11, 12]					
DV_{DD} Current			10	mA	Core clock = 1.57 MHz
		25	31	mA	Core clock = 12.58 MHz
AV_{DD} Current			180	µA	
Power-Down Mode[11, 12]					
DV_{DD} Current		40	53	µA	T_{MAX} = 85°C; OSC on; TIC on
		50		µA	T_{MAX} = 125°C; OSC on; TIC on
		20	33	µA	T_{MAX} = 85°C; OSC off
		30		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off
Typical Additional Peripheral Currents (AI_{DD} and DI_{DD})					5 V V_{DD}, CD = 3
Primary ADC		1		mA	
Auxiliary ADC (ADuC845 Only)		0.5		mA	
Power Supply Monitor		30		µA	
DAC		60		µA	DACH/L = 000H
Dual Excitation Current Sources		200		µA	200 µA each. Can be combined to give 400 µA on a single output.
ALE Off		−20		µA	PCON.4 = 1 (see Table 6)
WDT		10		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = $\pm(V_{REF}\ 2^{RN})/1.25$, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still $-V_{REF}$ to $+V_{REF}$.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions:
Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop.
Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

ABOSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
AV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
AGND to DGND[1]	−0.3 V to +0.3 V
AV_{DD} to DV_{DD}	−2 V to +5 V
Analog Input Voltage to AGND[2]	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MQFP)	90°C/W
θ_{JA} Thermal Impedance (LFCSP)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC845, ADuC847, and ADuC848.
[2] Applies to the P1.0 to P1.7 pins operating in analog or digital input modes.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 2. 52-Lead MQFP Pin Configuration

Figure 3. 56-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.				
52-MQFP	**56-LFCSP**	**Mnemonic**	**Type[1]**	**Description**
1	56	P1.0/AIN1	I	By power-on default, P1.0/AIN1 is configured as the AIN1 analog input. AIN1 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN2. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
2	1	P1.1/AIN2	I	On power-on default, P1.1/AIN2 is configured as the AIN2 analog input. AIN2 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN1. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
3	2	P1.2/AIN3/REFIN2+	I	On power-on default, P1.2/AIN3 is configured as the AIN3 analog input. AIN3 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN4. P1.2 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, positive terminal.
4	3	P1.3/AIN4/REFIN2–	I	On power-on default, P1.3/AIN4 is configured as the AIN4 analog input. AIN4 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN3. P1.3 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, negative terminal.
5	4	AV_{DD}	S	Analog Supply Voltage.
6	5	AGND	S	Analog Ground.
Not applicable	6	AGND	S	A second analog ground is provided with the LFCSP version only.
7	7	REFIN–	I	External Differential Reference Input, Negative Terminal.
8	8	REFIN+	I	External Differential Reference Input, Positive Terminal.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
9	9	P1.4/AIN5	I	On power-on default, P1.4/AIN5 is configured as the AIN5 analog input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	On power-on default, P1.5/AIN6 is configured as the AIN6 analog input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	On power-on default, P1.6/AIN7 is configured as the AIN7 analog input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or both current sources can also be configured at this pin. P1.6 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
12	12	P1.7/AIN8/IEXC2	I/O	On power-on default, P1.7/AIN8 is configured as the AIN8 analog input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or both current sources can also be configured at this pin. P1.7 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin, provided that a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, appears at this pin.
Not applicable	15	AIN9	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10 (LFCSP version only).
Not applicable	16	AIN10	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9 (LFCSP version only).
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. This pin has an internal weak pull-down and a Schmitt trigger input stage.
16 to 19, 22 to 25	18 to 21, 24 to 27	P3.0 to P3.7	I/O	P3.0 to P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for one core clock period of the instruction cycle. Port 3 pins also have the various secondary functions described in this table.
16	18	P3.0/RxD		Receiver Data for UART Serial Port.
17	19	P3.1/TxD		Transmitter Data for UART Serial Port.
18	20	P3.2/$\overline{\text{INT0}}$		External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
19	21	P3.3/$\overline{\text{INT1}}$		External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
22	24	P3.4/T0		Timer/Counter 0 External Input.
23	25	P3.5/T1		Timer/Counter 1 External Input.
24	26	P3.6/$\overline{\text{WR}}$		External Data Memory Write Strobe. This pin latches the data byte from Port 0 into an external data memory.
25	27	P3.7/$\overline{\text{RD}}$		External Data Memory Read Strobe. This pin enables the data from an external data memory to Port 0.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
20, 34, 48	22, 36, 51	DV_{DD}	S	Digital Supply Voltage.
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground.
26	28	SCLK (I^2C)	I/O	Serial Interface Clock for the I^2C Interface. As an input, this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be controlled in software as a digital output pin.
27	29	SDATA	I/O	Serial Data Pin for the I^2C Interface. As an input, this pin has a weak internal pull-up present unless it is outputting logic low.
28 to 31, 36 to 39	30 to 33, 39 to 42	P2.0 to P2.7	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. Port 2 emits the middle and high-order address bytes during accesses to the 24-bit external data memory space. Port 2 pins also have the various secondary functions described in this table.
28	30	P2.0/SCLOCK (SPI)		Serial Interface Clock for the SPI Interface. As an input this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low.
29	31	P2.1/MOSI		Serial Master Output/Slave Input Data for the SPI Interface. A strong internal pull-up is present on this pin when the SPI interface outputs a logic high. A strong internal pull-down is present on this pin when the SPI interface outputs a logic low.
30	32	P2.2/MISO		Master Input/Slave Output for the SPI Interface. A weak pull-up is present on this input pin.
31	33	P2.3/$\overline{SS}$/T2		Slave Select Input for the SPI Interface. A weak pull-up is present on this pin. For both package options, this pin can also be used to provide a clock input to Timer 2. When enabled, Counter 2 is incremented in response to a negative transition on the T2 input pin.
36	39	P2.4/T2EX		Control Input to Timer 2. When enabled, a negative transition on the T2EX input pin causes a Timer 2 capture or reload event.
37	40	P2.5/PWM0		If the PWM is enabled, the PWM0 output appears at this pin.
38	41	P2.6/PWM1		If the PWM is enabled, the PWM1 output appears at this pin.
39	42	P2.7/PWMCLK		If the PWM is enabled, an external PWM clock can be provided at this pin.
32	34	XTAL1	I	Input to the Crystal Oscillator Inverter.
33	35	XTAL2	O	Output from the Crystal Oscillator Inverter. See the Hardware Design Considerations section for a description.
40	43	$\overline{EA}$		External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to F7FFH. No external program memory access is available on the ADuC845, ADuC847, or ADuC848. To determine the mode of code execution, the $\overline{EA}$ pin is sampled at the end of an external RESET assertion or as part of a device power cycle. $\overline{EA}$ can also be used as an external emulation I/O pin, and therefore the voltage level at this pin must not be changed during normal operation because this might cause an emulation interrupt that halts code execution.
41	44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This function is not used on the ADuC845, ADuC847, or ADuC848. This pin remains high during internal program execution. $\overline{PSEN}$ can also be used to enable serial download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external data memory access cycles. It can be disabled by setting the PCON.4 bit in the PCON SFR.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
43 to 46, 49 to 52	46 to 49, 52 to 55	P0.0 to P0.7	I/O	These pins are part of Port 0, which is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and, in that state, can be used as high impedance inputs. An external pull-up resistor is required on P0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and data bus during accesses to external data memory. In this application, Port 0 uses strong internal pull-ups when emitting 1s.
	EP	EPAD		Exposed Pad. For the LFCSP, the exposed paddle must be left unconnected.

[1] I = input, S = supply, I/O means input/output, and O = output.

GENERAL DESCRIPTION

The ADuC845, ADuC847, and ADuC848 are single-cycle, 12.58 MIPs, 8052 core upgrades to the ADuC834 and ADuC836. They include additional analog inputs for applications requiring more ADC channels.

The ADuC845, ADuC847, and ADuC848 are complete smart transducer front ends. The family integrates high resolution Σ-Δ ADCs with flexible, up to 10-channel, input multiplexing, a fast 8-bit MCU, and program and data Flash/EE memory on a single chip.

The ADuC845 includes two (primary and auxiliary) 24-bit Σ-Δ ADCs with internal buffering and PGA on the primary ADC. The ADuC847 includes the same primary ADC as the ADuC845 (auxiliary ADC removed). The ADuC848 is a 16-bit ADC version of the ADuC847.

The ADCs incorporate flexible input multiplexing, a temperature sensor (ADuC845 only), and a PGA (primary ADC only) allowing direct measurement of low-level signals. The ADCs include on-chip digital filtering and programmable output data rates that are intended for measuring wide dynamic range and low frequency signals, such as those in weigh scale, strain gage, pressure transducer, or temperature measurement applications.

The devices operate from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The micro-controller core is an optimized single-cycle 8052 offering up to 12.58 MIPs performance while maintaining 8051 instruction set compatibility.

The available nonvolatile Flash/EE program memory options are 62 kbytes, 32 kbytes, and 8 kbytes. 4 kbytes of nonvolatile Flash/EE data memory and 2304 bytes of data RAM are also provided on-chip. The program memory can be configured as data memory to give up to 60 kbytes of NV data memory in data logging applications.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the $\overline{EA}$ pin. The ADuC845, ADuC847, and ADuC848 are supported by the QuickStart™ development system featuring low cost software and hardware development tools.

NOTES
1. THE PIN NUMBERS REFER TO THE LFCSP PACKAGE ONLY.

Figure 4. Detailed Block Diagram of the ADuC845

NOTES
1. THE PIN NUMBERS REFER TO THE LFCSP PACKAGE ONLY.

Figure 5. Detailed Block Diagram of the ADuC847

Figure 6. Detailed Block Diagram of the ADuC848

8052 INSTRUCTION SET

Table 4 documents the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles resulting in 12.58 MIPs peak performance when operating at PLLCON = 00H.

TIMER OPERATION

Timers on a standard 8052 increment by one with each machine cycle. On the ADuC845, ADuC847, and ADuC848, one machine cycle is equal to one clock cycle; therefore, the timers increment at the same rate as the core clock.

ALE

On the ADuC834, the output on the ALE pin is a clock at 1/6th of the core operating frequency. On the ADuC845, ADuC847, and ADuC848, the ALE pin operates as follows. For a single machine cycle instruction, ALE is high for the entire machine cycle. For a two or more machine cycle instruction, ALE is high for the first machine cycle and then low for the remainder of the machine cycles.

EXTERNAL MEMORY ACCESS

The ADuC845, ADuC847, and ADuC848 do not support external program memory access, but the devices can access up to 16 MB (24 address bits) of external data memory. When accessing external RAM, the EWAIT register might need to be programmed to give extra machine cycles to MOVX commands to allow differing external RAM access speeds.

COMPLETE SFR MAP

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RS1 D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH 0	PT0 B9H 0	PX0 B8H 0	BITS
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	TI 99H 0	RI 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON F8H 05H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	I2CADD1 F2H 7FH	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	GN0L[2] E9H xxH	GN0M[2] EAH xxH	GN0H[2] EBH xxH	GN1L[2] ADuC845 ONLY ECH xxH	GN1H[2] ADuC845 ONLY EDH xxH	RESERVED	RESERVED
ACC E0H 00H	OF0L E1H xxH	OF0M E2H xxH	OF0H E3H xxH	OF1L ADuC845 ONLY E4H xxH	OF1H ADuC845 ONLY E5H xxH	ADC0CON2 E6H 00H	RESERVED
ADCSTAT D8H 00H	ADC0L NOT AVAILABLE ON ADuC848 D9H 00H	ADC0M DAH 00H	ADC0H DBH 00H	ADC1M ADuC845 ONLY DCH 00H	ADC1H ADuC845 ONLY DDH 00H	ADC1L ADuC845 ONLY DEH 00H	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 08H	ADC0CON1 D2H 07H	ADC1CON ADuC845 ONLY D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 53H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H A0H	RESERVED	RESERVED	RESERVED	EDARL C6H 00H	EDARH C7H 00H
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	RESERVED	RESERVED	SPH B7H 00H
IE A8H 00H	IEIP2 A9H A 0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG845/7/8 AFH 00H
P2 A0H FFH	TIMECON A1H 00H	HTHSEC[1] A2H 00H	SEC[1] A3H 00H	MIN[1] A4H 00H	HOUR[1] A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SCON 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	RESERVED	T3FD 9DH 00H	T3CON 9EH 00H	EWAIT 9FH 00H
P1 90H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

[1] THESE SFRs MAINTAIN THEIR PRE-RESET VALUES AFTER A RESET IF TIMECON.0 = 1.
[2] CALIBRATION COEFFICIENTS ARE PRECONFIGURED ON POWER-UP TO FACTORY CALIBRATED VALUES.

SFR MAP KEY:

SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT ADDRESSABLE.

04741-073

Figure 7. Complete SFR Map for the ADuC845, ADuC847, and ADuC848

FUNCTIONAL DESCRIPTION

8051 INSTRUCTION SET

Table 4. Optimized Single-Cycle 8051 Instruction Set

Mnemonic	Description	Bytes	Cycles[1]
Arithmetic			
A A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carry	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @Ri	Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	4
DIV AB	Divide A by B	1	9
DA A	Decimal adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3
XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,dir	Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1

Mnemonic	Description	Bytes	Cycles[1]
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX[2] A,@Ri	Move external (A8) data to A	1	4
MOVX[2] A,@DPTR	Move external (A16) data to A	1	4
MOVX[2] @Ri,A	Move A to external data (A8)	1	4
MOVX[2] @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3

Mnemonic	Description	Bytes	Cycles[1]
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator ! = 0	2	3
DJNZ Rn,rel	Decrement register, JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL[3] addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

[1] One cycle is one clock.
[2] MOVX instructions are four cycles when they have 0 wait state. Cycles of MOVX instructions are 4 + *n* cycles when they have *n* wait states as programmed via EWAIT.
[3] LCALL instructions are three cycles when the LCALL instruction comes from an interrupt.

MEMORY ORGANIZATION

The ADuC845, ADuC847, and ADuC848 contain four memory blocks:

- 62 kbytes/32 kbytes/8 kbytes of on-chip Flash/EE program memory
- 4 kbytes of on-chip Flash/EE data memory
- 256 bytes of general-purpose RAM
- 2 kbytes of internal XRAM

Flash/EE Program Memory

The devices provide up to 62 kbytes of Flash/EE program memory to run user code. All further references to Flash/EE program memory assume the 62-kbyte option.

When $\overline{EA}$ is pulled high externally during a power cycle or a hardware reset, the devices default to code execution from their internal 62 kbytes of Flash/EE program memory. The devices do not support the rollover from internal code space to external code space. No external code space is available on the devices. Permanently embedded firmware allows code to be serially downloaded to the 62 kbytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

During run time, 56 kbytes of the 62-kbyte program memory can be reprogrammed. This means that the code space can be upgraded in the field by using a user-defined protocol running on the devices, or it can be used as a data memory. For details, see the Nonvolatile Flash/EE Memory Overview section.

Flash/EE Data Memory

The user has 4 kbytes of Flash/EE data memory available that can be accessed indirectly by using a group of registers mapped into the special function register (SFR) space. For details, see the Nonvolatile Flash/EE Memory Overview section.

General-Purpose RAM

The general-purpose RAM is divided into two separate memories, the upper and the lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing. The upper 128 bytes of RAM can be accessed only through indirect addressing because it shares the same address space as the SFR space, which must be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 8. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 to R7. The next 16 bytes (128 bits), locations 20H to 2FH above the register banks, form a block of directly addressable bit locations at Bit Addresses 00H to 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

Reset initializes the stack pointer to location 07H. Any call or push pre-increments the SP before loading the stack. Therefore, loading the stack starts from location 08H, which is also the first register (R0) of Register Bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

Figure 8. Lower 128 Bytes of Internal Data Memory

Internal XRAM

The ADuC845, ADuC847, and ADuC848 contain 2 kbytes of on-chip extended data memory. This memory, although on-chip, is accessed via the MOVX instruction. The 2 kbytes of internal XRAM are mapped into the bottom 2 kbytes of the external address space if the CFG84x.0 (Table 7) bit is set; otherwise, access to the external data memory occurs just like a standard 8051.

Even with the CFG84x.0 bit set, access to the external (off chip), XRAM occurs once the 24-bit DPTR is greater than 0007FFH.

Figure 9. Internal and External XRAM

When enabled and when accessing the internal XRAM, the P0 and P2 port pin operations, as well as the $\overline{RD}$ and $\overline{WR}$ strobes, do not operate as a standard 8051 MOVX instruction. This allows the user to use these port pins as standard I/O. The internal XRAM can be configured as part of the extended 11-bit stack pointer. By default, the stack operates exactly like an 8052 in that it rolls over from FFH to 00H in the general-purpose RAM. On the ADuC845, ADuC847, and ADuC848, however, it is possible (by setting CFG845.7/ADuC847.7/ADuC848.7) to enable the 11-bit extended stack pointer. In this case, the stack rolls over from FFH in RAM to 0100H in XRAM.

The 11-bit stack pointer is visible in the SPH and SP SFRs. The SP SFR is located at 81H as with a standard 8052. The SPH SFR is located at B7H. The 3 LSBs of the SPH SFR contain the 3 extra bits necessary to extend the 8-bit stack pointer in the SP SFR into an 11-bit stack pointer.

Figure 10. Extended Stack Pointer Operation

External Data Memory (External XRAM)

There is no support for external program memory access to the devices. However, just like a standard 8051-compatible core, the ADuC845/ADuC847/ADuC848 can access external data memory using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory. The devices, however, can access up to 16 Mbytes of external data memory. This is an enhancement of the 64 kbytes of external data memory space available on a standard 8051-compatible core. See the Hardware Design Considerations section for details.

When accessing external RAM, the EWAIT register might need to be programmed to give extra machine cycles to the MOVX operation. This is to account for differing external RAM access speeds.

EWAIT SFR

SFR Address:	9FH
Power-On Default:	00H
Bit Addressable:	No

This special function register (SFR), when programmed, dictates the number of wait states for the MOVX instruction. The value can vary between 0H and 7H. The MOVX instruction increases by one machine cycle (4 + *n*, where *n* = EWAIT number in decimal) for every increase in the EWAIT value.

SPECIAL FUNCTION REGISTERS (SFRs)

The SFR space is mapped into the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC845/ADuC847/ADuC848 via the SFR area is shown in Figure 11.

All registers except the program counter (PC) and the four general-purpose register banks reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

Figure 11. Programming Model

Accumulator SFR (ACC)

ACC is the accumulator register, which is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions usually refer to the accumulator as A.

B SFR (B)

The B register is used with the accumulator for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratch pad register.

Data Pointer (DPTR)

The data pointer is made up of three 8-bit registers: DPP (page byte), DPH (high byte), and DPL (low byte). These provide memory addresses for internal code and data memory access. The DPTR can be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).

The ADuC845/ADuC847/ADuC848 support dual data pointers. See the Dual Data Pointers section.

Stack Pointer (SP and SPH)

The SP SFR is the stack pointer, which is used to hold an internal RAM address called the *top of the stack*. The SP register is incremented before data is stored during PUSH and CALL executions. Although the stack can reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

As mentioned earlier, the devices offer an extended 11-bit stack pointer. The three extra bits needed to make up the 11-bit stack pointer are the three LSBs of the SPH byte located at B7H. To enable the SPH SFR, the EXSP (CFG84x.7) bit must be set; otherwise, the SPH SFR can be neither written to nor read from.

Program Status Word (PSW)

The PSW SFR contains several bits that reflect the current status of the CPU as listed in Table 5.

SFR Address: D0H
Power-On Default: 00H
Bit Addressable: Yes

Table 5. PSW SFR Bit Designations

Bit No.	Name	Description
7	CY	Carry Flag.
6	AC	Auxiliary Carry Flag.
5	F0	General-Purpose Flag.
4, 3	RS1, RS0	Register Bank Select Bits. RS1 RS0 Selected Bank 0 0 0 0 1 1 1 0 2 1 1 3
2	OV	Overflow Flag.
1	F1	General-Purpose Flag.
0	P	Parity Bit.

Power Control Register (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags as listed in Table 6.

SFR Address: 87H
Power-On Default: 00H
Bit Addressable: No

Table 6. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate. 0 = Normal, 1 = Double Baud Rate.
6	SERIPD	Serial Power-Down Interrupt Enable. If this bit is set, a serial interrupt from either SPI or I^2C can terminate the power-down mode.
5	INT0PD	INT0 Power-Down Interrupt Enable. If this bit is set, either a level ($\overline{IT0}$ = 0) or a negative-going transition ($\overline{IT0}$ = 1) on the INT0 pin terminates power-down mode.
4	ALEOFF	If set to 1, the ALE output is disabled.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable. If set to 1, the device enters power-down mode.
0	-----	Not Implemented. Write Don't Care.

ADuC845/ADuC847/ADuC848 Configuration Register (CFG845/CFG847/CFG848)

The CFG845/CFG847/CFG848 SFR contains the bits necessary to configure the internal XRAM and the extended SP. By default, it configures the user into 8051 mode, that is, extended SP, and the internal XRAM are disabled. When using in a program, use the device name only, that is, CFG845, CFG847, or CFG848.

SFR Address: AFH
Power-On Default: 00H
Bit Addressable: No

Table 7. CFG845/CFG847/CFG848 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1, the stack rolls over from SPH/SP = 00FFH to 0100H. If this bit is cleared to 0, SPH SFR is disabled and the stack rolls over from SP = FFH to SP = 00H.
6	----	Not Implemented. Write Don't Care.
5	----	Not Implemented. Write Don't Care.
4	----	Not Implemented. Write Don't Care.
3	----	Not Implemented. Write Don't Care.
2	----	Not Implemented. Write Don't Care.
1	----	Not Implemented. Write Don't Care.
0	XRAMEN	If this bit is set to 1, the internal XRAM is mapped into the lower 2 kbytes of the external address space. If this bit is cleared to 0, the internal XRAM is accessible and up to 16 MB of external data memory become available. See Figure 8.

ADC CIRCUIT INFORMATION

The ADuC845 incorporates two 10-channel (8-channel on the MQFP package) 24-bit Σ-Δ ADCs, while the ADuC847 and ADuC848 each incorporate a single 10-channel (8-channel on the MQFP package) 24-bit and 16-bit Σ-Δ ADC.

Each device also includes an on-chip programmable gain amplifier and configurable buffering (neither is available on the auxiliary ADC on the ADuC845). The devices also incorporate digital filtering intended for measuring wide dynamic range and low frequency signals such as those in weigh-scale, strain-gage, pressure transducer, or temperature measurement applications.

The ADuC845/ADuC847/ADuC848 can be configured as four or five (MQFP/LFCSP package) fully-differential input channels or as eight or ten (MQFP/LFCSP package) pseudo differential input channels referenced to AINCOM. The ADC on each device (primary only on the ADuC845) can be fully buffered internally, and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V (V_{REF} × 1.024). Buffering the input channel means that the device can handle significant source impedances on the selected analog input and that RC filtering (for noise rejection or RFI reduction) can be placed on the analog inputs. If the ADC is used with internal buffering disabled (ADC0CON1.7 = 1, ADC0CON1.6 = 0), these un-buffered inputs provide a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the inputs can cause dc gain errors, depending on the output impedance of the source that is driving the ADC inputs.

Table 8 and Table 9 show the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 16-bit and 20-bit levels, respectively, is introduced. When used with internal buffering enabled, it is recommended that a capacitor (10 nF to 100 nF) be placed on the input to the ADC (usually as part of an antialiasing filter) to aid in noise performance.

The input channels are intended to convert signals directly from sensors without the need for external signal conditioning. With internal buffering disabled (relevant bits set/cleared in ADC0CON1), external buffering might be required.

When the internal buffer is enabled, it might be necessary to offset the negative input channel by +100 mV and to offset the positive channel by −100 mV if the reference range is AV_{DD}. This accounts for the restricted common-mode input range in the buffer. Some circuits, for example, bridge circuits, are inherently suitable to use without having to offset where the output voltage is balanced around $V_{REF}/2$ and is not sufficiently large to encroach on the supply rails. Internal buffering is not available on the auxiliary ADC (ADuC845 only). The auxiliary ADC (ADuC845 only) is fixed at a gain range of ±2.50 V.

The ADCs use a Σ-Δ conversion technique to realize up to 24 bits on the ADuC845 and the ADuC847, and up to 16 bits on the ADuC848 of no missing codes performance (20 Hz update rate, chop enabled). The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $sinc^3$ programmable low-pass filter (see Table 28) is then used to decimate the modulator output data stream to give a valid data conversion result at programmable output rates. The signal chain has two modes of operation, chop enabled and chop disabled. The $\overline{CHOP}$ bit in the ADCMODE register enables or disables the chopping scheme.

Table 8. Maximum Resistance for No 16-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	111.3 kΩ	27.8 kΩ	16.7 kΩ	4.5 kΩ	2.58 kΩ	700 Ω
2	53.7 kΩ	13.5 kΩ	8.1 kΩ	2.2 kΩ	1.26 kΩ	360 Ω
4	25.4 kΩ	6.4 kΩ	3.9 kΩ	1.0 kΩ	600 Ω	170 Ω
8–128	10.7 kΩ	2.9 kΩ	1.7 kΩ	480 Ω	270 Ω	75 Ω

Table 9. Maximum Resistance for No 20-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	84.9 kΩ	21.1 kΩ	12.5 kΩ	3.2 kΩ	1.77 kΩ	440 Ω
2	42.0 kΩ	10.4 kΩ	6.1 kΩ	1.6 kΩ	880 Ω	220 Ω
4	20.5 kΩ	5.0 kΩ	2.9 kΩ	790 Ω	430 Ω	110 Ω
8–128	8.8 kΩ	2.3 k Ω	1.3 k Ω	370 Ω	195 Ω	50 Ω

Signal Chain Overview (Chop Enabled, $\overline{CHOP}$ = 0)

With the $\overline{CHOP}$ bit = 0 (see the ADCMODE SFR bit designations in Table 24), the chopping scheme is enabled. This is the default condition and gives optimum performance in terms of offset errors and drift performance. With chop enabled, the available output rates vary from 5.35 Hz to 105 Hz (SF = 255 and 13, respectively). A typical block diagram of the ADC input channel with chop enabled is shown in Figure 12.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band limited, low noise output from the ADCs.

The ADC filter is a low-pass $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the Sinc filter word loaded into the filter (SF) register (see Table 28). The complete signal chain is chopped, resulting in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important.

With chop enabled, the ADC repeatedly reverses its inputs. The decimated digital output words from the $Sinc^3$ filter, therefore, have a positive offset and a negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register. Programming the $Sinc^3$ decimation factor is restricted to an 8-bit register called SF (see Table 28), the actual decimation factor is the register value times 8. Therefore, the decimated output rate from the $Sinc^3$ filter (and the ADC conversion rate) is

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The chop rate of the channel is half the output data rate:

$$f_{CHOP} = \frac{1}{2 \times f_{ADC}}$$

As shown in the block diagram (Figure 12), the $Sinc^3$ filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset.

Figure 12. Block Diagram of the ADC Input Channel with Chop Enabled

This offset is removed by performing a running average of 2. This average by 2 means that the settling time to any change in programming of the ADC is twice the normal conversion time, while an asynchronous step change on the analog input is not fully reflected until the third subsequent output. See Figure 13.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF (chop enabled) is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, rms and peak-to-peak noise performances are shown in Table 10, Table 11, Table 12, and Table 13. The numbers are typical and generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. Note that the conversion time increases by 0.732 ms for each increment in SF.

Figure 13. ADC Settling Time Following a Synchronous Change with Chop Enabled

Figure 14. ADC Settling Time Following an Asynchronous Change with Chop Enabled

ADC Noise Performance with Chop Enabled ($\overline{CHOP}$ = 0)

Table 10, Table 11, Table 12, and Table 13 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates for the ADuC845, ADuC847, and ADuC848. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are in the same range as the bipolar figures, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution.

Table 10. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	**Data Update Rate (Hz)**	**±20 mV**	**±40 mV**	**±80 mV**	**±160 mV**	**±320 mV**	**±640 mV**	**±1.28 V**	**±2.56 V**
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 11. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	**Data Update Rate (Hz)**	**±20 mV**	**±40 mV**	**±80 mV**	**±160 mV**	**±320 mV**	**±640 mV**	**±1.28 V**	**±2.56 V**
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16.5	16.5	17	16.5
27	50.56	12.5	13.5	15	16	16.5	17	17	17.5
69	19.79	13	14	15.5	16	17.5	17.5	18	18
255	5.35	14.5	15	16	17	18	18.5	19	19.5

Table 12. ADuC848 Typical Output Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	**Data Update Rate (Hz)**	**±20 mV**	**±40 mV**	**±80 mV**	**±160 mV**	**±320 mV**	**±640 mV**	**±1.28 V**	**±2.56 V**
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 13. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	**Data Update Rate (Hz)**	**±20 mV**	**±40 mV**	**±80 mV**	**±160 mV**	**±320 mV**	**±640 mV**	**±1.28 V**	**±2.56 V**
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16	16	17	16
27	50.56	12.5	13.5	15	16	16	16	16	16
69	19.79	13	14	15.5	16	16	16	16	16
255	5.35	14.5	15	16	16	16	16	16	16

Signal Chain Overview with Chop Disabled ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ = 1, chop is disabled and the available output rates vary from 16.06 Hz to 1.365 kHz. The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is higher than when chop is enabled. The drawback with chop disabled is that the drift performance is degraded and offset calibration is required following a gain range change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 15.

The signal chain includes a multiplex or buffer, PGA, Σ-Δ modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. Programming the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is therefore

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change requires a settling time of three times the programmed update rate; a channel change can be treated as a synchronized step change. This is one conversion longer than the case for chop enabled. However, because the ADC throughput is three times faster with chop disabled than it is with chop enabled, the actual time to a settled ADC output is significantly less also. This means that following a synchronized step change, the ADC requires three conversions (note: data is not output following a synchronized ADC change until data has settled) before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change requires four conversions to accurately reflect the new analog input at its output. Note that with an unsynchronized change the ADC continues to output data and so the user must take unsettled outputs into account. Again, this is one conversion longer than with chop enabled, but because the ADC throughput with chop disabled is faster than with chop enabled, the actual time taken to obtain a settled ADC output is less.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, rms, and peak-to-peak noise performances are shown in Table 14, Table 15, Table 16, and Table 17. Note that the conversion time increases by 0.244 ms for each increment in SF.

Figure 15. Block Diagram of ADC Input Channel with Chop Disabled

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24})$ = 152.6 nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(\pm 640\ mV)/2^{24})$ = 76.3 nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

(see Table 30). These burnout current sources are also available only with buffering enabled via the BUF0/BUF1 bits in the ADC0CON1 SFR. Once the burnout currents are turned on, a current flows in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. When the resulting voltage measured is full scale, the transducer has gone open circuit. When the voltage measured is 0 V, this indicates that the transducer has gone short circuit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE DETECT CIRCUIT

The main and auxiliary (ADuC845 only) ADCs can be configured to allow the use of the internal band gap reference or an external reference that is applied to the REFIN± pins by means of the XREF0/1 bit in the Control Registers AD0CON2 and AD1CON (ADuC845 only). A reference detection circuit is provided to detect whether a valid voltage is applied to the REFIN± pins. This feature arose in connection with strain-gage sensors in weigh scales where the reference and signal are provided via a cable from the remote sensor. It is desirable to detect whether the cable is disconnected. If either of the pins is floating or if the applied voltage is below a specified threshold, a flag (NOXREF) is set in the ADC status register (ADCSTAT), conversion results are clamped, and calibration registers are not updated if a calibration is in progress.

Note that the reference detect does not look at REFIN2± pins.

If, during either an offset or gain calibration, the NOEXREF bit becomes active, indicating an incorrect V_{REF}, updating the relevant calibration register is inhibited to avoid loading incorrect data into these registers, and the appropriate bits in ADCSTAT (ERR0 or ERR1) are set. If the user needs to verify that a valid reference is in place every time a calibration is performed, the status of the ERR0 and ERR1 bits should be checked at the end of every calibration cycle.

SINC FILTER REGISTER (SF)

The number entered into the SF register sets the decimation factor of the $Sinc^3$ filter for the ADC. See Table 28 and Table 29.

The range of operation of the SF word depends on whether ADC chop is on or off. With chop disabled, the minimum SF word is 3 and the maximum is 255. This gives an ADC throughput rate from 16.06 Hz to 1.365 kHz. With chop enabled, the minimum SF word is 13 (all values lower than 13 are clamped to 13) and the maximum is 255. This gives an ADC throughput rate of 5.4 Hz to 105 Hz. See the f_{ADC} equation in the ADC description preceding section.

An additional feature of the $Sinc^3$ filter is a second notch filter positioned in the frequency response at 60 Hz. This gives simultaneous 60 Hz rejection to whatever notch is defined by the SF filter. This 60 Hz filter is enabled via the REJ60 bit in the ADCMODE register (ADCMODE.6). The notch is valid only for SF words ≥ 68; otherwise, ADC errors occur, and, the notch is best used with an SF word of 82d giving simultaneous 50 Hz and 60 Hz rejection. This function is useful only with an ADC clock (modulator rate) of 32.768 kHz. During calibration, the current (user-written) value of the SF register is used.

Σ-Δ MODULATOR

A Σ-Δ ADC usually consists of two main blocks, an analog modulator, and a digital filter. For the ADuC845/ADuC847/ADuC848, the analog modulator consists of a difference amplifier, an integrator block, a comparator, and a feedback DAC as shown in Figure 16.

Figure 16. Σ-Δ Modulator Simplified Block Diagram

In operation, the analog signal is fed to the difference amplifier along with the output from the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output from the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data-word by using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (that results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

DIGITAL FILTER

The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the device.

The ADuC845/ADuC847/ADuC848 filter is a low-pass, $Sinc^3$ or $[(SINx)/x]^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc filter) SFR as listed in Table 28 and Table 29.

Figure 22, Figure 23, Figure 24, and Figure 25 show the frequency response of the ADC, yielding an overall output rate of 16.6 Hz with chop enabled and 50 Hz with chop disabled. Also detailed in these plots is the effect of the fixed 60 Hz drop-in notch filter

(REJ60 bit, ADCMODE.6). This fixed filter can be enabled or disabled by setting or clearing the REJ60 bit in the ADCMODE register (ADCMODE.6). This 60 Hz drop-in notch filter can be enabled for any SF word that yields an ADC throughput that is less than 20 Hz with chop enabled (SF ≥ 68 decimal).

ADC CHOPPING

The ADCs on the ADuC845/ADuC847/ADuC848 implement a chopping scheme whereby the ADC repeatedly reverses its inputs. The decimated digital output words from the $Sinc^3$ filter, therefore, have a positive and negative offset term included. As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. The ADC throughput or update rate is listed in Table 29. The chopping scheme incorporated into the devices results in excellent dc offset and offset drift specifications, and is extremely beneficial in applications where drift, noise rejection, and optimum EMI performance are important. ADC chop can be disabled via the chop bit in the ADCMODE SFR (ADCMODE.3). Setting this bit to 1 (logic high) disables chop mode.

CALIBRATION

The ADuC845/ADuC847/ADuC848 incorporate four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table 24. Every device is calibrated before it leaves the factory. The resulting offset and gain calibration coefficients for both the primary and auxiliary (ADuC845 only) ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on or after a reset, these factory calibration registers are automatically downloaded to the ADC calibration registers in the SFR space of the device. To facilitate user calibration, each of the primary and auxiliary (ADuC845 only) ADCs have dedicated calibration control SFRs, which are described in the ADC SFR Interface section. Once a user initiates a calibration procedure, the factory calibration values that were initially downloaded during the power-on sequence to the ADC calibration SFRs are overwritten. The ADC to be calibrated must be enabled via the ADC enable bits in the ADCMODE register.

Even though an internal offset calibration mode is described in this section, note that the ADCs can be chopped. This chopping scheme inherently minimizes offset errors and means that an offset calibration should never be required. Also, because factory 5 V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration is required only if the device is operated at 3 V or at temperatures significantly different from 25°C.

If the device is operated in chop disabled mode, a calibration may need to be done with every gain range change that occurs via the PGA.

The ADuC845/ADuC847/ADuC848 each offer internal or system calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two input conditions: zero-scale and full-scale points. These points are derived by performing a conversion on the different input voltages (zero-scale and full-scale) provided to the input of the modulator during calibration. The result of the zero-scale calibration conversion is stored in the offset calibration registers for the appropriate ADC. The result of the full-scale calibration conversion is stored in the gain calibration registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an internal zero-scale or full-scale calibration, the respective zero-scale input or full-scale input is automatically connected to the ADC inputs internally. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied externally to the ADC pins by the user before the calibration mode is initiated. In this way, external errors are taken into account and minimized. Note that all ADuC845/ADuC847/ADuC848 ADC calibrations are carried out at the user-selected SF word update rate. To optimize calibration accuracy, it is recommended that the slowest possible update rate be used.

Internally in the devices, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.

From an operational point of view, a calibration should be treated just like an ordinary ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine the end of calibration by using a polling sequence or an interrupt driven routine. If required, the NOEXREF0/1 bits can be monitored to detect unconnected or low voltage errors in the reference during conversion. In the event of the reference becoming disconnected, causing a NOXREF flag during a calibration, the calibration is immediately halted and no write to the calibration SFRs takes place.

Internal Calibration Example

With chop enabled, a zero-scale or offset calibration should never be required, although a full-scale or gain calibration may be required. However, if a full internal calibration is required, the procedure should be to select a PGA gain of 1 (±2.56 V) and perform a zero-scale calibration (MD2...0 = 100B in the ADCMODE register). Next, select and perform full-scale calibration by setting MD2...0 = 101B in the ADCMODE SFR. Now select the desired PGA range and perform a zero-scale calibration again (MD2..0 = 100B in ADCMODE) at the new PGA range. The reason for the double zero-scale calibration is

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

Figure 17. Unipolar and Bipolar Channel Pairs

DATA OUTPUT CODING

When the primary ADC is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential input voltage resulting in a code of 000...000, a midscale voltage resulting in a code of 100...000, and a full-scale voltage resulting in a code of 111...111. The output code for any analog input voltage on the main ADC can be represented as follows:

$$Code - (AIN \times GAIN \times 2^N)/(1.024 \times V_{REF})$$

where:

AIN is the analog input voltage.
GAIN is the PGA gain setting, that is, 1 on the 2.56 V range and 128 on the 20 mV range, and $N = 24$ (16 on the ADuC848).

The output code for any analog input voltage on the auxiliary ADC can be represented as follows:

$$Code = (AIN \times 2^N)/(V_{REF})$$

with the same definitions as used for the primary ADC above.

When the primary ADC is configured for bipolar operation, the coding is offset binary with negative full-scale voltage resulting in a code of 000...000, a zero differential voltage resulting in a code of 800…000, and a positive full-scale voltage resulting in a code of 111...111. The output from the primary ADC for any analog input voltage can be represented as follows:

$$Code = 2^{N-1}[(AIN \times GAIN)/(1.024 \times V_{REF}) + 1]$$

where:

AIN is the analog input voltage.
GAIN is the PGA gain, that is, 1 on the ±2.56 V range and 128 on the ±20 mV range.
$N = 24$ (16 on the ADuC848).

The output from the auxiliary ADC in bipolar mode can be represented as follows:

$$Code = 2^{N-1}\ [(AIN/V_{REF}) + 1]$$

EXCITATION CURRENTS

The ADuC845/ADuC847/ADuC848 contain two matched, software-configurable 200 µA current sources. Both source current from AV_{DD}, which is directed to either or both of the IEXC1 (Pin 11 whose alternate functions are P1.6/AIN7) or IEXC2 (Pin 12, whose alternate functions are P1.7/AIN8) pins on the device. These currents are controlled via the lower four bits in the ICON register (Table 30). These bits not only enable the current sources but also allow the configuration of the currents such that 200 µA can be sourced individually from both pins or can be combined to give a 400 µA source from one or the other of the outputs. These sources can be used to excite external resistive bridge or RTD sensors (see Figure 71).

ADC POWER-ON

The ADC typically takes 0.5 ms to power up from an initial start-up sequence or following a power-down event.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 18. Filter Response, Chop On, SF = 69 Decimal

Figure 19. Filter Response, Chop On, SF = 255 Decimal

Figure 20. 50 Hz Normal Mode Rejection vs. SF Word, Chop On

Figure 21. 60 Hz Normal Mode Rejection vs. SF, Chop On

Figure 22. Chop Off, Fadc = 50 Hz, SF = 52H

Figure 23. Chop Off, SF = 52H, REJ60 Enabled

Figure 24. Chop On, Fadc = 16.6 Hz, SF = 52H

Figure 25. Chop On, Fadc = 16.6 Hz, SF = 52H, REJ60 Enabled

FUNCTIONAL DESCRIPTION

ADC SFR INTERFACE

The ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following sections.

Table 22. ADC SFR Interface

Name	Description
ADCSTAT	ADC Status Register. Holds the general status of the primary and auxiliary (ADuC845 only) ADCs.
ADCMODE	ADC Mode Register. Controls the general modes of operation for primary and auxiliary (ADuC845 only) ADCs.
ADC0CON1	Primary ADC Control Register 1. Controls the specific configuration of the primary ADC.
ADC0CON2	Primary ADC Control Register 2. Controls the specific configuration of the primary ADC.
ADC1CON	Auxiliary ADC Control Register. Controls the specific configuration of the auxiliary ADC. ADuC845 only.
SF	Sinc Filter Register. Configures the decimation factor for the $Sinc^3$ filter and, therefore, the primary and auxiliary (ADuC845 only) ADC update rates.
ICON	Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H	Primary ADC 24-bit (16-bit on the ADuC848) conversion result is held in these three 8-bit registers. ADC0L is not available on the ADuC848.
ADC1L/M/H	Auxiliary ADC 24-bit conversion result is held in these two 8-bit registers. ADuC845 only.
OF0L/M/H	Primary ADC 24-bit offset calibration coefficient is held in these three 8-bit registers. OF0L is not available on the ADuC848.
OF1L/H	Auxiliary ADC 16-bit offset calibration coefficient is held in these two 8-bit registers. ADuC845 only.
GN0L/M/H	Primary ADC 24-bit gain calibration coefficient is held in these three 8-bit registers. GN0L is not available on the ADuC848.
GN1L/H	Auxiliary ADC 16-bit gain calibration coefficient is held in these two 8-bit registers. ADuC845 only.

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

ADCMODE (ADC MODE REGISTER)

Used to control the operational mode of both ADCs.

SFR Address: D1H
Power-On Default: 08H
Bit Addressable: No

Table 24. ADCMODE SFR Bit Designations

Bit No.	Name	Description
7	---	Not Implemented. Write Don't Care.
6	REJ60	Automatic 60 Hz Notch Select Bit. Setting this bit places a notch in the frequency response at 60 Hz, allowing simultaneous 50 Hz and 60 Hz rejection at an SF word of 82 decimal. This 60 Hz notch can be set only if SF ≥68 decimal, that is, the regular filter notch must be ≤60 Hz. This second notch is placed at 60 Hz only if the device clock is at 32.768 kHz.
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the primary ADC into power-down mode.
4	ADC1EN (ADuC845 only)	Auxiliary (ADuC845 only) ADC Enable. Set by the user to enable the auxiliary (ADuC845 only) ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the auxiliary (ADuC845 only) ADC in power-down mode.
3	$\overline{\text{CHOP}}$	Chop Mode Disable. Set by the user to disable chop mode on both the primary and auxiliary (ADuC845 only) ADC allowing a three times higher ADC data throughput. SF values as low as 3 are allowed with this bit set, giving up to 1.3 kHz ADC update rates. Cleared by the user to enable chop mode on both the primary and auxiliary (ADuC845 only) ADC.
2, 1, 0	MD2, MD1, MD0	Primary and Auxiliary (ADuC845 only) ADC Mode Bits. These bits select the operational mode of the enabled ADC as follows: MD2 MD1 MD0 0 0 0 ADC Power-Down Mode (Power-On Default). 0 0 1 Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode. In single conversion mode, a single conversion is performed on the enabled ADC. Upon completion of a conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/M/L (ADuC845 only)) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. Note that ADC0L is not available on the ADuC848. 0 1 1 Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see the Sinc Filter SFR Bit Designations in Table 28). 1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s). 1 0 1 Internal Full-Scale Calibration. Internal or external REFIN± or REFIN2± V_{REF} (as determined by XREF bits in ADC0CON2 and/or AXREF (ADuC845 only) in ADC1CON (ADuC845 only) is automatically connected to the enabled ADC input(s) for this calibration. 1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers. 1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers.

Notes on the ADCMODE Register

Any change to the MD bits immediately resets both ADCs (auxiliary ADC only applicable to the ADuC845). A write to the MD2–MD0 bits with no change in contents is also treated as a reset. (See the exception to this in the third note of this section.)

If ADC1CON1 and ADC1CON2 are written when ADC0EN = 1, or if ADC0EN is changed from 0 to 1, both ADCs are also immediately reset. In other words, the primary ADC is given priority over the auxiliary ADC and any change requested on the primary ADC is immediately responded to. Only applicable to the ADuC845.

On the other hand, if ADC1CON is written to or if ADC1EN is changed from 0 to 1, only the auxiliary ADC is reset. For example, if the primary ADC is continuously converting when the auxiliary ADC change or enable occurs, the primary ADC continues undisturbed. Rather than allow the auxiliary ADC to operate with a phase difference from the primary ADC, the auxiliary ADC falls into step with the outputs of the primary ADC. The result is that the first conversion time for the auxiliary ADC is delayed by up to three outputs while the auxiliary ADC update rate is synchronized to the primary ADC. Only applicable to ADuC845. If the ADC1CON write occurs after the primary ADC has completed its operation, the auxiliary ADC can respond immediately without having to fall into step with the primary ADCs output cycle.

If the devices are powered down via the PD bit in the PCON register, the current ADCMODE bits are preserved, that is, they are not reset to default state. Upon a subsequent resumption of normal operating mode, the ADCs restarts the selected operation defined by the ADCMODE register.

Once ADCMODE has been written with a calibration mode, the RDY0/1 (ADuC845 only) bits (ADCSTAT) are reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in ADCSTAT are written, and the MD2–MD0 bits are reset to 000B to indicate that the ADC is back in power-down mode.

Any calibration request of the auxiliary ADC while the temperature sensor is selected fails to complete. Although the RDY1 bit is set at the end of the calibration cycle, no update of the calibration SFRs takes place, and the ERR1 bit is set. ADuC845 only.

Calibrations performed at maximum SF (see Table 28) value (slowest ADC throughput rate) help to ensure optimum calibration.

The duration of a calibration cycle is 2/Fadc for chop-on mode and 4/Fadc for chop-off mode.

ADC0CON1 (PRIMARY ADC CONTROL REGISTER)

ADC0CON1 is used to configure the primary ADC for buffer, unipolar, or bipolar coding, and ADC range configuration.

SFR Address: D2H
Power-On Default: 07H
Bit Addressable: No

Table 25. ADC0CON1 SFR Bit Designations

Bit No.	Name	Description
7, 6	BUF1, BUF0	Buffer Configuration Bits. BUF1 BUF0 Buffer Configuration 0 0 ADC0+ and ADC0− are buffered 0 1 Reserved 1 0 Buffer Bypass 1 1 Reserved
5	UNI	Primary ADC Unipolar Bit. Set by the user to enable unipolar coding; zero differential input results in 000000H output. Cleared by the user to enable bipolar coding; zero differential input results in 800000H output.
4	–––	Not Implemented. Write Don't Care.
3	–––	Not Implemented. Write Don't Care.
2, 1, 0	RN2, RN1, RN0	Primary ADC Range Bits. Written by the user to select the primary ADC input range as follows: RN2 RN1 RN0 Selected primary ADC input range (V_{REF} = 2.5 V) 0 0 0 ±20 mV (0 mV to 20 mV in unipolar mode) 0 0 1 ±40 mV (0 mV to 40 mV in unipolar mode) 0 1 0 ±80 mV (0 mV to 80 mV in unipolar mode) 0 1 1 ±160 mV (0 mV to 160 mV in unipolar mode) 1 0 0 ±320 mV (0 mV to 320 mV in unipolar mode) 1 0 1 ±640 mV (0 mV to 640 mV in unipolar mode) 1 1 0 ±1.28 V (0 V to 1.28 V in unipolar mode) 1 1 1 ±2.56 V (0 V to 2.56 V in unipolar mode)

ADC0CON2 (PRIMARY ADC CHANNEL SELECT REGISTER)

ADC0CON2 is used to select a reference source and channel for the primary ADC.

SFR Address: E6H
Power-On Default: 00H
Bit Addressable: No

Table 26. ADC0CON2 SFR Bit Designations

Bit No.	Name	Description
7, 6	XREF1, XREF0	Primary ADC External Reference Select Bit. Set by the user to enable the primary ADC to use the external reference via REFIN± or REFIN2±. Cleared by the user to enable the primary ADC to use the internal band gap reference (V_{REF} = 1.25 V). XREF1 XREF0 0 0 Internal 1.25 V Reference. 0 1 REFIN± Selected. 1 0 REFIN2± (AIN3/AIN4) Selected. 1 1 Reserved.
5	–––	Not Implemented. Write Don't Care.
4	–––	Not Implemented. Write Don't Care.
3, 2, 1, 0	CH3, CH2, CH1, CH0	Primary ADC Channel Select Bits. Written by the user to select the primary ADC channel as follows: CH3 CH2 CH1 CH0 Selected Primary ADC Input Channel. 0 0 0 0 AIN1–AINCOM 0 0 0 1 AIN2–AINCOM 0 0 1 0 AIN3–AINCOM 0 0 1 1 AIN4–AINCOM 0 1 0 0 AIN5–AINCOM 0 1 0 1 AIN6–AINCOM 0 1 1 0 AIN7–AINCOM 0 1 1 1 AIN8–AINCOM 1 0 0 0 AIN9–AINCOM (LFCSP package only; not a valid selection on the MQFP package) 1 0 0 1 AIN10–AINCOM (LFCSP package only; not a valid selection on the MQFP package) 1 0 1 0 AIN1–AIN2 1 0 1 1 AIN3–AIN4 1 1 0 0 AIN5–AIN6 1 1 0 1 AIN7–AIN8 1 1 1 0 AIN9–AIN10 (LFCSP package only; not a valid selection on the MQFP package) 1 1 1 1 AINCOM–AINCOM

Note that because the reference-detect does not operate on the REFIN2± pair, the REFIN2± pins can go below 1 V.

ADC1CON (AUXILIARY ADC CONTROL REGISTER) (ADUC845 ONLY)

ADC1CON is used to configure the auxiliary ADC for reference, channel selection, and unipolar or bipolar coding. The auxiliary ADC is available only on the ADuC845.

SFR Address: D3H
Power-On Default: 00H
Bit Addressable: No

Table 27. ADC1CON SFR Bit Designations

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	AXREF	Auxiliary (ADuC845 only) ADC External Reference Bit. Set by the user to enable the auxiliary ADC to use the external reference via REFIN±. Cleared by the user to enable the auxiliary ADC to use the internal band gap reference. Auxiliary ADC cannot use the REFIN2± reference inputs.
5	AUNI	Auxiliary (ADuC845 only) ADC Unipolar Bit. Set by the user to enable unipolar coding, that is, zero input results in 000000H output. Cleared by the user to enable bipolar coding, zero input results in 800000H output.
4	–––	Not Implemented. Write Don't Care.
3, 2, 1, 0	ACH3, ACH2, ACH1, ACH0	Auxiliary ADC Channel Select Bits. Written by the user to select the auxiliary ADC channel.

ACH3	ACH2	ACH1	ACH0	Selected Auxiliary ADC Input Range (V_{REF} = 2.5 V).
0	0	0	0	AIN1–AINCOM
0	0	0	1	AIN2–AINCOM
0	0	1	0	AIN3–AINCOM
0	0	1	1	AIN4–AINCOM
0	1	0	0	AIN5–AINCOM
0	1	0	1	AIN6–AINCOM
0	1	1	0	AIN7–AINCOM
0	1	1	1	AIN8–AINCOM
1	0	0	0	AIN9–AINCOM (not a valid selection on the MQFP package)
1	0	0	1	AIN10–AINCOM (not a valid selection on the MQFP package)
1	0	1	0	AIN1–AIN2
1	0	1	1	AIN3–AIN4
1	1	0	0	AIN5–AIN6
1	1	0	1	AIN7–AIN8
1	1	1	0	Temperature Sensor[1]
1	1	1	1	AINCOM–AINCOM

[1] Note the following about the temperature sensor:
When the temperature sensor is selected, user code must select the internal reference via the AXREF bit and clear the AUNI bit (ADC1CON.5) to select bipolar coding.
Chop mode must be enabled for correct temperature sensor operation.
The temperature sensor is factory calibrated to yield conversion results 800000H at 0°C (ADC chop on).
A +1°C change in temperature results in a +1 LSB change in the ADC1H register ADC conversion result
The temperature sensor is not available on the ADuC847 or ADuC848.

SF (ADC SINC FILTER CONTROL REGISTER)

The SF register is used to configure the decimation factor for the ADC, and therefore, has a direct influence on the ADC throughput rate.

SFR Address: D4H
Power-On Default: 45H
Bit Addressable: No

Table 28. Sinc Filter SFR Bit Designations

SF.7	SF.6	SF.5	SF.4	SF.3	SF.2	SF.1	SF.0
0	1	0	0	0	1	0	1

The bits in this register set the decimation factor of the ADC. This has a direct bearing on the throughput rate of the ADC along with the chop setting. The equations used to determine the ADC throughput rate are

$$Fadc\ (Chop\ On) = \frac{1}{3 \times 8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

$$Fadc\ (Chop\ Off) = \frac{1}{8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

Table 29. SF SFR Bit Examples

Chop Enabled (ADCMODE.3 = 0)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
13[1]	0D	105.3	9.52	19.04
69	45	19.79	50.53	101.1
82	52	16.65	60.06	120.1
255	FF	5.35	186.77	373.54

Chop Disabled (ADCMODE.3 = 1)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
3	03	1365.3	0.73	2.2
69	45	59.36	16.84	50.52
82	52	49.95	20.02	60.06
255	FF	16.06	62.25	186.8

[1] With chop enabled, if an SF word smaller than 13 is written to this SF register, the filter automatically defaults to 13.

During ADC calibration, the user-programmed value of SF word is used. The SF word does not default to the maximum setting (255) as it did on previous MicroConverter® products. However, for optimum calibration results, it is recommended that the maximum SF word be set.

ICON (EXCITATION CURRENT SOURCES CONTROL REGISTER)

The ICON register is used to configure the current sources and the burnout detection source.

SFR Address: D5H
Power-On Default: 00H
Bit Addressable: No

Table 30. Excitation Current Source SFR Bit Designations

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	ICON.6	Burnout Current Enable Bit. When set, this bit enables the sensor burnout current sources on primary ADC channels AIN5/AIN6 or AIN7/AIN8. Not available on any other ADC input pins or on the auxiliary ADC (ADuC845 only).
5	ICON.5	Not Implemented. Write Don't Care.
4	ICON.4	Not Implemented. Write Don't Care.
3	ICON.3	IEXC2 Pin Select. 0 selects AIN8, 1 selects AIN7
2	ICON.2	IEXC1 Pin Select. 0 selects AIN7, 1 selects AIN8
1	ICON.1	IEXC2 Enable Bit (0 = disable).
0	ICON.0	IEXC1 Enable Bit (0 = disable).

A write to the ICON register has an immediate effect but does not reset the ADCs. Therefore, if a current source is changed while an ADC is already converting, the user must wait until the third or fourth output at least (depending on the status of the chop mode) to see a fully settled new output.

Both IEXC1 and IEXC2 can be configured to operate on the same output pin thereby increasing the current source capability to 400 µA.

NONVOLATILE FLASH/EE MEMORY OVERVIEW

The ADuC845/ADuC847/ADuC848 incorporate Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable code and data memory space.

Like EEPROM, flash memory can be programmed in-system at the byte level, although it must first be erased, in page blocks. Thus, flash memory is often and more correctly referred to as Flash/EE memory.

Figure 26. Flash/EE Memory Development

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. The Flash/EE memory technology allows the user to update program code space in-circuit, without needing to replace onetime programmable (OTP) devices at remote operating nodes.

Flash/EE Memory on the ADuC845, ADuC847, ADuC848

The ADuC845/ADuC847/ADuC848 provide two arrays of Flash/EE memory for user applications—up to 62 kbytes of Flash/EE program space and 4 kbytes of Flash/EE data memory space. Also, 8-kbyte and 32-kbyte program memory options are available. All examples and references in this datasheet use the 62-kbyte option; however, similar protocols and procedures are applicable to the 32-kbyte and 8-kbyte options unless otherwise noted, provided that the difference in memory size is taken into account.

The 62 kbytes Flash/EE code space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download mode provided, using conventional third party memory programmers, or via any user-defined protocol in user download (ULOAD) mode.

The 4-kbyte Flash/EE data memory space can be used as a general-purpose, nonvolatile scratchpad area. User access to this area is via a group of seven SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

All the following sections use the 62-kbyte program space as an example when referring to program and ULOAD mode. For the 64-kbyte part, the ULOAD area takes up the top 6 kbytes of the program space, that is, from 56 kbytes to 62 kbytes. For the 32-kbyte part, the ULOAD space moves to the top 8 kbytes of the on-chip program memory, that is., from 24 kbytes to 32 kbytes.

No ULOAD mode is available on the 8-kbyte part since the bootload area on the 8-kbyte part is 8 kbytes long, so no usable user program space remains. The kernel still resides in the protected area from 62 kbytes to 64 kbytes.

Flash/EE Memory Reliability

The Flash/EE program and data memory arrays on the ADuC845/ADuC847/ADuC848 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications table, the ADuC845/ADuC847/ ADuC848 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C, +25°C, +85°C, and +125°C. (The LFCSP package is qualified to +85°C only.) The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention is the ability of the Flash/EE memory to retain its programmed data over time. Again, the devices have been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 27.

Figure 27. Flash/EE Memory Data Retention

FLASH/EE PROGRAM MEMORY

The ADuC845/ADuC847/ADuC848 contain a 64-kbyte array of Flash/EE program memory. The lower 62 kbytes of this program memory are available to the user for program storage or as additional NV data memory.

The upper 2 kbytes of this Flash/EE program memory array contain permanently embedded firmware, allowing in-circuit serial download, serial debug, and nonintrusive single-pin emulation. These 2 kbytes of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals such as ADC, temperature sensor, current sources, band gap, and references.

These 2 kbytes of embedded firmware are hidden from the user code. Attempts to read this space read 0s; therefore, the embedded firmware appears as NOP instructions to user code.

In normal operating mode (power-on default), the 62 kbytes of user Flash/EE program memory appear as a single block. This block is used to store the user code as shown in Figure 28.

Figure 28. Flash/EE Program Memory Map in Normal Mode

In normal mode, the 62 kbytes of Flash/EE program memory can be programmed by serial downloading and by parallel programming.

Serial Downloading (In-Circuit Programming)

The ADuC845/ADuC847/ADuC848 facilitate code download via the standard UART serial port. The devices enter serial download mode after a reset or a power cycle if the $\overline{\text{PSEN}}$ pin is pulled low through an external 1 kΩ resistor. Once in serial download mode, the hidden embedded download kernel executes. This allows the user to download code to the full 62 kbytes of Flash/EE program memory while the device is in circuit in its target application hardware.

A PC serial download executable (WSD.EXE) is provided as part of the ADuC845/ADuC847/ADuC848 Quick Start development system. The AN-1074 Application Note fully describes the serial download protocol that is used by the embedded download kernel.

Parallel Programming

The parallel programming mode is fully compatible with conventional third-party flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 29. In this mode, Ports 0 and 2 operate as the external address bus interface, P3 operates as the external data bus interface, and P1.0 operates as the write enable strobe. P1.1, P1.2, P1.3, and P1.4 are used as general configuration ports that configure the device for various program and erase operations during parallel programming.

Figure 29. Flash/EE Memory Parallel Programming

The command words that are assigned to P1.1, P1.2, P1.3, and P1.4 are described in Table 31.

Table 31. Flash/EE Memory Parallel Programming Modes

Port 1 Pins				
P1.4	**P1.3**	**P1.2**	**P1.1**	**Programming Mode**
0	0	0	0	Erase Flash/EE Program, Data, and Security Mode
1	0	1	0	Program Code Byte
0	0	1	0	Program Data Byte
1	0	1	1	Read Code Byte
0	0	1	1	Read Data Byte
1	1	0	0	Program Security Modes
1	1	0	1	Read/Verify Security Modes
All other codes				Redundant

USER DOWNLOAD MODE (ULOAD)

Figure 28 shows that it is possible to use the 62 kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode, all the Flash/EE memory is read-only to user code.

However, most of the Flash/EE program memory can also be written to during run time simply by entering ULOAD mode. In ULOAD mode, the lower 56 kbytes of program memory can be erased and reprogrammed by the user software as shown in Figure 30. ULOAD mode can be used to upgrade the code in the field via any user-defined download protocol. By configuring the SPI port on the ADuC845/ADuC847/ADuC848 as a slave, it is possible to completely reprogram the 56 kbytes of Flash/EE program memory in under 5 s (see the AN-1074 Application Note).

Alternatively, ULOAD mode can be used to save data to the 56 kbytes of Flash/EE memory. This can be extremely useful in data logging applications where the devices can provide up to 60 kbytes of data memory on-chip (4 kbytes of dedicated Flash/EE data memory also exist).

The upper 6 kbytes of the 62 kbytes of Flash/EE program memory (8 kbytes on the 32-kbyte parts) are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code; therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, making it very suitable to use the 6 kbytes as a bootloader. A bootload enable option exists in the Windows® serial downloader (WSD) to "Always RUN from E000H after Reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD mode is described in the Flash/EE Memory Control SFR section of ECON and also in the AN-1074 Application Note.

Figure 30. Flash/EE Program Memory Map in ULOAD Mode (62-kbyte Part)

The 32-kbyte memory parts have the user bootload space starting at 6000H. The memory mapping is shown in Figure 31.

Figure 31. Flash/EE Program Memory Map in ULOAD Mode (32-kbyte Part)

ULOAD mode is not available on the 8-kbyte Flash/EE program memory parts.

Flash/EE Program Memory Security

The ADuC845/ADuC847/ADuC848 facilitate three modes of Flash/EE program memory security: the lock, secure, and serial safe modes. These modes can be independently activated, restricting access to the internal code space. They can be enabled as part of serial download protocol, as described in the AN-1074 Application Note, or via parallel programming.

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/verifying the memory in parallel mode and reading the internal memory via a MOVC command from external memory are also disabled. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the device into serial download mode, that is, RESET asserted (pulled high) and de-asserted (pulled low) with $\overline{\text{PSEN}}$ low, the device interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode, but executes only a normal reset sequence. Serial safe mode can be disabled only by initiating an ERASE CODE AND DATA command in parallel programming mode.

USING FLASH/EE DATA MEMORY

The 4 kbytes of Flash/EE data memory are configured as 1024 pages, each of 4 bytes. As with the other ADuC845/ADuC847/ADuC848 peripherals, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) holds the 4 bytes of data at each page. The page is addressed via the EADRH and EADRL registers. Finally, ECON is an 8-bit control register that can be written to with one of nine Flash/EE memory access commands to trigger various read, write, erase, and verify functions. A block diagram of the SFR interface to the Flash/EE data memory array is shown in Figure 32.

ECON—Flash/EE Memory Control SFR

Programming either Flash/EE data memory or Flash/EE program memory is done through the Flash/EE memory control SFR (ECON). This SFR allows the user to read, write, erase, or verify the 4 kbytes of Flash/EE data memory or the 56 kbytes of Flash/EE program memory.

Figure 32. Flash/EE Data Memory Control and Configuration

Table 32. ECON—Flash/EE Memory Commands

ECON Value	Command Description (Normal Mode, Power-On Default)	Command Description (ULOAD Mode)
01H Read	4 bytes in the Flash/EE data memory, addressed by the page address EADRH/L, are read into EDATA1–4.	Not implemented. Use the MOVC instruction.
02H Write	Results in 4 bytes in EDATA1–4 being written to the Flash/EE data memory, at the page address given by EADRH (0 ≤ EADRH < 0400H). Note that the 4 bytes in the page being addressed must be pre-erased.	Bytes 0 to 255 of internal XRAM are written to the 256 bytes of Flash/EE program memory at the page address given by EADRH/L (0 ≤ EADRH/L < E0H). Note that the 256 bytes in the page being addressed must be pre-erased.
03H	Reserved.	Reserved.
04H Verify	Verifies that the data in EDATA1–4 is contained in the page address given by EADRH/L. A subsequent read of the ECON SFR results in a 0 being read if the verification is valid, or a nonzero value being read to indicate an invalid verification.	Not implemented. Use the MOVC and MOVX instructions to verify the Write in software.
05H Erase Page	4-byte page of Flash/EE data memory address is erased by the page address EADRH/L.	64-byte page of FLASH/EE program memory addressed by the byte address EADRH/L is erased. A new page starts when EADRL is equal to 00H, 80H, or C0H.
06H Erase All	4 kbytes of Flash/EE data memory are erased.	The entire 56 kbytes of ULOAD are erased.
81H ReadByte	The byte in the Flash/EE data memory, addressed by the byte address EADRH/L, is read into EDATA1 (0 ≤ EADRH/L ≤ 0FFFH).	Not implemented. Use the MOVC command.
82H WriteByte	The byte in EDATA1 is written into Flash/EE data memory at the byte address EADRH/L.	The byte in EDATA1 is written into Flash/EE program memory at the byte address EADRH/L (0 ≤ EADRH/L ≤ DFFFH).
0FH EXULOAD	Configures the ECON instructions (above) to operate on Flash/EE data memory.	Enters normal mode, directing subsequent ECON instructions to operate on the Flash/EE data memory.
F0H ULOAD	Enters ULOAD mode; subsequent ECON instructions operate on Flash/EE program memory.	Enables the ECON instructions to operate on the Flash/EE program memory. ULOAD entry mode.

Example: Programming the Flash/EE Data Memory

A user wants to program F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other 3 bytes already in this page. A typical program of the Flash/EE data array involves

1. Setting EADRH/L with the page address.
2. Writing the data to be programmed to the EDATA1–4.
3. Writing the ECON SFR with the appropriate command.

Step 1: Set Up the Page Address
Address registers EADRH and EADRL hold the high byte address and the low byte address of the page to be addressed. The assembly language to set up the address may appear as

```
MOV EADRH, #0    ;Set Page Address Pointer
MOV EADRL, #03H
```

Step 2: Set Up the EDATA Registers
Write the four values to be written into the page into the four SFRs EDATA1–4. Unfortunately, the user does not know three of them. Thus, the user must read the current page and overwrite the second byte.

```
MOV ECON,   #1    ;Read Page into EDATA1-4
MOV EDATA2, #0F3H ;Overwrite Byte 2
```

Step 3: Program Page
A byte in the Flash/EE array can be programmed only if it has previously been erased. Specifically, a byte can be programmed only if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of 4 bytes (1 page) are erased when an erase command is initiated. Once the page is erased, the user can program the 4 bytes in-page and then perform a verification of the data.

```
MOV ECON, #5   ;ERASE Page
MOV ECON, #2   ;WRITE Page
MOV ECON, #4   ;VERIFY Page
MOV A, ECON    ;Check if ECON = 0 (OK!)
```

Although the 4 kbytes of Flash/EE data memory are factory pre-erased, that is, byte locations set to FFH, it is good programming practice to include an ERASEALL routine as part of any configuration/set-up code running on the devices. An ERASEALL command consists of writing 06H to the ECON SFR, which initiates an erase of the 4-kbyte Flash/EE array. This command coded in 8051 assembly language would appear as

```
MOV ECON, #06H     ;ERASE all Command
                   ;2ms duration
```

FLASH/EE MEMORY TIMING

Typical program and erase times for the devices are as follows:

Normal Mode (Operating on Flash/EE Data Memory)

Command	Bytes Affected	
READPAGE	4 bytes	25 machine cycles
WRITEPAGE	4 bytes	380 µs
VERIFYPAGE	4 bytes	25 machine cycles
ERASEPAGE	4 bytes	2 ms
ERASEALL	4 kbytes	2 ms
READBYTE	1 byte	10 machine cycles
WRITEBYTE	1 byte	200 µs

ULOAD Mode (Operating on Flash/EE Program Memory)

WRITEPAGE	256 bytes	15 ms
ERASEPAGE	64 bytes	2 ms
ERASEALL	56 kbytes	2 ms
WRITEBYTE	1 byte	200 µs

A given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine-cycle MOV instruction (to write to the ECON SFR), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions such as counter/timers continue to count as configured throughout this period.

DAC CIRCUIT INFORMATION

The ADuC845/ADuC847/ADuC848 incorporate a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF, and has two selectable ranges, 0 V to V_{REF} and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 14 (DAC) or Pin 13 (AINCOM).

In 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR is written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower 8 bits, and the lower nibble of DACH contains the upper 4 bits.

DACCON Control Register

SFR Address: FDH
Power-On Default: 00H
Bit Addressable: No

Table 33. DACCON—DAC Configuration Commands

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	–––	Not Implemented. Write Don't Care.
5	–––	Not Implemented. Write Don't Care.
4	DACPIN	DAC Output Pin Select. Set to 1 by the user to direct the DAC output to Pin 13 (AINCOM). Cleared to 0 by the user to direct the DAC output to Pin 14 (DAC).
3	DAC8	DAC 8-Bit Mode Bit. Set to 1 by the user to enable 8-bit DAC operation. In this mode, the 8 bits in DACL SFR are routed to the 8 MSBs of the DAC, and the 4 LSBs of the DAC are set to 0. Cleared to 0 by the user to enable 12-bit DAC operation. In this mode, the 8 LSBs of the result are routed to DACL, and the upper 4 MSB bits are routed to the lower 4 bits of DACH.
2	DACRN	DAC Output Range Bit. Set to 1 by the user to configure the DAC range of 0 V to AV_{DD}. Cleared to 0 by the user to configure the DAC range of 0 V to 2.5 V (V_{REF}).
1	DACCLR	DAC Clear Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to reset the DAC data registers DACL/H to 0.
0	DACEN	DAC Enable Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to power down the DAC.

DACH/DACL Data Registers

These DAC data registers are written to by the user to update the DAC output.

SFR Address: DACL (DAC data low byte)—FBH
DACH (DAC data high byte)—FCH
Power-On Default: 00H (both registers)
Bit Addressable: No (both registers)

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is shown in Figure 33.

Figure 33. Resistor String DAC Functional Equivalent

Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity. As shown in Figure 33, the reference source for the DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} (2.5 V). The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that, unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 48 in 0 V-to-V_{REF} mode; Codes 0 to 100; and Codes 3950 to 4095 in 0 V-to-V_{DD} mode.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier; a general representation of its effects (neglecting offset and gain error) is shown in Figure 34. The dotted line indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier.

Note that Figure 34 represents a transfer function in 0-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line to the end, showing no signs of the high-end endpoint linearity error.

Figure 34. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities shown in Figure 34 become worse as a function of output loading. Most data sheet specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom, respectively, of Figure 34 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 35 and Figure 36 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V to AV_{DD}. In 0 V-to-V_{REF} mode, DAC loading does not cause high-side voltage nonlinearities while the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage is not affected by loads of less than 5 mA. But around 7 mA, the upper curve in Figure 36 drops below 2.5 V (V_{REF}), indicating that at these higher currents, the output is not capable of reaching V_{REF}.

Figure 35. Source and Sink Current Capability with $V_{REF} = AV_{DD} = 5$ V

Figure 36. Source and Sink Current Capability with $V_{REF} = AV_{DD} = 3$ V

For larger loads, the current drive capability may not be sufficient. To increase the source and sink current capability of the DAC, an external buffer should be added as shown in Figure 37.

Figure 37. Buffering the DAC Output

The internal DAC output buffer also features a high impedance disable function. In the chip's default power-on state, the DAC is disabled and its output is in a high impedance state (or three-state) where it remains inactive until enabled in software. This means that if a zero output is desired during power-on or power-down transient conditions, a pull-down resistor must be added to each DAC output. Assuming that this resistor is in place, the DAC output remains at ground potential whenever the DAC is disabled.

PULSE-WIDTH MODULATOR (PWM)

The ADuC845/ADuC847/ADuC848 has a highly flexible PWM offering programmable resolution and an input clock. The PWM can be configured in six different modes of operation. Two of these modes allow the PWM to be configured as a Σ-Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 38.

Figure 38. PWM Block Diagram

The PWM uses control SFR, PWMCON, and four data SFRs: PWM0H, PWM0L, PWM1H, and PWM1L.

PWMCON (as described in Table 34) controls the different modes of operation of the PWM as well as the PWM clock frequency. PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs at P2.5 and P2.6.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

PWMCON PWM Control SFR

SFR Address: AEH
Power-On Default: 00H
Bit Addressable: No

Table 34. PWMCON PWM Control SFR

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6, 5, 4	PWM2, PWM1, PWM0	PMW Mode Selection.
		PWM2 PWM1 PWM0
		0 0 0 Mode 0: PWM disabled.
		0 0 1 Mode 1: Single 16-bit output with programmable pulse and cycle time.
		0 1 0 Mode 2: Twin 8-bit outputs.
		0 1 1 Mode 3: Twin 16-bit outputs.
		1 0 0 Mode 4: Dual 16-bit pulse density outputs.
		1 0 1 Mode 5: Dual 8-bit outputs.
		1 1 0 Mode 6: Dual 16-bit pulse density RZ outputs.
		1 1 1 Mode 7: PWM counter reset with outputs not used.
3, 2	PWS1, PWS0	PWM Clock Source Divider.
		PWS1 PWS0
		0 0 Selected clock.
		0 1 Selected clock divided by 4.
		1 0 Selected clock divided by 16.
		1 1 Selected clock divided by 64.
1, 0	PWC1, PWC0	PWM Clock Source Selection.
		PWC1 PWC0
		0 0 F_{XTAL}/15 (2.184 kHz).
		0 1 F_{XTAL} (32.768 kHz).
		1 0 External input on P2.7.
		1 1 F_{VCO} (12.58 MHz).

PWM Pulse Width High Byte (PWM0H)

SFR Address: B2H
Power-On Default: 00H
Bit Addressable: No

Table 35. PWM0H: PWM Pulse Width High Byte

PWM0H.7	PWM0H.6	PWM0H.5	PWM0H.4	PWM0H.3	PWM0H.2	PWM0H.1	PWM0H.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Pulse Width Low Byte (PWM0L)

SFR Address: B1H
Power-On Default: 00H
Bit Addressable: No

Table 36. PWM0L: PWM Pulse Width Low Byte

PWM0L.7	PWM0L.6	PWM0L.5	PWM0L.4	PWM0L.3	PWM0L.2	PWM0L.1	PWM0L.0
0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W

PWM Cycle Width High Byte (PWM1H)

SFR Address: B4H
Power-On Default: 00H
Bit Addressable: No

Table 37. PWM1H: PWM Cycle Width High Byte

PWM1H.7	PWM1H.6	PWM1H.5	PWM1H.4	PWM1H.3	PWM1H.2	PWM1H.1	PWM1H.0
0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W

PWM Cycle Width Low Byte (PWM1L)

SFR Address: B3H
Power-On Default: 00H
Bit Addressable: No

Table 38. PWM1L: PWM Cycle Width Low Byte

PWM1L.7	PWM1L.6	PWM1L.5	PWM1L.4	PWM1L.3	PWM1L.2	PWM1L.1	PWM1L.0
0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W

Mode 0

In Mode 0, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal digital I/Os.

Mode 1 (Single-Variable Resolution PWM)

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable. PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM. For example, setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 192 Hz (12.583 MHz/65536). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 3072 Hz (12.583 MHz/4096).

PWM0H/L sets the duty cycle of the PWM output waveform as shown in Figure 39.

Figure 39. PWM in Mode 1

Mode 2 (Twin 8-Bit PWM)

In Mode 2, the duty cycle and the resolution of the PWM outputs are programmable. The maximum resolution of the PWM output is 8 bits.

PWM1L sets the period for both PWM outputs. Typically, this is set to 255 (FFH) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 can be loaded here to give a percentage PWM, that is, the PWM is accurate to 1%.

The outputs of the PWM at P2.5 and P2.6 are shown in Figure 40. As can be seen, the output of PWM0 (P2.5) goes low when the PWM counter equals PWM0L. The output of PWM1 (P2.6) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

Figure 40. PWM Mode 2

Mode 3 (Twin 16-Bit PWM)

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P2.5 and P2.6 are independently programmable.

As shown in Figure 41, while the PWM counter is less than PWM0H/L, the output of PWM0 (P2.5) is high. Once the PWM counter equals PWM0H/L, PWM0 (P2.5) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P2.6) is high. Once the PWM counter equals PWM1H/L, PWM1 (P2.6) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized, that is, once the PWM counter rolls over to 0, both PWM0 (P2.5) and PWM1 (P2.6) go high.

Figure 41. PWM Mode 3

Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC)

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 12.58 MHz.

In this mode, P2.5 and P2.6 are updated every PWM clock (80 ns in the case of 12.58 MHz). Over any 65536 cycles (16-bit PWM), PWM0 (P2.5) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.6) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three clocks and high for one clock (each clock is approximately 80 ns). Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale, by having a high cycle followed by only two low cycles.

Figure 42. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

ON-CHIP PLL (PLLCON)

The ADuC845/ADuC847/ADuC848 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The control register for the PLL is called PLLCON and is described as follows.

The 5 V parts can be set to a maximum core frequency of 12.58 MHz (CD2...0 = 000) while at 3 V, the maximum core clock rate is 6.29 MHz (CD2...0 = 001). The CD bits should not be set to 000b on the 3 V parts.

The 3 V parts are limited to a core clock speed of 6.29 MHz (CD = 1).

PLLCON PLL Control Register

SFR Address: D7H
Power-On Default: 53H
Bit Addressable: No

Table 39. PLLCON PLL Control Register

Bit No.	Name	Description
7	OSC_PD	Oscillator Power-Down Bit. If low, the 32 kHz crystal oscillator continues running in power-down mode. If high, the 32.768 kHz oscillator is powered down. When this bit is low, the seconds counter continues to count in power-down mode and can interrupt the CPU to exit power-down. The oscillator is always enabled in normal mode.
6	LOCK	PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. After power-down, this bit can be polled to wait for the PLL to lock. Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This might be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. After the device wakes up from power-down, user code can poll this bit to wait for the PLL to lock. If LOCK = 0, the PLL is not locked.
5	–––	Not Implemented. Write Don't Care.
4	LTEA	EA Status. Read-only bit. Reading this bit returns the state of the external $\overline{EA}$ pin latched at reset or power-on.
3	FINT	Fast Interrupt Response Bit. Set by the user to enable the response to any interrupt to be executed at the fastest core clock frequency. Cleared by the user to disable the fast interrupt response feature. This function must not be used on 3 V parts.
2, 1, 0	CD2, CD1, CD0	CPU (Core Clock) Divider Bits. This number determines the frequency at which the core operates. CD2 CD1 CD0 Core Clock Frequency (MHz) 0 0 0 12.582912. Not a valid selection on 3 V parts. 0 0 1 6.291456 (Maximum core clock rate allowed on the 3 V parts) 0 1 0 3.145728 0 1 1 1.572864 (Default core frequency) 1 0 0 0.786432 1 0 1 0.393216 1 1 0 0.196608 1 1 1 0.098304 On 3 V parts (ADuC84xBCPxx-3 or ADuC84xBSxx-3), the CD settings can be only CD = 1; CD = 0 is not a valid selection. If CD = 0 is selected on a 3 V part by writing to PLLCON, the instruction is ignored, and the previous CD value is retained. The Fast Interrupt bit (FINT) must not be used on 3 V parts since it automatically sets the CD bits to 0, which is not a valid setting.

I²C SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA (Pin 27 on the MQFP package and Pin 29 on the LFCSP package) is the data I/O pin. SCLK (Pin 26 on the MQFP package and Pin 28 on the LFCSP package) is the serial interface clock for the SPI interface. The I²C interface on the devices is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845/ADuC847/ADuC848 also includes a second address register (I2CADD1) at SFR Address F2H with a default power-on value of 7FH. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that the I²C and SPI interfaces can be used at the same time.

Note that when using the I²C and SPI interfaces simultaneously, they both use the same interrupt routine (Vector Address 3BH). When an interrupt occurs from one of these, it is necessary to interrogate each interface to see which one has triggered the ISR request.

The four SFRs that are used to control the I²C interface are described next.

I2CCON—I²C Control Register

SFR Address: E8H
Power-On Default: 00H
Bit Addressable: Yes

Table 40. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (master mode only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (master mode only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (master mode only). This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit is output on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (master mode only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (slave mode only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (slave mode only). Set by the MicroConverter if the I²C interface is transmitting. Cleared by the MicroConverter if the I²C interface is receiving.
0	I2CI	I²C Interrupt Bit (slave mode only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

I2CADD—I²C Address Register 1

Function:	Holds one of the I²C peripheral addresses for the device. It may be overwritten by user code. The uC001 Application Note describes the format of the I²C standard 7-bit address.
SFR Address:	9BH
Power-On Default:	55H
Bit Addressable:	No

I2CADD1—I²C Address Register 2

Function:	Same as the I2CADD.
SFR Address:	F2H
Power-On Default:	7FH
Bit Addressable:	No

I2CDAT—I²C Data Register

Function:	The I2CDAT SFR is written to by user code to transmit data, or read by user code to read data just received by the I²C interface. Accessing I2CDAT automatically clears any pending I²C interrupt and the I2CI bit in the I2CCON SFR. User code should access I2CDAT only once per interrupt cycle.
SFR Address:	9AH
Power-On Default:	00H
Bit Addressable:	No

The main features of the MicroConverter I²C interface are

- Only two bus lines are required: a serial data line (SDATA) and a serial clock line (SCLOCK).
- An I²C master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address, single master/slave relationships can exist at all times even in a multislave environment.
- The ability to respond to two separate addresses when operating in slave mode.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

Figure 45. Typical I²C System

Software Master Mode

The ADuC845/ADuC847/ADuC848 can be used as an I²C master device by configuring the I²C peripheral in master mode and writing software to output the data bit-by-bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin is high on the last rising edge of SCLOCK. MDI is cleared if the SDATA pin is low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in the uC001 Application Note.

Hardware Slave Mode

After reset, the ADuC845/ADuC847/ADuC848 default to hardware slave mode. Slave mode is enabled by clearing the I2CM bit in I2CCON. The devices have a full hardware slave. In slave mode, the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode, the slave controller waits for a start condition. If the parts detect a valid start condition, followed by a valid address, followed by the R/W bit, then the I2CI interrupt bit is automatically set by hardware. The I²C peripheral generates a core interrupt only if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit, EA, in the IE SFR. Therefore,

```
MOV IEIP2, #01h    ;Enable I²C Interrupt
SETB EA
```

An autoclear of the I2CI bit is implemented on the devices so that this bit is cleared automatically upon read or write access to the I2CDAT SFR.

```
MOV I2CDAT, A      ;I2CI auto-cleared
MOV A, I2CDAT      ;I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once, that is, access the data SFR more than once per interrupt, the I²C controller stops. The interface then must be reset by using the I2CRS bit.

The user can choose to poll the I2CI bit or to enable the interrupt. In the case of the interrupt, the PC counter vectors to 003BH at the end of each complete byte. For the first byte, when the user gets to the I2CI ISR, the 7-bit address and the R/W bit appear in the I2CDAT SFR.

The I2CTX bit contains the R/W bit sent from the master. If I2CTX is set, the master is ready to receive a byte; therefore the slave transmits data by writing to the I2CDAT register. If I2CTX is cleared, the master is ready to transmit a byte; therefore the slave receives a serial byte. Software can interrogate the state of I2CTX to determine whether it should write to or read from I2CDAT.

Once the device has received a valid address, hardware holds SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

The I2CI interrupt bit is set every time a complete data byte is received or transmitted, provided that it is followed by a valid ACK. If the byte is followed by a NACK, an interrupt is not generated.

The device continues to issue interrupts for each complete data byte transferred until a stop condition is received or the interface is reset.

When a stop condition is received, the interface resets to a state in which it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence, it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

SPI SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 integrate a complete hardware serial peripheral interface (SPI) interface on-chip. SPI is an industry-standard synchronous serial interface that allows 8 bits of data to be synchronously transmitted and received simultaneously, that is, full duplex. Note that the SPI pins are multiplexed with the Port 2 pins, P2.0, P2.1, P2.2, and P2.3. These pins have SPI functionality only if SPE is set. Otherwise, with SPE cleared, standard Port 2 functionality is maintained. SPI can be configured for master or slave operation and typically consists of Pins SCLOCK, MISO, MOSI, and $\overline{SS}$.

SCLOCK (Serial Clock I/O Pin)

Pin 28 (MQFP Package), Pin 30 (LFCSP Package)
The master clock (SCLOCK) is used to synchronize the data transmitted and received through the MOSI and MISO data lines.

A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 41). In slave mode, the SPICON register must be configured with the same phase and polarity (CPHA and CPOL) as the master. The data is transmitted on one edge of the SCLOCK signal and sampled on the other.

MISO (Master In, Slave Out Pin)

Pin 30 (MQFP Package), Pin 32 (LFCSP Package)
The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

Pin 29 (MQFP Package), Pin31 (LFCSP Package)
The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

$\overline{SS}$ (Slave Select Input Pin)

Pin 31 (MQFP Package), Pin 33 (LFCSP Package)
The $\overline{SS}$ pin is used only when the ADuC845/ADuC847/ADuC848 are configured in SPI slave mode. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the devices to be used in single-master, multislave SPI configurations. If CPHA = 1, the $\overline{SS}$ input can be pulled low permanently. If CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and must return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin (Pin 31/Pin 33) can be read via the SPR0 bit in the SPICON SFR.

The SFR register in Table 41 is used to control the SPI interface.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

USING THE SPI INTERFACE

Depending on the configuration of the bits in the SPICON SFR shown in Table 41, the SPI interface transmits or receives data in a number of possible modes. Figure 46 shows all possible ADuC845/ADuC847/ADuC848 SPI configurations and the timing relationships and synchronization among the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

Figure 46. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. Also note that the $\overline{SS}$ pin is not used in master mode. If the devices need to assert the $\overline{SS}$ pin on an external slave device, use a port digital output pin.

In master mode, a byte transmission or reception is initiated by a byte write to SPIDAT. The hardware automatically generates eight clock periods via the SCLOCK pin, and the data is transmitted via MOSI. With each SCLOCK period, a data bit is also sampled via MISO. After eight clocks, the transmitted byte is completely transmitted (via MOSI), and the input byte (if required) is waiting in the input shift register (after being received via MISO). The ISPI flag is set automatically, and an interrupt occurs if enabled. The value in the input shift register is latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode, the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication. Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO, and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte is completely transmitted, and the input byte is waiting in the input shift register. The ISPI flag is set automatically, and an interrupt occurs, if enabled. The value in the shift register is latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received if CPHA = 1, or when $\overline{SS}$ returns high if CPHA = 0.

DUAL DATA POINTERS

The devices incorporate two data pointers. The second data pointer is a shadow data pointer and is selected via the data pointer control SFR (DPCON). DPCON features automatic hardware post-increment and post-decrement as well as an automatic data pointer toggle.

DPCON—Data Pointer Control SFR

SFR Address: A7H
Power-On Default: 00H
Bit Addressable: No

Table 42. DPCON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	DPT	Data Pointer Automatic Toggle Enable. Cleared by the user to disable autoswapping of the DPTR. Set in user software to enable automatic toggling of the DPTR after each MOVX or MOVC instruction.
5, 4	DP1m1, DP1m0	Shadow Data Pointer Mode. These bits enable extra modes of the shadow data pointer operation, allowing more compact and more efficient code size and execution. DP1m1 DP1m0 Behavior of the Shadow Data Pointer 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.)
3, 2	DP0m1, DP0m0	Main Data Pointer Mode. These bits enable extra modes of the main data pointer operation, allowing more compact and more efficient code size and execution. DP0m1 DP0m0 Behavior of the Main Data Pointer 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction is useful for moving 8-bit blocks to/from 16-bit devices.)
1	----	Not Implemented. Write Don't Care.
0	DPSEL	Data Pointer Select. Cleared by the user to select the main data pointer. This means that the contents of this 24-bit register are placed into the DPL, DPH, and DPP SFRs. Set by the user to select the shadow data pointer. This means that the contents of a separate 24-bit register appear in the DPL, DPH, and DPP SFRs.

Note the following:

- The Dual Data Pointer section is the only place in which main and shadow data pointers are distinguished. Whenever the DPTR is mentioned elsewhere in this data sheet, active DPTR is implied.
- Only the MOVC/MOVX @DPTR instructions automatically post-increment and post-decrement the DPTR. Other MOVC/MOVX instructions, such as MOVC PC or MOVC @Ri, do not cause the DPTR to automatically post-increment and post-decrement.

To illustrate the operation of DPCON, the following code copies 256 bytes of code memory at Address D000H into XRAM, starting from Address 0000H.

```
          MOV DPTR,#0       ;Main DPTR = 0
          MOV DPCON,#55H    ;Select shadow DPTR
                            ;DPTR1 increment mode
                            ;DPTR0 increment mode
                            ;DPTR auto toggling ON
          MOV DPTR,#0D000H  ;DPTR = D000H
MOVELOOP: CLR A
          MOVC A,@A+DPTR    ;Get data
                            ;Post Inc DPTR
                            ;Swap to Main DPTR(Data)
           MOVX @DPTR,A     ;Put ACC in XRAM
                            ;Increment main DPTR
                            ;Swap Shadow DPTR(Code)
           MOV A, DPL
           JNZ MOVELOOP
```

POWER SUPPLY MONITOR

The power supply monitor, once enabled, monitors the DV_{DD} and AV_{DD} supplies on the devices. It indicates when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the power supply monitor function, AV_{DD} must be equal to or greater than 2.63 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor interrupts the core by using the PSMI bit in the PSMCON SFR. This bit is not cleared until the failing power supply returns above the trip point for at least 250 ms.

The monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution does not resume until a safe supply level is well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

The 5 V part has an internal POR trip level of 4.63 V, which means that there are no usable DV_{DD} PSM trip levels on the 5 V part. The 3 V part has a POR trip level of 2.63 V following a reset and initialization sequence, allowing all relevant PSM trip points to be used.

PSMCON—Power Supply Monitor Control Register

SFR Address: DFH
Power-On Default: DEH
Bit Addressable: No

Table 43. PSMCON SFR Bit Designations

Bit No.	Name	Description
7	CMPD	DV_{DD} Comparator Bit. This read-only bit directly reflects the state of the DV_{DD} comparator. Read 1 indicates that the DV_{DD} supply is above its selected trip point. Read 0 indicates that the DV_{DD} supply is below its selected trip point.
6	CMPA	AV_{DD} Comparator Bit. This read-only bit directly reflects the state of the AV_{DD} comparator. Read 1 indicates that the AV_{DD} supply is above its selected trip point. Read 0 indicates that the AV_{DD} supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. Set high by the MicroConverter if either CMPA or CMPD is low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA returns (and remains) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4, 3	TPD1, TPD0	DV_{DD} Trip Point Selection Bits. A 5 V part has no valid PSM trip points. If the DV_{DD} supply falls below the 4.63 V point, the device resets (POR). For a 3 V part, all relevant PSM trip points are valid. The 3 V POR trip point is 2.63 V (fixed). These bits select the DV_{DD} trip point voltage as follows: TPD1 TPD0 Selected DV_{DD} Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
2, 1	TPA1, TPA0	AV_{DD} Trip Point Selection Bits. These bits select the AV_{DD} trip point voltage as follows: TPA1 TPA0 Selected AV_{DD} Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
0	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.

WATCHDOG TIMER

The watchdog timer generates a device reset or interrupt within a reasonable amount of time if the ADuC845/ADuC847/ADuC848 enters an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the WDE bit within a predetermined amount of time (see the PRE3…0 bits in Table 44). The watchdog timer is clocked from the 32 kHz external crystal connected between the XTAL1 and XTAL2 pins. The WDCON SFR can be written only by user software if the double write sequence described in WDWR is initiated on every write access to the WDCON SFR.

WDCON—Watchdog Control Register

SFR Address:	C0H
Power-On Default:	10H
Bit Addressable:	Yes

Table 44. WDCON SFR Bit Designations

Bit No.	Name	Description
7, 6, 5, 4	PRE3, PRE2, PRE1, PRE0	Watchdog Timer Prescale Bits. The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/ f_{XTAL}))$ $(0 \le PRE \le 7; f_{XTAL} = 32.768$ kHz)
		PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action
		0 0 0 0 15.6 Reset or interrupt
		0 0 0 1 31.2 Reset or interrupt
		0 0 1 0 62.5 Reset or interrupt
		0 0 1 1 125 Reset or interrupt
		0 1 0 0 250 Reset or interrupt
		0 1 0 1 500 Reset or interrupt
		0 1 1 0 1000 Reset or interrupt
		0 1 1 1 2000 Reset or interrupt
		1 0 0 0 0.0 Immediate reset
		PRE3–PRE0 > 1000b Reserved. Not a valid selection.
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period expires. This interrupt is not disabled by the CLR EA instruction, and it is also a fixed, high priority interrupt. If the watchdog timer is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated.
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog timer generates a reset or interrupt, depending on WDIR. Cleared under the following conditions: user writes 0; watchdog reset (WDIR = 0); hardware reset; PSM interrupt.

0	WDWR	Watchdog Write Enable Bit.
		Writing data to the WDCON SFR involves a double instruction sequence. Global interrupts must first be disabled. The WDWR bit is set with the very next instruction, a write to the WDCON SFR. For example:
		`CLR EA ;Disable Interrupts while configuring to WDT`
		`SETB WDWR ;Allow Write to WDCON`
		`MOV WDCON, #72H ;Enable WDT for 2.0s timeout`
		`SETB EA ;Enable Interrupts again (if required)`

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051-compatible timers can count. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Also, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it can remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required. Note that instructions to the TIC SFRs are also clocked at 32.768 kHz, so sufficient time must be allowed in user code for these instructions to execute.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled. If the device is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 45. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A basic block diagram of the TIC is shown in Figure 47.

Because the TIC is clocked directly from a 32 kHz external crystal on the devices, instructions that access the TIC registers are also clocked at 32 kHz (not at the core frequency). The user must ensure that sufficient time is given for these instructions to execute.

Figure 47. TIC Simplified Block Diagram

TIMECON—TIC Control Register

SFR Address: A1H
Power-On Default: 00H
Bit Addressable: No

Table 45. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.
5, 4	ITS1, ITS0	Interval Timebase Selection Bits. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	ST1	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.

INTVAL—User Timer Interval Select Register

Function:	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled.
SFR Address:	A6H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 255 decimal

HTHSEC—Hundredths of Seconds Time Register

Function:	This register is incremented in 1/128-second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address:	A2H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 127 decimal

SEC—Seconds Time Register

Function:	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address:	A3H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

MIN—Minutes Time Register

Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address:	A4H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

HOUR—Hours Time Register

Function:	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address:	A5H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 23 decimal

To enable the TIC as a real-time clock, the HOUR, MIN, SEC, and HTHSEC registers can be loaded with the current time. Once the TCEN bit is high, the TIC starts. To use the TIC as a time interval counter, select the count interval—hundredths of seconds, seconds, minutes, and hours via the ITS0 and ITS1 bits in the TIMECON SFR. Load the count required into the INTVAL SFR.

Note that INTVAL is only an 8-bit register, so user software must take into account any intervals longer than are possible with 8 bits. Therefore, to count an interval of 20 seconds, use the following procedure:

```
MOV TIMECON, #0D0H ;Enable 24Hour mode, count seconds, Clear TCEN.
MOV INTVAL,  #14H  ;Load INTVAL with required count interval...in this case 14H = 20
MOV TIMECON, #0D3H ;Start TIC counting and enable the 8bit INTVAL counter.
```

8052-COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits that are available to the user on-chip. These features are mostly 8052-compatible (with a few additional features) and are controlled via standard 8052 SFR bit definitions.

Parallel I/O

The ADuC845/ADuC847/ADuC848 use four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some are capable of external memory operations, while others are multiplexed with alternate functions for the peripheral functions available on-chip. In general, when a peripheral is enabled, that pin cannot be used as a general-purpose I/O pin.

Port 0

Port 0 is an 8-bit open-drain bidirectional I/O port that is directly controlled via the Port 0 SFR (80H). Port 0 is also the multiplexed low-order address and data bus during accesses to external data memory.

Figure 48 shows a typical bit latch and I/O buffer for a Port 0 pin. The bit latch (one bit in the SFRof the port) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a write to latch signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a read latch signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a read pin signal from the CPU. Some instructions that read a port activate the read latch signal, and others activate the read pin signal. See the Read-Modify-Write Instructions section for details.

Figure 48. Port 0 Bit Latch and I/O Buffer

As shown in Figure 48, the output drivers of Port 0 pins are switchable to an internal ADDR and ADDR/DATA bus by an internal control signal for use in external memory accesses. During external memory accesses, the P0 SFR has 1s written to it; therefore, all its bit latches become 1. When accessing external memory, the control signal in Figure 48 goes high, enabling push-pull operation of the output pin from the internal address or data bus (ADDR/DATA line). Therefore, no external pull-ups are required on Port 0 for it to access external memory.

In general-purpose I/O port mode, Port 0 pins that have 1s written to them via the Port 0 SFR are configured as open-drain and, therefore, float. In this state, Port 0 pins can be used as high impedance inputs. This is represented in Figure 48 by the NAND gate whose output remains high as long as the control signal is low, thereby disabling the top FET. External pull-up resistors are, therefore, required when Port 0 pins are used as general-purpose outputs. Port 0 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

Port 1

Port 1 is also an 8-bit port directly controlled via the P1 SFR (90H). Port 1 digital output capability is not supported on this device. Port 1 pins can be configured as digital inputs or analog inputs. By (power-on) default, these pins are configured as analog inputs, that is, 1 is written to the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a 0 to these port bits to configure the corresponding pin as a high impedance digital input. These pins also have various secondary functions aside from their analog input capability, as described in Table 46.

Table 46. Port 1 Alternate Functions

Pin No.	Alternate Function
P1.2	REFIN2+ (second reference input, postive)
P1.3	REFIN2− (second reference input, negative)
P1.6	IEXC1 (200 µA excitation current source)
P1.7	IEXC2 (200 µA excitation current source)

Figure 49. Port 1 Bit Latch and I/O Buffer

Port 2

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR. Port 2 also emits the middle- and high-order address bytes during accesses to the 24-bit external data memory space.

In general-purpose I/O port mode, Port 2 pins that have 1s written to them are pulled high by the internal pull-ups as shown in Figure 50 and, in that state, can be used as inputs. As inputs, Port 2 pins pulled externally low source current because of the internal pull-up resistors. Port 2 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

P2.5 and P2.6 can also be used as PWM outputs, while P2.7 can act as an alternate PWM clock source. When selected as the PWM outputs, they overwrite anything written to P2.5 or P2.6.

Table 47. Port 2 Alternate Functions

Pin No.	Alternate Function
P2.0	SCLOCK for SPI
P2.1	MOSI for SPI
P2.2	MISO for SPI
P2.3	$\overline{SS}$ and T2 clock input
P2.4	T2EX alternate control for T2
P2.5	PWM0 output
P2.6	PWM1 output
P2.7	PWMCLK

Figure 50. Port 2 Bit Latch and I/O Buffer

Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 48. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin remains at 0.

Table 48. Port 3 Alternate Functions

Pin No.	Alternate Function
P3.0	RxD (UART input pin, or serial data I/O in Mode 0)
P3.1	TxD (UART output pin, or serial clock output in Mode 0)
P3.2	$\overline{INT0}$ (External Interrupt 0)
P3.3	$\overline{INT1}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Figure 51. Port 3 Bit Latch and I/O Buffer

Read-Modify-Write Instructions

Some 8051 instructions read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and rewrite it to the latch. These are called read-modify-write instructions, which are listed in Table 49. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 49. Read-Modify-Write Instructions

Instruction	Description
ANL	Logical AND, for example, ANL P1, A
ORL	Logical OR, for example, ORL P2, A
XRL	Logical EX-OR, for example, XRL P3, A
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL
CPL	Complement bit, for example, CPL P3.0
INC	Increment, for example, INC P2
DEC	Decrement, for example, DEC P2
DJNZ	Decrement and jump if not zero, for example, DJNZ P3, LABEL
MOV PX.Y, C[1]	Move Carry to Bit Y of Port X
CLR PX.Y[1]	Clear Bit Y of Port X
SETB PX.Y[1]	Set Bit Y of Port X

[1] These instructions read the port byte (all 8 bits), modify the addressed bit, and write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

TIMERS/COUNTERS

The ADuC845/ADuC847/ADuC848 have three 16-bit timer/counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware is included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2). All three can be configured to operate either as timers or as event counters.

When functioning as a timer, the TLx register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Because a machine cycle on a single-cycle core consists of one core clock period, the maximum count rate is the core clock frequency.

When functioning as a counter, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin:

TMOD—Timer/Counter 0 and 1 Mode Register

SFR Address: 89H
Power-On Default: 00H
Bit Addressable: No

T0, T1, or T2. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. Because it takes two machine cycles (two core clock periods) to recognize a 1-to-0 transition, the maximum count rate is half the core clock frequency.

There are no restrictions on the duty cycle of the external input signal, but, to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. User configuration and control of all timer operating modes is achieved via three SFRs:

TMOD, TCON—Control and Configuration for Timers 0 and 1

T2CON—Control and Configuration for Timer 2.

Table 50. TMOD SFR Bit Designation

Bit No.	Name	Description
7	Gate	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while the $\overline{INT1}$ pin is high and the TR1 control is set. Cleared by software to enable Timer 1 whenever the TR1control bit is set.
6	C/T	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select the timer operation (input from internal system clock).
5, 4	M1, M0	Timer 1 Mode Select Bits. M1 M0 Description 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.
2	C/T	Timer 0 Timer or Counter Select Bit. Set by software to the select counter operation (input from T0 pin). Cleared by software to the select timer operation (input from internal system clock).
1, 0	M1, M0	Timer 0 Mode Select Bits. M1 M0 Description 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

TCON—Timer/Counter 0 and 1 Control Register

SFR Address: 88H
Power-On Default: 00H
Bit Addressable: Yes

Table 51. TCON SFR Bit Designations

Bit No.	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	IE1[1]	External Interrupt 1 ($\overline{\text{INT1}}$) Flag. Set by hardware by a falling edge or by a zero level applied to the external interrupt pin, $\overline{\text{INT1}}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
2	IT1[1]	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.
1	IE0[1]	External Interrupt 0 ($\overline{\text{INT0}}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{\text{INT0}}$, depending on the statue of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
0	IT0[1]	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.

[1] These bits are not used to control Timer/Counters 0 and 1, but are used instead to control and monitor the external $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ interrupt pins.

Timer/Counter 0 and 1 Data Registers

Each timer consists of two 8-bit registers. These can be used as independent registers or combined into a single 16-bit register, depending on the timers' mode configuration.

TH0 and TL0—Timer 0 high and low bytes.
SFR Address: 8CH and 8AH, respectively.
Power-On Default: 00H and 00H, respectively.

TH1 and TL1—Timer 1 high and low bytes.
SFR Address: 8DH and 8BH, respectively.
Power-On Default: 00H and 00H, respectively.

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

Figure 52. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.

Figure 53. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

Figure 54. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

Figure 55. Timer/Counter 0, Mode 3

T2CON—Timer/Counter 2 Control Register

SFR Address: C8H
Power-On Default: 00H
Bit Addressable: Yes

Table 52. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select the counter function (input from external T2 pin). Cleared by the user to select the timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and as timer capture/reload registers.

TH2 and TL2—Timer 2 data high byte and low byte.
SFR Address: CDH and CCH respectively.
Power-On Default: 00H and 00H, respectively.

RCAP2H and RCAP2L—Timer 2 capture/reload byte and low byte.
SFR Address: CBH and CAH, respectively.
Power-On Default: 00H and 00H, respectively.

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 53.

Table 53. T2CON Operating Modes

RCLK (or) TCLK	CAP2	TR2	Mode
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 56.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into Registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 57. The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur, so they do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts, which can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in the following section.

Figure 56. Timer/Counter 2, 16-Bit Autoreload Mode

Figure 57. Timer/Counter 2, 16-Bit Capture Mode

UART SERIAL INTERFACE

The serial port is full duplex, meaning that it can transmit and receive simultaneously. It is also receive buffered, meaning that it can begin receiving a second byte before a previously received byte is read from the receive register. However, if the first byte is still not read by the time reception of the second byte is complete, the first byte is lost. The physical interface to the serial data network is via Pins RxD(P3.0) and TxD(P3.1), while the SFR interface to the UART comprises SBUF and SCON, as described in this section.

SBUF SFR

Both the serial port receive and transmit registers are accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

SCON UART—Serial Port Control Register

SFR Address: 98H
Power-On Default: 00H
Bit Addressable: Yes

Table 54. SCON SFR Bit Designations

Bit No.	Name	Description
7, 6	SM0, SM1	UART Serial Mode Select Bits. These bits select the serial port operating mode as follows: SM0 SM1 Selected Operating Mode. 0 0 Mode 0: Shift register, fixed baud rate (Core_Clk/2). 0 1 Mode 1: 8-bit UART, variable baud rate. 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/32) or (Core_Clk/16). 1 1 Mode 3: 9-bit UART, variable baud rate.
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit was not received. If SM2 is cleared, RI is set as soon as the byte of data is received. In Modes 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.
4	REN	Serial Port Receive Enable Bit. Set by user software to enable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 is the ninth data bit transmitted in Modes 2 and 3. Cleared by user software to disable serial port reception.
2	RB8	Serial Port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Serial Port Transmit Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by software.

SBUF—UART Serial Port Data Register

SFR Address: 99H
Power-On Default: 00H
Bit Addressable: No

Mode 0 (8-Bit Shift Register Mode)

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line as shown in Figure 58.

Figure 58. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, 10 bits are transmitted on TxD or are received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write to SBUF signal also loads a 1 (stop bit) into the 9th bit position of the transmit shift register. The data is output bit-by-bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 59.

Figure 59. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The start bit is skipped and the 8 data bits are clocked into the serial port shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th bit (stop bit) is clocked into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is *not* met, the received frame is irretrievably lost, and RI is not set.

Mode 2 (9-Bit UART with Fixed Baud Rate)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received: a start bit (0), 8 data bits, a programmable 9th bit, and a stop bit (1). The 9th bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the 8 data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the 8 data bits (from SBUF) are loaded into the transmit shift register (LSB first). The contents of TB8 are loaded into the 9th bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TxD.

Reception for Mode 2 is similar to that of Mode 1. The 8 data bytes are input at RxD (LSB first) and loaded onto the receive shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th data bit is latched into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ Clock\ Frequency}{(16 \times [65536 - (RCAP\ 2H : RCAP\ 2L)])}$$

Figure 60. Timer 2, UART Baud Rates

Timer 3 Generated Baud Rates

The high integer dividers in a UART block mean that high speed baud rates are not always possible. Also, generating baud rates requires the exclusive use of a timer, rendering it unusable for other applications when the UART is required. To address this problem, the ADuC845/ADuC847/ADuC848 have a dedicated baud rate timer (Timer 3) specifically for generating highly accurate baud rates. Timer 3 can be used instead of Timer 1 or Timer 2 for generating very accurate high speed UART baud rates including 115200 and 230400. Timer 3 also allows a much wider range of baud rates to be obtained. In fact, every desired bit rate from 12 bps to 393216 bps can be generated to within an error of ±0.8%. Timer 3 also frees up the other three timers, allowing them to be used for different applications. A block diagram of Timer 3 is shown in Figure 61.

Figure 61. Timer 3, UART Baud Rate

Two SFRs (T3CON and T3FD) are used to control Timer 3. T3CON is the baud rate control SFR, allowing Timer 3 to be used to set up the UART baud rate, and to set up the binary divider (DIV).

The appropriate value to write to the DIV2-1-0 bits can be calculated using the following formula where f_{CORE} is defined in PLLCON SFR. Note that the DIV value must be rounded down.

$$DIV = \frac{\log\left(\frac{Core\ Clock\ Frequency}{16 \times Baud\ Rate}\right)}{\log(2)}$$

T3FD is the fractional divider ratio required to achieve the required baud rate. The appropriate value for T3FD can be calculated with the following formula:

$$T3FD = \frac{2 \times Core\ Clock\ Frequency}{2^{DIV-1} \times Baud\ Rate} - 64$$

Note that T3FD should be rounded to the nearest integer. Once the values for DIV and T3FD are calculated, the actual baud rate can be calculated with the following formula:

$$Actual\ Baud\ Rate = \frac{2 \times Core\ Clock\ Frequency}{2^{DIV-1} \times (T3FD + 64)}$$

For example, to get a baud rate of 9600 while operating at a core clock frequency of 1.5725 MHz, that is, CD = 3,

$$DIV = \log(1572500/(16 \times 9600))/\log 2 = 3.35 = 3$$

Note that the DIV result is rounded down.

$$T3FD = (2 \times 1572500)/(2^{3-1} \times 9600) - 64 = 18 = 12H$$

Therefore, the actual baud rate is 9588 bps, which gives an error of 0.12%.

The T3CON and T3FD registers are used to control Timer 3.

T3CON – Timer 3 Control Register

SFR Address:	9EH
Power-On Default:	00H
Bit Addressable:	No

Table 55. T3CON SFR Bit Designations

Bit No.	Name	Description
7	T3BAUDEN	T3UARTBAUD Enable. Set to enable Timer 3 to generate the baud rate. When set, PCON.7, T2CON.4, and T2CON.5 are ignored. Cleared to let the baud rate be generated as per a standard 8052.
6		Not Implemented. Write Don't Care.
5		Not Implemented. Write Don't Care.
4		Not Implemented. Write Don't Care.
3		Not Implemented. Write Don't Care.
2, 1, 0	DIV2, DIV1, DIV0	Binary Divider DIV2 DIV1 DIV0 0 0 0 Binary Divider 0. See Table 57. 0 0 1 Binary Divider 1. See Table 57. 0 1 0 Binary Divider 2. See Table 57. 0 1 1 Binary Divider 3. See Table 57. 1 0 0 Binary Divider 4. See Table 57. 1 0 1 Binary Divider 5. See Table 57. 1 1 0 Binary Divider 6. See Table 57.

T3FD—Timer 3 Fractional Divider Register

See Table 57 for values.

SFR Address: 9DH
Power-On Default: 00H
Bit Addressable: No

Table 56. T3FD SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	----	Not Implemented. Write Don't Care.
5	T3FD.5	Timer 3 Fractional Divider Bit 5.
4	T3FD.4	Timer 3 Fractional Divider Bit 4.
3	T3FD.3	Timer 3 Fractional Divider Bit 3.
2	T3FD.2	Timer 3 Fractional Divider Bit 2.
1	T3FD.1	Timer 3 Fractional Divider Bit 1.
0	T3FD.0	Timer 3 Fractional Divider Bit 0.

Table 57. Common Baud Rates Using Timer 3 with a 12.58 MHz PLL Clock

Ideal Baud	CD	DIV	T3CON	T3FD	% Error
230400	0	1	81H	2DH	0.18
115200	0	2	82H	2DH	0.18
115200	1	1	81H	2DH	0.18
57600	0	3	83H	2DH	0.18
57600	1	2	82H	2DH	0.18
57600	2	1	81H	2DH	0.18
38400	0	4	84H	12H	0.12
38400	1	3	83H	12H	0.12
38400	2	2	82H	12H	0.12
38400	3	1	81H	12H	0.12
19200	0	5	85H	12H	0.12
19200	1	4	84H	12H	0.12
19200	2	3	83H	12H	0.12
19200	3	2	82H	12H	0.12
19200	4	1	81H	12H	0.12
9600	0	6	86H	12H	0.12
9600	1	5	85H	12H	0.12
9600	2	4	84H	12H	0.12
9600	3	3	83H	12H	0.12
9600	4	2	82H	12H	0.12
9600	5	1	81H	12H	0.12

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

IEIP2—Secondary Interrupt Enable Register

SFR Address: A9H
Power-On Default: A0H
Bit Addressable: No

Table 60. IEIP2 Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	PTI	Time Interval Counter Interrupt Priority Setting (1 = High, 0 = Low).
5	PPSM	Power Supply Monitor Interrupt Priority Setting (1 = High, 0 = Low).
4	PSI	SPI/I²C Interrupt Priority Setting (1 = High, 0 = Low).
3	----	This bit must contain 0.
2	ETI	Set by the user to enable the time interval counter interrupt. Cleared by the user to disable the time interval counter interrupt.
1	EPSMI	Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	Set by the user to enable the SPI/I²C serial port interrupt. Cleared by the user to disable the SPI/I²C serial port interrupt.

INTERRUPT PRIORITY

The interrupt enable registers are written by the user to enable individual interrupt sources; the interrupt priority registers allow the user to select one of two priority levels for each interrupt. A high priority interrupt can interrupt the service routine of a low priority interrupt, and if two interrupts of different priorities occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, the polling sequence, as shown in Table 61, is observed.

Table 61. Priority within Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Timer Interrupt
IE0	2	External Interrupt 0
RDY0/RDY1	3	ADC Interrupt
TF0	4	Timer/Counter 0 Interrupt
IE1	5	External Interrupt 1
TF1	6	Timer/Counter 1 Interrupt
ISPI/I2CI	7	SPI/I²C Interrupt
RI/TI	8	UART Serial Port Interrupt
TF2/EXF2	9	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Timer Interval Counter Interrupt

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 62.

Table 62. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
RDY0/RDY1 (ADuC845 only)	0033H
ISPI/I2CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

HARDWARE DESIGN CONSIDERATIONS

This section outlines some of the key hardware design considerations that must be addressed when integrating the ADuC845/ADuC847/ADuC848 into any hardware system.

EXTERNAL MEMORY INTERFACE

In addition to their internal program and data memories, the devices can access up to 16 Mbytes of external data memory (SRAM). No external program memory access is available.

To begin executing code, tie the $\overline{EA}$ (external access) pin high. When $\overline{EA}$ is high (pulled up to V_{DD}—see Figure 70), user program execution starts at Address 0 in the internal 62-kbyte Flash/EE code space. When executing from internal code space, accesses to the program space above F7FFH (62 kbytes) are read as NOP instructions.

Note that a second very important function of the $\overline{EA}$ pin is described in the Single-Pin Emulation Mode section under the Other Hardware Considerations section.

Figure 62 shows a hardware configuration for accessing up to 64 kbytes of external data memory. This interface is standard to any 8051-compatible MCU.

Figure 62. External Data Memory Interface (64-kbyte Address Space)

If access to more than 64 kbytes of RAM is desired, a feature unique to the MicroConverter allows addressing up to 16 Mbytes of external RAM simply by adding another latch as shown in Figure 63.

Figure 63. External Data Memory Interface (16-Mbtye Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by ALE prior to data being placed on the bus by the devices (write operation) or the external data memory (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64-kbyte external data memory access is maintained.

The following example shows the code used to write data to external data memory.

```
MOV DPP, #10h ;Set addr to 100000h
MOV DPH, #00h
MOV DPL, #00h
MOV A,   #'B' ;Write Char ‘B’ (42h)
MOVX @DPTR,A  ;Move to DPP:DPH:DPL addr
```

POWER SUPPLIES

The operational power supply voltage range of the device is 2.7 V to 5.25 V. Although the guaranteed data sheet specifications are given only for power supplies within 2.7 V to 3.6 V and 4.75 V to 5.25 V (±5% of the nominal 5 V level), the chip functions equally well at any power supply level between 2.7 V and 5.25 V.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD}, respectively) allow AV_{DD} to be kept relatively free of the noisy digital signals often present on a system DV_{DD} line. In this mode, the device can also operate with split supplies, that is, using different voltage supply levels for each supply. For example, the system can be designed to operate with a DV_{DD} voltage level of 3 V and the AV_{DD} level can be at 5 V, or vice versa, if required. A typical split-supply configuration is shown in Figure 64.

Figure 64. External Dual-Supply Connections (56-Lead LFCSP Pin Numbering)

As an alternative to providing two separate power supplies, AV_{DD} can be kept quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 65. In this configuration, other analog circuitry (such

as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

Figure 65. External Single-Supply Connections (56-Lead LFCSP Pin Numbering)

Notice that in both Figure 64 and Figure 65 a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local decoupling capacitors (0.1 µF) are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are closer than the 10 µF capacitors to each V_{DD} pin with lead lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that, at all times, the analog and digital ground pins on the device must be referenced to the same system ground reference point. It is recommended that the LFCSP paddle be soldered to ensure mechanical stability but be floated with respect to system V_{DD}s or grounds.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC845/ADuC847/ADuC848.

3 V Part

For DV_{DD} below 2.63 V, the internal POR holds the device in reset. As DV_{DD} rises above 2.63 V, an internal timer times out for typically 128 ms before the device is released from reset. The user must ensure that the power supply has at least reached a stable 2.7 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 66 illustrates the operation of the internal POR.

Figure 66. 3 V Part POR operation

5 V Part

For DV_{DD} below 4.5 V, the internal POR holds the device in reset. As DV_{DD} rises above 4.5 V, an internal timer times out for approximately 128 ms before the device is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 67 illustrates this operation.

Figure 67. 5 V Part POR Operation

POWER CONSUMPTION

The DV_{DD} power supply current consumption is specified in normal and power-down modes. The AV_{DD} power supply current is specified with the analog peripherals disabled. The normal mode power consumption represents the current drawn from DV_{DD} by the digital core. The other on-chip peripherals (such as the watchdog timer and power supply monitor) consume negligible current and are therefore included with the normal operating current. The user must add any currents sourced by the parallel and serial I/O pins, and those sourced by the DAC to determine the total current needed at the ADuC845/ADuC847/ADuC848 DV_{DD} and AV_{DD} supply pins. Also, current drawn from the DV_{DD} supply increases by approximately 5 mA during Flash/EE erase and program cycles.

POWER-SAVING MODES

Setting the power-down mode bit, PCON.1, in the PCON SFR described in Table 6, allows the chip to be switched from normal mode into full power-down mode.

In power-down mode, both the PLL and the clock to the core are stopped. The on-chip oscillator can be halted or can continue to oscillate, depending on the state of the oscillator power-down bit (OSC_PD) in the PLLCON SFR. The TIC, driven directly from the oscillator, can also be enabled during power-down. However, all other on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state) while ALE and $\overline{PSEN}$ outputs are held low. There are five ways to terminate power-down mode:

- **Asserting the RESET Pin**
  Returns to normal mode. All registers are set to their reset default value and program execution starts at the reset vector once the RESET pin is de-asserted.

- **Cycling Power**
  All registers are set to their default state and program execution starts at the reset vector approximately 128 ms later.

- **Time Interval Counter (TIC) Interrupt**
  If the OSC_PD bit in the PLLCON SFR is clear, the 32 kHz oscillator remains powered up even in power-down mode. If the time interval counter (wake-up/RTC timer) is enabled, a TIC interrupt wakes the device from power-down mode. The CPU services the TIC interrupt. The RETI at the end of the TIC ISR returns the core to the next instruction after that one the enabled power-down.

- **SPI Interrupt**
  If the SERIPD bit in the PCON SFR is set, an SPI interrupt, if enabled, wakes up the device from power-down mode. The CPU services the SPI interrupt. The RETI at the end of the ISR returns the core to the next instruction after the one that enabled power-down.

- **$\overline{\text{INT0}}$ Interrupt**
  If the INT0PD bit in the PCON SFR is set, an external interrupt 0, if enabled, wakes up the device from power-down. The CPU services the interrupt. The RETI at the end of the ISR returns the core to the next instruction after the one that enabled power-down.

Wake-Up from Power-Down Latency

Even with the 32 kHz crystal enabled during power-down, the PLL takes some time to lock after a wake-up from power-down. Typically, the PLL takes about 1 ms to lock. During this time, code executes, but not at the specified frequency. Some operations, for example, UART communications, require an accurate clock to achieve the specified 50 Hz/60 Hz rejection from the ADCs. Therefore, it is advisable to wait until the PLL has locked before proceeding with normal code execution. The following code can be used to wait for the PLL to lock:

```
WAITFORLOCK:  MOV  A, PLLCON
              JNB  ACC.6, WAITFORLOCK
```

If the crystal is powered down during power-down, an additional delay is associated with the startup of the crystal oscillator before the PLL can lock. Typically taking about 150 ms, 32 kHz crystals are inherently slow to oscillate. During this time before lock, code executes, but the exact frequency of the clock cannot be guaranteed. For any timing-sensitive operations, it is recommended to wait for lock by using the lock bit in PLLCON as previously shown.

An alternative way of saving power in power-down mode is to slow down the core clock by using the CD bits in the PLLCON register.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of ADuC845/ADuC847/ADuC848-based designs to achieve optimum performance from the ADCs and DAC.

Although the devices have separate pins for analog and digital ground (AGND and DGND), the user must not tie these to separate ground planes unless the two ground planes are connected together very close to the device as shown in the simplified example in Figure 68 (a). In systems where digital and analog ground planes are connected together somewhere else (at the system's power supply, for example), they cannot be connected again near the device since a ground loop would result. In these cases, tie the AGND and DGND pins of the device to the analog ground plane, as shown in Figure 68 (b). In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board such that digital return currents do not flow near analog circuitry and vice versa. The parts can then be placed between the digital and analog sections, as shown in Figure 68 (c).

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. For example, do not power components on the analog side of Figure 68 (b) with DV_{DD} since that would force return currents from DV_{DD} to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which may happen if the user placed a noisy digital chip on the left half of the board in Figure 68 (c). Whenever possible, avoid large discontinuities in the ground plane(s) (such as are formed by a long trace on the same layer), since they force return signals to travel a longer path. Make all connections directly to the ground plane, with little or no trace separating the pin from its via to ground.

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

Figure 70. UART Connectivity in Typical System

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 70. To get the devices into download mode, connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is ready to receive a new program serially. With the jumper removed, the device powers on in normal mode (and runs the program) whenever power is cycled or RESET is toggled. Note that $\overline{\text{PSEN}}$ is normally an output and that it is sampled as an input only on the falling edge of RESET, that is, at power-on or upon an external manual reset. Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-on or reset events, it may cause the chip to enter download mode and fail to begin user code execution. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself or the method of download entry in use during a reset or power-cycle condition.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described previously. In fact, both serial download and serial port debug modes are essentially one mode of operation used in two different ways.

The serial port debugger is fully contained on the device, unlike ROM monitor type debuggers, and, therefore, no external memory is needed to enable in-system debug sessions.

Single-Pin Emulation Mode

Built into the ADuC845/ADuC847/ADuC848 is a dedicated controller for single-pin in-circuit emulation (ICE). In this mode, emulation access is gained by connection to a single pin, the $\overline{EA}$ pin. Normally on the 8051 standard, this pin is hardwired either high or low to select execution from internal or external program memory space. Note that external program memory or execution from external program memory is not allowed on the devices. To enable single-pin emulation mode, users need to pull the $\overline{EA}$ pin high through a 1 kΩ resistor as shown in Figure 70. The emulator then connects to the 2-pin header also shown in Figure 70. To be compatible with the standard connector that comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch Friction Lock header from Molex (www.molex.com) such as part number 22-27-2021. Be sure to observe the polarity of this header. As shown in Figure 70, when the Friction Lock tab is at the right, the ground pin should be the lower of the two pins when viewed from the top.

Typical System Configuration

A typical ADuC845/ADuC847/ADuC848 configuration is shown in Figure 70. Figure 70 also includes connections for a typical analog measurement application of the devices, namely an interface to a resistive temperature device (RTD). The arrangement shown is commonly referred to as a 4-wire RTD configuration.

Here, the on-chip excitation current sources are enabled to excite the sensor. The excitation current flows directly through the RTD generating a voltage across the RTD proportional to its resistance. This differential voltage is routed directly to one set of the positive and negative inputs of the ADC (AIN1, AIN2, respectively in this case). The same current that excited the RTD also flows through a series resistance, R_{REF}, generating a ratiometric voltage reference, V_{REF}. The ratiometric voltage reference ensures that variations in the excitation current do not affect the measurement system since the input voltage from the RTD and reference voltage across R_{REF} vary ratiometrically with the excitation current. Resistor R_{REF} must, however, have a low temperature coefficient to avoid errors in the reference voltage overtemperature. R_{REF} must also be large enough to generate at least a 1 V voltage reference.

The preceding example shows just a single differential ADC connection using a single reference input pair. The ADuC845/ADuC847/ADuC848 have the capability of connecting to five differential inputs directly or ten single-ended inputs (LFCSP package only) as well as having a second reference input. This arrangement means that different sensors with different reference ranges can be connected to the device with the need for external multiplexing circuitry. This arrangement is shown in Figure 71. The bridge sensor shown can be a load cell or a pressure sensor. The RTD is shown using a reference voltage derived from the R_{REF} resistor via the REFIN± inputs, and the bridge sensor is shown using a divided down AV_{DD} reference via the REFIN2± inputs.

Figure 71. Dual Reference Typical Connectivity

QuickStart DEVELOPMENT SYSTEM

The QuickStart Development System is an entry-level, low cost development tool suite supporting the ADuC8xx MicroConverter product family. The system consists of the following PC-based (Windows®-compatible) hardware and software development tools:

Hardware:	Evaluation board and serial port programming cable.
Software:	Serial download software.
Miscellaneous:	CD-ROM documentation and prototype evaluation board.

A brief description of some of the software tools and components in the QuickStart system follows.

Download—In-Circuit Serial Downloader

The serial downloader is a Windows application that allows the user to serially download an assembled program (Intel® hexa-decimal format file) to the on-chip program flash memory via the serial COM port on a standard PC. The AN-1074 Application Note details this serial download protocol.

ASPIRE—IDE

The ASPIRE® integrated development environment is a Windows application that allows the user to compile, edit, and debug code in the same environment. The ASPIRE software allows users to debug code execution on silicon using the MicroConverter UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step, animate (automatic single stepping), and break-point code execution control.

Note that the ASPIRE IDE is also included as part of the QuickStart-PLUS system. As part of the QuickStart-PLUS system the ASPIRE IDE also supports mixed level and C source debugging. This is not available in the QuickStart system where the program is limited to assembly only.

QuickStart-PLUS DEVELOPMENT SYSTEM

The QuickStart-PLUS development system offers users enhanced nonintrusive debug and emulation tools. The system consists of the following PC-based (Windows-compatible) hardware and software development tools:

Hardware:	Prototype Board, Accutron NonIntrusive Single-Pin Emulator.
Software:	ASPIRE Integrated Development Environment. Features full C and Assembly emulation using the Accutron single-pin emulator.
Miscellaneous:	CD-ROM documentation.

TIMING SPECIFICATIONS

AC inputs during testing are driven at DV_{DD} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 72.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 72.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 64. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	Typ	Max	Unit
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	0.098	1.57	12.58	MHz
t_{CORE}	Core Clock Period[2]		0.636		µs
t_{CYC}	Machine Cycle Time[3]	10.2	0.636	0.08	µs

[1] ADuC845/ADuC847/ADuC848 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[2] This number is measured at the default Core_Clk operating frequency of 1.57 MHz.
[3] ADuC845/ADuC847/ADuC848 machine cycle time is nominally defined as 1/Core_Clk.

Figure 72. Timing Waveform Characteristics

Table 65. EXTERNAL DATA MEMORY READ CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{RLRH}	$\overline{RD}$ Pulse Width	60		125		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	145		290		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		48		100	ns
t_{RHDX}	Data and Address Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		150		625	ns
t_{LLDV}	ALE Low to Valid Data In		170		350	ns
t_{AVDV}	Address to Valid Data In		230		470	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	130		255		ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		15		35	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		120		ns

Figure 73. External Data Memory Read Cycle

Table 66. EXTERNAL DATA MEMORY WRITE CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{WLWH}	$\overline{WR}$ Pulse Width	65		130		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	65		135		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		130		260	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	60		120		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	120		250		ns
t_{WHQX}	Data and Address Hold After $\overline{WR}$	380		755		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		125		ns

Figure 74. External Data Memory Write Cycle

Table 67. I²C-COMPATIBLE INTERFACE TIMING Parameter

Parameter		Min	Max	Unit
t_L	SCLCK Low Pulse Width	1.3		µs
t_H	SCLCK High Pulse Width	0.6		µs
t_{SHD}	Start Condition Hold Time	0.6		µs
t_{DSU}	Data Setup Time	100		µs
t_{DHD}	Data Hold Time		0.9	µs
t_{RSU}	Setup Time for Repeated Start	0.6		µs
t_{PSU}	Stop Condition Setup Time	0.6		µs
t_{BUF}	Bus Free Time Between a Stop Condition and a Start Condition	1.3		µs
t_R	Rise Time of Both SCLCK and SDATA		300	ns
t_F	Fall Time of Both SCLCK and SDATA		300	ns
t_{SUP}[1]	Pulse Width of Spike Suppressed		50	ns

[1] Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

Figure 75. I²C-Compatible Interface Timing

Table 68. SPI MASTER MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

Figure 76. SPI Master Mode Timing (CHPA = 1)

Table 69. SPI MASTER MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup Before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

Figure 77. SPI Master Mode Timing (CHPA = 0)

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

Figure 78. SPI Slave Mode Timing (CHPA = 1)

Table 71. SPI SLAVE MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{DOSS}	Data Output Valid After $\overline{SS}$ Edge			20	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge				ns

Figure 79. SPI Slave Mode Timing (CHPA = 0)

Table 72. UART TIMING (SHIFT REGISTER MODE) Parameter

		12.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		954			$12t_{core}$		ns
TQVXH	Output Data Setup to Clock	662						ns
TDVXH	Input Data Setup to Clock	292						ns
TXHDX	Input Data Hold After Clock	0						ns
TXHQX	Output Data Hold After Clock	22						ns

Figure 80. UART Timing in Shift Register Mode

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-112-AC-2

Figure 81. 52-Lead Metric Quad Flat Package [MQFP]
(S-52-2)
Dimensions shown in millimeters

*COMPLIANT TO JEDEC STANDARDS MO-220-WLLD-2
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 82. 56-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 8 mm Body and 0.75 mm Package Height
(CP-56-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.

NOTES

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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