AN 26.2

Implementation Guidelines for SMSC's USB553x Family of USB 3.0 Hub Devices

1 Introduction

This application note provides information on general printed circuit board layout considerations for SMSC's USB553x family of Hub Controller devices. To date, these include the USB5434, USB5534, USB5534B, USB5537, and USB5537B.

This information is broadly applicable to any of SMSC's USB 3.0 device implementations.

1.1 References

- Datasheets: USB5434, USB5534, USB5534B, USB5537, USB5537B Hub Controller devices
- Application Note: *AN18.15*
- Evaluation designs that are referenced in this document can be found on our web site.

1.2 Audience

This application note is written for readers that are familiar with PCB design, including signal integrity, differential signalling, and thermal management implementation concepts.

1.3 Objective

The goal of this document is to provide implementation information that specifically applies to designing PCBs using SMSC's USB553x family of Hub Controller devices.

1.4 Overview

Successful operation of SMSC's USB Hub Controllers requires special consideration for printed circuit board (PCB) layout. All SMSC Hub controllers contain a mix of sensitive analog circuitry, digital core logic, and high speed I/O circuitry. The PCB's design is part of the system circuit for all of these subsystems that can either enhance or detract from desired operation.

General issues such as placement and stack up are covered. Additionally, subsystem issues such as USB 2.0/3.0 signalling/impedance, crystal connections, and other critical circuits are discussed. Controlling EMI, system power distribution, and signal return path management will also be addressed.

The guidelines presented are specifically applicable to SMSC's USB553x family of Hub Controllers and supersede earlier notes for these devices. The following recommendations are based on SMSC's experience and knowledge and may be accepted or rejected. SMSC does not guarantee any design. Each company is ultimately responsible for determining the suitability of its own design.

2 Schematic Guidelines

Specific requirements and suggestions for the schematic implementation of the USB553x family are indicated in this section. Product datasheets specify basic circuit needs.

2.1 Chassis and Cable Ground

USB hub devices can be implemented in the following ways:

- embedded with a host controller
- embedded with a mix of inaccessible ports with embedded devices and user-accessible ports
- embedded with a mix of a host, inaccessible ports with embedded devices, and user-accessible ports
- a stand-alone hub

Each of these implementation details can affect the best method to use for connecting the chassis and USB cable shields to digital ground. The best way to make these connections will depend on the design's system details. Refer to the many reference documents and white papers on this topic available on the internet, especially those published by members of the USB consortium and providers of USB-enabled motherboards and devices.

SMSC has observed positive EMI and ESD behavior on stand-alone designs when connecting the USB cable shield to digital ground with an RC network (330 Ω resistor and a 0.1 µF capacitor in parallel) at each USB connector.

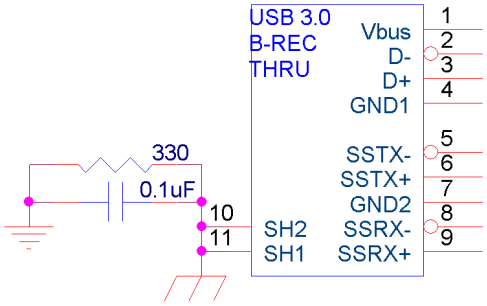


Figure 2.1 Example Chassis Ground Connection

2.2 VDD12 and VDD33 Power Regulator

The USB553x family of hubs use two external power voltages: VDD12 at 1.25 V, and VDD33 at 3.3 V.

The VDD12 rail is used for core digital functions and for the USB 3.0 PHYs. The VDD12 current consumed by the hub device will vary greatly. When the device is in "suspend" it will consume very little current. It will consume maximum current when all USB 3.0 SuperSpeed interfaces are active. The selected regulator must be stable and accurate across all power consumption ranges.

The VDD33 rail is used by the PLL and other circuitry. Therefore, the VDD33 supply must be very clean. Noise on VDD33 must be filtered out before it is received by the hub device. Some systems require < 5 mV of ripple on VDD33 at the hub device pins to pass SSC certification of the USB 3.0 test suite. Switching regulators are a common source for VDD33 noise. The example in Figure 2.2 shows an effective filter to block switching regulator noise from VDD33.

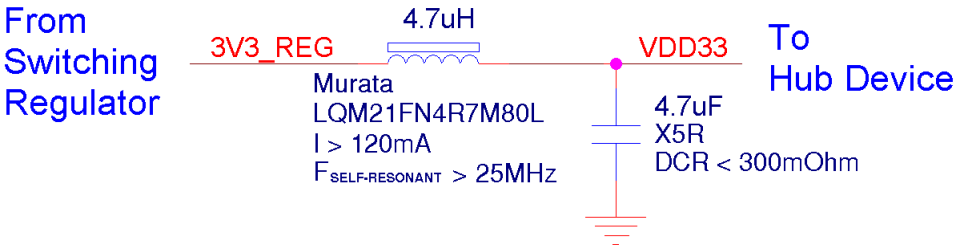


Figure 2.2 Example Switching Regulator Noise Filter

2.3 VBUS_DET

VBUS_DET is used to initiate a connect event to the hub device.

For stand-alone applications, this should be connected to the upstream VBUS through a resistor divider. The divider prevents back-powering the hub and reduces the VIN on the **VBUS_DET** pin. The 1.0 µF capacitor is required by the USB specification.

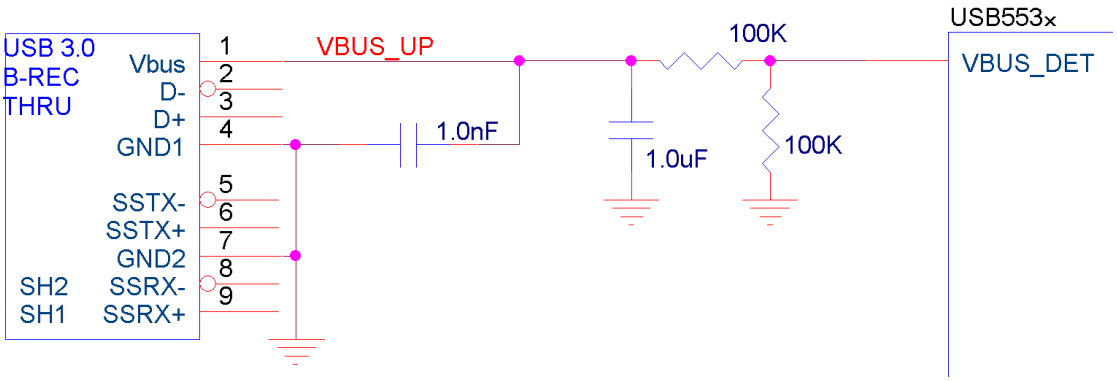


Figure 2.3 Stand-Alone VBUS_DET Connection

Embedded applications should actively control this pin with a 3.3 V signal.

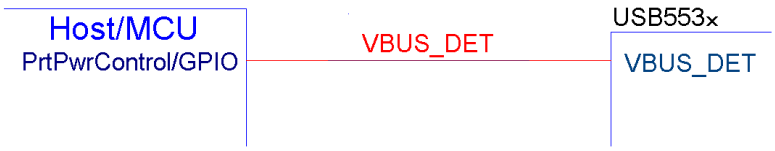


Figure 2.4 Embedded VBUS_DET Connection

VBUS_DET may also be tied directly to 3.3 V for certain always-on applications. This is not usually recommended.

2.4 RESETn

RESETn is used to force a reconfigure cycle and restart within the hub. This signal should be driven high only when all power rails are stable and within operational conditions.

For stand-alone applications, **RESETn** should be connected to a supervisory circuit that monitors VDD12 and VDD33. **RESETn** should be asserted when either voltage is below its threshold. **RESETn** could also be asserted under manual or host control. A simple RC circuit may be used for stand-alone

applications, but this only follows one voltage rail and may not work well when power is quickly removed then reapplied to the system, and is therefore not recommended.

For embedded applications, **RESETn** should be slaved to both a supervisory circuit and to the host controller.

2.5 In-System OTP Programming with the SM Port

In-system programming of the USB553x family of hubs is done through the **SM_DAT** and **SM_CLK** pins and by manipulating the **RESETn** pin. Be sure to provide access to these signals on the system board (plus ground) to program the hub device.

Initially, **SM_DAT** must be pulled up with a 10 KΩ resistor and **SM_CLK** pulled down with a 10 KΩ resistor. **SM_CLK** is then pulled up with a 1 KΩ resistor during programming (usually with a resistor in the programmer). When the programmer is removed and the system is reset, the new code takes effect.

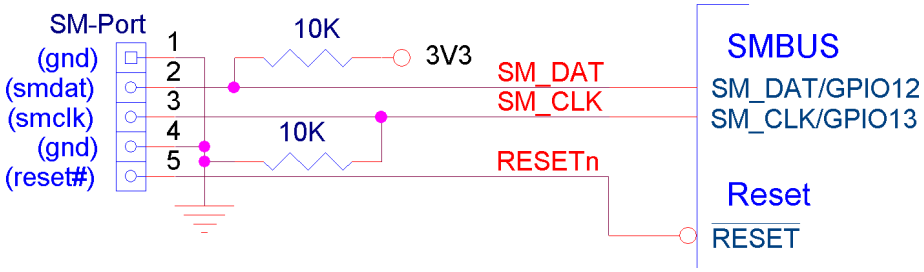


Figure 2.5 Provision for In-System Programming

2.6 OCS Capacitors

Place 10 KΩ resistors and 0.1 µF capacitors on the OCS lines to prevent ESD events from occasionally causing false OCS triggers. Place the capacitors as close as possible to the hub device pins.

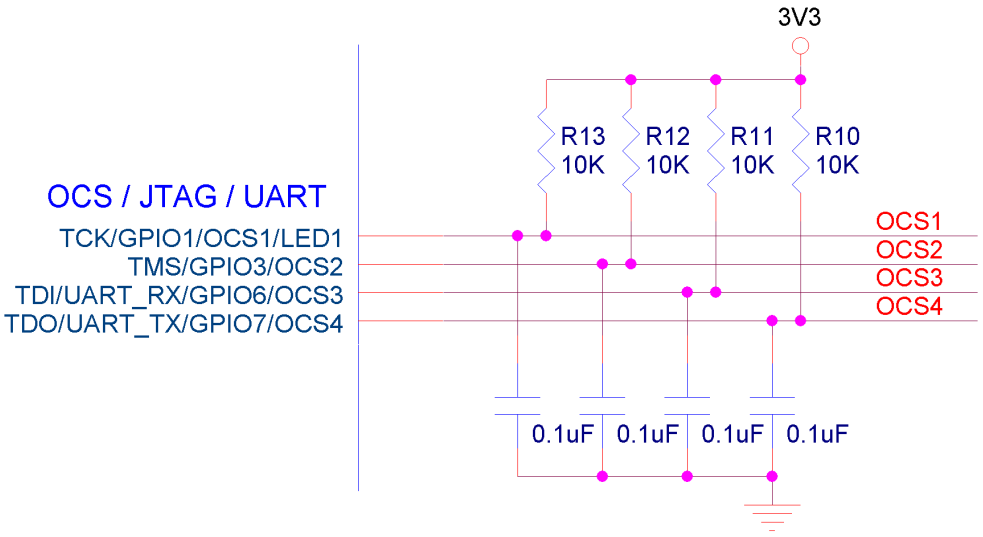


Figure 2.6 OCS ESD Capacitors

3 PCB Layout Guidelines

Specific requirements and suggestions for the PCB system implementation of the USB553x family are indicated in this section.

3.1 Placement

SMSC USB hubs are designed to allow placement of all support components on the top side (the same side as the hub device) of the PCB. Prevent placement details from causing the signal routing to introduce unwanted currents into sensitive lines.

1. Place the bypass capacitors as close as possible to the hub power pins. The 1.0 µF and larger capacitors indicated in the datasheets are part of the internal regulator circuits and should also be placed near the pins indicated. These capacitors are usually less effective if they are placed on the bottom of the PCB because of the intervening via inductances.
2. Place the **RBIAS** resistor close to its pin.
3. Place the crystal components near the related hub device crystal pins.
4. Place electrically noisy devices, including switching regulators, far away from the hub device and support circuits. Avoid placing or routing noisy circuits near the sensitive **RBIAS** resistor, its signal trace, its ground return path, the crystal circuit, and the USB differential pair signals.
5. ESD protection devices on the USB SuperSpeed lines will degrade SuperSpeed signalling, and therefore should only be used if needed. Place any ESD devices for the USB lines near the USB connectors. Follow the manufacturer's recommendations for placement and use.
6. Common mode chokes that are used for EMI or ESD purposes will degrade SuperSpeed (SS) signalling, and should only be used if proven to be needed. USB High-Speed (HS) signalling is somewhat less sensitive. Both the SuperSpeed (SS) (USB 3.0) and High-Speed (HS) (USB 2.0 and 3.0) chokes must be chosen carefully and must match the USB differential impedance of 90 Ω. Manufacturers typically only specify the common mode impedance. Special devices are currently advertised for USB 2.0 and USB 3.0 use, but must be confirmed for use in each application.
7. Place the **SS_TX** AC coupling capacitors near the USB connectors for more effective common-mode noise rejection. The USB specification calls out 0.1 µF ceramic capacitors for this application.

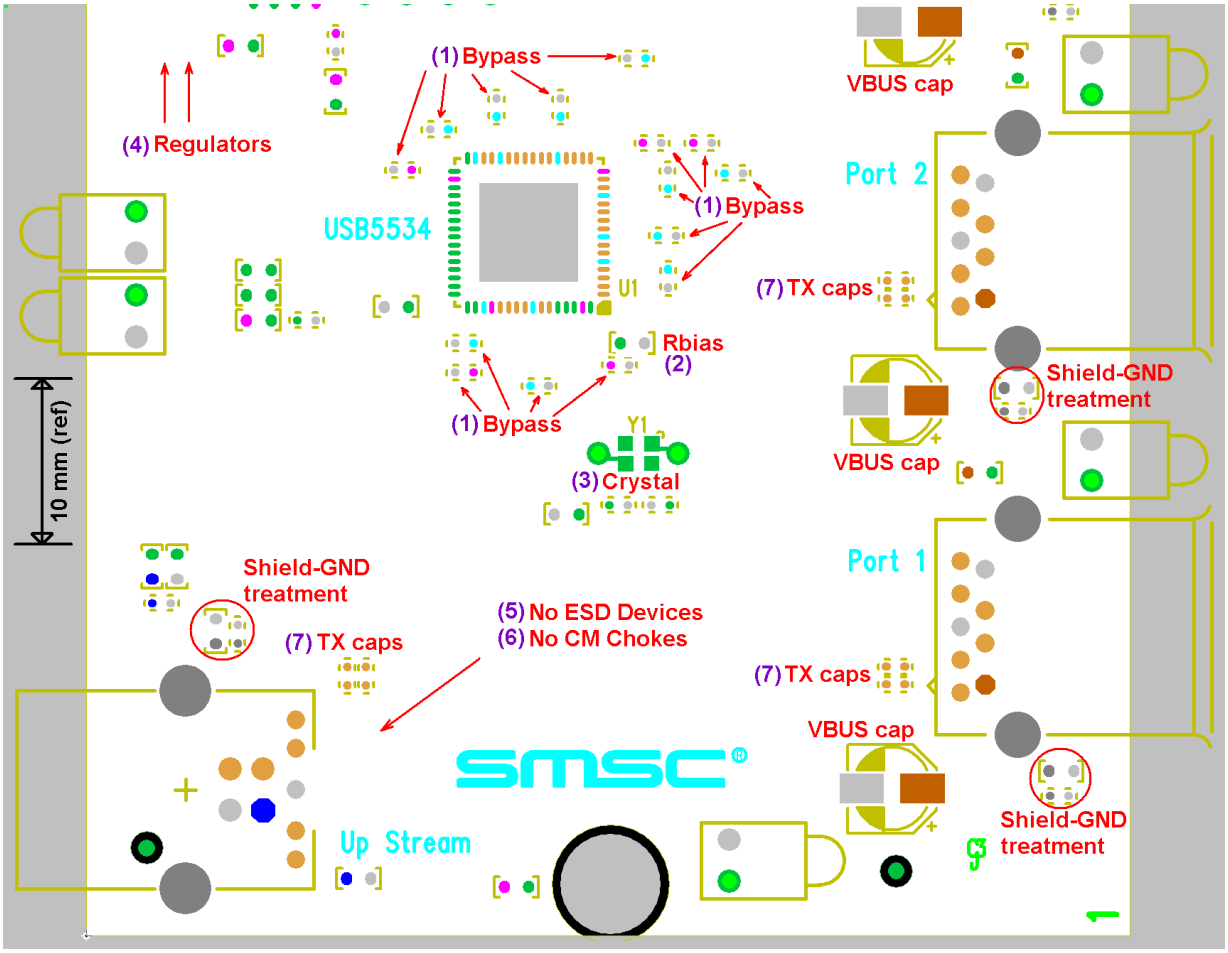


Figure 3.1 Example Analog Signal Considerations

3.2 PCB Construction

Elements of the PCB fabrication impact proper implementation of the USB553x family of hub devices.

3.2.1 PCB Materials

Signal losses for copper traces running on FR-4 materials can be very significant at USB 3.0 SuperSpeed (SS) signalling rates.

Ways to mitigate losses:

1. Keep SS traces as short as practical. This is the single most practical and cost-effective thing that can be done to reduce signal loss.
2. Route SS traces on outer layers, rather than on inner layers.
3. Consider laminates with lower DF and DK ratings. These lower loss materials include FR408HR, FR408HRIS, N4000-13SI, Rogers, Polyimide, etc.
4. Try to route SS signals at a 45^{o} angle to the material weave direction so that the trace does not occasionally line up with a high-resin, high-loss path.
5. Consider low-loss materials, like N4000-13SI or Rogers

3.2.2 Stack Up

The pinout of SMSC's USB553x family of hub devices allows for possible implementation on a two-layer structure. However, using more than two layers will provide greater control of impedances, return paths, and thermal management. The side on which the SMSC Hub device is mounted is designated layer one for reference.

1. When designing with greater than two layers, assign ground to layer two and flood the bottom layer with ground. For two-layer structures, flood the bottom layer with ground. (*Note: A two-layer structure will require a heat spreader, heat sink, or other specific thermal management.)
2. Choose a thin dielectric between layer one and ground to simplify attaining accurate impedance for critical lines, especially for the USB differential pairs. Make the boards as thin as practical.
3. Choose copper thicknesses of at least 1 oz./ft.^{2} to help with power delivery and thermal conduction.

The EVB reference designs have the following structures: four layers with ground on layer two, dielectric thickness of 0.1-0.117 mm (4-4.6 mil) between layers one (top) and two, with the same 0.1-0.117 mm (4-4.6 mil) between layers three and four (bottom). Inner copper thickness is 1 oz./ft.^{2} and outer copper thickness is 1.5 oz./ft.^{2} (finished).The overall thickness for the *EVB-USB5534_C* and the *EVB-USB5537_C* platforms is nominally 1.57 mm (62 mil).

These stackups allow for a 0.178 mm (7 mil) line to have a single-ended impedance of approximately 50 Ω, while a differential pair routed at 0.197 mm (7.75 mil) with a spacing of 0.185 mm (7.25 mil) yields an approximate differential impedance (Z_{diff}) of 90 Ω.

3.2.3 Impedance Control

Several signals in a USB hub design need to be impedance controlled, including the differential USB lines. Control the trace widths, spacings, copper thickness, and dielectric type and thicknesses to meet the following requirements:

1. The differential impedance of the USB differential pairs needs to be controlled to 90 Ω, +/- 10% (81-99 Ω). These paired signals are DP and DM for each USB 2.0 interface, and also SS_TX+ and SS_TX-, and SS_RX+ and SS_RX- for each USB 3.0 interface.
2. The connection of bypass capacitors to their pins, and to power and ground, need to be low inductance (short and very wide).
3. Due to relatively high operational load currents (from 900 mA to several Amps), the VBUS path to each downstream USB connector needs to be very low impedance.
4. The **RBIAS** connection and return path need to be relatively low inductance (short).
5. Adhere to the Section 3.4, "Power Distribution" guidelines.

3.3 Ground Distribution

The USB environment requires that the ground return paths across the system be implemented carefully and that they be substantial and contiguous. Employ "stitching vias" to connect ground floods between multiple layers and to terminate ground flood "spurs".

3.3.1 Flag is the Only Ground and Thermal Pad

QFN packages have one row of perimeter pads (*pads*) around a larger central pad (*flag* or *ePAD*) encapsulated in a plastic body. All ground connections from the SMSC Hub Controllers in QFN packaging are done through the device's *flag*. The flag is used for the following:

- The device's **only** signal ground (VSS)
- The primary thermal conduction path to remove package heat

To address these issues, constraints are imposed for the use of these packages, including filling the GND flag with a pattern of vias, especially around the periphery of the flag. Also use 1 oz. or higher copper weights on inner plane layers and 1.5 oz. or higher copper weights for outer layers, with a large, uninterrupted ground flood on the bottom layer.

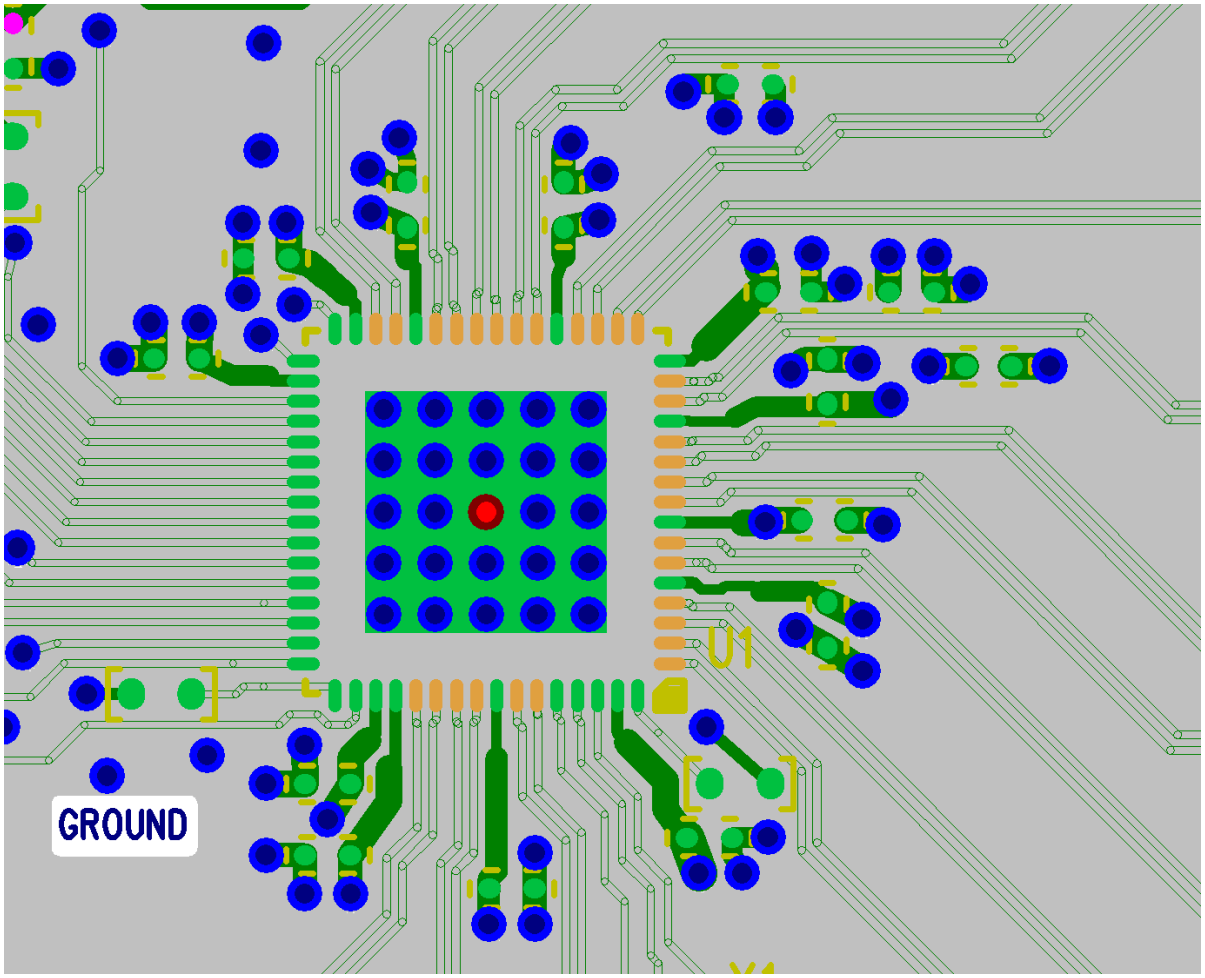


Figure 3.2 Example GROUND on Plane Layer 3 with Via Field in Flag Pad

3.3.2 Return Path

A return path exists for each signal flowing between circuit nodes, and controlling these paths is advantageous. To control these paths, a solid ground plane on the layer just below the device is preferred. All ground floods should connect together and careful consideration should be given to the integrity of the return path for each signal connection.

3.3.3 Bypass Ground Connections

All ground connections from the bypass capacitors should be low inductance. To reduce bypass GND inductance:

- Make the fanout to ground short and wide.
- Use 0402 or smaller capacitors, where possible, that have lower package inductance.
- Use vias with as large a hole diameter as practical -- up to 0.5 mm FHS.
- Use multiple ground vias per capacitor to divide the effect of the fanout trace's and via's impedances.

3.3.4 Chassis GND Connections

The shield of the USB connectors (Chassis Ground) must be considered carefully. Some kind of shield-ground isolation is usually desired for EMI or ESD reasons. Embedded systems may require a direct ground connection. An RC network of 330 Ω and 0.1 µF is used on most of SMSC's hub evaluation boards for this purpose.

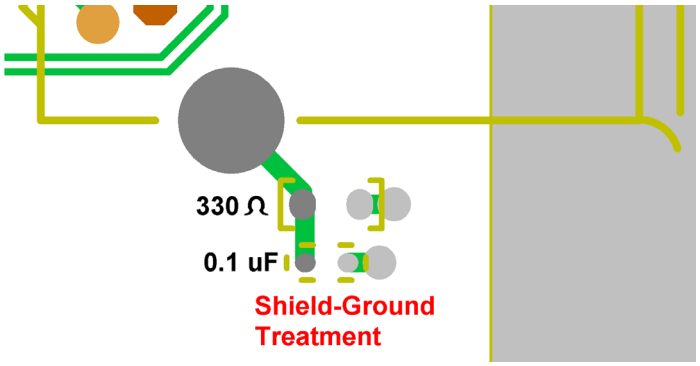


Figure 3.3 Example Chassis-Ground Connection

3.4 Power Distribution

3.4.1 Hub Device Power

The USB5534 family of devices are supplied by both a VDD33 supply and a VDD12 supply (1.25V nominal). We strongly suggest using four or more PCB layers. This greatly simplifies proper power delivery, as well as improved thermal management.

The sensitive analog circuitry inside the hub devices requires a clean power and ground system for best operation. Control supply ripple carefully and make sure that the supply voltages are within specifications for both light and heavy power loads at all power pins. The hub device will represent a light load to the power supply when it is in "suspend" and a heavy load when the device is running all downstream ports at their highest speed. See the applicable datasheets for details.

- A power plane or flood structure should be implemented to provide a low impedance path for each of the power rails to the Hub, especially for the VDD12 supply which can draw 900 mA.
- Connect the Hub *flag* to the ground plane with many vias, especially around the periphery of the *flag*. (The ground *flag* is the device's only connection to signal ground [VSS].)

The figure below illustrates an example of good power distribution to the power pins using flood structures on a plane (layer 3). Note that layer 2 is a complete ground plane layer. The ground shown on layer 3 is to improve thermal and signal return performance of the board.

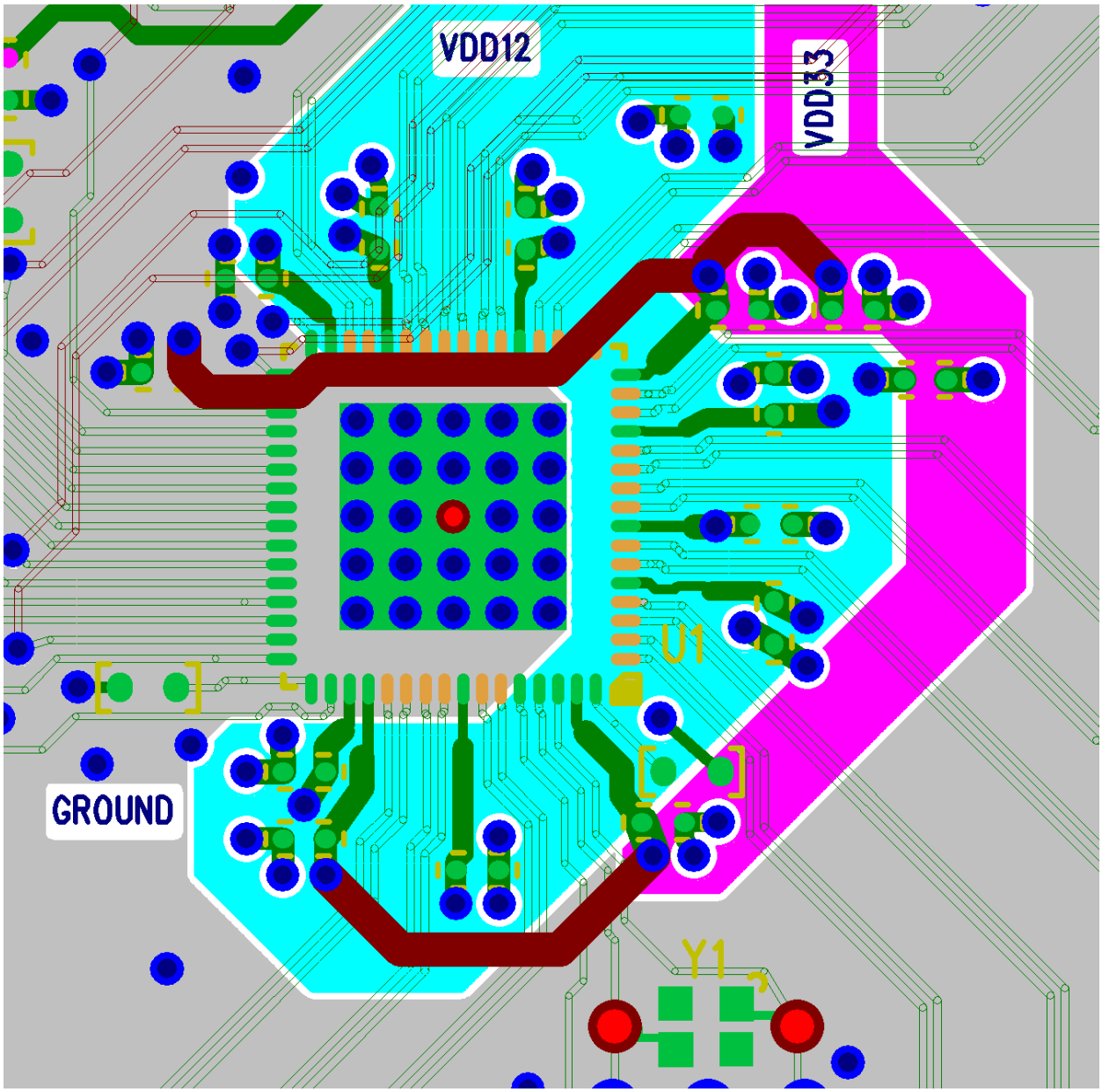


Figure 3.4 Example Power Floods on Plane Layer 3

3.4.2 Distributed USB Power

VBUS is distributed to each downstream connector for use by attached devices. The current is limited by specification to +5 V, 900 mA for USB 3.0 ports. Systems with battery charging enabled, or that comply with USB Power Delivery (PD), may supply even more current.

It is important that the power distribution meets the "droop" and "drop" elements of the USB specifications. Short and very wide paths, plus large value electrolytic capacitors, are provided on the reference EVBs to satisfy this requirement.

3.5 Thermal Management

3.5.1 Power Consumption

SuperSpeed signalling drives the internal switching rates up for USB 3.0 devices. This drives up the power consumption for USB 3.0 devices. Systems must prevent these devices from overheating.

When operating at maximum capacity, the USB5534 consumes about 1.45 W of power. The USB5537 consumes slightly more.

3.5.2 QFN Package Thermal Properties

QFN packages were chosen for these devices because of their excellent thermal properties and package sizes. The flag pad is very efficient at transferring heat to the PCB through a proper via field. This heat energy can then be pulled out of the system.

3.5.3 Planes and Floods

Generally, planes or flood structures should be used to deliver power and ground to the hub device, not only to help with power distribution, but to also improve thermal conduction.

Thermal guidelines for planes and floods:

- Specify a minimum of 1 oz./ft. copper for outer and plane layers.
- Flood the bottom layer with a solid ground at least 4 square inches in area.
- Fill the flag pad with a field of vias (See Figure 3.2).
- Fill inner layers with floods, preferably ground floods, in the region under and around the hub device.
- Flood the region around the hub device on the top layer with ground.
- Stitch all ground floods together with vias.

3.6 Routing

3.6.1 General Routing Rules

- Route critical signals over solid ground planes
- Avoid 90 degree trace corners and use arcs or 45 degree mitered routing instead
- Always consider the ground return path for each critical signal

3.6.2 Analog Signal Considerations

Isolate the current paths of each analog circuit (the USB signal pairs, crystal circuit, and **RBIAS** circuit) from each other. Also ensure that currents flowing through the digital VDD circuits are not also flowing through the analog VDDA circuits, including return currents.

Control this with layout and placement, power/ground "moating", circuit and ground isolation, or other techniques, as needed. See Figure 3.5.

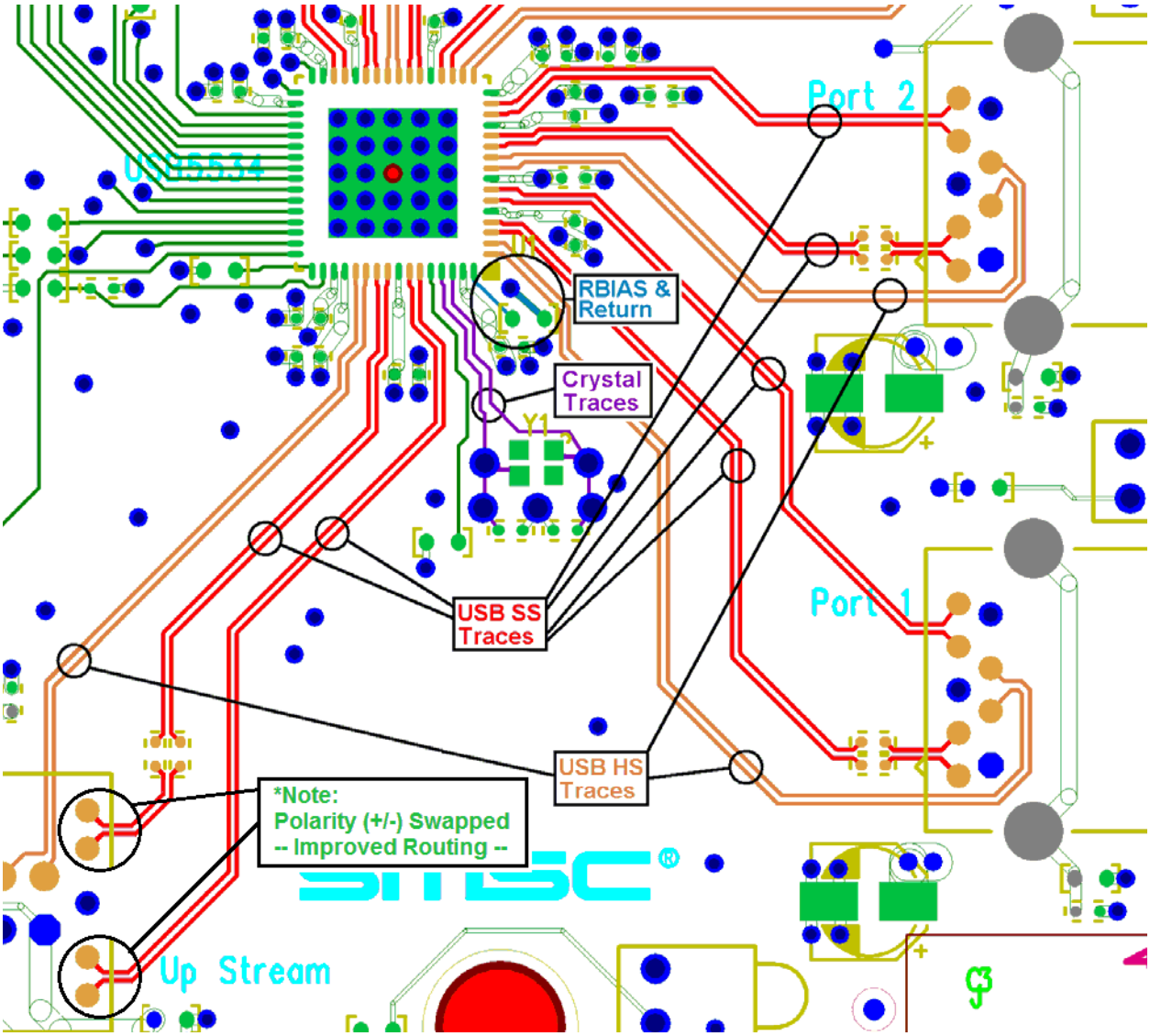


Figure 3.5 Analog Signal Considerations

3.6.3 Bypass Capacitors

Ideally, all of the capacitors used for bypass should be connected such that the power signal originates at the voltage rail source, then to the capacitor, then to the Hub Controller pin. Consider using double ground vias for each bypass capacitor to reduce the inductance of the connection. The power and ground traces to the bypass capacitors should be short and wide (low inductance).

MLCC capacitors of 0402 size or less have lower parasitic inductance and fit closer to the hub device pins, making proper placement easier. Use capacitors with appropriate temperature coefficients. (Ex., X7R -- not Y5V.)

Note: The less the bypass routing conforms to this ideal, the less effective it will be.

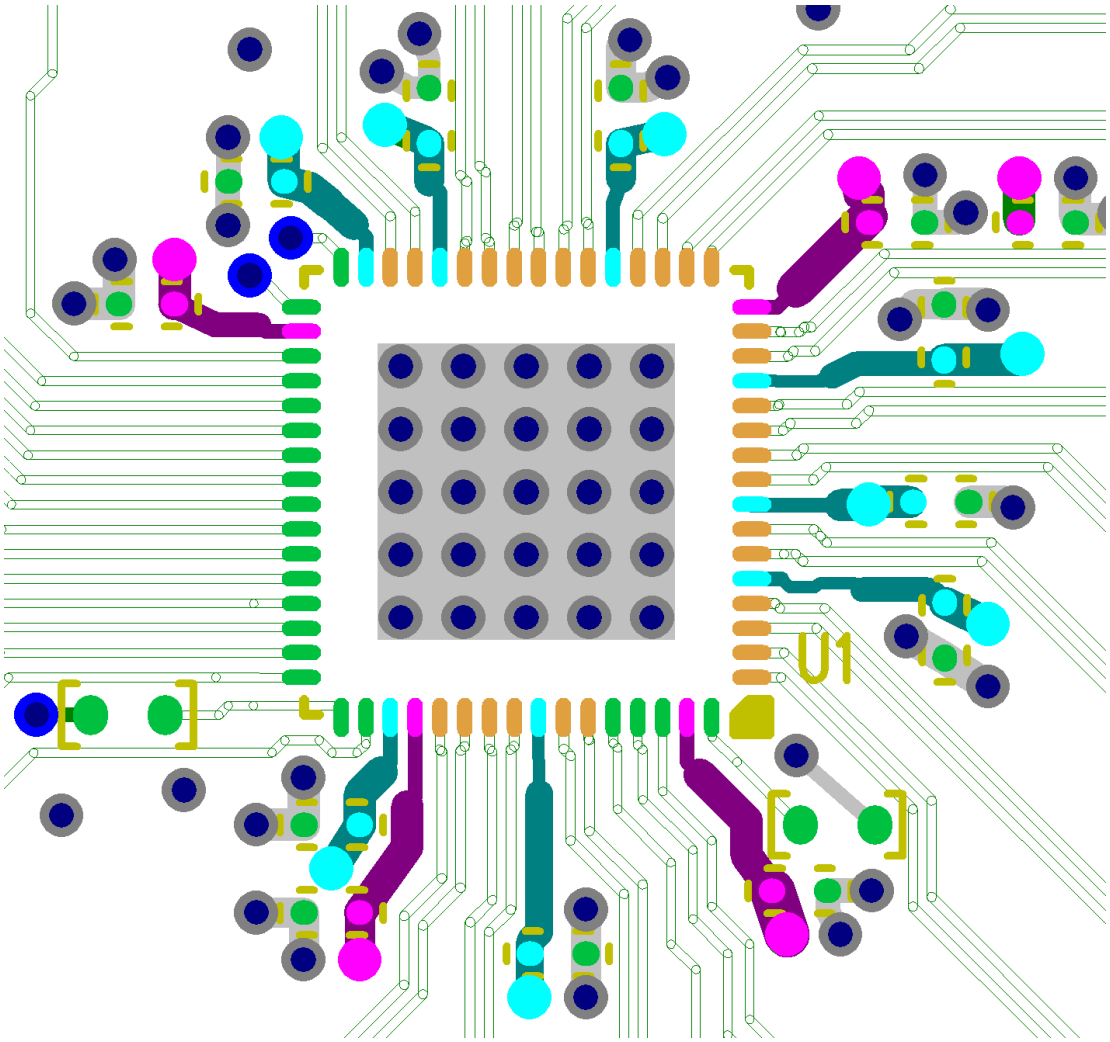


Figure 3.6 Bypass Capacitors

3.6.4 RBIAS Resistor

The USB553x products use an external resistor to set a bias current for internal circuitry, similar to many other SMSC devices. This is a very sensitive analog input.

3.6.4.1 RBIAS Signal Routing

The resistor should be connected with a short trace to the **RBIAS** pin of the device to reduce signal coupling from other circuits.

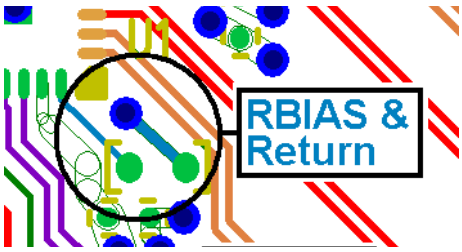


Figure 3.7 RBIAS Return Routing

3.6.4.2 RBIAS Return Routing

The return ground on the **RBIAS** resistor should flow directly to the ground flag nearest to the **RBIAS** pin on the Hub controller.

Note: The ground via on the **RBIAS** resistor, if any, should not be shared with any other devices, particularly the bypass capacitors.

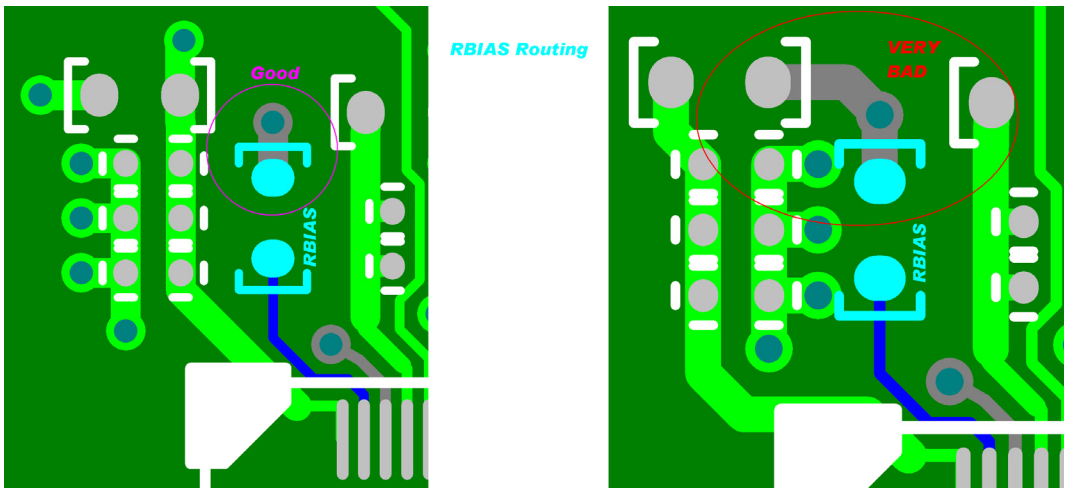


Figure 3.8 RBIAS Return Routing

3.6.5 USB Signal Routing

The USB lines are constrained by the USB 2.0 and USB 3.0 specifications. Critical conditions for the lines are detailed in this section.

3.6.5.1 Differential Impedance

The differential impedance of the USB differential pairs needs to be controlled to 90Ω (nominal). These paired signals are DP and DM for each USB 2.0 interface, and also SS_TX+ and SS_TX-, and SS_RX+ and SS_RX- for each USB 3.0 interface. See the applicable USB specifications for further details.

3.6.5.2 USB Differential Routing

These differential routing guidelines are critical for maintaining good signal integrity for the USB signals. Reference Figure 3.5.

1. All of the USB traces must be routed as differential pairs. Avoid using any stubs on these lines.
2. The SuperSpeed (SS) USB signals may be routed with their polarity swapped to simplify routing. (E.g., RX- may be swapped with RX+ and TX- may be swapped with TX+ for any port.) DP and DM on a particular port may only be swapped if PortSwap is configured for that port.
3. The USB traces must not be exposed to cross-talk from adjacent lines.

   Maintain a routing spacing (gap) of at least 3 times the differential spacing (3X) between High-Speed USB signals (DP and DM) to the signals outside of the USB pair. For example, if the differential spacing is 0.178 mm (7 mil), the minimum spacing to signals not in that USB pair will be at least 0.54 mm (21 mil).

   Maintain a routing spacing (gap) of as wide as practicable and at least 5 times the differential spacing (5X) between SuperSpeed USB signals (RX+/- and TX+/-) to the signals outside of the USB pair. This implies that the spacing from the RX signals to the TX signals, or to the DP/DM signals, must be at least 5X. For example, if the differential spacing is 0.178 mm (7 mil), the minimum spacing to signals not in that USB pair will be at least 0.89 mm (35 mil).
4. The USB differential traces must be length-matched very carefully. Add any needed length so that minimal phase skew is introduced between pair members.

   Each member of a High-Speed differential pair should be no more than 1.25 mm (50 mil) longer than the other member. Each member of a SuperSpeed differential pair should be no more than 0.13 mm (5 mil) longer than the other member. The transmit differential pair (TX+ and TX-) does not have to be the same length as the receive differential pair (RX+ and RX-). Minimize the trace length of the differential pairs.
5. Vias are not typically needed to route the USB signal pairs for SMSC hubs. Minimize the number of vias used and use a balanced number and placement of them per pair if used.
6. Route the differential pairs over unbroken ground planes or floods.
7. Keep USB pairs as short as possible to reduce signal loss. Traces longer than ~15 cm (~6 in) may significantly degrade signal quality.

3.6.6 USB Connectors

Selection of specific USB connectors can significantly impact the transmission line characteristics of the USB SS and HS signals. How the pin padstacks are defined and routed can also greatly impact USB transmission line integrity.

1. "Sanitize" the thru-hole (TH) pad stacks of USB connector pins, meaning simplify the TH padstacks to simplify their effects on the USB transmission lines.

   If a TH USB connector must be used, remove pin pads on unused layers to ease the task of controlling impedance discontinuities and capacitance caused by the hole geometries. Clearances around these pins should generally be 0.5mm or more.

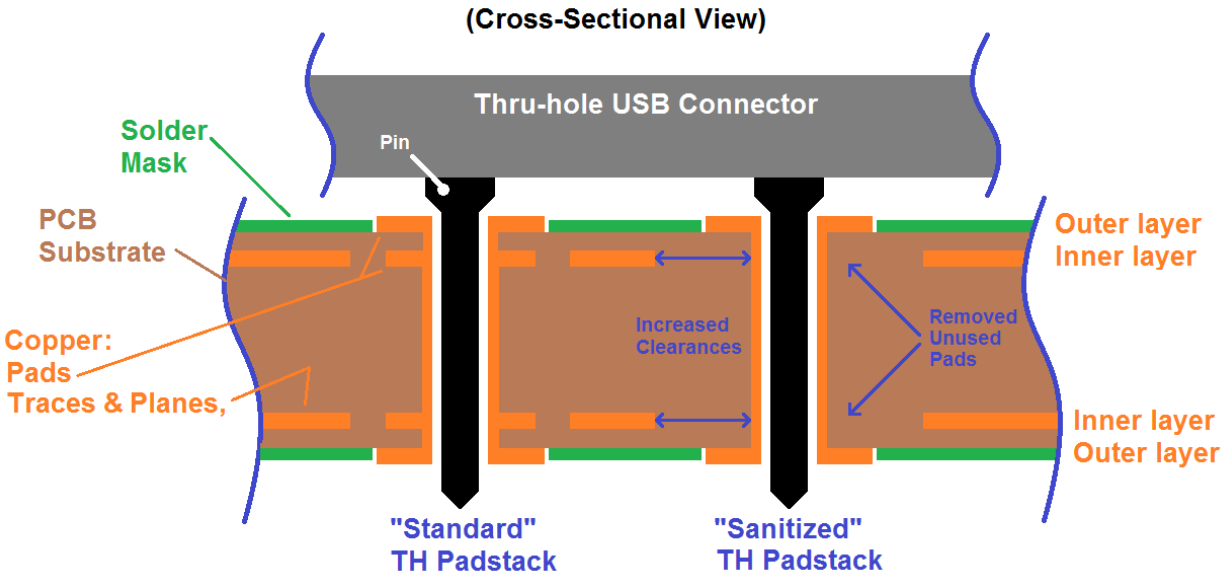


Figure 3.9 "Sanitizing" a USB Pin Padstack

2. Reduce the stub effects of USB pins.

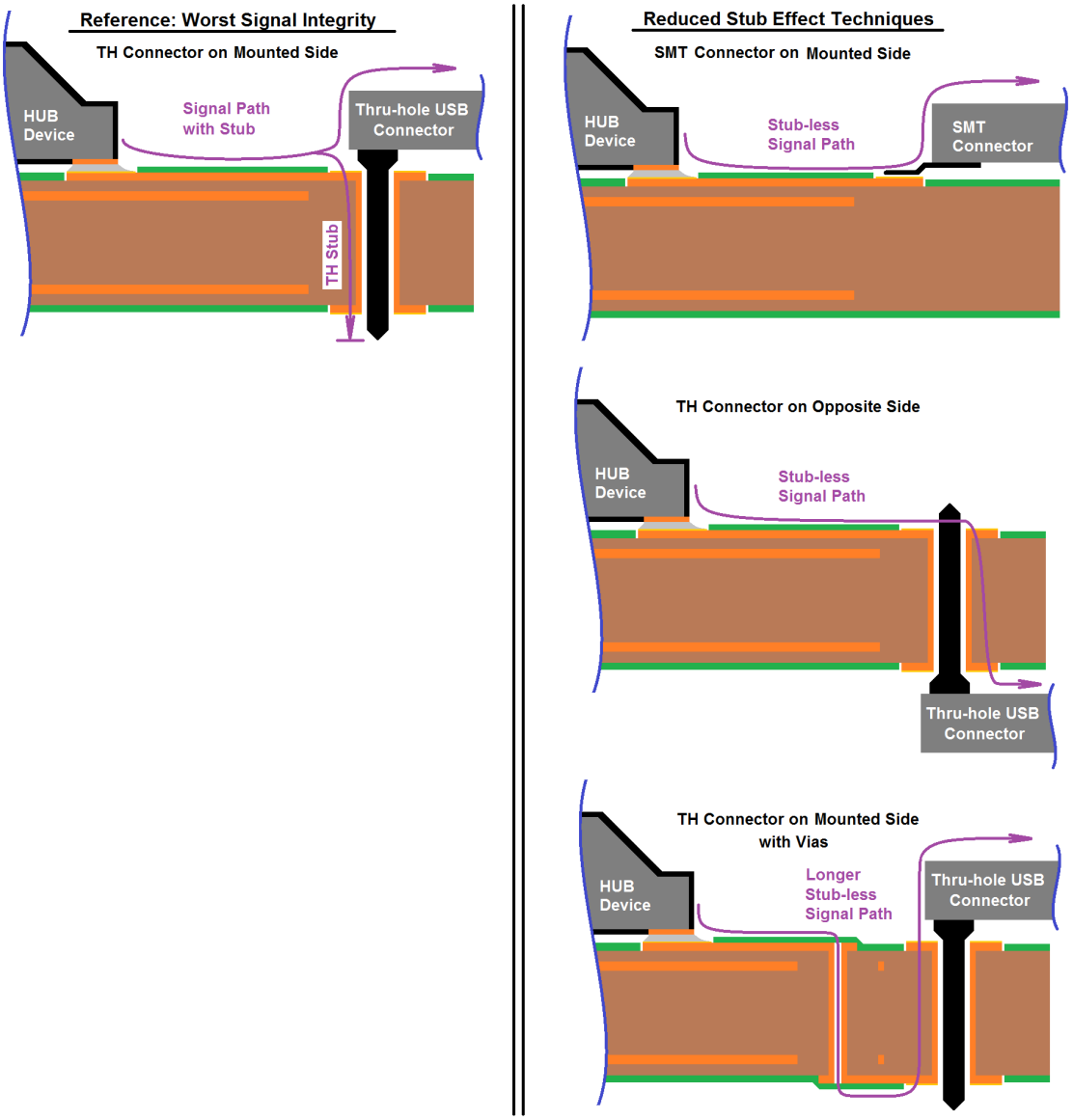


Figure 3.10 Reduce the Stub Effects of TH USB Connector Pins

A. Transmission line characteristics of surface mount (SMT) USB connectors are easiest to control. Use surface mount USB connectors for optimal signal integrity.

B. When possible, place any thru-hole (TH) USB connectors on the opposite side of the board from the USB hub -- especially on thicker PCB's -- to prevent the TH pins from acting as stubs that will degrade signal quality.

C. Another method of controlling this stub effect is to use a via pair to allow the signal traces to enter the pin padstack on the side opposite the connector. This can be used when the USB connectors are placed on the same side as the hub device.

3.6.7 Crystal Oscillator

XTAL1 and **XTAL2** are the crystal oscillator connection pins. The circuit requires the use of two load capacitors. See the applicable datasheet for values and details.

Crystals for the USB553x devices require a tolerance of +/- 30 ppm. See the applicable datasheet for additional details.

3.6.7.1 XTAL1 and XTAL2 Routing

The crystal oscillator pins should route directly to the crystal pins and their associated load capacitors, if required. Route foreign traces no closer than five times (5X) the minimum trace spacing to these traces.

A clock signal may be applied to the **XTAL1** pin instead of using a crystal. In this case, leave the **XTAL2** pin unconnected (open). See the applicable datasheet for voltage levels and other details of this clock signal.

4 Application Note Revision History

Table 4.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (02-01-13)		▪ Co-branded document with Microchip logo, modified legal disclaimer ▪ Corrected typos
	Figure 3.1, "Example Analog Signal Considerations", Figure 3.5, "Analog Signal Considerations"	▪ Figures updated
	Section 3.6.6, "USB Connectors"	▪ New section created
Rev. 1.0 (04-23-12)	Initial release	

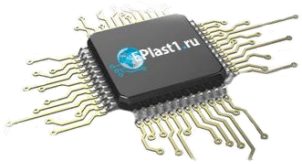
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.