XC9572XL High Performance CPLD

DS057 (v2.0) April 3, 2007

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (38 user I/O pins)
  - 64-pin VQFP (52 user I/O pins)
  - 100-pin TQFP (72 user I/O pins)
  - Pb-free available for all packages
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS Fast FLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC9572 device in the 44-pin PLCC package and the 100-pin TQFP package

WARNING: Programming temperature range of T_A = 0° C to +70° C

Description

The XC9572XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 5 ns. See Figure 2 for overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$I_{CC}(mA) = MC_{HS}(0.175*PT_{HS} + 0.345) + MC_{LP}(0.052*PT_{LP} + 0.272) + 0.04 * MC_{TOG}(MC_{HS} + MC_{LP})* f$$

where:

MC_{HS} = # macrocells in high-speed configuration
PT_{HS} = average number of high-speed product terms per macrocell
MC_{LP} = # macrocells in low power configuration
PT_{LP} = average number of low power product terms per macrocell
f = maximum clock frequency
MCTOG = average % of flip-flops toggling per clock (~12%)

This calculation was derived from laboratory measurements of an XC9500XL part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx

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application note **XAPP114, "Understanding XC9500XL CPLD Power."**

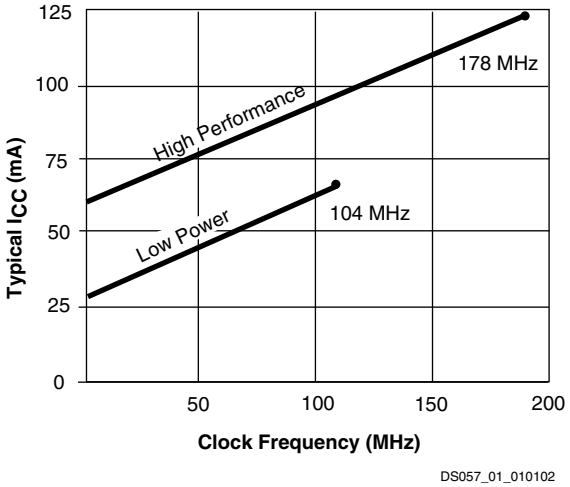


Figure 1: **Typical I_{CC} vs. Frequency for XC9572XL**

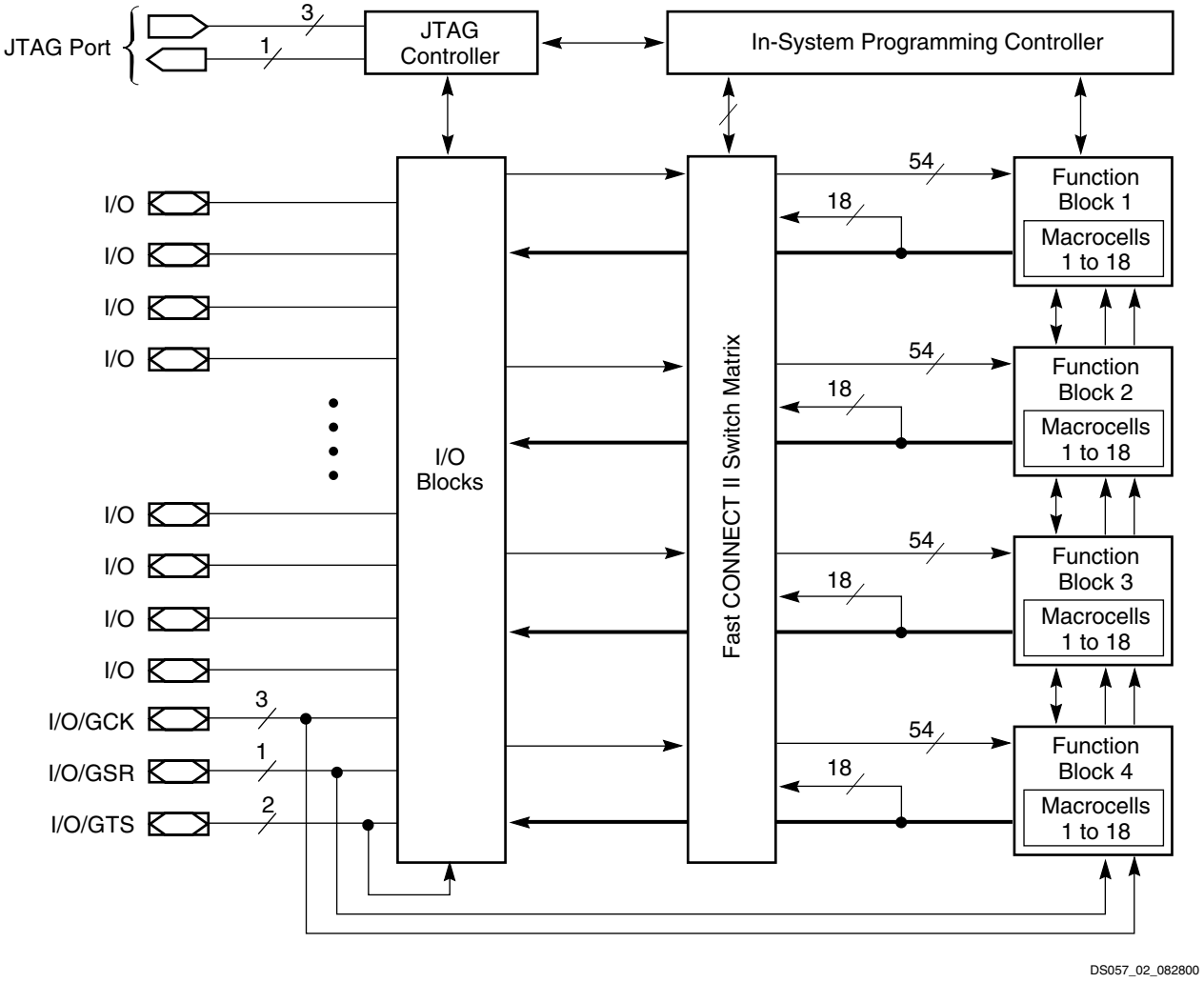


Figure 2: **XC9572XL Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings(2)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)(3)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. External I/O voltage may not exceed V_{CCINT} by 4.0V.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

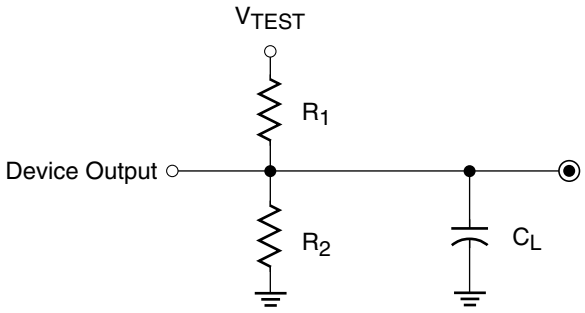
Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{CCIO} = Max; V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} Min < V_{IN} < 5.5V	-	±50	µA
C_{IN}	I/O capacitance	V_{IN} = GND; f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_{IN} = GND, No load; f = 1.0 MHz	20 (Typical)		mA

AC Characteristics

Symbol	Parameter	XC9572XL-5		XC9572XL-7		XC9572XL-10		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	7.5	-	10.0	ns
T_{SU}	I/O setup time before GCK	3.7	-	4.8	-	6.5	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.5	-	4.5	-	5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	178.6	-	125.0	-	100.0	MHz
T_{PSU}	I/O setup time before p-term clock input	1.7	-	1.6	-	2.1	-	ns
T_{PH}	I/O hold time after p-term clock input	2.0	-	3.2	-	4.4	-	ns
T_{PCO}	P-term clock output valid	-	5.5	-	7.7	-	10.2	ns
T_{OE}	GTS to output valid	-	4.0	-	5.0	-	7.0	ns
T_{OD}	GTS to output disable	-	4.0	-	5.0	-	7.0	ns
T_{POE}	Product term OE to output enabled	-	7.0	-	9.5	-	11.0	ns
T_{POD}	Product term OE to output disabled	-	7.0	-	9.5	-	11.0	ns
T_{AO}	GSR to output valid	-	10.0	-	12.0	-	14.5	ns
T_{PAO}	P-term S/R to output valid	-	10.5	-	12.6	-	15.3	ns
T_{WLH}	GCK pulse width (High or Low)	2.8	-	4.0	-	4.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320 Ω	360 Ω	35 pF
	2.5V	2.5V	250 Ω	660 Ω	35 pF

DS058_03_081500

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC9572XL-5		XC9572XL-7		XC9572XL-10		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.5	-	2.3	-	3.5	ns
T_{GCK}	GCK buffer delay	-	1.1	-	1.5	-	1.8	ns
T_{GSR}	GSR buffer delay	-	2.0	-	3.1	-	4.5	ns
T_{GTS}	GTS buffer delay	-	4.0	-	5.0	-	7.0	ns
T_{OUT}	Output buffer delay	-	2.0	-	2.5	-	3.0	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	1.6	-	2.4	-	2.7	ns
T_{PTSR}	Product term set/reset delay	-	1.0	-	1.4	-	1.8	ns
T_{PTTS}	Product term 3-state delay	-	5.5	-	7.2	-	7.5	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.5	-	1.3	-	1.7	ns
T_{SUI}	Register setup time	2.3	-	2.6	-	3.0	-	ns
T_{HI}	Register hold time	1.4	-	2.2	-	3.5	-	ns
T_{ECSU}	Register clock enable setup time	2.4	-	2.6	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	1.4	-	2.2	-	3.5	-	ns
T_{COI}	Register clock to output valid time	-	0.4	-	0.5	-	1.0	ns
T_{AOI}	Register async. S/R to output delay	-	6.0	-	6.4	-	7.0	ns
T_{RAI}	Register async. S/R recover before clock	5.0		7.5		10.0		ns
T_{LOGI}	Internal logic delay	-	1.0	-	1.4	-	1.8	ns
T_{LOGILP}	Internal low power logic delay	-	5.0	-	6.4	-	7.3	ns
Feedback Delays								
T_F	Fast CONNECT II feedback delay	-	1.9	-	3.5	-	4.2	ns
Time Adders								
T_{PTA}	Incremental product term allocator delay	-	0.7	-	0.8	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	3.0	-	4.0	-	4.5	ns

XC9572XL I/O Pins[4]

Function Block	Macrocell	PC44	VQ44	CS48	VQ64	TQ100	BScan Order
1	1	-	-	-	-	16	213
1	2	1	39	D7	8	13	210
1	3	-	-	D4	12	18	207
1	4	-	-	-	13	20	204
1	5	2	40	D6	9	14	201
1	6	3	41	C7	10	15	198
1	7	-	-	-	-	25	195
1	8	4	42	C6	11	17	192
1	9	5[1]	43[1]	B7[1]	15[1]	22[1]	189
1	10	-	-	-	18	28	186
1	11	6[1]	44[1]	B6[1]	16[1]	23[1]	183
1	12	-	-	-	23	33	180
1	13	-	-	-	-	36	177
1	14	7[1]	1[1]	A7[1]	17[1]	27[1]	174
1	15	8	2	A6	19	29	171
1	16	-	-	-	-	39	168
1	17	9	3	C5	20	30	165
1	18	-	-	-	-	40	162
2	1	-	-	-	-	87	159
2	2	35	29	F4	60	94	156
2	3	-	-	-	58	91	153
2	4	-	-	-	59	93	150
2	5	36	30	G5	61	95	147
2	6	37	31	F5	62	96	144
2	7	-	-	-	-	3[2]	141
2	8	38	32	G6	63	97	138
2	9	39[1]	33[1]	G7[1]	64[1]	99[1]	135
2	10	-	-	-	1	1	132
2	11	40[1]	34[1]	F6[1]	2[1]	4[1]	129
2	12	-	-	-	4	6	126
2	13	-	-	-	-	8	123
2	14	42[3]	36[3]	E6[3]	5[3]	9[3]	120
2	15	43	37	E7	6	11	117
2	16	-	-	-	-	10	114
2	17	44	38	E5	7	12	111
2	18	-	-	-	-	92	108
3	1	-	-	-	-	41	105
3	2	11	5	B5	22	32	102
3	3	-	-	C4	31	49	99
3	4	-	-	-	32	50	96
3	5	12	6	A4	24	35	93
3	6	-	-	-	34	53	90
3	7	-	-	-	-	54	87
3	8	13	7	B4	25	37	84
3	9	14	8	A3	27	42	81
3	10	-	-	D3	39	60	78
3	11	18	12	B2	33	52	75
3	12	-	-	-	40	61	72
3	13	-	-	-	-	63	69
3	14	19	13	B1	35	55	66
3	15	20	14	C2	36	56	63
3	16	24	18	D2	42	64	60
3	17	22	16	C3	38	58	57
3	18	-	-	-	-	59	54
4	1	-	-	-	-	65	51
4	2	25	19	E1	43	67	48
4	3	-	-	-	46	71	45
4	4	-	-	-	47	72	42
4	5	26	20	E2	44	68	39
4	6	-	-	E4	49	76	36
4	7	-	-	-	-	77	33
4	8	27	21	F1	45	70	30
4	9	-	-	-	-	66	27
4	10	-	-	-	51	81	24
4	11	28	22	G1	48	74	21
4	12	-	-	-	52	82	18
4	13	-	-	-	-	85	15
4	14	29	23	F2	50	78	12
4	15	33	27	E3	56	89	9
4	16	-	-	-	-	86	6
4	17	34	28	G4	57	90	3
4	18	-	-	-	-	79	0

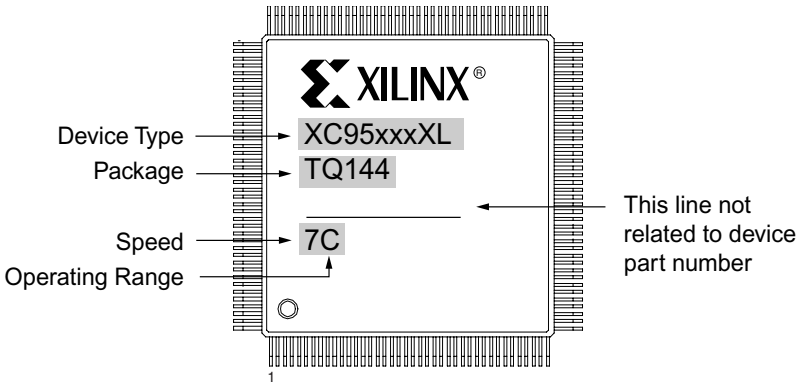
Notes:
1. Global control pin.
2. GTS1 for TQ100.
3. GTS1 for PC44, VQ44, CS48, and VQ64.
4. The pin-outs are the same for Pb-free versions of packages.

XC9572XL Global, JTAG and Power Pins(1)

Pin Type	PC44	VQ44	CS48	VQ64	TQ100
I/O/GCK1	5	43	B7	15	22
I/O/GCK2	6	44	B6	16	23
I/O/GCK3	7	1	A7	17	27
I/O/GTS1	42	36	E6	5	3
I/O/GTS2	40	34	F6	2	4
I/O/GSR	39	33	G7	64	99
TCK	17	11	A1	30	48
TDI	15	9	B3	28	45
TDO	30	24	G2	53	83
TMS	16	10	A2	29	47
V_{CCINT} 3.3V	21, 41	15, 35	C1, F7	3, 37	5, 57, 98
V_{CCIO} 2.5V/3.3V	32	26	G3	26, 55	26, 38, 51, 88
GND	10, 23, 31	4, 17, 25	A5, D1, F3	14, 21, 41, 54	21, 31, 44, 62, 69, 75, 84, 100
No Connects	-	-	-	-	2, 7, 19, 24, 34, 43, 46, 73, 80

Notes:
1. The pin-outs are the same for Pb-free versions of packages.

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Notes:

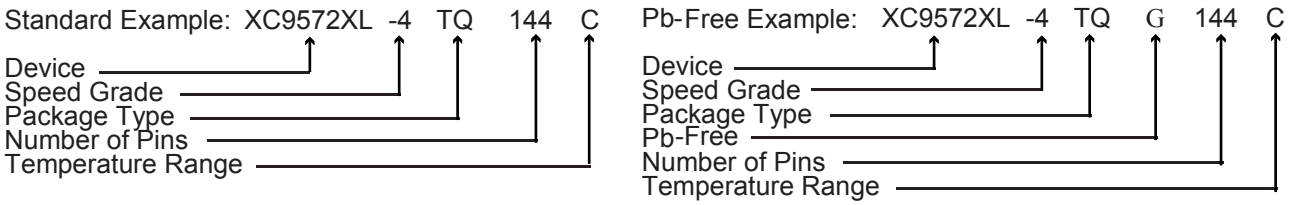
1. Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
   - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 95xxxXL.
   - Line 2 = Not related to device part number.
   - Line 3 = Not related to device part number.
   - Line 4 = Package code, speed, operating temperature, three digits not related to device part number. Package codes: C1 = CS48, C2 = CSG48.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9572XL-5PC44C	5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572XL-5VQ44C	5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9572XL-5CS48C	5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9572XL-5VQ64C	5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9572XL-5TQ100C	5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572XL-7PC44C	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572XL-7VQ44C	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9572XL-7CS48C	7.5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9572XL-7VQ64C	7.5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9572XL-7TQ100C	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572XL-7PC44I	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9572XL-7VQ44I	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	I
XC9572XL-7CS48I	7.5 ns	CS48	48-ball	Chip Scale Package (CSP)	I
XC9572XL-7VQ64I	7.5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	I
XC9572XL-7TQ100I	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC9572XL-10PC44C	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572XL-10VQ44C	10 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9572XL-10CS48C	10 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9572XL-10VQ64C	10 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9572XL-10TQ100C	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572XL-10PC44I	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9572XL-10VQ44I	10 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	I
XC9572XL-10CS48I	10 ns	CS48	48-ball	Chip Scale Package (CSP)	I
XC9572XL-10VQ64I	10 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	I
XC9572XL-10TQ100I	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I

Notes:
C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9572XL-5PCG44C	5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9572XL-5VQG44C	5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-5CSG48C	5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9572XL-5VQG64C	5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-5TQG100C	5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC9572XL-7PCG44C	7.5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9572XL-7VQG44C	7.5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-7CSG48C	7.5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9572XL-7VQG64C	7.5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-7TQG100C	7.5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC9572XL-7PCG44I	7.5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	I
XC9572XL-7VQG44I	7.5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9572XL-7CSG48I	7.5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	I
XC9572XL-7VQG64I	7.5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9572XL-7TQG100I	7.5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	I
XC9572XL-10PCG44C	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9572XL-10VQG44C	10 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-10CSG48C	10 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9572XL-10VQG64C	10 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9572XL-10TQG100C	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC9572XL-10PCG44I	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	I
XC9572XL-10VQG44I	10 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9572XL-10CSG48I	10 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	I
XC9572XL-10VQG64I	10 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9572XL-10TQG100I	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C



Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Further Reading

The following Xilinx links go to relevant XC9500XL CPLD documentation, including XAPP111, Using the XC9500XL Timing Model, and XAPP784, Bulletproof CPLD Design Practices. Simply click on the link and scroll down.

Data Sheets, Application Notes, and White Papers.

Packaging

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/28/98	1.0	Initial Xilinx release.
08/28/01	1.1	Added VQ44 package.
06/20/02	1.2	Updated I_{CC} equation, page 1. Updated Component Availability table. Added additional I_{IH} test conditions and measurements to DC Characteristics table.
05/27/03	1.3	Updated T_{SOL} from 260 to 220ºC. Added Part Marking and updated Ordering Information.
08/21/03	1.4	Updated Package Device Marking Pin 1 orientation.
07/15/04	1.5	Added Pb-free documentation
09/15/04	1.6	Added T_{APRPW} specification to AC Characteristics.
04/29/05	1.7	No change to documentation.
07/15/05	1.8	Move to Product Specification
03/22/06	1.9	Add Warranty Disclaimer.
04/03/07	2.0	Add programming temperature range warning on page 1.

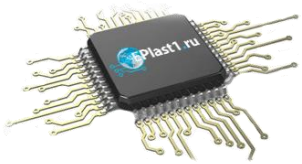
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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