A High Performance Differential Line Driver/Receiver for DSL Applications
Demo Board DC261A-A

Revision 1.1
July 12, 1999

By Tim Regan
LTC Amplifier Applications

This Demo Manual describes the versatile features and measured performance of the DC261A demo board. Key features of this demo board include:

- High Speed, Low Distortion Differential Line Driver using the LT1795
- Low Noise Differential 4 wire to 2 wire Hybrid Receiver using the LT1358
- Single or Dual Supply Operation
- Adjustable Line Driver Operating Current for Optimum Power Dissipation
- External Driver ON/OFF Control
- Direct Phone Line Interface through 2:1 Transformer
- Low Thermal Resistance (22°C/W junction to ambient) PCB Layout

Introduction

The schematic for the system is shown in Figure 1.

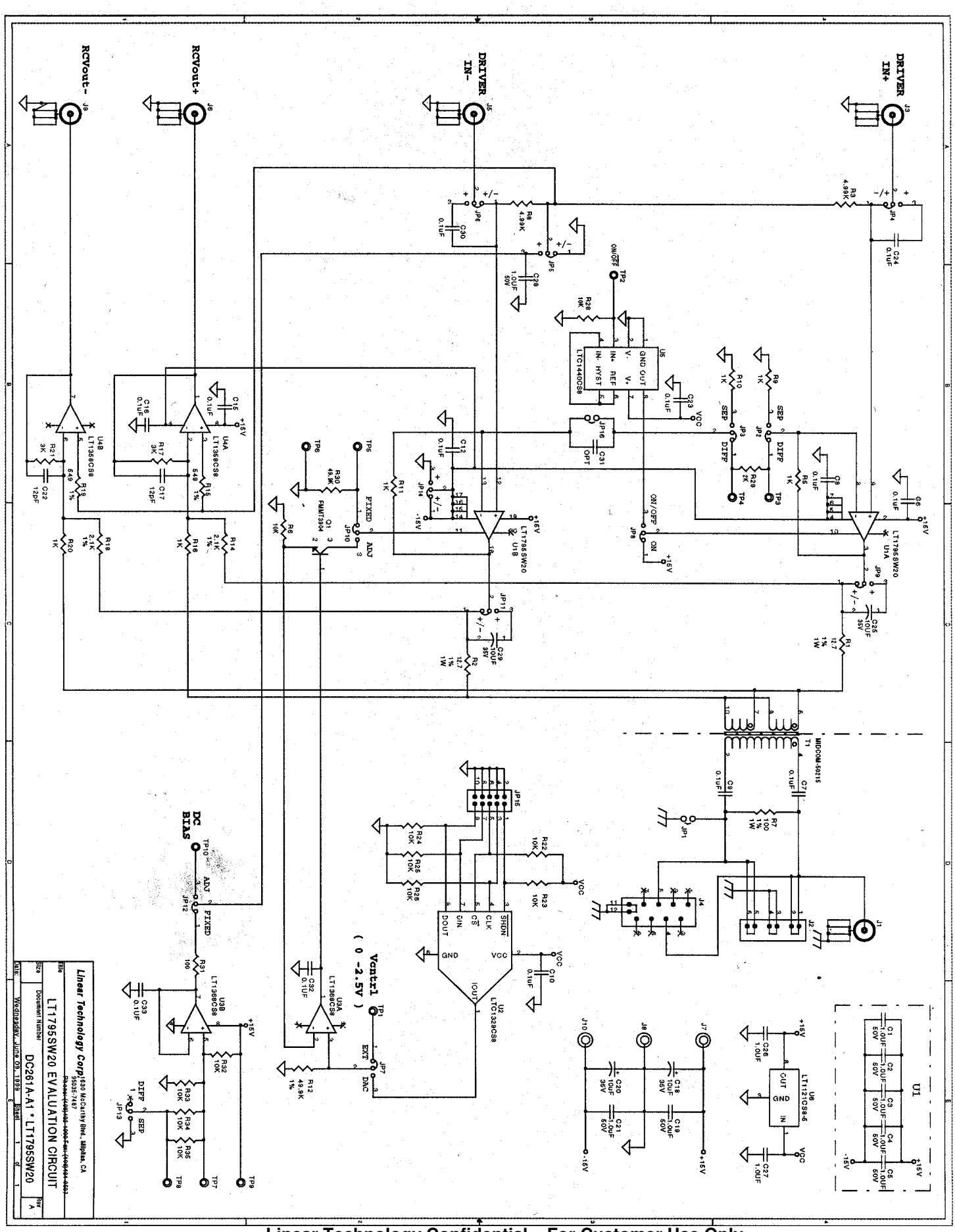
The Line Driver is amplifier U1 A and B, an LT1795. The LT1795 is a Dual, 50MHz, 900V/µS current feedback amplifier with 500mA output current capability. The high output current drive allows for the use of higher turns ratio line coupling transformers with lower total supply voltage for the driver. The LT1795 has a wide 20-pin surface mount package with an enhanced power dissipating lead frame. These amplifiers are sufficient for the most demanding ADSL applications. Jumpers configure the line driver for operation as either a differential amplifier with a gain of 2, or as two separate non-inverting amplifiers, each with gain of 2. Provision has been made to allow adding an external resistor, at points TP3 and TP4; to modify the gain as required.

The Line Receiver function is implemented by U4 A and B, an LT1358. These amplifiers provide 25MHz Gain-Bandwidth, 600V/µS slew rate, low power consumption (2.5mA supply current per amplifier) and low noise (8nV/√Hz). The differential receiver senses and amplifies the voltage across the line transformer back-termination resistors. The gain setting resistors are scaled in such a manner as to provide first order cancellation of the transmitted signals from the line drivers so that only the received signal from the line is amplified.

Shutdown and Adjustable Operating Current

The LT1795 has a unique shutdown feature that can also be used to control the operating current of the amplifiers. This provides total control over the quiescent current consumption and power dissipation of the line drivers. When the line is inactive an external CMOS or TTL compatible logic signal can shut down the drivers to only 200µA of quiescent current. This ON/OFF control is provided by U4, which is an LTC1440 CMOS voltage comparator with reference. The 1.2V reference is the ON/OFF threshold for the control signal applied at TP2. When commanded ON by a logic “1” input, the LT1795 drivers bias up very quickly and process signals within about 1µS.

Figure 1. DC261A Schematic (on next Page)


DRIVER IN+
DRIVER IN-
RCVout+
RCVout-
DC BIAS
Vcntrl
(0 -2.5V)
LT1795SW20 EVALUATION CIRCUIT
DC2261A-A1 * LT1795SW20
Linear Technology Corp.
Wednesday, June 09, 1999

The operating current of the LT1795 can be controlled in three ways with DC261A, by a fixed on board resistor (R30), by an external dc control voltage (applied at TP1) or by a dc voltage generated by an on board D to A converter (U2, an LTC1329). This control allows evaluation of how the quiescent, no signal, power dissipation can be minimized yet still provide enough bias current for the driver amplifiers to maintain low distortion operation. The maximum supply current for the LT1795 is 30mA/amplifier, which results in high quiescent power dissipation. However, only 10ma to 15mA per amplifier is required to obtain adequate distortion performance.

Figure 2 illustrates how this control is implemented on DC261A.

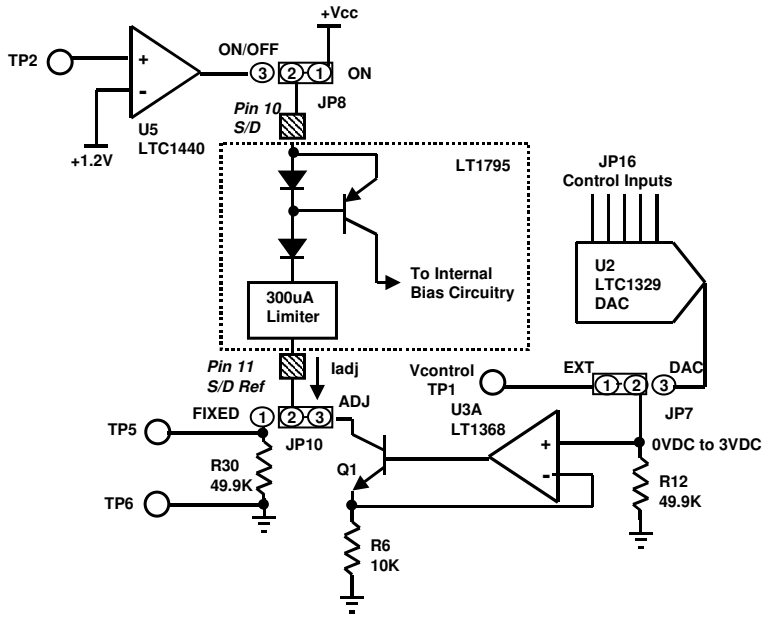


Figure 2. Adjusting the LT1795 Operating Current

Pin 10 of the LT1795 is the Shutdown Input used for ON/OFF control. Pin 11 is the reference voltage for the shutdown input. Effectively there are two diode drops internally between pin 11 and pin 10. With pin 11 grounded, the ON/OFF threshold for pin 10 is approximately 1.2V. Jumper JP8 connects pin 10 to either the +Vcc supply for the LT1795 to set the amplifiers ON continuously or to the output of comparator U5, which switches between +5V and ground, for external ON/OFF control.

The DC current flowing from pin 10 to pin 11, I_{adj}, is internally mirrored and scaled to provide the bias current to the driver amplifiers. This current is internally limited to approximately 300µA. The quiescent supply current for each amplifier is controlled linearly through I_{adj} and can be estimated by the following equation:

$$Iq_{(\,perAmplifier)} \approx 115 \bullet I_{adj}$$

Jumper JP10 sets the control for Pin 11. With JP10 in the FIXED position Pin 11 is connected to an on board 49.9KΩ resistor, R30, to fix I_{adj} to a current level proportional to +Vcc. This fixed biasing current can be found from the expression:

$$I_{adj} \approx \frac{+V_{cc} - 1.2V}{R30}$$

The value for R30 was chosen to provide the maximum bias current for the LT1795 when operated with a +15V positive supply voltage. For lower current fixed bias operation, R30 should be removed and another higher valued resistor can be connected between points TP5 and TP6. The value of this resistor is dependant on the desired I_{adj} level and the positive supply voltage to be used.

To observe the effects of bias current on amplifier performance, jumper JP10 can be set to the ADJ position. This setting connects Pin 11 to an adjustable current sink comprised of amplifier U3A, transistor Q1 and 10KΩ resistor R6. This provides linear control of the operating current to illustrate the improvement or degradation in signal distortion as a trade-off with the total quiescent operating current of the LT1795. For any set of DSL operating requirements, once proper distortion performance is achieved, the quiescent power consumption of the driver amplifiers will be less than the maximum providing a design with optimum overall performance/power consumption characteristics. Whatever I_{adj} current level is required can then be fixed in the manner previously mentioned.

For adjustable operation the following determines the I_{adj} current:

$$I_{adj} = \frac{V_{control}}{R6}$$

Jumper JP7 determines the source for Vcontrol. This jumper connects the (+)input of U3A to either an external adjustable voltage, EXT setting, or to the output of an LT1329 micro-power 8-bit CMOS D to A converter. The serial control of the D to A can provide automatic optimization of the line driver operating conditions during a pre-transmission train-up interval in a DSL application. If either the external voltage or the DAC output exceed 3V, transistor Q1 will saturate due to the internal I_{adj} current limiting of the LT1795 and the operating current will be at its maximum.

Both the DAC and the ON\OFF comparator are biased from an on board LT1121 low dropout +5V regulator powered from the +Vcc supply. In addition, the +Vcc supply also powers a DC voltage biasing resistor network and the Receiver amplifiers. With the LT1795 OFF, the +Vcc supply to the board will still conduct a total of approximately 5mA, but less than 200μA goes to the amplifiers.

Jumper Management for Different Operating Modes

DC261A can be configured through several Jumper settings for four different operating modes:

- Dual Supply (+/-V) Differential Driver Amplifier
- Dual Supply (+/-V) Separate Driver Amplifiers
- Single Supply Differential Driver Amplifier
- Single Supply Separate Driver Amplifiers

Referring to Figure 1, the feedback resistors, R5 and R11, for each driver is fixed at a value of 1KΩ. Jumpers JP2 and JP3 are used to configure the driver amplifiers. The differential amplifier configuration (DIFF Jumper positions) uses only resistor R29 as the gain setting resistor. The value of this resistor on the board is 2KΩ providing a differential gain of 2. Reducing the gain setting resistance by connecting a resistor in parallel with R29 (between posts TP3 and TP4) can increase the gain of the driver stage to any desired level. Any DC offset differences between the two amplifiers will also be amplified by the new higher gain setting. To maintain unity DC gain while having a higher AC gain requires adding a capacitor for C31 and removing Jumper JP16. This capacitor creates a high pass function and should be chosen to be large enough to ensure that the amplifiers pass the low frequency end of the required bandwidth:

$$C31 \geq \frac{1}{2\pi \bullet R29 \bullet F_{low}}$$

Moving Jumpers JP2 and JP3 to the SEP position configures the LT1795 as simply two separate non-inverting gain of 2 amplifiers. No provisions for easy gain adjustments have been provided with this configuration. To obtain higher gain, 1KΩ resistors R9 and R10 can be replaced with lower values.

For Dual or Split supply operation the amplifiers are all DC biased to ground or 0V. The substrate of the LT1795 is connected to the –supply (-Vee) potential. The middle four pins on each side of the package are connected to –Vee and directly connected to the large PCB metal area surrounding the LT1795. With Split supplies this metal is at the –Vee potential so care should be taken to not short this area to ground.

For Single supply operation, DC261A contains circuitry to bias the amplifiers to mid-supply to obtain maximum symmetrical output swing. Amplifier U3B, one half of an LT1368, together with resistor network R32 through R35

provide a dc bias voltage of either +Vcc/2 or +Vcc/4. The selection of this voltage is made through the setting of Jumper J13. This DC bias potential is applied to the inputs through Jumper JP5. The differential amplifier configuration has a DC gain of unity so +Vcc/2 is used to bias the inputs. With the two separate amplifier configuration each amplifier has a DC gain of 2, therefore the +Vcc/4 voltage is used to set the outputs to mid-supply. The Receive amplifier is also DC biased to these same potentials.

For flexibility any input DC bias voltage can be developed. External resistors can be added at Test Points TP7, TP8 and TP9 to modify the on board bias network. Alternatively an external DC voltage source can be applied at TP10 and selected by moving JP12 to the ADJ position to provide any DC bias required.

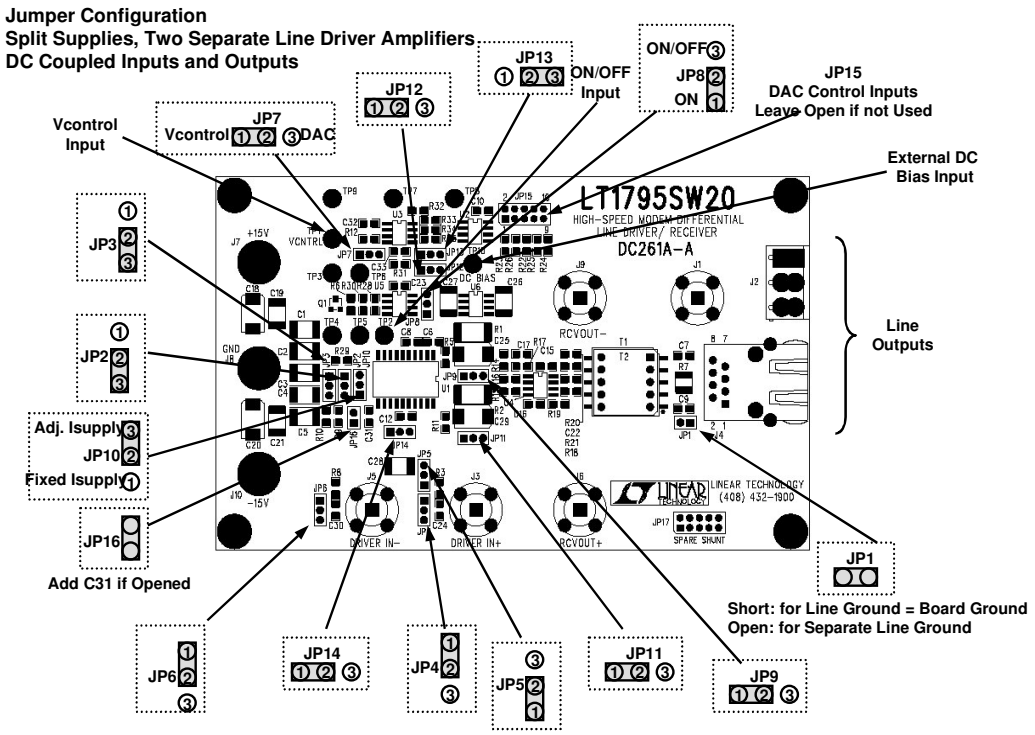
With Single supply operation all large metal areas on the PCB are at ground potential through the proper connection of Jumper JP14.

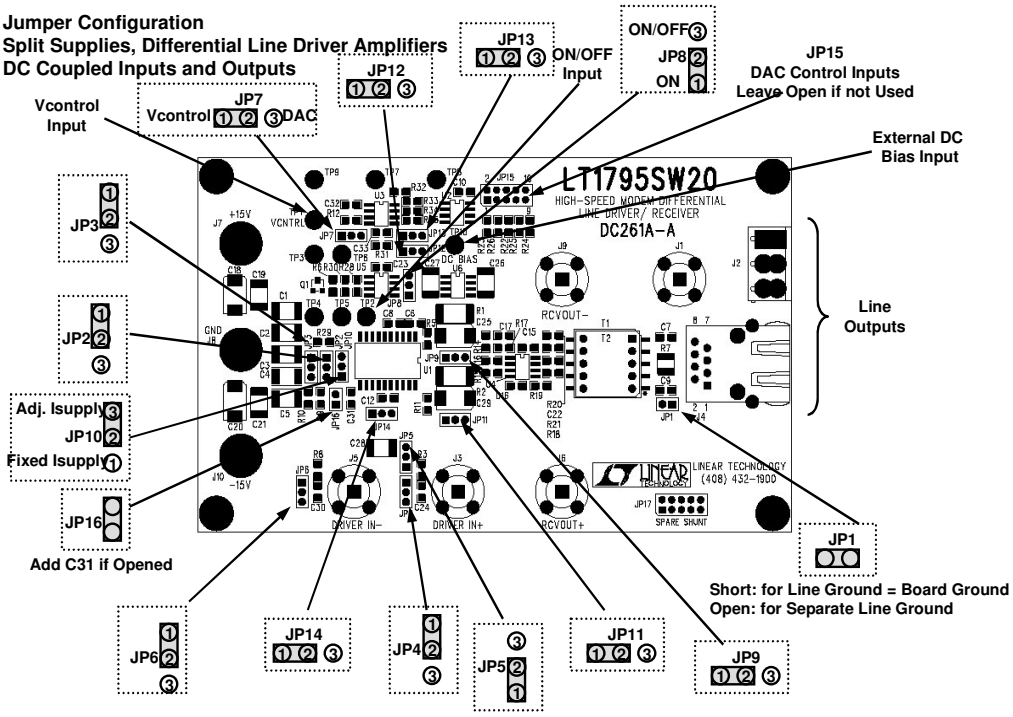
The inputs to the drivers in all cases can be ac or dc coupled through the settings of Jumpers JP4 and JP6.

The LT1795 amplifier outputs can be DC or AC coupled to the back-termination resistors and transformer primary through Jumpers JP9 and JP11. On this version of DC261A however, the DC bias for the Receive amplifiers still provides a common dc bias at each end of the transformer primary. This may be corrected in future versions of this demo board.

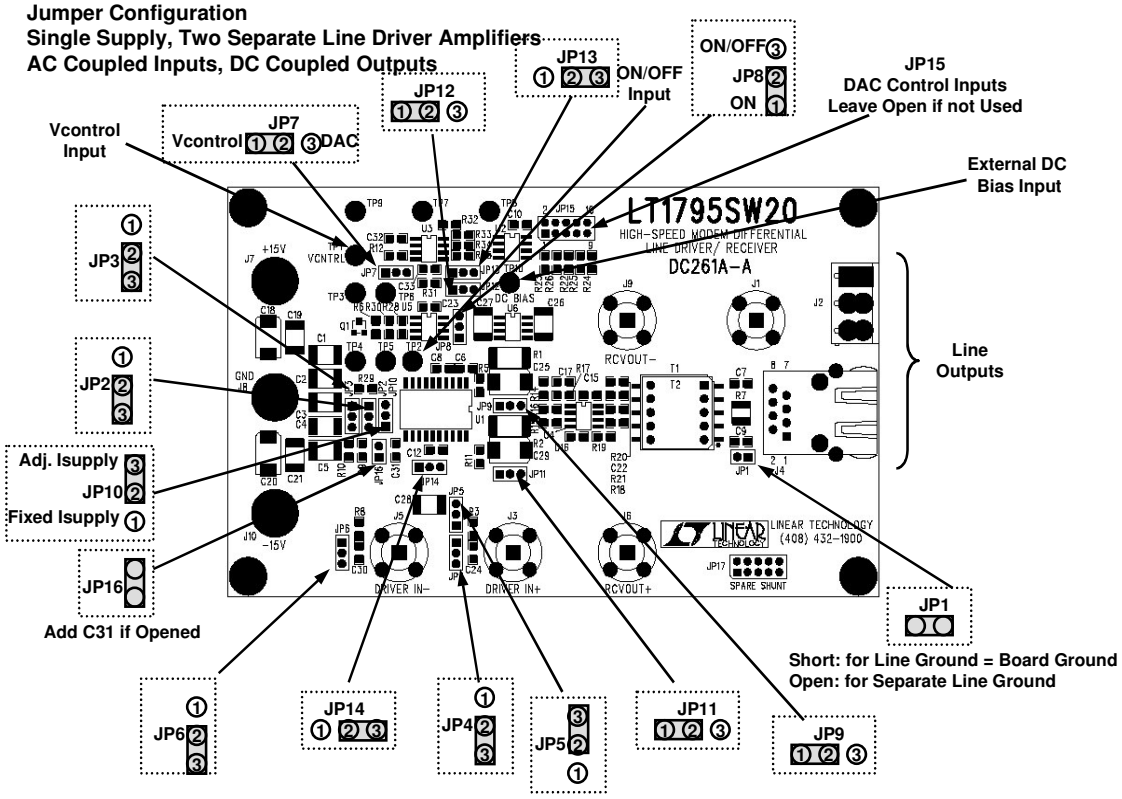
For convenience, the following top view illustrations show the Jumper connections recommended for each operating mode. Go all the way around the board checking each jumper connection before powering up the system.

Figure 3. Jumper Connections for Different Operating Modes

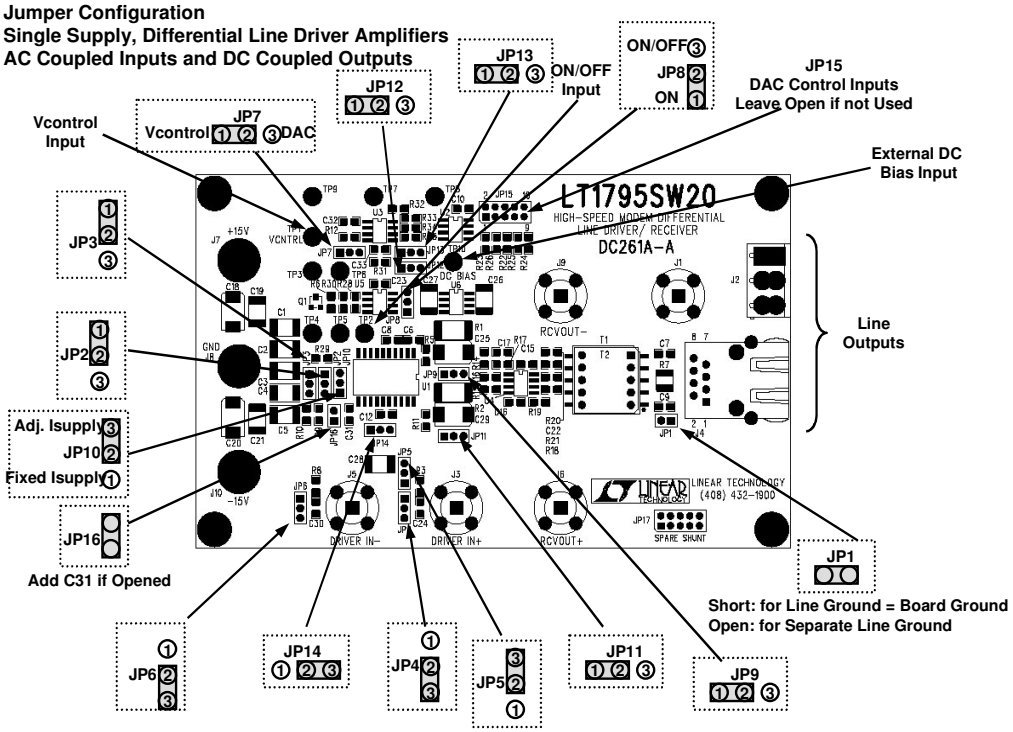




Jumper Configuration
Single Supply, Two Separate Line Driver Amplifiers
AC Coupled Inputs, DC Coupled Outputs



Jumper Configuration
Single Supply, Differential Line Driver Amplifiers
AC Coupled Inputs and DC Coupled Outputs



PCB Layout

Very important to the proper operation of the high power driver amplifiers is the ability to control the operating temperature of the drivers under the toughest continuous load conditions. The current version of DC261A has copper metallization to dissipate heat from the LT1795 package to produce a thermal resistance from the IC junction to the ambient air of only 22.2°C/W. This means that for every Watt of power dissipated in the driver, the junction temperature of the IC rises only 22 degrees above the ambient temperature. This helps to minimize heat generation on the PCB and also prevents the amplifiers from running near the temperature point where the built in thermal protection circuitry comes in to play (at approximately 160°C junction temperature).

DC261A is built on a four-layer metal PCB. A metal area of 1.75" by 2.5" on each of the metal layers serves as a heat sink. Each metal layer is "stitched" together through small, 15 mil, plated-through vias. Directly beneath the IC is the most critical area to have heat dissipating copper and there are 15 vias connecting the metal on all layers to produce, as closely as possible, a solid copper mass for heat sinking.

Figure 4 shows how the heat is conducted across the PCB in the area surrounding the LT1795. This is the amount of temperature rise above ambient (23.8°C) measured in ½" square sections over the area where the –Vee (or Ground) metal is provided. This was measured with an Infrared Pyrometer held 1.5" above the board surface and moved in ½" increments across and down the board. The hottest areas of course are right where the IC is located. The conditions for these measurements were made using a single 24V supply to produce a 4.7Vp-p signal into a 100Ω line load that results in approximately 3W of power being dissipated by the LT1795.

Figure 4. Temperature Gradient over the PCB while Dissipating 3W of Power.

Measured Performance Data

The following charts and printouts illustrate the performance of the DC261A demo board.

For various DSL applications the following table summarizes the minimum requirements when using DC261A. The demo board uses a line-coupling transformer from Midcom (MIDCOM 50215) configured with a 1:2 turns ratio which also contributes approximately 0.5dB of insertion loss. These two factors have been included in the values provided in the table.

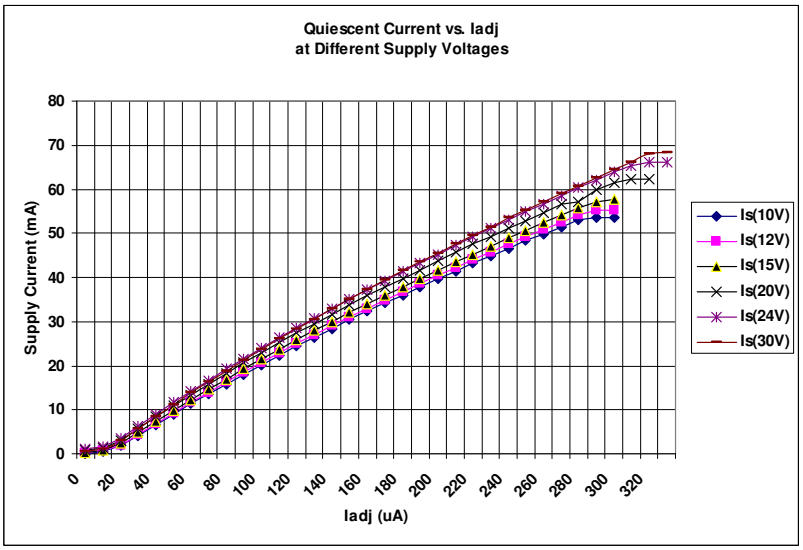
Table 1. Minimum Requirements for Various DSL Applications

Standard	Line Z (Ω)	Average Line Power (dBm)	Nom Line Voltage (rms)	Nom Line Voltage (pk-pk)	Peak to Average Ratio (PAR)	Peak Driver Output Current	Min Single Supply Voltage	Min Split Supply Voltage	Average Driver PDiss at min Supply (mW)
HDSL2 **Upstream** **Downstream**	135	16.4	2.43	6.87	3.82	146	12.5	+/-6.5V	580
ADSL G.Lite **Upstream**	100	13	1.41	4.0	5.33	159	11	+/-5.5	440
ADSL G.Lite **Downstream**	100	16.4	2.09	5.01	5.33	236	16	+/-8	1140
ADSL Full **Upstream**	100	13	1.41	4.0	5.33	159	11	+/-5.5	440
ADSL Full **Downstream**	100	20	3.16	8.94	5.33	357	22	+/-11	1930

Quiescent Operating Current and Power Dissipation Control

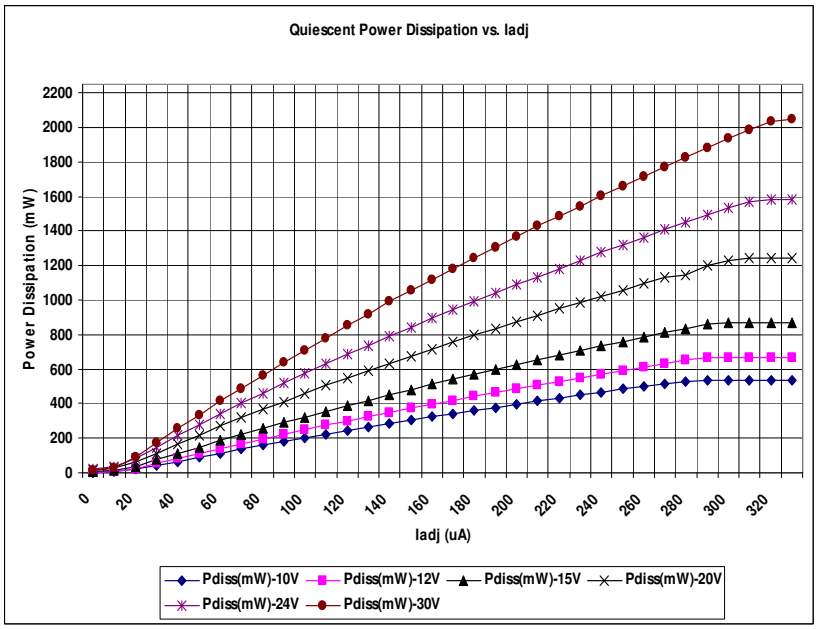
The following charts illustrate the dramatic effect on the quiescent (no signal) biasing of the LT1795 as the current through the S/D Ref pin is adjusted (I_{adj}). The current is adjusted using an external DC voltage at TP1 (Vcontrol). As will be seen it is not necessary to run the LT1795 at full current to achieve acceptable performance in all DSL applications. Only 100µA to 150µA for I_{adj} is required which is significantly less than the maximum power consumption.

Figure 5. Quiescent Supply Current Controlled by I_{adj}.



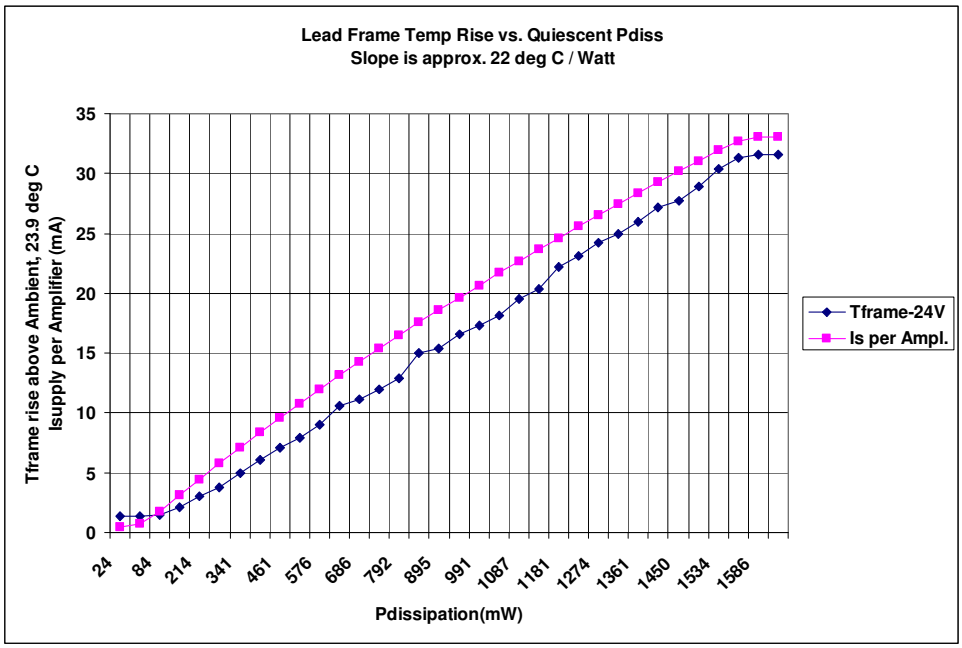
The operating current as shown in Figure 6 also directly controls the quiescent power dissipation.

Figure 6. No Signal Power Dissipation Controlled by I_{adj}.



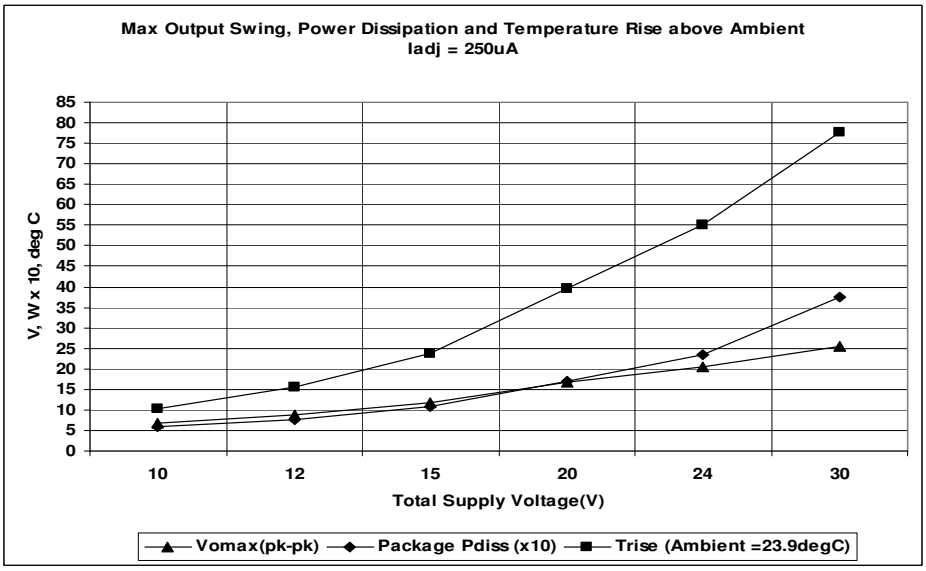
With power dissipation comes heat. Figure 7 illustrates the amount of heat generated by the Driver amplifiers, which can also be controlled by adjusting the operating current. For this measurement a thermocouple was soldered to one side of the package where the four -Vee pins connect to the PCB. This provides the lead frame temperature that is within a few degrees of the actual device junction temperature. Shown is the rise in temperature of the lead frame above ambient (which was 23.8°C) and the increase in supply current with the amplifier biased with a single 24V supply as I_{adj} is increased. This plot shows the thermal resistance of the PCB heat sinking design to be approximately 22°C/W.

Figure 7. Temperature Rise and Supply Current as Quiescent Power Dissipation is Increased (Vcc = 24Vdc).



Maximum output drive capability was measured with different supply voltages for the graph of Figure 8. Here the outputs of the amplifiers are driven to clipping while driving a 100Ω line load and left to warm up for at least 5 minutes. The adjust current was set high at 250µA to further increase the power dissipation. Under these worst case conditions the temperature of the drivers is well below the point where thermal shutdown of the LT1795 will come into effect. Note that the vertical axis serves triple duty to compare three different quantities.

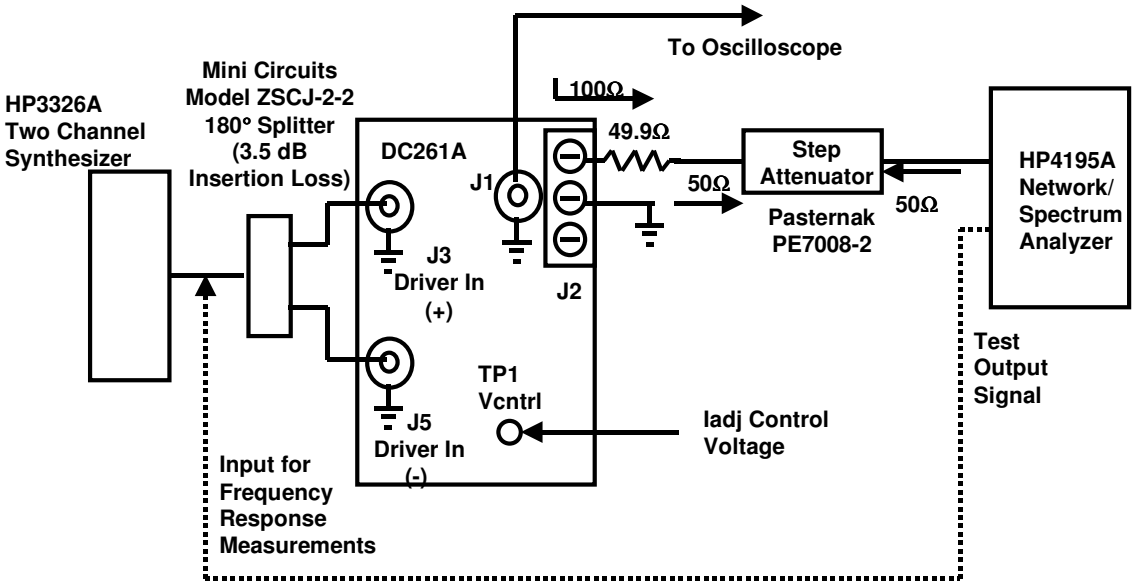
Figure 8. Maximum Drive Characteristics.



Dynamic Performance Characteristics

Figure 9 shows the test set-up for performing Frequency Response, Total Harmonic Distortion and Inter-modulation Distortion tests.

Figure 9. Test Setup for Dynamic Measurements



Frequency Response Measurements

The frequency response of each of the driver amplifiers is flat to within 0.5dB over the range of 30KHz to 1Mhz. These measurements were taken with a +/-15V supply and I_{adj} set to 150µA with the differential amplifier configuration. The lower trace is the gain and the upper trace is the phase on each plot.

Figure 10. Driver(+) Amplifier Frequency Response

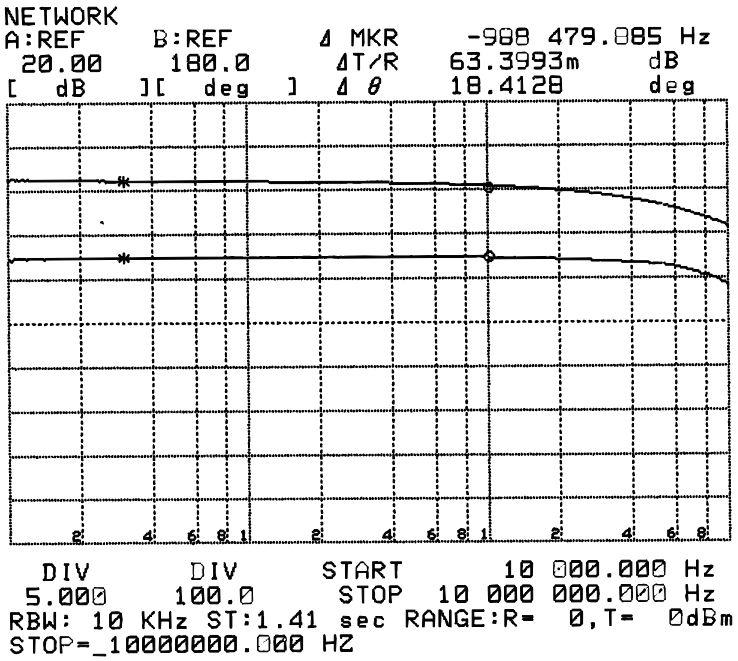


Figure 11. Driver(-) Amplifier Frequency Response

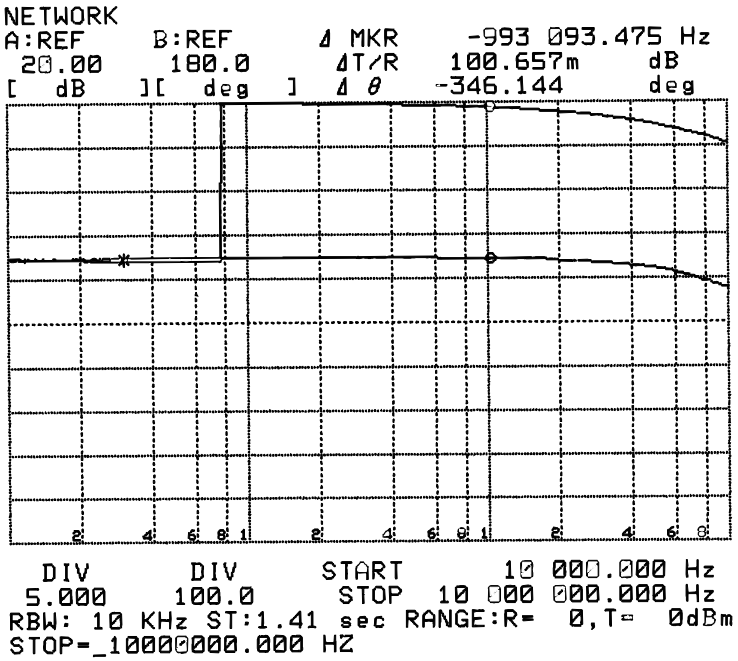
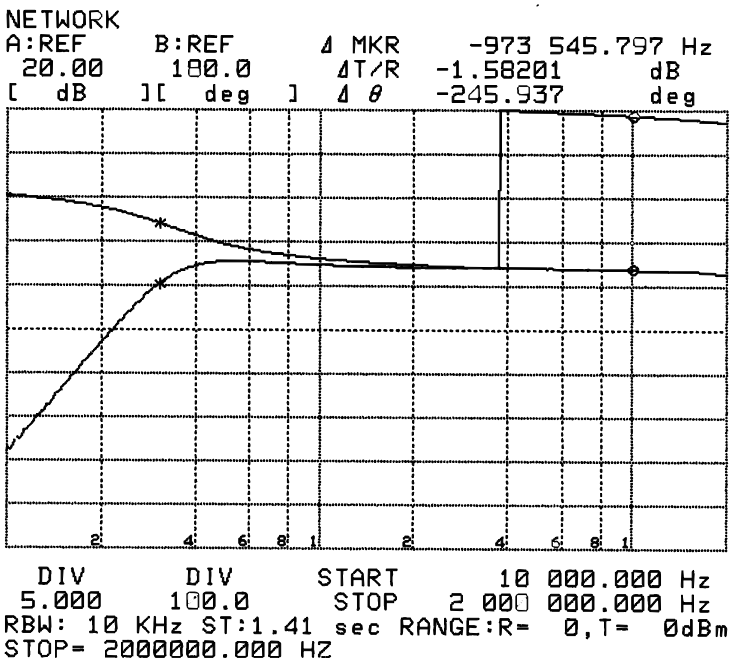


Figure 12. Frequency Response from Input to Line Output (R_{line}=100Ω)



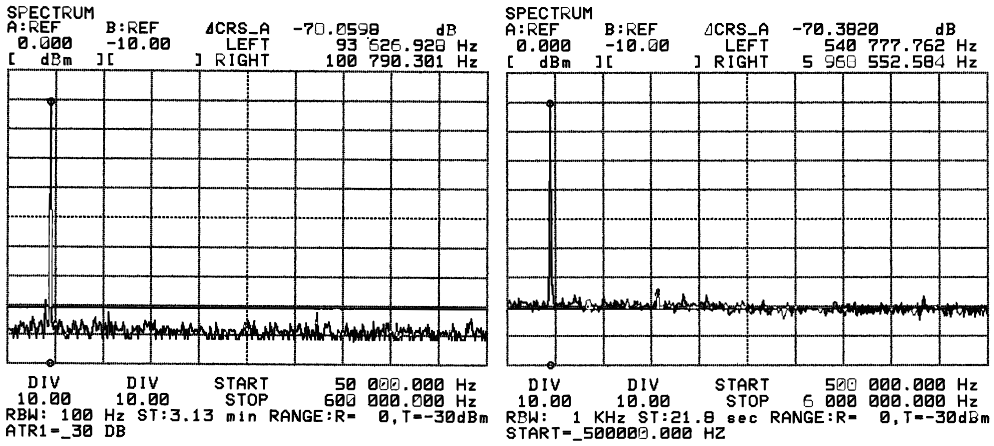
The line-coupling transformer causes the low frequency roll-off in gain.

Total Harmonic Distortion Tests

At all required line power levels, adjusting the operating current can reduce all of the harmonic distortion products down to the noise floor of the test system used for the measurement, <70dBc. It has been observed that an I_{adj} level between 100µA and 150µA, which results in a quiescent supply current between 10mA and 15mA per amplifier is adequate.

Figure 13 shows the spectrum plot of the tone generator used for these measurements.

Figure 13. Signal Generator Distortion

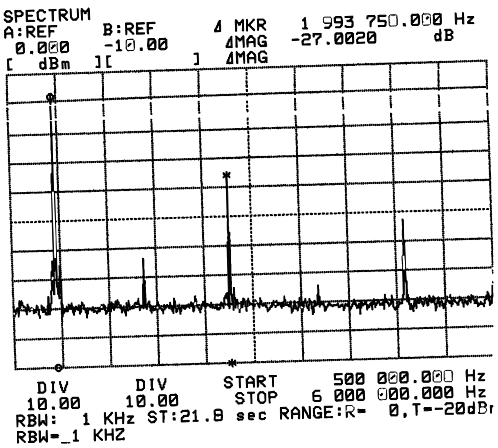


100KHz **1MHz**

As an example of how the operating current adjustment can be used to tune out the harmonic distortion the sequence shown in Figure 14 is presented. Here the drivers have been configured as a differential amplifier and the gain has been increased to 10 by adding a 191Ω resistor between TP3 and TP4. The supply voltage is +/-5V, the line power level is 13dBm and the fundamental tone is 1MHz. The observed range is set to capture up to the 5th harmonic product.

Figure 14. Tuning out Distortion with I_{adj}.
Spurious Free Dynamic Range, SFDR, represents the largest of the distortion products.

a) I_{adj} = 20µA, SFDR = 26dBc



b) I_{adj} = 100µA, SFDR = 62dBc

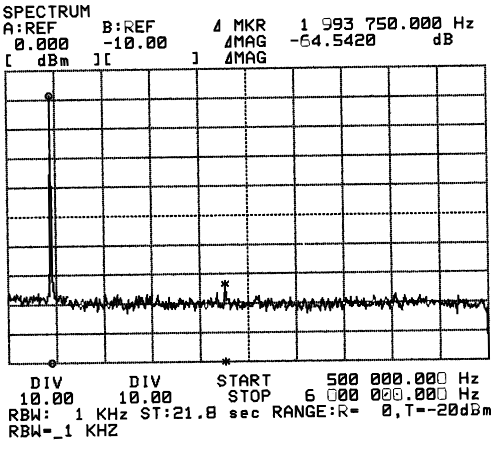
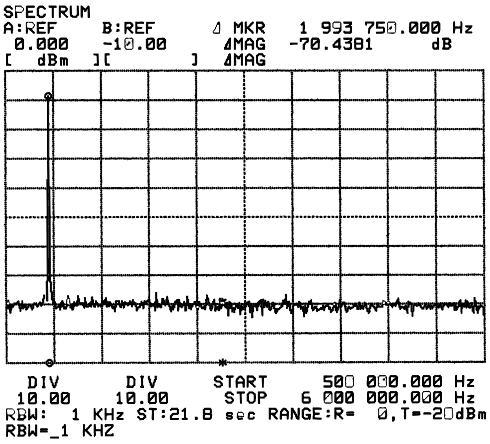
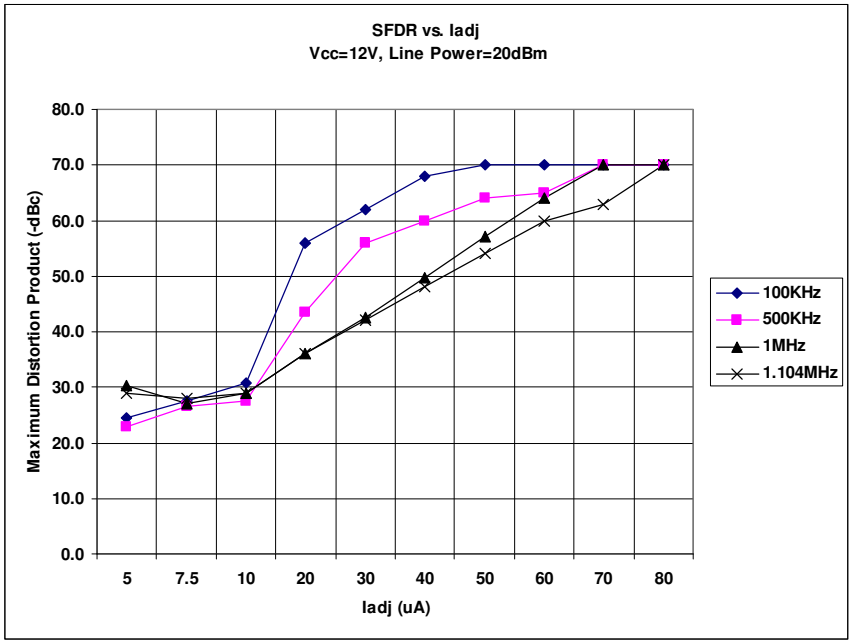


Figure 14c) I_{adj} = 150µA, SFDR = 70dBc



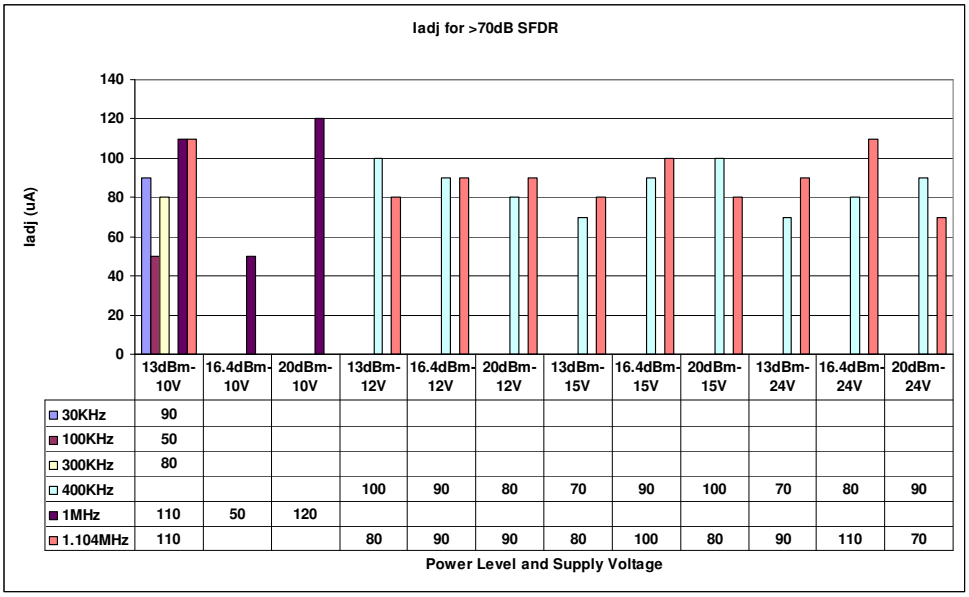
Another indication of improving the SFDR by increasing the operating current is shown in Figure 15. Here the amplifiers are in a gain of 2 differential configuration and various frequencies are applied. The SFDR is noted at several I_{adj} levels until it reaches 70dBc. The increased loop gain over the previous example shows that equivalent distortion can be achieved at even lower levels of operating current. For this test the Line Power was a full 20dBm with a single +12V supply to the board.

Figure 15. SFDR vs. I_{adj} for Various Frequencies



A spot check of different power levels, frequencies and operating supply voltage shows that less than 150µA for I_{adj} is sufficient to achieve an SFDR of at least 70dBc. This is shown in Figure 16.

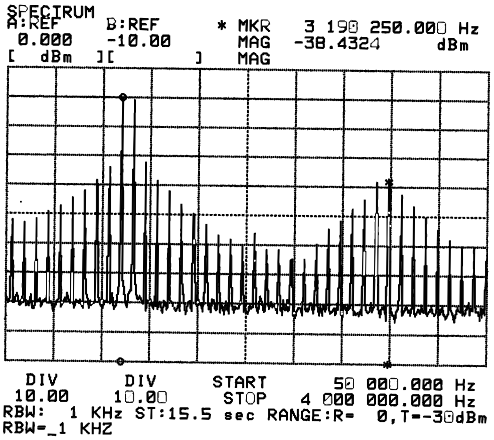
Figure 16. I_{adj} and SFDR Under a Variety of Operating Conditions



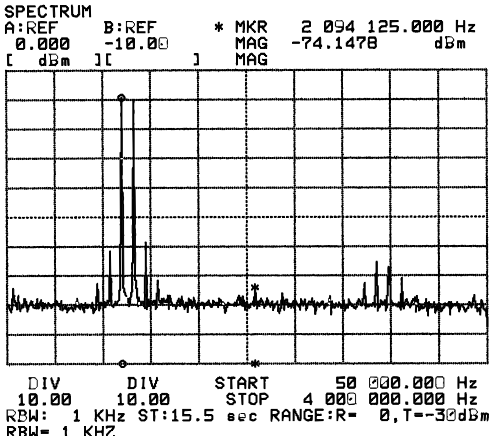
Inter-modulation Distortion

The same distortion minimization holds true for two-tone inter-modulation products also. Figure 17 illustrates the improvement created by increasing the operating current. For this test two equal magnitude tones of 1MHz and 1.1MHz are combined and applied to the 100Ω line load through the differential amplifier configuration. The envelope power is 16.4dBm (4V pk-pk) and the supply voltage is 24V. With I_{adj} of only 10µA, the output signal is very distorted with all harmonic and inter-modulation products evident as seen in Figure 17a. With just a slight increase in I_{adj} current to 40µA, only several of the inter-modulation products remain, Figure 17b. Then at 100µA all of the distortion is removed, 17c.

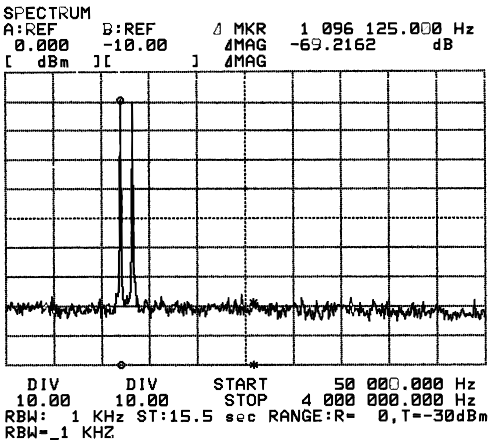
Figure 17. Inter-modulation Distortion Improvement



a) I_{adj} = 10µA



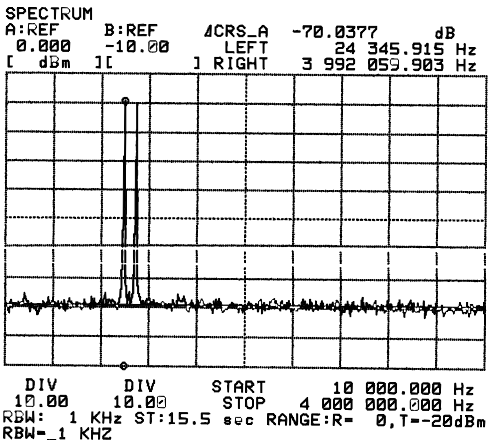
b) I_{adj} = 40µA



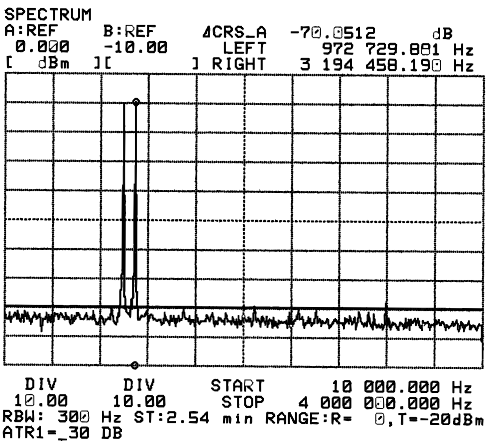
c) I_{adj} = 100µA

In Figure 18 the power level to the line is increased with all other conditions fixed. Here the I_{adj} current is set to 100µA, the supply voltage is +/-15V and the envelope power is varied from 13dBm to 16.4dBm then to 20dBm. As can be seen all of the distortion products are near the resolution of the test system.

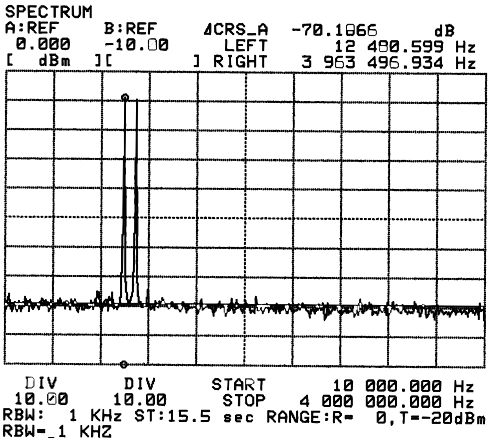
Figure 18. Inter-modulation Distortion at Different Line Power Levels.



a)13dBm



b) 16.4dBm



c) 20dBm

Summary

Demo board DC261 is a versatile tool for use in evaluating the LT1795 Dual amplifier as a line driver in all DSL applications. It provides sufficient heat sinking to handle all power levels and supply voltages. It can be easily configured for split or single supply operation. DC261 also provides the ability to adjust the quiescent operating current to optimize dynamic performance with power consumption and dissipation.

If fixed current operation is desired it is recommended to bias the LT1795 with a current from the Shutdown Reference pin (pin11) of 150µA. This level provides adequate distortion performance with moderate quiescent power consumption. To fix this operating current it is necessary to remove resistor R30 from the board and tack in a resistor from TP5 to TP6. The value of this resistor is dependent on the positive power supply to be used. The following Table provides recommended values for different common supply voltages.

Table 2: Values to Fix I_{adj} to 150µA.

Supply Voltage	Resistor R30 (from TP5 to TP6)
+10V	59KΩ
+12V	71.5KΩ
+15V	93.1KΩ
+24V	150KΩ
+/-5V	23.7KΩ
+/-10V	59KΩ
+/-12V	71.5KΩ
+/-15V	93.1KΩ

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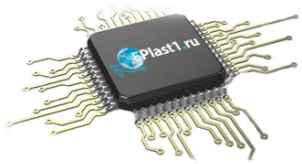
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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