Single-Chip HID USB to SMBus Master Bridge CP2112 Data Sheet

The CP2112 devices are designed to quickly add USB to your applications by eliminating firmware complexity and reducing development time.

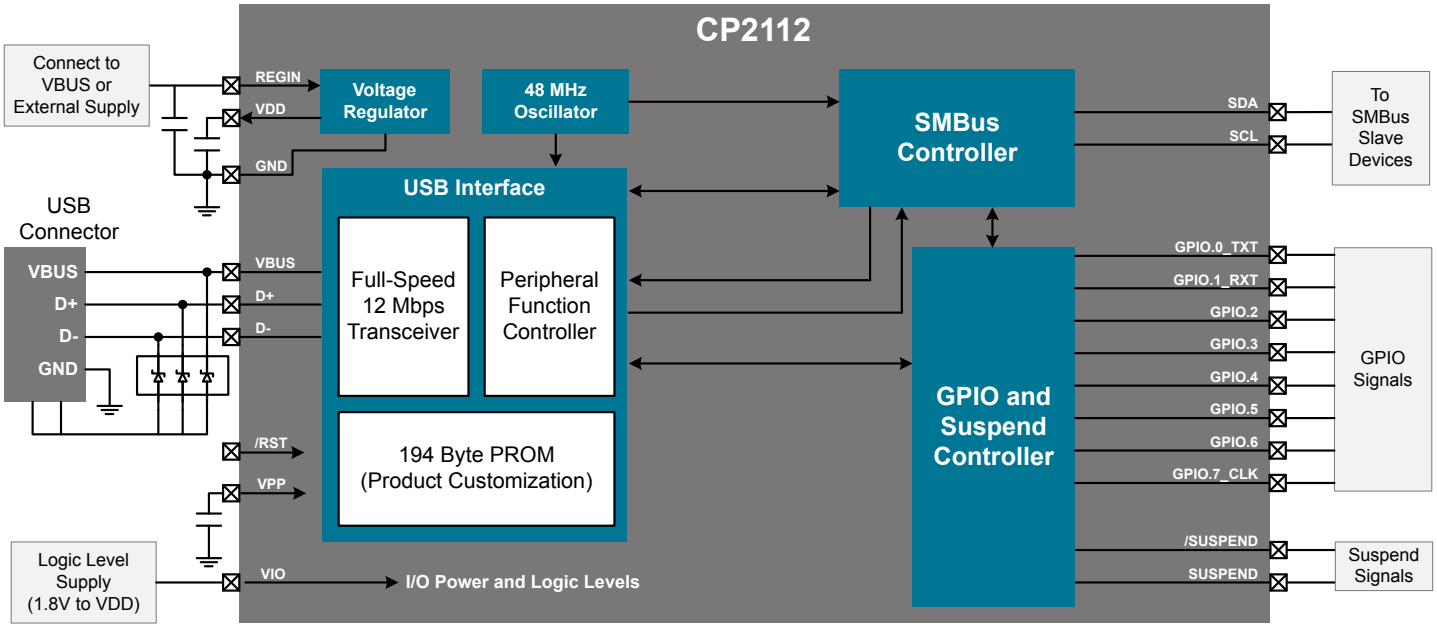
These highly-integrated USB-to-SMBus bridge controllers provide a simple solution for adding USB using a minimum of components and PCB space. The CP2112 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and a total of 8 GPIOs in a compact 4 x 4 mm QFN-24 package. All customization and configuration options can be selected using a simple GUI-based configurator. By eliminating the need for complex firmware and driver development, the CP2112 devices enable quick USB connectivity with minimal development effort.

CP2112 is ideal for a wide range of applications, including the following:

- USB dongles
- Medical meters
- Handheld controllers
- Point-of-Sale products
- Data loggers

KEY FEATURES

- No firmware development required
- Simple GUI-based configurator
- Integrated USB transceiver; no external resistors required
- Integrated clock; no external crystal required
- USB 2.0 full-speed compatible
- Standard HID class device – no custom driver needed
- 8 GPIOs with configurable options



1. Feature List and Ordering Information

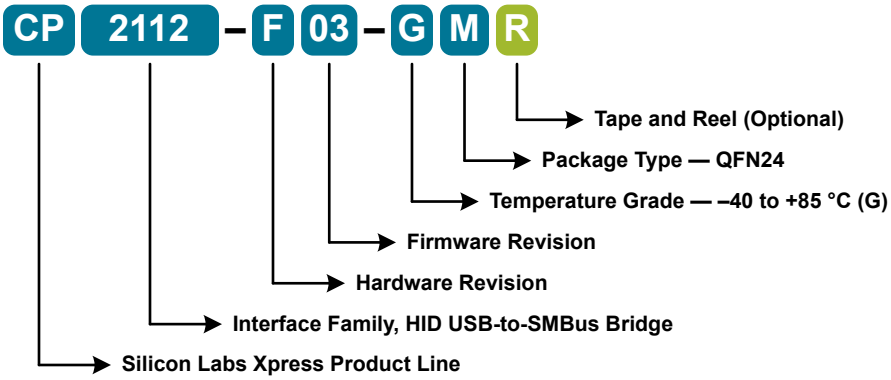


Figure 1.1. CP2112 Part Numbering

The CP2112 devices have the following features:

- **Single-Chip HID USB to SMBus Master Bridge**
  - Integrated USB transceiver; no external resistors or crystal required
  - SMBus master device
  - GPIO can be configured as Input/Output and Open-Drain/Push-Pull
  - 512 Byte SMBus data buffer
  - Integrated 194 Byte One-Time Programmable ROM for storing customizable product information
  - On-chip power-on reset circuit
  - On-chip voltage regulator: 3.45 V output
- **USB Peripheral Function Controller**
  - USB Specification 2.0 compliant; full-speed (12 Mbps)
  - USB Suspend states supported via SUSPEND and /SUSPEND pins
- **HID Interface**
  - Standard USB class device requires no custom driver
  - Supported on Windows, Mac, and Linux
  - Open access to interface specification
- **Windows, Mac, and Linux HID-to-SMBus Libraries**
  - APIs for quick application development
- **SMBus Configuration Options**
  - Configurable Clock Speed
  - Device Address: 7-bit value that is the slave address of the CP2112. The device will only ACK this address, but will not respond to any read/write requests
  - Read/Write Timeouts
  - SCL Low Timeout
  - Retry Counter Timeout
- **GPIO Interface Features**
  - 8 GPIO pins with configurable options
  - Usable as inputs, open-drain or push-pull outputs
  - Configurable clock output for external devices
    - 48 MHz to 94 kHz
  - Toggle LED during SMBus reads
  - Toggle LED during SMBus writes
- **Supply Voltage**
  - Self-powered: 3.0 to 3.6 V
  - USB bus powered: 4.0 to 5.25 V
  - I/O voltage: 1.8 V to V_{DD}
- **Ordering Part Number**
  - CP2112-F03-GM
- **Package**
  - RoHS-compliant 24-pin QFN (4 x 4 mm)
- **Temperature Range: –40 to +85 °C**

2. System Overview

The CP2112 is a highly-integrated HID USB-to-SMBus Bridge providing a simple solution for controlling SMBus slave devices with USB and using a minimum of components and PCB space. The CP2112 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and a one-time programmable ROM in a compact 4 x 4 mm QFN-24 package (sometimes called “MLF” or “MLP”).

The on-chip, one-time programmable ROM provides the option to customize the USB Vendor ID, Product ID, Manufacturer Product String, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired for OEM applications.

The CP2112 uses the standard USB HID device class, which is natively supported by most operating systems. A custom driver does not need to be installed for this device. Host applications communicate with the CP2112 through interface libraries provided by Silicon Labs. The interface specification for the CP2112 is also available to enable development of an API for any operating system that supports HID.

The CP2112 SMBus interface includes the SDA and SCL signals needed for SMBus communication and is configurable. The configurable options include the clock speed, read/write timeouts, retry counter timeout, SCL low timeouts, and a 7-bit device address. The CP2112 will only ACK the 7-bit device address assigned to it but will not respond to any read/write requests. External pull-up resistors are needed for the SCL and SDA signals.

The device also features a total of eight GPIO signals. The GPIO signals are controlled through USB and can be configured as Input/Output and Open-Drain/Push-Pull. Three of the GPIO signals support alternate features including a configurable clock output (48 MHz to 94 kHz) and TX and RX LED toggle. Support for I/O interface voltages down to 1.8 V is provided via a V_{IO} pin.

An evaluation kit for the CP2112 (Part Number: CP2112EK) is available. It includes a CP2112-based HID USB-to-SMBus evaluation board, Windows DLL and test application, USB cable, and full documentation. Go to www.silabs.com for the latest application notes and product support information for the CP2112. Contact a Silicon Labs sales representatives or go to http://www.silabs.com to order the CP2112 Evaluation Kit.

3. Electrical Specifications

3.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in 3.1.1 Recommended Operating Conditions, unless stated otherwise.

3.1.1 Recommended Operating Conditions

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_{DD}		3.0	—	3.6	V
Digital Port I/O Supply Voltage	V_{IO}		1.8	—	V_{DD}	V
Voltage on V_{PP} with respect to GND during a ROM programming operation	V_{PP}	$V_{IO} \geq 3.3$ V	5.75	—	V_{IO} + 3.6	V
Capacitor on V_{PP} for ROM programming	C_{PP}		—	4.7	—	µF
Supply Current [1]	I_{DD}	Normal Operation; V_{REG} Enabled	—	15	16	mA
		Suspended; V_{REG} Enabled	—	130	230	µA
Supply Current - USB Pull-up [2]	I_{USB}		—	200	228	µA
Specified Operating Temperature Range	T_A		-40	—	+85	°C

Note:

1. If the device is connected to the USB bus, the USB pull-up current should be added to the supply current to calculate total required current.
2. The USB pull-up supply current values are calculated values based on USB specifications.

3.1.2 SMBus, GPIO, and Suspend I/O Electrical Characteristics

Table 3.2. SMBus, GPIO, and Suspend I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	I_{OH} = -10 µA	V_{IO} – 0.1	—	—	V
		I_{OH} = -3 mA	V_{IO} – 0.2	—	—	V
		I_{OH} = -10 mA	—	V_{IO} – 0.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 10 µA	—	—	0.1	V
		I_{OL} = 8.5 mA	—	—	0.4	V
		I_{OL} = 25 mA	—	0.6	—	V
Input High Voltage	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Input Leakage Current	I_{LK}	Weak Pull-Up Off	—	—	1	µA
		Weak Pull-Up On, V_{IO} = 0 V	—	25	50	µA
Maximum Input Voltage	V_{IN-MAX}	Open drain, logic high (1)	—	—	5.8	V

3.1.3 Reset Electrical Characteristics

Table 3.3. Reset

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
/RST Input High Voltage	V_{IH-RST}		0.75 x V_{IO}	—	—	V
/RST Input Low Voltage	V_{IL-RST}		—	—	0.6	V
Minimum /RST Low Time to Generate a System Reset	t_{RSTL}		15	—	—	µs
VDD Ramp Time	t_{RMP}		—	—	1	ms

3.1.4 Voltage Regulator

Table 3.4. Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range	V_{REGIN}		3.0	—	5.25	V
Output Voltage	V_{DD}	Output Current = 1 to 100 mA[1]	3.3	3.45	3.6	V
VBUS Detection Input Threshold	$V_{IH-VBUS}$		2.5	—	—	V
Bias Current	I_{REG}		—	—	120	µA

Note:
1. The maximum regulator supply current is 100 mA. This includes the supply current of the CP2112.

3.1.5 GPIO

Table 3.5. GPIO Output Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GPIO.7 Clock Output	f_{CLK}		Output x 0.985	Output[1]	Output x 1.015	Hz
TX Toggle Rate	f_{TX}		—	10	—	Hz
RX Toggle Rate	f_{RX}		—	10	—	Hz

Note:
1. The output frequency is configurable from 48 MHz to 94 kHz.

3.1.6 SMBus Timing

Table 3.6. SMBus Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[3]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	255[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[3]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

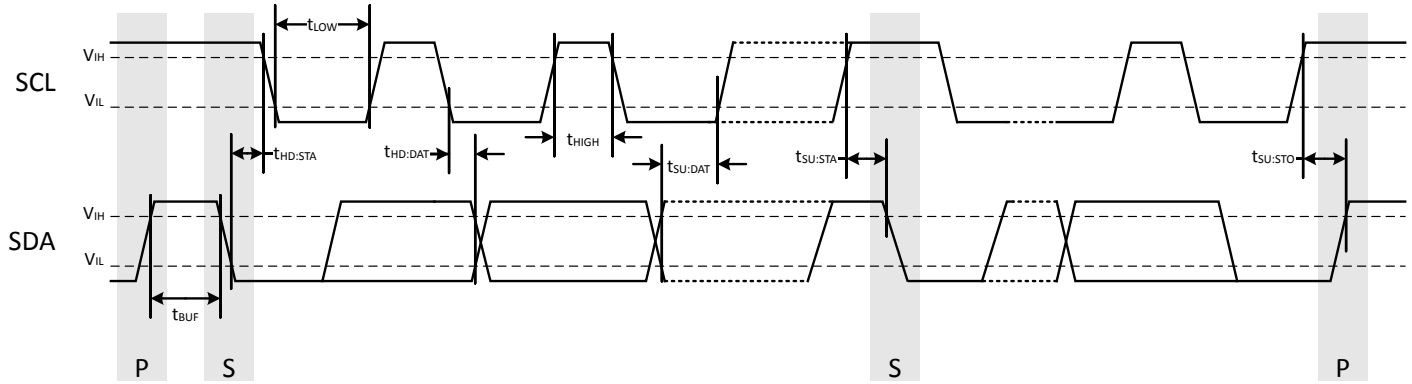


Figure 3.1. SMBus Timing Diagram (Master Mode)

3.2 Absolute Maximum Ratings

Stresses above those listed in 3.2 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 3.7. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on /RST, SDA, SCL, or GPIO Pins with respect to GND	V_{GPIO}	VIO ≥ 2.2 V	-0.3	5.8	V
		VIO < 2.2 V	-0.3	V_{IO} + 3.6	V
Voltage on VBUS with respect to GND	V_{BUS}	VDD ≥ 3.0 V	-0.3	5.8	V
		VDD not powered	-0.3	V_{IO} + 3.6	V
Voltage on V_{DD} or V_{IO} with respect to GND	V_{DD} or V_{IO}		-0.3	4.2	V
Maximum Total Current through V_{DD}, V_{IO}, and GND	I_{DD} or I_{IO}		—	500	mA
Maximum Output Current sunk by /RST or any I/O pin	I_{GPIO}		—	100	mA
Operating Junction Temperature	T_J		-40	105	°C

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Pin Definitions

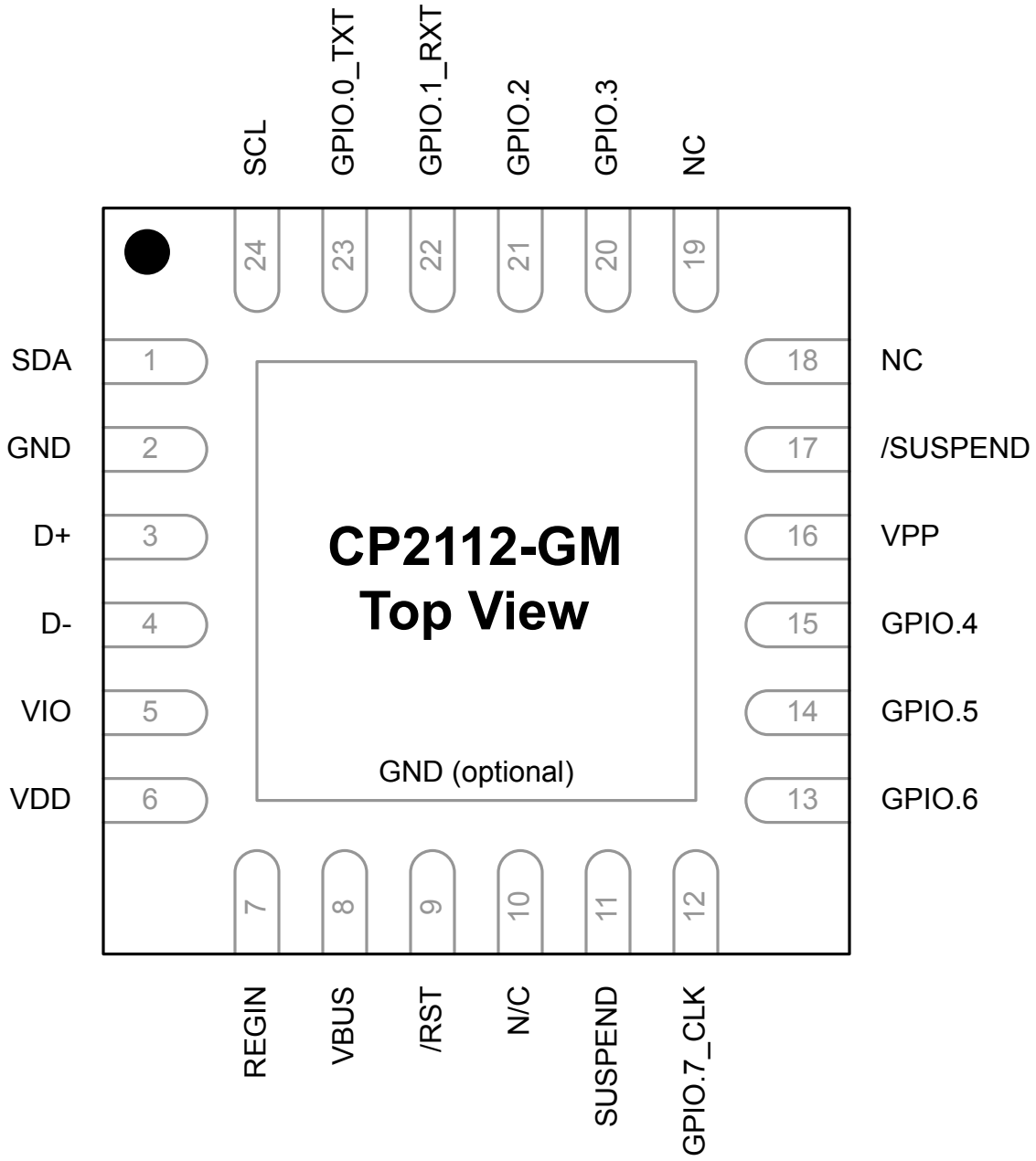


Figure 4.1. CP2112 Pin Definitions

Table 4.1. Pin Definitions for CP2112 QFN24

Pin #	Name	Type	Description
1	SDA	D I/O	Serial Data signal for SMBus interface.
2	GND		Ground. Must be tied to ground.
3	D+	D I/O	USB D+
4	D–	D I/O	USB D–

Pin #	Name	Type	Description
5	VIO	Power In	I/O Supply Voltage Input.
6	VDD	Power In	Power Supply Voltage Input.
		Power Out	Voltage Regulator Output. See Section 9.
7	REGIN	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
8	VBUS	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.
9	RST	D I/O	Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 4.
10[1]	NC	—	This pin should be left unconnected or tied to VIO
11[1]	SUSPEND	D Out	This pin is logic high when the CP2112 is in the USB Suspend state.
12[1]	GPIO.7	D I/O	This pin is a user-configurable input or output.
	CLK	D Out	In CLK mode, this pin outputs a clock signal whose frequency is configurable.
13[1]	GPIO.6	D I/O	This pin is a user-configurable input or output.
14[1]	GPIO.5	D I/O	This pin is a user-configurable input or output.
15[1]	GPIO.4	D I/O	This pin is a user-configurable input or output.
16[1]	VPP	Special	Connect a 4.7 µF capacitor between this pin and ground to support ROM programming via the USB interface.
17[1]	/SUSPEND	D Out	This pin is logic low when the CP2112 is in the USB Suspend state.
18[1], 19[1]	NC	—	No connect
20[1]	GPIO.3	D I/O	This pin is a user-configurable input or output.
21[1]	GPIO.2	D I/O	This pin is a user-configurable input or output.
22[1]	GPIO.1	D I/O	This pin is a user-configurable input or output.
	RXT	D Out	In RXT mode, this pin is the Receive Toggle pin and toggles to indicate SMBus transmission. The pin is logic high when a transmission is not in progress.
23[1]	GPIO.0	D I/O	This pin is a user-configurable input or output.
	TXT	D Out	In TXT mode, this pin is the Transmit Toggle pin and toggles to indicate SMBus transmission. The pin is logic high when a transmission is not in progress.
24	SCL	D I/O	Serial Clock signal for SMBus interface.
Center	GND	—	Ground

Note:

1. Pins can be left unconnected when not in use.

5. QFN24 Package Specifications

5.1 QFN24 Package Dimensions

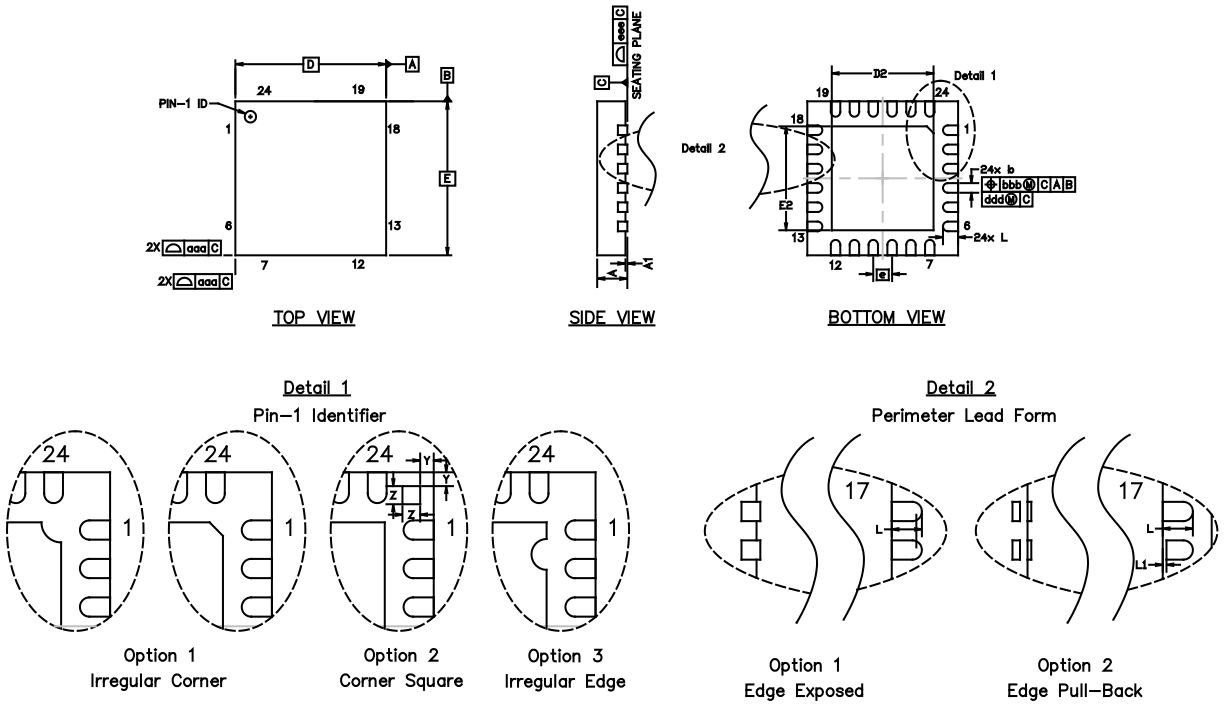


Figure 5.1. QFN24 Package Drawing

Table 5.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.55	2.70	2.80
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.55	2.70	2.80
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2 QFN24 PCB Land Pattern

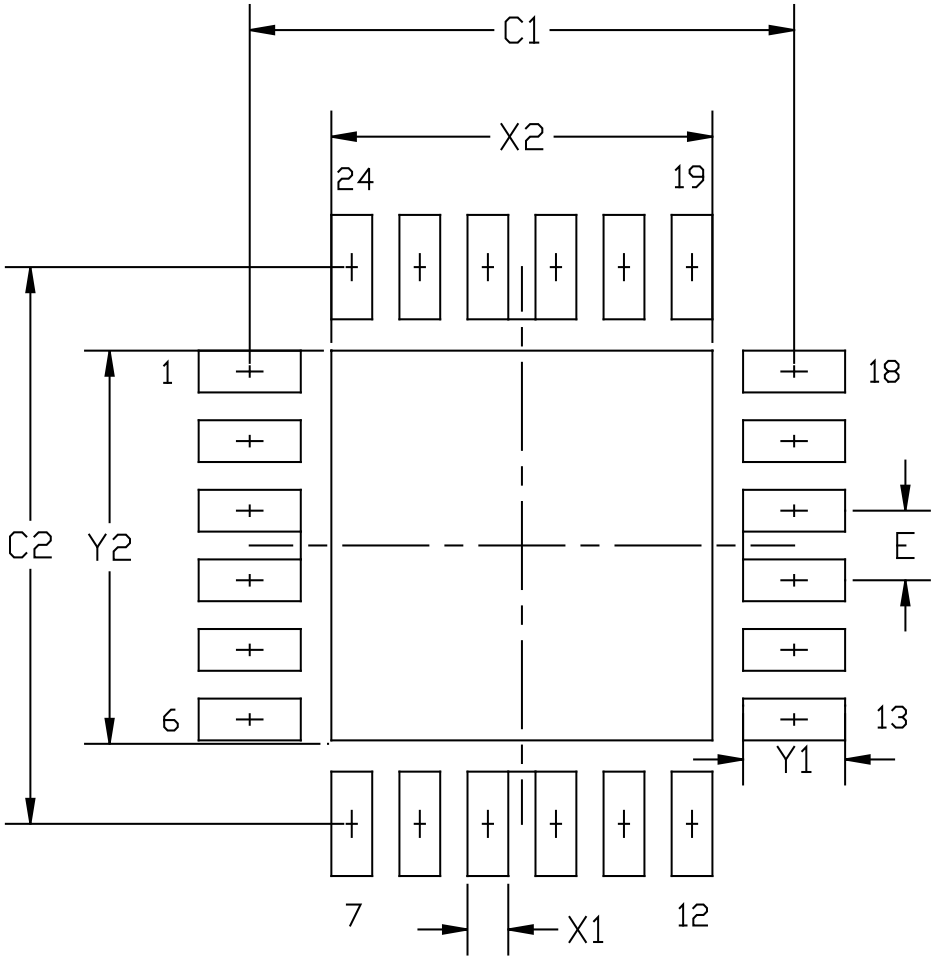


Figure 5.2. QFN24 Recommended PCB Land Pattern

Table 5.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC	
X1	0.20	0.30
X2	2.70	2.80
Y1	0.65	0.75
Y2	2.70	2.80

Dimension	Min	Max

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.3 QFN24 Package Marking

Figure 5.3. QFN24 Package Marking

The package marking consists of:

- TTTTT – A trace or manufacturing code. The first letter of this code is the silicon revision.
- YY – The last two digits of the assembly year.
- WW – The two-digit workweek when the device was assembled.
- + – Lead-free (RoHS compliance) designator.

6. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2112 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all data transfers between the USB and the SMBus interface as well as command requests generated by the USB host controller and commands for controlling the function of the SMBus interface and GPIO pins.

The USB Suspend and Resume modes are supported for power management of both the CP2112 device and external circuitry. The CP2112 enters Suspend mode when Suspend signaling is detected on the bus. Upon entering Suspend mode, the Suspend signals are asserted. The Suspend signals are also asserted after a CP2112 reset until device configuration during USB enumeration is complete. SUSPEND is logic high when the device is in the Suspend state and logic low when the device is in normal mode. The /SUSPEND pin has the opposite logic value of the SUSPEND pin.

The CP2112 exits Suspend mode when any of the following events occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. SUSPEND and SUSPEND are weakly pulled to VIO in a high-impedance state during a CP2112 reset. If this behavior is undesirable, a strong pulldown resistor (10 kΩ) can be used to ensure /SUSPEND remains low during reset. The eight GPIO pins will retain their state during Suspend mode.

7. System Management Bus (SMBus) Interface

The SMBus I/O interface is a two-wire, bidirectional serial bus. The SMBus is compliant with the System Management Bus Specification, Version 1.1, and compatible with the I^2C serial bus. Reads and writes to the interface by the system controller are byte-oriented with the SMBus interface autonomously controlling the serial transfer of the data. The CP2112 operates as an SMBus master; however, it has an SMBus slave address that is configurable. The CP2112 will only ACK this address and will not respond to any read or write requests. If the least significant bit of the address is set, the device will ignore it.

7.1 SMBus Configuration

The following figure shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bidirectional serial clock (SCL) and serial data (SDA) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively. The SMBus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation.

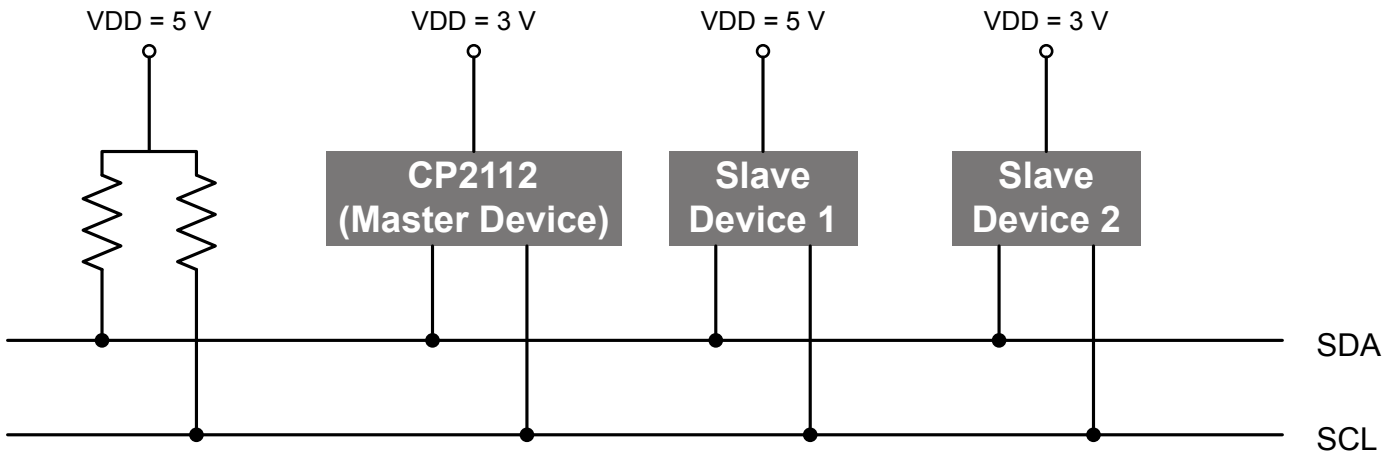


Figure 7.1. Typical SMBus Configuration

7.2 SMBus Operation

The CP2112 supports reads, writes, and addressed reads. The master device initiates all three types of data transfers and provides the clock pulses on SCL. The SMBus interface on the CP2112 operates as a master, but also has a configurable slave address associated with it that the CP2112 will only ACK upon receiving. Multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the Master in a system; any device that transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figures 6, 7, and 8). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation. All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data one byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. The first figure illustrates a typical CP2112 read transaction, and the second figure illustrates a typical CP2112 write transaction.

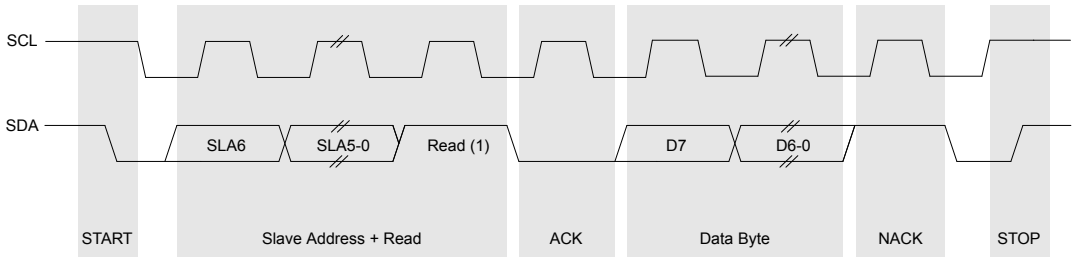


Figure 7.2. Typical CP2112 Read

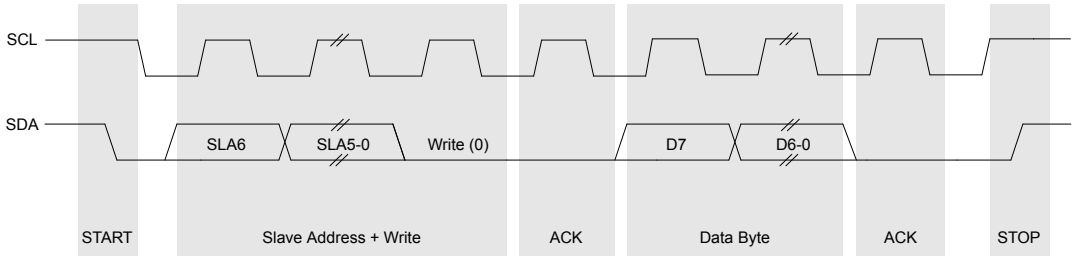


Figure 7.3. Typical CP2112 Write

The CP2112 performs addressed reads using a repeated start. Addressed Reads are implemented by issuing a START condition followed by a slave address write and logical address. Next the CP2112 issues a repeated START followed by a slave address read. After this sequence, the CP2112 reads bytes from the slave device. The CP2112 supports addressed reads on slave devices with up to a 16 byte logical address field. The following figure illustrates a typical addressed read transaction (with a one byte logical address field).

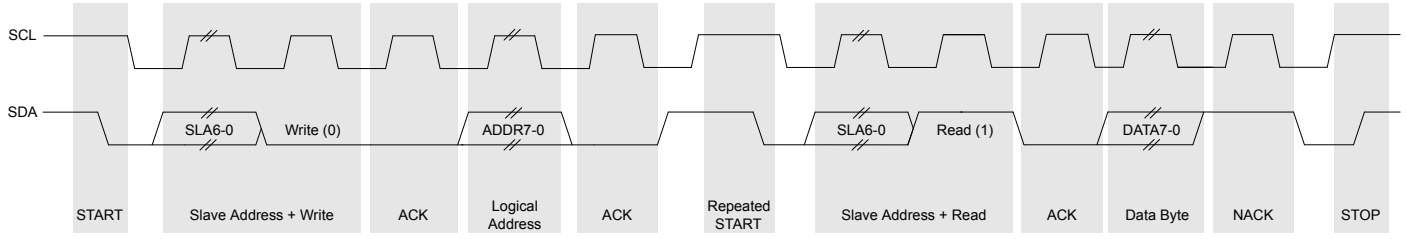


Figure 7.4. Typical CP2112 Addressed Read

7.3 CP2112 Configuration Options

The CP2112 has the following SMBus configuration options, which are all configured through USB: clock speed, device address, auto send read, read timeout, write timeout, SCL low timeout, and retry time.

- The SMBus clock speed is configurable with a recommended operating range of 10 kHz to 400 kHz.
- The device address is a configurable 7-bit address, which is the slave address of the CP2112. Although the CP2112 is a master device, the CP2112 will ACK this address but will not respond to any read or write requests. If the least significant bit is set, the CP2112 will ignore it.
- If auto read send is set to 0x01, the CP2112 will return the results of a read automatically. If this is set to 0x00, the device will wait for a "data read response" request to respond to data.
- The read and write timeouts are the time limit before the device will automatically cancel a transfer that has been initiated and can range from 0 to 1000 ms. If set to 0 ms, this indicates that there is no timeout.
- The SCL low timeout is either enabled or disabled. If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a "timeout" condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.
- The retry time is the number of times the device will attempt a transfer before terminating the transfer. This can be set from 0 to 1000. If set to 0, there is no retry limit.

These configuration options cannot be changed while a transfer is in progress.

8. GPIO Pins

The CP2112 supports 8 user-configurable GPIO pins. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. Three of these GPIO pins also have alternate functions which are listed in the following table.

Table 8.1. GPIO Pin Alternate Functions

GPIO Pin	Alternate Function
GPIO.0	TX Toggle
GPIO.1	RX Toggle
GPIO.7	CLK Output

By default, all of the GPIO pins are configured as a GPIO input. The pins must be configured each time the device is reset. For example, if a device is unplugged and then plugged into a PC, the GPIO pins would be configured as inputs and would need to be reconfigured as needed.

The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

8.1 GPIO.0-1—Transmit and Receive Toggle

GPIO.0 and GPIO.1 are configurable as Transmit Toggle and Receive Toggle pins. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 3.5 GPIO Output Specifications on page 5 when data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

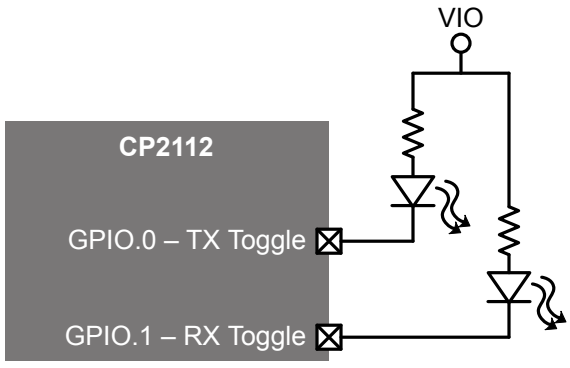


Figure 8.1. Transmit and Receive Toggle Typical Connection Diagram

8.2 GPIO.7—Clock Output (CLK)

GPIO.7 is configurable to output a configurable CMOS clock output. The clock output appears at the pin at the same time the device completes enumeration and exits USB Suspend mode. The clock output is removed from the pin when the device enters USB Suspend mode. The output frequency is configurable through the use of a divider and the accuracy is specified in Table 6. When the divider is set to 0, the output frequency is 48 MHz. For divider values between 1 and 255, the output frequency is determined by the formula:

$$\text{GPIO.7 Clock Frequency} = \frac{48\ \text{MHz}}{2 \times \text{Clock Divider}}$$

9. One-Time Programmable ROM

The CP2112 includes an internal, one-time programmable ROM that may be used to customize the USB vendor ID (VID), product ID (PID), manufacturer string, product description string, power descriptor, device release number, and device serial number as desired for OEM applications. If the programmable ROM has not been customized, the default configuration data shown in the table below is used.

Table 9.1. Default USB Configuration Data

Name	Description	Default Value
Vendor ID (VID)	The Vendor ID is a four digit hexadecimal number that is unique to a particular vendor. 10C4h, for example, is the Silicon Labs Vendor ID.	10C4h
Product ID (PID)	The Product ID is a four digit hexadecimal number that identifies the vendor's device. EA90h, for example, is the default Product ID for Silicon Labs' CP2112 HID USB-to-SMBus Bridge devices.	EA90h
Power Descriptor (Attributes)	This setting determines whether the device is Bus-Powered, i.e. it is powered by the host, or Self-Powered, i.e. it is powered from a supply on the device.	80h (Bus-Powered)
Power Descriptor (Max Power)	This describes the maximum amount of power that the device will draw from the host in mA multiplied by 2. For example, 32h equates to 100 mA.	32h (100 mA)
Release Number	The Release Version is a binary-coded-decimal value that is assigned by the device manufacturer.	0100h (Release Version 01.00)
Manufacturer String	This string is customizable and can be a maximum of 30 ASCII characters.	"Silicon Laboratories" (30 ASCII characters maximum)
Product Description String	The Product String is an optional string that describes the product. It is limited to 30 ASCII characters.	"CP2112 HID USB-to-SMBus Bridge" (30 ASCII characters maximum)
Serial String	The Serial String is an optional string that is used by the host to distinguish between multiple devices with the same VID and PID combination. It is limited to 30 ASCII characters.	Unique 8-character ASCII string (30 ASCII characters maximum)

While customization of the USB configuration data is optional, customizing the VID/PID combination is strongly recommended. A unique VID/PID will prevent the device from being recognized by any other manufacturer's software application. A vendor ID can be obtained from www.usb.org, or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Labs VID. Customizing the serial string for each individual device is also recommended if the OEM application is one in which it is possible for multiple CP2112-based devices to be connected to the same PC.

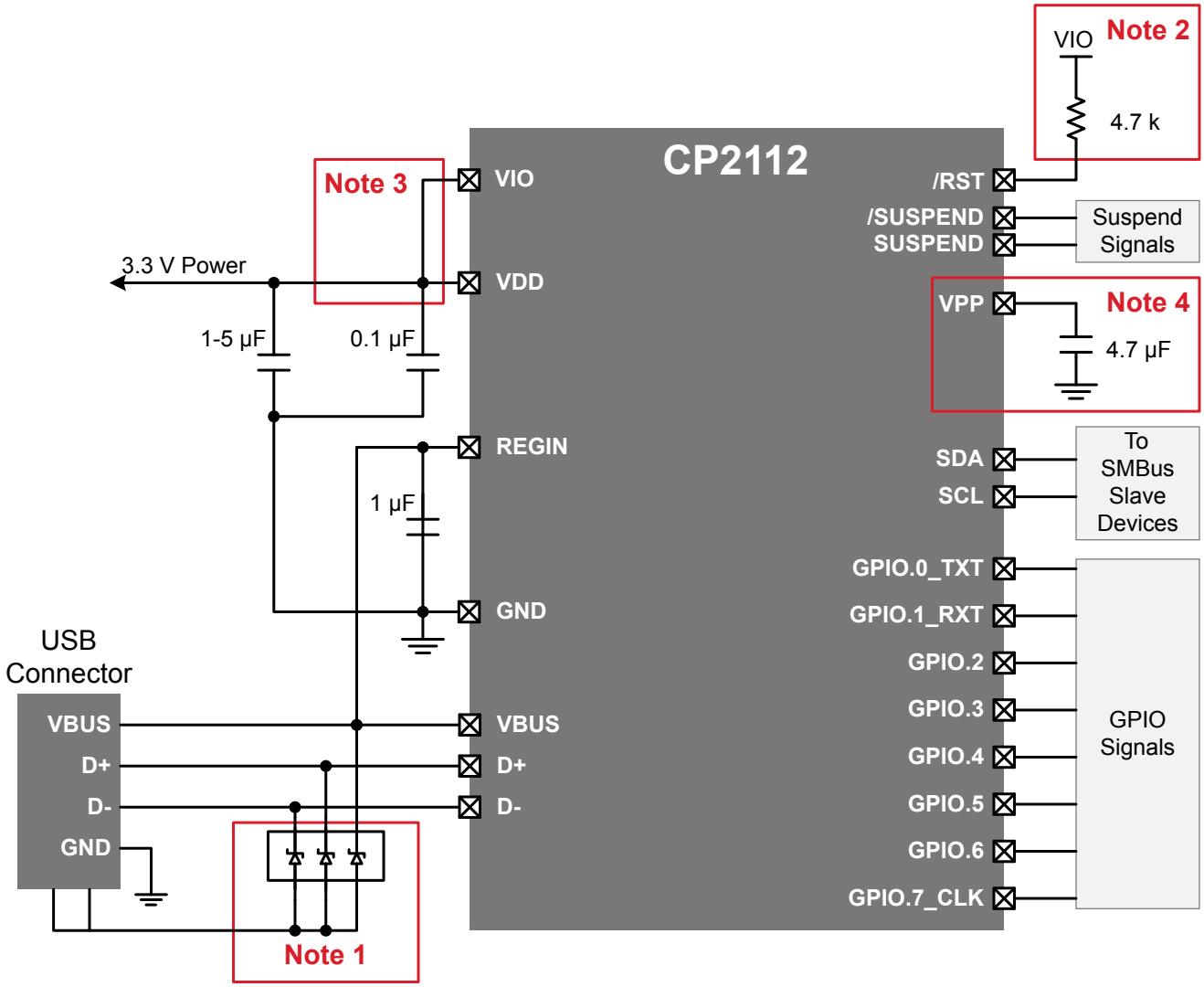
AN495: CP2112 Interface Specification includes more information about the programmable values and their valid options. Note that certain items in the PROM are programmed as a group, and programming one of these items in a group prevents further programming of any of the other items in the group.

The configuration data ROM is programmable by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface by adding a capacitor to the PCB. If configuration ROM is to be programmed in-system, a 4.7 µF capacitor must be added between the VPP pin and ground. No other circuitry should be connected to VPP during a programming operation, and VIO must remain at 3.3 V or higher to successfully write to the configuration ROM.

10. Voltage Regulator

The CP2112 includes an on-chip 5.0 to 3.45 V voltage regulator. This allows the CP2112 to be configured as either a USB bus-powered device or a USB self-powered device. A typical connection diagram of the device in a bus-powered application using the regulator is shown in Figure 10.1 Typical Bus-Powered Connection Diagram on page 20. When enabled, the voltage regulator output appears on the V_{DD} pin and can be used to power external devices. See 3.1.4 Voltage Regulator for the voltage regulator electrical characteristics.

If the regulator is used to provide VDD in a self-powered application, use the same connections from Figure 10.1 Typical Bus-Powered Connection Diagram on page 20, but connect REGIN to an onboard 5 V supply, and disconnect it from the VBUS pin. In addition, if REGIN may be unpowered while VBUS is 5 V, a resistor divider shown in Note 5 of Figure 10.2 Typical Self-Powered Connection Diagram (Regulator Bypass) on page 21 is required to meet the absolute maximum voltage on VBUS specification in 3.2 Absolute Maximum Ratings.

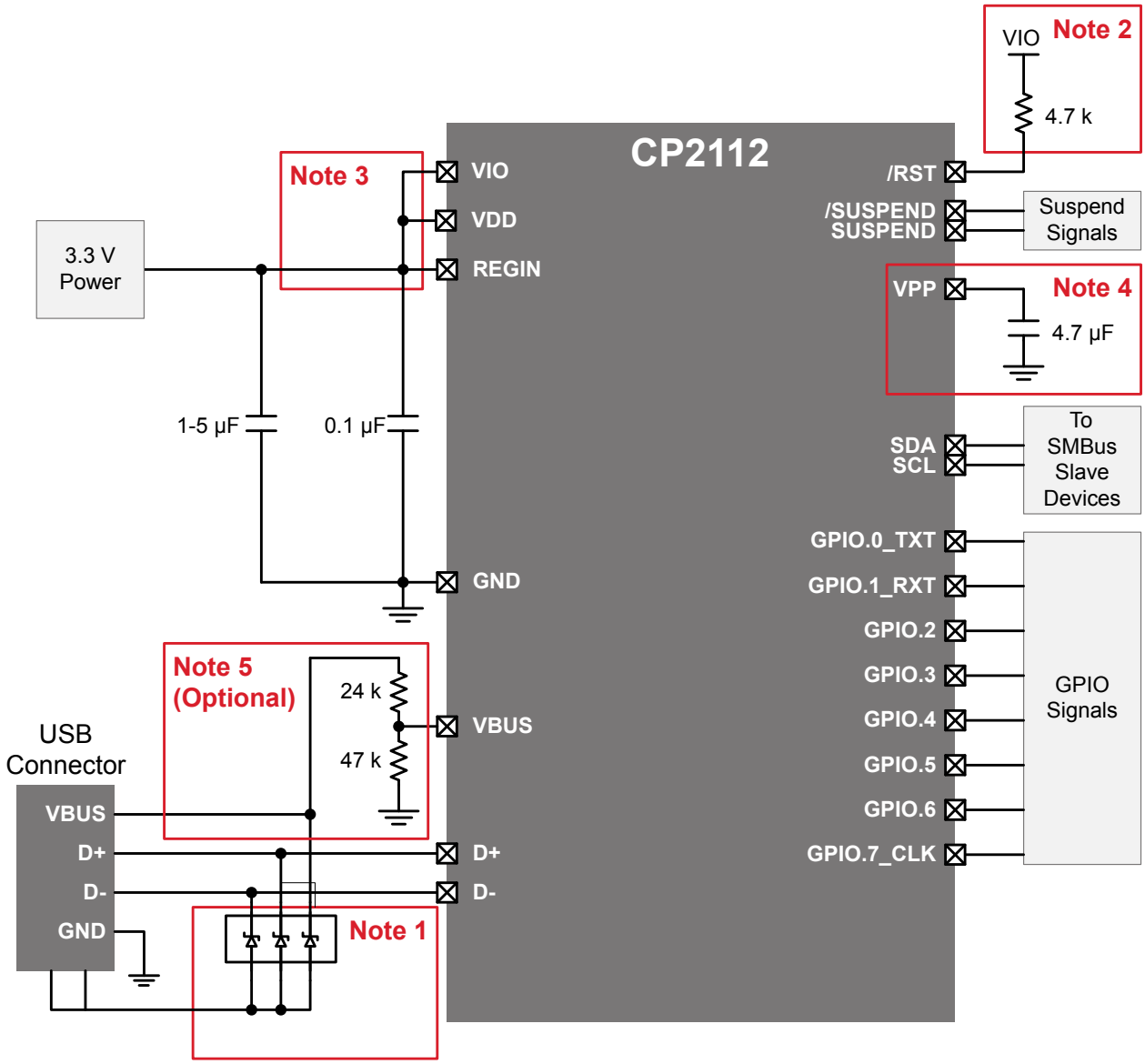


Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If programming the configuration ROM via USB, add a 4.7 µF capacitor between VPP and ground. During a programming operation, do not connect the VPP pin to other circuitry, and ensure that VIO is at least 3.3 V.

Figure 10.1. Typical Bus-Powered Connection Diagram

Alternatively, if 3.0 to 3.6 V power is supplied to the VDD pin, the CP2112 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, tie the REGIN input to VDD to bypass the voltage regulator. A typical connection diagram showing the device in a self-powered application with the regulator bypassed is shown in the following figure.

The USB max power and power attributes descriptor must match the device power usage and configuration. See the Xpress Configurator utility within Simplicity Studio (www.silabs.com/simplicity) for information on how to customize USB descriptors for the CP2112.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If programming the configuration ROM via USB, add a 4.7 µF capacitor between VPP and ground. During a programming operation, do not connect the VPP pin to other circuitry, and ensure that VIO is at least 3.3 V.
Note 5 : For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 10.2. Typical Self-Powered Connection Diagram (Regulator Bypass)

11. Relevant Application Notes and Software

The following Application Notes are applicable to the CP2112 devices. The latest versions of these application notes and their accompanying software are available at www.silabs.com/interface-appnotes or within Simplicity Studio in the [**Application Notes**] area.

- *AN721: CP210x Device Customization Guide* — This application note guides developers through the configuration process of devices using Simplicity Studio [**Xpress Configurator**].
- *AN495: CP2112 Interface Specification* — This document describes how to interface to the CP2112 using the low-level, HID Interface.
- *AN496: CP2112 HID USB-to-SMBus API Specification* — This document describes how to interface to the CP2112 using the interface library, available for various operating systems.

The CP2112 Software Development Kit can be downloaded from www.silabs.com/interface-software. See the Xpress Configurator utility in Simplicity Studio (www.silabs.com/simplicity) for information on how to customize USB descriptors for the CP2112.

The CP2112 is a USB Human Interface Device (HID), and, since most operating systems include native drivers, custom drivers do not need to be installed. Because the CP2112 does not fit a standard HID device type, such as a keyboard or mouse, any CP2112 PC application needs to use the CP2112's HID specification to communicate with the device. The low-level HID specification for the CP2112 is provided in *AN495: CP2112 Interface Specification*. This document describes all of the basic functions for opening, reading from, writing to, and closing the device, as well as the ROM programming functions.

An interface library is available for various operating systems that encapsulates the CP2112 HID interface and also adds higher level features, such as read/write timeouts is provided by Silicon Labs. This library is the recommended interface for the CP2112. The interface library is documented in *AN496: CP2112 HID USB-to-SMBus API Specification*.

12. Revision History

12.1 Revision 1.3

February 1st, 2017

Updated orderable part number to CP2112-F03-GM.

Updated document formatting.

Removed specific operating system versions supported.

Added 3.1.6 SMBus Timing.

Added Operating Junction Temperature to Table 3.7 Absolute Maximum Ratings on page 7.

Swapped the pin number and name columns in Table 4.1 Pin Definitions for CP2112 QFN24 on page 8 and reordered the rows based on pin number. Also added the GND center pad to the table.

Added 5.3 QFN24 Package Marking.

Added the Description column to Table 9.1 Default USB Configuration Data on page 19.

Updated all references from VDD to VIO when discussing minimum voltage requirements when programming the One-Time Programmable ROM.

Updated Figure 10.1 Typical Bus-Powered Connection Diagram on page 20 and Figure 10.2 Typical Self-Powered Connection Diagram (Regulator Bypass) on page 21 to remove an extra, erroneous GPIO.

Updated all references of CP2112_SetIDs to Xpress Configurator in Simplicity Studio.

Combined the CP2112 Interface Specification and Windows Interface DLL and 11. Relevant Application Notes and Software into one section.

Removed the Device Specific Behavior section and moved this information to the device errata.

12.2 Revision 1.2

November 2013

Added a row for VBUS in 3.2 Absolute Maximum Ratings.

Added VDD Ramp Time for Power On specification to 3.1.3 Reset Electrical Characteristics.

Added VPP Voltage and Capacitor specifications to 3.1.1 Recommended Operating Conditions.

Removed AN144 references.

Added references to the CP2112_SetIDs software and CP2112 SDK.

Updated 10. Voltage Regulator to add absolute maximum voltage on VBUS requirements in self-powered systems.

12.3 Revision 1.1

July 2011

Updated ordering part number.

Updated 7.2 SMBus Operation to describe SMBus transactions supported by CP2112.

Updated Figure 7.2 Typical CP2112 Read on page 16 and added Figure 7.3 Typical CP2112 Write on page 16 and Figure 7.4 Typical CP2112 Addressed Read on page 16.

Added Device Specific Behavior chapter, which documents the differences between revisions F01 and F02.

12.4 Revision 1.0

October 2010

Removed preliminary language.

12.5 Revision 0.5

Updated 3.1.2 SMBus, GPIO, and Suspend I/O Electrical Characteristics.

Updated 3.1.3 Reset Electrical Characteristics.

Updated 3.1.4 Voltage Regulator.

Updated Table 9.1 Default USB Configuration Data on page 19.

12.6 Revision 0.1

May 2010

Initial release.

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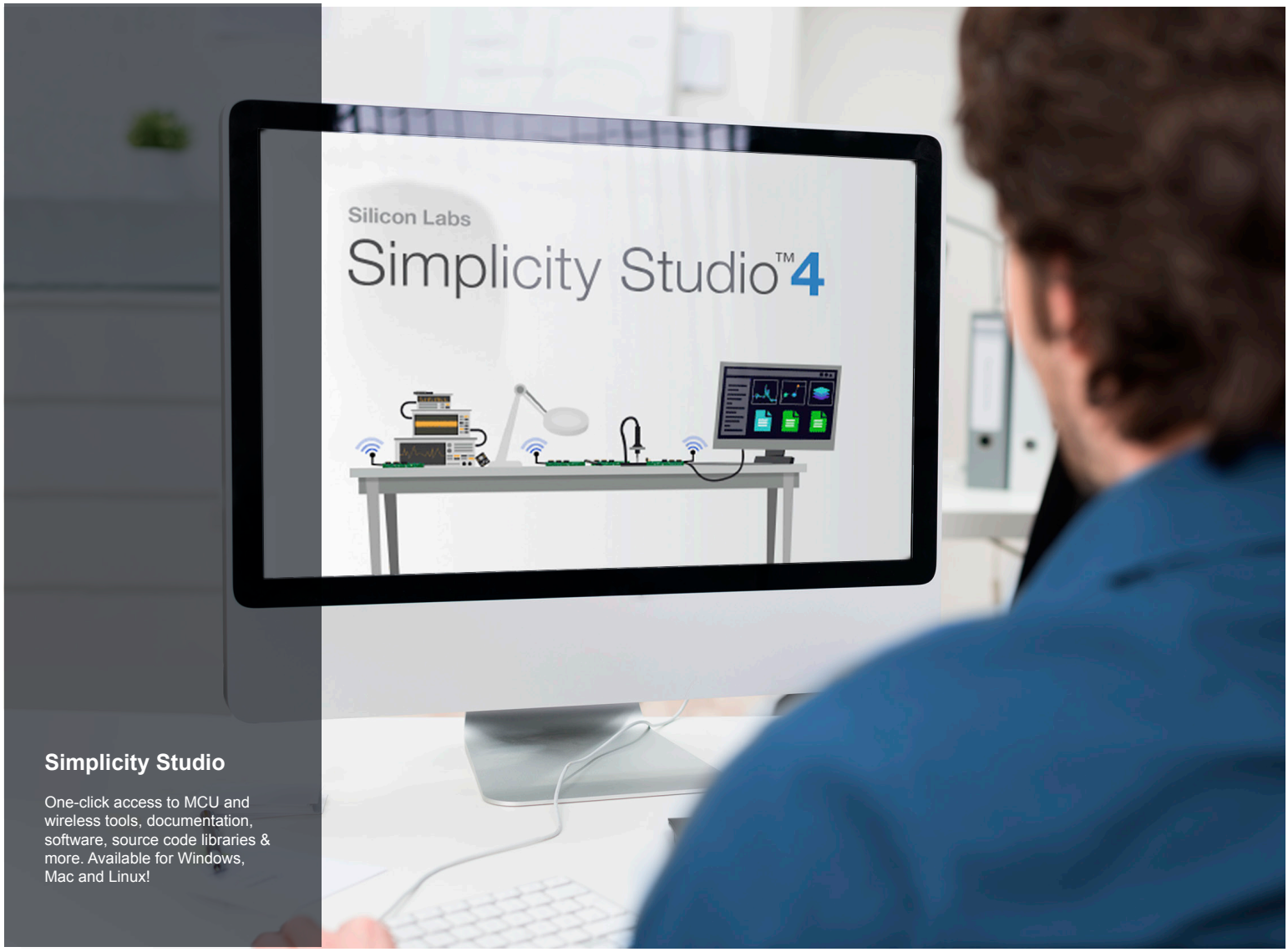

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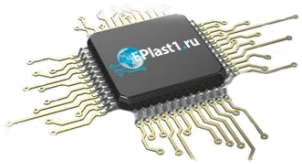

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.