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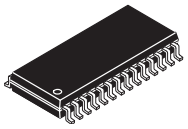
# System basis chip (SBC) with low speed fault tolerant CAN interface

**33889**

**SYSTEM BASIS CHIP**



**EG SUFFIX (PB-FREE)**
**PLASTIC PACKAGE**
**98ASB42345B**
**28-PIN SOICW**

The 33889 is an SBC having a fully protected, fixed 5.0 V low drop-out regulator, with current limit, overtemperature prewarning and reset. An SBC device is a monolithic IC combining many functions repeatedly found in standard microcontroller-based systems, e.g., protection, diagnostics, communication, power, etc.

An output drive with sense input is also provided to implement a second 5.0 V regulator using an external PNP. The 33889 has Normal, Standby, Stop and Sleep modes; an internally switched high-side power supply output with two wake-up inputs; programmable timeout or window watchdog, Interrupt, Reset, serial peripheral interface (SPI) input control, and a low-speed fault tolerant CAN transceiver, compatible with CAN 2.0 A and B protocols for module-to-module communications. The combination is an economical solution for power management, high-speed communication, and control in MCU-based systems. This device is powered by SMARTMOS technology.

### Features

- VDD1: 5.0 V low drop voltage regulator, current limitation, overtemperature detection, monitoring and reset function with total current capability 200 mA
- V2: tracking function of VDD1 regulator; control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply
- Four operational modes
- Low standby current consumption in Stop and Sleep modes
- Built-in low speed 125 kbps fault tolerant CAN physical interface.
- External high voltage wake-up input, associated with HS1 $V_{BAT}$ switch
- 150 mA output current capability for HS1 $V_{BAT}$ switch allowing drive of external switches pull-up resistors or relays

| ORDERING INFORMATION | | |
|---|---|---|
| **Device** (Add R2 Suffix for Tape and Reel) | **Temperature Range ($T_A$)** | **Package** |
| MC33889BPEG | -40 to 125 °C | 28 SOICW |
| *MC33889DPEG | | |

*Recommended for new designs

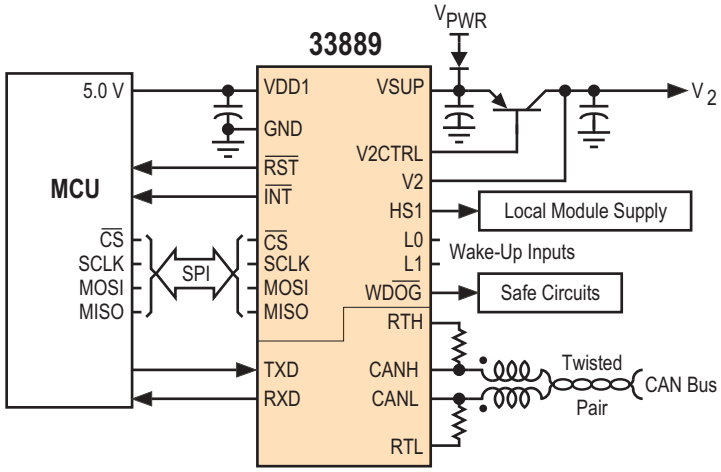



**Figure 1. 33889 simplified application diagram**

# 1 Device variations

**Table 1. Device variations between the 33889D and 33889B versions [(1)]**

| Parameters | Symbol | Trait | Device part number | |
|---|---|---|---|---|
| | | | MC33889B[(2)] | MC33889D[(2)] |
| Differential Receiver, Recessive To Dominant Threshold (By Definition, $V_{DIFF} = V_{CANH}-V_{CANL}$) | $V_{DIFF1}$ | Min. | 3.2 V | 3.5 V |
| | | Typ | 2.6 V | 3.0 V |
| | | Max. | 2.1 V | 2.5 V |
| Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5) | $V_{DIFF2}$ | Min. | 3.2 V | 3.5 V |
| | | Typ | 2.6 V | 3.0 V |
| | | Max. | 2.1 V | 2.5 V |
| CANH Output Current ($V_{CANH}$ = 0; TX = 0.0) | $I_{CANH}$ | Min. | 50 mA | 50 mA |
| | | Typ | 75 mA | 100 mA |
| | | Max. | 110 mA | 130 mA |
| CANL Output Current ($V_{CANL}$ = 14 V; TX = 0.0) | $I_{CANL}$ | Min. | 50 mA | 50 mA |
| | | Typ | 90 mA | 140 mA |
| | | Max. | 135 mA | 170 mA |
| Detection threshold for Short circuit to Battery voltage | Vcanh | Max. | Vsup/2 + 5V | Vsup/2 + 4.55V |
| loop time Tx to Rx, no bus failure, ISO configuration | tLOOPRD | Max. | N/A | 1.5us |
| loop time Tx to Rx, with bus failure, ISO configuration | tLOOPRD-F | Max. | N/A | 1.9us |
| loop time Tx to Rx, with bus failure and +-1.5V gnd shift, 5 node network, ISO configuration | tLOOPRD/DR-F+GS | | N/A | 3.6us |
| Minimum Dominant time for Wake up on CANL or CANH (Tem Vbat mode) | tWAKE | Min. | N/A | 8 |
| | | typ | 30 | 16 |
| | | Max. | N/A | 30 |
| T2SPI timing | T2spi | Min. | not specified, 25us spec applied | 25us |
| **Device behavior** | | | | |
| CANH or CANL open wire recovery principle | Reference MC33889B on page 32 | | after 4 non consecutive pulses | after 4 consecutive pulses |
| Rx behavior in TermVbat mode | Reference MC333889D on page 32 | | Rx recessive, no pulse | Rx recessive, dominant pulse to signal bus traffic |

Notes

1. This datasheet uses the term 33889 in the inclusive sense, referring to both the D version (33889D) and the B version (33689B).
2. The 33889D and 33889B versions are nearly identical. However, where variations in characteristic occur, these items will be separated onto individual lines.

# 2 Internal block diagram

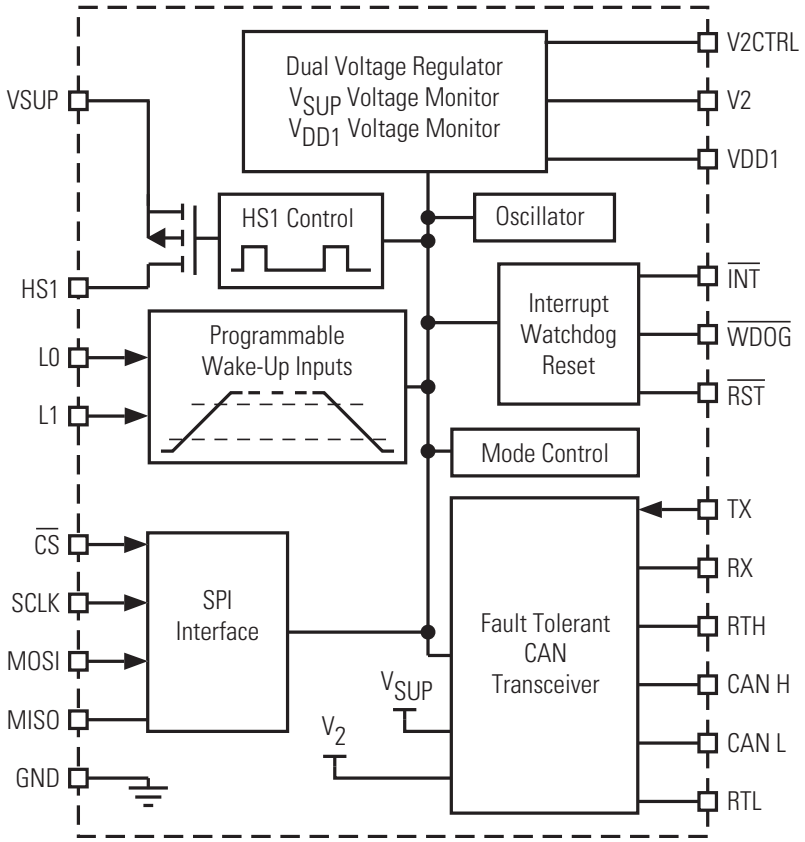



**Figure 2. 33889 internal block diagram**

# 3 Pin connections

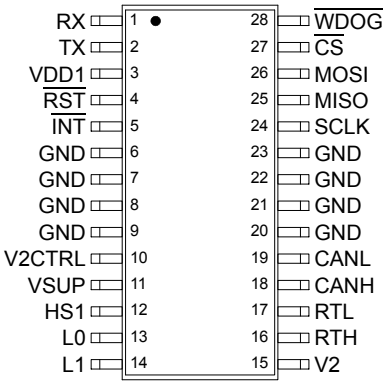



**Figure 3. 33889 pin connections**

A functional description of each pin can be found in the Functional pin description section page 20.

**Table 2. Pin definitions**

| Pin | Pin name | Pin function | Formal Name | Definition |
|---|---|---|---|---|
| 1 | RX | Output | Receiver Data | CAN bus receive data output pin |
| 2 | TX | Input | Transmitter Data | CAN bus receive data input pin |
| 3 | VDD1 | Power Output | Voltage Regulator One | 5.0 V pin is a 2% low drop voltage regulator for to the microcontroller supply. |
| 4 | $\overline{\text{RST}}$ | Output | Reset | This is the device reset output pin whose main function is to reset the MCU. |
| 5 | $\overline{\text{INT}}$ | Output | Interrupt | This output is asserted LOW when an enabled interrupt condition occurs. |
| 6 -9, 20 - 23 | GND | Ground | Ground | These device ground pins are internally connected to the package lead frame to provide a 33889-to-PCB thermal path. |
| 10 | V2CTRL | Output | Voltage Source 2 Control | Output drive source for the V2 regulator connected to the external series pass transistor. |
| 11 | VSUP | Power Input | Voltage Supply | Supply input pin. |
| 12 | HS1 | Output | High-Side Output | Output of the internal high-side switch. |
| 13 - 14 | L0, L1 | Input | Level 0 - 1 Inputs | Inputs from external switches or from logic circuitry. |
| 15 | V2 | Input | Voltage Regulator Two | 5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply. |
| 16 | RTH | Output | RTH | Pin for connection of the bus termination resistor to CANH. |
| 17 | RTL | Output | RTL | Pin for connection of the bus termination resistor to CANL. |
| 18 | CANH | Output | CAN High | CAN high output pin. |
| 19 | CANL | Output | CAN Low | CAN low output pin. |
| 24 | SCLK | Input | System Clock | Clock input pin for the Serial Peripheral Interface (SPI). |
| 25 | MISO | Output | Master In/Slave Out | SPI data sent to the MCU by the 33889. When $CS_{LOW}$ is HIGH, the pin is in the high impedance state. |
| 26 | MOSI | Input | Master Out/Slave In | SPI data received by the 33889. |
| 27 | $\overline{\text{CS}}$ | Input | Chip Select | The $CS_{LOW}$ input pin is used with the SPI bus to select the 33889. When the $CS_{LOW}$ is asserted LOW, the 33889 is the selected device of the SPI bus. |
| 28 | WDOG | Output | Watchdog | The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered. |

# 4 Electrical characteristics

## 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Max. | Unit | Notes |
|---|---|---|---|---|
| **Electrical ratings** | | | | |
| $V_{SUP}$ | Supply Voltage at VSUP<br>Continuous voltage<br>Transient voltage (Load dump) | <br>-0.3 to 27<br>40 | <br>V | |
| $V_{LOG}$ | Logic Signals (RX, TX, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WDOG}$, $\overline{INT}$) | -0.3 to $V_{DD1}$ +0.3 | V | |
| I | Output current VDD1 | Internally Limited | mA | |
| V<br>I | HS1<br>Voltage<br>Output Current | <br>-0.2 to $V_{SUP}$ +0.3<br>Internally Limited | <br>V<br>A | |
| $V_{WU}$<br>$I_{WU}$<br>$V_{TRWU}$ | L0, L1<br>DC Input voltage<br>DC Input current<br>Transient input voltage (according to ISO7637 specification) and with external component per Figure 4. | <br>-0.3 to 40<br>-2.0 to 2.0<br>+-100 | <br>V<br>mA<br>V | |
| $V_{2INT}$ | DC voltage at V2 (V2INT) | 0 to 5.25 | V | |
| $V_{BUS}$ | DC Voltage On Pins CANH, CANL | -20 to +27 | V | |
| $V_{CANH}/V_{CANL}$ | Transient Voltage At Pins CANH, CANL<br>0.0 < V2-INT < 5.5 V; VSUP = 0.0; T < 500 ms | -40 to +40 | V | |
| $V_{TR}$ | Transient Voltage On Pins CANH, CANL<br>(Coupled Through 1.0 nF Capacitor) | -150 to +100 | V | |
| $V_{RTL}$, $V_{RTH}$ | DC Voltage On Pins RTH, RTL | -0.3 to +27 | V | |
| $V_{RTH}/V_{RTL}$ | Transient Voltage At Pins RTH, RTL<br>0.0 < V2-INT < 5.5 V; VSUP = 0.0; T < 500 ms | -0.3 to +40 | V | |
| $V_{ESDH}$ | ESD voltage (HBM 100 pF, 1.5 k)<br>CANL, CANH, HS1, L0, L1<br>RTH, RTL<br>All other pins | <br>±4.0<br>±3.0<br>±2.0 | kV | (3) |
| $V_{ESD-MM}$ | ESD voltage (Machine Model) All pins, MC33889B | ±200 | V | (3) (4) |
| $V_{ESD-CDM}$ | ESD voltage (CDM) All pins, MC33889D<br>Pins 1,14,15, & 28<br>All other pins | <br>750<br>500 | V | (4) |
| $R_T$ | RTH, RTL Termination Resistance | 500 to 16000 | Ω | |

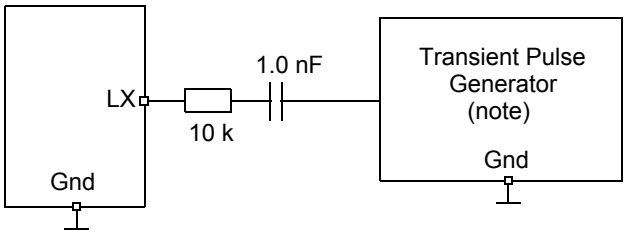
**Table 3. Maximum ratings (continued)**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Max. | Unit | Notes |
|---|---|---|---|---|
| **Thermal ratings** | | | | |
| $T_J$ | Junction Temperature | -40 to 150 | °C | |
| $T_S$ | Storage Temperature | -55 to 165 | °C | |
| $T_A$ | Ambient Temperature (for info only) | -40 to 125 | °C | |
| $R_{THJ/P}$ | Thermal resistance junction to gnd pin (5) | 20 | °C/W | |

Notes:

3. Testing done in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω).
4. ESD machine model (MM) is for MC33889B only. MM is now replaced by CDM (Charged Discharged model).
5. Gnd pins 6,7,8,9,20, 21, 22, 23.




Note: Waveform in accordance to ISO7637 part1, test pulses 1, 2, 3a and 3b.

**Figure 4. Transient test pulse for L0 and L1 inputs**

## 4.2 Static electrical characteristics

**Table 4. Static electrical characteristics**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Input pin (VSUP)** | | | | | | |
| $V_{SUP}$ | Nominal DC Voltage range | 5.5 | - | 18 | V | |
| $V_{SUP-EX1}$ | Extended DC Voltage range 1<br>Reduced functionality | 4.5 | - | 5.5 | V | (6) |
| $V_{SUP-EX2}$ | Extended DC Voltage range 2 | 18 | - | 27 | V | (8) |
| $V_{SUPLD}$ | Input Voltage during Load Dump<br>Load dump situation | - | - | 40 | V | |
| $V_{SUPJS}$ | Input Voltage during jump start<br>Jump start situation | - | - | 27 | V | |
| $I_{SUP}$ (SLEEP1) | Supply Current in Sleep Mode<br>$V_{DD1}$ & V2 off, $V_{SUP} \leq 12$ V, oscillator running | - | 95 | 130 | µA | (7) (10) |
| $I_{SUP}$ (SLEEP2) | Supply Current in Sleep Mode<br>$V_{DD1}$ & V2 off, $V_{SUP} \leq 12$ V, oscillator not running | - | 55 | 90 | µA | (7) |
| $I_{SUP}$ (SLEEP3) | Supply current in sleep mode<br>$V_{DD1}$ & V2 off, $V_{SUP}$ = 18 V, oscillator running | - | 170 | 270 | µA | (7) (10) |
| $I_{SUP(STDBY)}$ | Supply Current in Stand-by Mode<br>$I_{OUT}$ at $V_{DD1}$ = 40 mA, CAN recessive state or disabled | - | 42 | 45 | mA | (7),(9) |
| $I_{SUP(NORM)}$ | Supply Current in Normal Mode<br>$I_{OUT}$ at $V_{DD1}$ = 40 mA, CAN recessive state or disabled | - | 42.5 | 45 | mA | (7) |
| $I_{SUP}$ (STOP1) | Supply Current in Stop mode<br>$I_{OUT}$ $V_{DD1}$ < 2.0 mA, $V_{DD1}$ on , $V_{SUP} \leq 12$ V, oscillator running | - | 120 | 150 | µA | (7),(9)(10) (11) |
| $I_{SUP}$ (STOP2) | Supply Current in Stop mode<br>$I_{OUT}$ $V_{DD1}$ < 2.0 mA, $V_{DD1}$ on, $V_{SUP} \leq 12$ V, oscillator not running | - | 80 | 110 | µA | (7),(9)(10) (11) |
| $I_{SUP}$ (STOP3) | Supply Current in Stop mode<br>Iout $V_{DD1}$ < 2.0 mA, $V_{DD1}$ on, $V_{SUP}$ = 18 V, oscillator running | - | 200 | 285 | µA | (7),(9)(10) (11) |
| $V_{THRESH}$ | Supply Fail Flag internal threshold | 1.5 | 3.0 | 4.0 | V | |
| $V_{DETHYST}$ | Supply Fail Flag hysteresis | - | 1.0 | - | V | (12) |
| $BF_{EW}$ | Battery fall early warning threshold<br>In normal & standby mode | 5.8 | 6.1 | 6.4 | V | |
| $BF_{EWH}$ | Battery fall early warning hysteresis<br>In normal & standby mode | 0.1 | 0.2 | 0.3 | V | (12) |

Notes

6. $V_{DD1}$ > 4.0 V, reset high, if $R_{STTH-2}$ selected and $I_{OUT}$ $V_{DD1}$ reduced, logic pin high level reduced, device is functional.
7. Current measured at $V_{SUP}$ pin.
8. Device is fully functional. All modes available and operating, Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0 and L1 inputs operating, SPI read write operation. Over temperature may occur.
9. Measured in worst case condition with 5.0 V at V2 pin (V2 pin tied to VDD1).
10. Oscillator running means “Forced Wake-up” or “Cyclic Sense” or “Software Watchdog” timer activated. Software Watchdog is available in stop mode only.
11. $V_{DD1}$ is ON with 2.0 mA typical output current capability.
12. Guaranteed by design

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Output pin (VDD1)** (14) | | | | | | |
| $V_{DD1OUT}$ | VDD1 Output Voltage<br>$I_{DD1}$ from 2.0 to 200 mA<br>5.5 V < $V_{SUP}$ < 27 V<br>4.5 V < $V_{SUP}$ < 5.5 V | <br><br>4.9<br>4.0 | <br><br>5.0<br>- | <br><br>5.1<br>- | V | |
| $V_{DD1DROP}$ | Drop Voltage $V_{SUP}$ > $V_{DDOUT}$<br>$I_{DD1}$ = 200 mA | - | 0.2 | 0.5 | V | |
| $V_{DD1DP2}$ | Drop Voltage $V_{SUP}$ > $V_{DDOUT}$, limited output current<br>$I_{DD1}$ = 50 mA<br>4.5 V < $V_{SUP}$ < 27 V | - | 0.1 | 0.25 | V | |
| $I_{DD1}$ | $I_{DD1}$ Output Current<br>Internally limited | 200 | 270 | 350 | mA | |
| $V_{DDSTOP}$ | VDD1 Output Voltage in stop mode<br>$I_{OUT}$ < 2.0 mA | 4.75 | 5.00 | 5.25 | V | |
| $I_{DD1S-WU1}$ | $I_{DD1}$ stop output current to wake-up SBC<br>Default value after reset. | 2.0 | 3.5 | 6.0 | mA | (15) |
| $I_{DD1S-WU2}$ | $I_{DD1}$ stop output current to wake-up SBC | 10 | 14 | 18 | mA | (15) |
| $I_{DD1-DGIT11}$ | $I_{DD1}$ overcurrent wake deglitcher<br>(with $I_{DD1S-WU1}$ selected) | 40 | 55 | 75 | µs | (13) |
| $I_{DD1-DGIT2}$ | $I_{DD1}$ overcurrent wake deglitcher<br>(with $I_{DD1S-WU2}$ selected) | - | 150 | - | µs | (13) |
| $T_{SD}$ | Thermal Shutdown<br>Normal or standby mode | 160 | - | 190 | °C | |
| $T_{PW}$ | Overtemperature prewarning<br>VDDTEMP bit set | 130 | - | 160 | °C | |
| $T_{SD}$-$T_{PW}$ | Temperature Threshold difference | 20 | - | 40 | °C | |
| $V_{RST-TH1}$ | Reset threshold 1<br>Default value after reset. (15) | 4.5 | 4.6 | 4.7 | V | |
| $V_{RST-TH2}$ | Reset threshold 2 (15) | 4.1 | 4.2 | 4.3 | V | |
| RESET-DUR | Reset duration | 0.85 | 1.0 | 2.0 | ms | |
| $V_{DD}$ | VDD1 range for Reset Active | 1.0 | - | - | V | |
| $t_D$ | Reset Delay Time<br>Measured at 50% of reset signal. (13) | 5.0 | - | 20 | µs | |
| LR1 | Line Regulation<br>9.0 V < $V_{SUP}$ < 18 V, $I_{DD}$ = 10 mA | - | 5.0 | 25 | mV | |
| LR2 | Line Regulation<br>5.5 V < $V_{SUP}$ < 27 V, $I_{DD}$ = 10 mA | - | 10 | 25 | mV | |
| LD | Load Regulation<br>1.0 mA < $I_{IDD}$ < 200 mA | - | 25 | 75 | mV | |
| THERMS | Thermal stability<br>$V_{SUP}$ = 13.5 V, I = 100 mA | - | 5.0 | - | mV | |

Notes

13. Guaranteed by design
14. $I_{DD1}$ is the total regulator output current. VDD specification with external capacitor C ≥ 22 µF and ESR < 10 Ω.
15. Selectable by SPI

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V2 regulator (V2)** (16) | | | | | | |
| V2 | V2 Output Voltage<br>I2 from 2.0 to 200 mA, 5.5 V < $V_{SUP}$ < 27 V (17) | 0.99 | 1.0 | 1.01 | $V_{DD1}$ | |
| I2 | I2 output current (for information only)<br>Depending on the external ballast transistor | 200 | - | - | mA | |
| $I2_{CTRL}$ | V2 CTRL sink current capability | 10 | - | - | mA | |
| $V2L_{TH}$ | V2LOW flag threshold | 3.75 | 4.0 | 4.25 | V | |
| $I_{V2RS}$ | Internal V2 Supply Current (CAN and SBC in Normal Mode). TX = 5.0 V, CAN in Recessive State | 3.8 | 5.6 | 6.8 | mA | |
| $I_{V2DS}$ | Internal V2 Supply Current (CAN and SBC in Normal Mode). TX = 0.0 V, No Load, CAN in Dominant State | 4.0 | 5.8 | 7.0 | mA | |
| $I_{V2R}$ | Internal V2 Supply Current (CAN in Receive Only Mode, SBC in Normal mode). $V_{SUP}$ = 12 V | - | 80 | 120 | µA | |
| $I_{V2BT}$ | Internal V2 Supply Current (CAN in Bus TermVbat mode, SBC in normal mode), $V_{SUP}$ = 12 V | - | 35 | 60 | µA | |
| **Logic output pins (MISO)** | | | | | | |
| $V_{OL}$ | Low Level Output Voltage<br>$I_{OUT}$ = 1.5 mA | - | - | 1.0 | V | |
| $V_{OH}$ | High Level Output Voltage<br>$I_{OUT}$ = -250 µA | $V_{DD1-0.9}$ | - | - | V | |
| $I_{HZ}$ | Tri-state MISO Leakage Current<br>0.0 V < $V_{MISO}$ < $V_{DD}$ | -2.0 | - | +2.0 | µA | |
| **Logic input pins (MOSI, SCLK, CS)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | $0.7V_{DD1}$ | - | $V_{DD1}$+0.3V | | |
| $V_{IL}$ | Low Level Input Voltage | -0.3 | - | 0.3 $V_{DD1}$ | V | |
| $I_{IH}$<br>$I_{IL}$ | Input Current on $\overline{CS}$<br>$V_I$ = 4.0 V<br>$V_I$ = 1.0 V | -100 | - | -20 | µA | |
| $I_{IL}$ | Low Level Input Current $\overline{CS}$<br>$V_I$ = 1.0 V | -100 | - | -20 | µA | |
| $I_{IN}$ | MOSI, SCLK Input Current<br>0.0 < $V_{IN}$ < $V_{DD}$ | -10 | - | 10 | µA | |
| **Reset pin (RST)** | | | | | | |
| $I_{OH}$ | High Level Output current<br>0.0 < $V_{OUT}$ < 0.7 $V_{DD}$ | -350 | -250 | -150 | µA | |
| $V_{OL}$ | Low Level Output Voltage ($I_0$ = 1.5 mA)<br>5.5 V < $V_{SUP}$ < 27 V<br>1.0 V < $V_{DD1}$ | <br>0.0<br>0.0 | <br>-<br>- | <br>0.9<br>0.9 | V | |
| $I_{PDW}$ | Reset pull-down current | 2.3 | - | 5.0 | mA | |

Notes

16. V2 tracking voltage regulator - V2 specification with external capacitor
- option 1: C ≥ 22 µF and ESR < 10 Ω. Using a resistor of 2 kΩ or less between the base and emitter of the external PNP is recommended.
- option2: 1.0 µF < C < 22 µF and ESR < 10 Ω. In this case depending on the ballast transistor gain an additional resistor and capacitor network between emitter and base of PNP ballast transistor might be required. Refer to NXP application information or contact your local technical support.
- option 3: 10 uF < C < 22 µF ESR > 0.2 Ω: a resistor of 2 kΩ or less is required between the base and emitter of the external PNP.

17. For $I_{VDD1}$ > 10 mA

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Watchdog pin (Wdog)** | | | | | | |
| $V_{OL}$ | Low Level Output Voltage ($I_0$ = 1.5 mA)<br>5.5 V < $V_{SUP}$ < 27 V | 0.0 | - | 0.9 | V | |
| $V_{OH}$ | High Level Output Voltage ($I_0$ = -250 µA) | $V_{DD1}$ -0.9 | - | $V_{DD1}$ | V | |
| **Interrupt Pin (INT)** | | | | | | |
| $V_{OL}$ | Low Level Output Voltage ($I_0$ = 1.5 mA) | 0.0 | - | 0.9 | V | |
| $V_{OH}$ | High Level Output Voltage ($I_0$ = -250 µA) | $V_{DD1}$ -0.9 | - | $V_{DD1}$ | V | |
| **High-side output pin (HS1)** | | | | | | |
| $R_{DSON25}$ | $R_{DSON}$ at Tj = 25 °C, and $I_{OUT}$ -150 mA<br>$V_{SUP}$ > 9.0 V | - | - | 2.5 | W | |
| $R_{DSON125}$ | $R_{DSON}$ at $T_J$ = 125 °C, and $I_{OUT}$ -150 mA<br>$V_{SUP}$ > 9.0 V | - | - | 5.0 | W | |
| $R_{DON125-2}$ | $R_{DSON}$ at $T_J$ = 125 °C, and $I_{OUT}$ -120 mA<br>5.5 V < $V_{SUP}$ < 9.0 V | - | 4.0 | 5.5 | W | |
| $I_{LIM}$ | Output current limitation | 160 | - | 500 | mA | |
| $O_{VT}$ | Overtemperature Shutdown | 155 | - | 190 | °C | |
| $I_{LEAK}$ | Leakage current | - | - | 10 | µA | |
| $V_{CL}$ | Output Clamp Voltage at $I_{OUT}$ = -1.0 mA<br>no inductive load drive capability | -1.5 | - | -0.3 | V | (18) |
| **Input pins (L0 and L1)** | | | | | | |
| $V_{TH0N}$ | L0 Negative Switching Threshold<br>5.5 V < $V_{SUP}$ < 6.0 V<br>6.0 V < $V_{SUP}$ < 18 V<br>18 V < $V_{SUP}$ < 27 V | <br>1.7<br>2.0<br>2.0 | <br>2.0<br>2.4<br>2.5 | <br>3.0<br>3.0<br>3.1 | V | |
| $V_{TH0P}$ | L0 Positive Switching Threshold<br>5.5 V < $V_{SUP}$ < 6.0 V<br>6.0 V < $V_{SUP}$ < 18 V<br>18 V < $V_{SUP}$ < 27 V | <br>2.2<br>2.5<br>2.5 | <br>2.75<br>3.4<br>3.5 | <br>4.0<br>4.0<br>4.1 | V | |
| $V_{TH1N}$ | L1 Negative Switching Threshold<br>5.5 V < $V_{SUP}$ < 6.0 V<br>6.0 V < $V_{SUP}$ < 18 V<br>18 V < $V_{SUP}$ < 27 V | <br>2.0<br>2.5<br>2.7 | <br>2.5<br>3.0<br>3.2 | <br>3.0<br>3.7<br>3.8 | V | |
| $V_{TH1P}$ | L1 Positive Switching Threshold<br>5.5 V < $V_{SUP}$ < 6.0 V<br>6.0 V < $V_{SUP}$ < 18V<br>18 V < $V_{SUP}$ < 27 V | <br>2.7<br>3.0<br>3.5 | <br>3.3<br>4.0<br>4.2 | <br>3.8<br>4.7<br>4.8 | V | |
| $V_{HYST}$ | Hysteresis<br>5.5 V < $V_{SUP}$ < 27 V | 0.6 | 1.0 | 1.3 | V | |
| $I_{IN}$ | Input current<br>-0.2 V < $V_{IN}$ < 40 V | -10 | - | 10 | µA | |

Notes
18. Refer to HS1 negative maximum rating voltage limitation of -0.2 V.

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **CAN module specification (TX, RX, CANH, CANL, RTH, and RTL)** | | | | | | |
| $V_{LOGIC}$ | DC Voltage On Pins TX, RX | -0.3 | | $V_{DD1}$ + 0.3 | V | |
| $V2_{INT}$ | DC voltage at V2 (V2INT) | 0.0 | | 5.25 | V | |
| $V_{BUS}$ | DC Voltage On Pins CANH, CANL | -20 | | +27 | V | |
| $V_{CANH}/V_{CANL}$ | Transient Voltage At Pins CANH, CANL<br>$0.0 < V_{2\text{-}INT} < 5.5$ V; $V_{SUP} \geq 0.0$; T < 500 ms | -40 | - | 40 | V | |
| $V_{TR}$ | Transient Voltage On Pins CANH, CANL (Coupled Through 1.0 nF Capacitor) | -150 | - | 100 | V | |
| $V_{CANH}$ | Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode) MC33889B | $V_{SUP}$/2+3 | - | $V_{SUP}$/2+5 | V | |
| $V_{CANH}$ | Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode) MC33889D | $V_{SUP}$/2+3 | - | $V_{SUP}$/ 2+4.55 | V | |
| $V_{RTL}$, $V_{RTH}$ | DC Voltage On Pins RTH, RTL | -0.3 | - | +27 | V | |
| $V_{RTH}/V_{RTL}$ | Transient Voltage At Pins RTH, RTL<br>$0.0 < V_{2\text{-}INT} < 5.5$ V; $V_{SUP} \geq 0.0$; T < 500 ms | -0.3 | - | 40 | V | |
| **Transmitter Data Pin (TX)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | 0.7*$V_2$ | - | $V_2$+0.3V | V | |
| $V_{IL}$ | Low Level Input Voltage | -0.3 | - | 0.3 * $V_2$ | V | |
| $I_{TXH}$ | TX High Level Input Current ($V_I$ = 4.0 V) | -100 | -50 | -25 | µA | |
| $I_{TXL}$ | TX Low Level Input Current ($V_I$ = 1.0 V) | -100 | -50 | -25 | µA | |
| **Receive data pin (rX)** | | | | | | |
| $V_{OH}$ | High Level Output Voltage RX ($I_0$ = -250 µA) | $V_{2\text{-}INT}$ - 0.9 | - | $V_{2\text{-}INT}$ | V | |
| $V_{OL}$ | Low Level Output Voltage ($I_0$ = 1.5 mA) | 0.0 | - | 0.9 | V | |
| **CAN high and can low pins (CANH, CANL)** | | | | | | |
| $V_{DIFF1}$ | Differential Receiver, Recessive To Dominant Threshold<br>(By Definition, $V_{DIFF} = V_{CANH}$-$V_{CANL}$)<br>For 33889D<br>For 33889B | <br><br>-3.5<br>-3.2 | <br><br>-3.0<br>-2.6 | <br><br>-2.5<br>-2.1 | V | |
| $V_{DIFF2}$ | Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5)<br>For 33889D<br>For 33889B | <br><br>-3.5<br>-3.2 | <br><br>-3.0<br>-2.6 | <br><br>-2.5<br>-2.1 | V | |
| $V_{CANH}$ | CANH Recessive Output Voltage<br>TX = 5.0 V; $R_{(RTH)}$ < 4.0 k | - | - | 0.2 | V | |
| $V_{CANL}$ | CANL Recessive Output Voltage<br>TX = 5.0 V; $R_{(RTL)}$ < 4.0 k | $V_{2\text{-}INT}$ - 0.2 | - | - | V | |

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions - $V_{SUP}$ From 5.5 V to 18 V and $T_J$ from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions unless otherwise noted.

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CANH}$ | CANH Output Voltage, Dominant<br>TX = 0.0 V; $I_{CANH}$ = -40 mA; Normal Operating Mode | $V_2$ - 1.4 | - | - | V | (19) |
| $V_{CANL}$ | CANL Output Voltage, Dominant<br>TX = 0.0 V; $I_{CANL}$ = 40 mA; Normal Operating Mode | - | - | 1.4 | V | (19) |
| $I_{CANH}$ | CANH Output Current ($V_{CANH}$ = 0; TX = 0.0)<br>For 33889D<br>For 33889B | <br>50<br>50 | <br>100<br>75 | <br>130<br>110 | mA | |
| $I_{CANL}$ | CANL Output Current ($V_{CANL}$ = 14 V; TX = 0.0)<br>For 33889D<br>For 33889B | <br>50<br>50 | <br>140<br>90 | <br>170<br>135 | mA | |
| $V_{CANH}$, $V_{CANL}$ | Detection Threshold For Short-circuit To Battery Voltage (Normal Mode) | 7.3 | 7.9 | 8.9 | V | |
| VcanH | Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode), MC33889B | Vsup/2+3 | - | Vsup/2+5 | V | |
| VcanH | Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode), MC33889D | Vsup/2+3 | - | Vsup/ 2+4.55 | V | |
| $I_{CANH}$ | CANH Output Current (Term $V_{BAT}$ Mode; $V_{CANH}$ = 12 V, Failure3) | - | 5.0 | 10 | µA | |
| $I_{CANL}$ | CANL Output Current (Term $V_{BAT}$ Mode; $V_{CANL}$ = 0.0 V; $V_{BAT}$ = 12 V, Failure 4) | - | 0.0 | 2.0 | µA | |
| $V_{WAKE,L}$ | CANL Wake-up Voltage Threshold | 2.5 | 3.0 | 3.9 | V | |
| $V_{WAKE,H}$ | CANH Wake-up Voltage Threshold | 1.2 | 2.0 | 2.7 | V | |
| $V_{WAKEL}$-$V_{WAKEH}$ | Wake-up Threshold Difference (Hysteresis) | 0.2 | - | - | V | |
| $V_{SE, CANH}$ | CANH Single Ended Receiver Threshold (Failures 4, 6, 7) | 1.5 | 1.85 | 2.15 | V | |
| $V_{SE, CANL}$ | CANL Single Ended Receiver Threshold (Failures 3, 8) | 2.8 | 3.05 | 3.4 | V | |
| $I_{CANL,PU}$ | CANL Pull-up Current (Normal Mode) | 45 | 75 | 90 | µA | |
| $I_{CANH,PD}$ | CANH Pull-down Current (Normal Mode) | 45 | 75 | 90 | µA | |
| $R_{DIFF}$ | Receiver Differential Input Impedance CANH / CANL | 100 | - | 300 | kΩ | |
| $V_{COM}$ | Differential Receiver Common Mode Voltage Range | -10 | - | 10 | V | (20) |
| $C_{CANH}$ | CANH To Ground Capacitance | - | - | 50 | pF | |
| $C_{CANL}$ | CANL To Ground Capacitance | - | - | 50 | pF | |
| $DC_{CAN}$ | $C_{CANL}$ to $C_{CANH}$ Capacitor Difference | - | - | 10 | pF | |
| $t_{CSD}$ | CAN Driver Thermal Shutdown | 150 | 160 | - | °C | |
| **Bus termination pins (RTH, RTL)** | | | | | | |
| $R_{RTL}$ | RTL to V2 Switch On Resistance<br>($I_{OUT}$ < -10 mA; Normal Operating Mode) | 10 | 30 | 90 | W | |
| $R_{RTL}$ | RTL to BAT Switch Series Resistance (term $V_{BAT}$ Mode) | 8.0 | 12.5 | 20 | kΩ | |
| $R_{RTH}$ | RTH To Ground Switch On Resistance ($I_{OUT}$ < 10 mA; Normal Operating Mode) | 10 | 30 | 90 | W | |

Notes

19. For MC33889B, after 128 pulses on TX and no bus failure.
20. Guaranteed by design

## 4.3 Dynamic electrical characteristics

**Table 5. Dynamic electrical characteristics**

$V_{SUP}$ From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and $T_J$ from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Symbol | Conditions | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Digital interface timing (SCLK, CS, MOSI, MISO)** | | | | | | |
| FREQ | SPI operation frequency | - | - | 4.0 | MHz | |
| $t_{PCLK}$ | SCLK Clock Period | 250 | - | - | ns | |
| $t_{WSCLKH}$ | SCLK Clock High Time | 125 | - | - | ns | |
| $t_{WSCLKL}$ | SCLK Clock Low Time | 125 | - | - | ns | |
| $t_{ILEAD}$ | Falling Edge of $\overline{CS}$ to Rising Edge of SCLK | 100 | 50 | - | ns | |
| $t_{LAG}$ | Falling Edge of SCLK to Rising Edge of $\overline{CS}$ | 100 | 50 | - | ns | |
| $t_{SISU}$ | MOSI to Falling Edge of SCLK | 40 | 25 | - | ns | |
| $t_{SIH}$ | Falling Edge of SCLK to MOSI | 40 | 25 | - | ns | |
| $t_{RSO}$ | MISO Rise Time (CL = 220 pF) | - | 25 | 50 | ns | |
| $t_{fSO}$ | MISO Fall Time (CL = 220 pF) | - | 25 | 50 | ns | |
| $t_{SOEN}$<br>$t_{SODIS}$ | Time from Falling or Rising Edges of $\overline{CS}$ to:<br>- MISO Low-impedance<br>- MISO High-impedance | <br>-<br>- | <br>-<br>- | <br>50<br>50 | ns | |
| $t_{VALID}$ | Time from Rising Edge of SCLK to MISO Data Valid<br>0.2 V1 ≤ SO ≥ 0.8 V1, $C_L$ = 200 pF | - | - | 50 | ns | |
| $T_{\overline{CS}\text{-STOP}}$ | Delay between $\overline{CS}$ low to high transition (at end of SPI stop command) and Stop or sleep mode activation detected by V2 off | 18 | - | 34 | µs | (21) |
| $T_{INT}$ | Interrupt low level duration<br>SBC in stop mode | 7.0 | 10 | 13 | µs | |
| $O_{SC\text{-}F1}$ | Internal oscillator frequency<br>All modes except Sleep and Stop | - | 100 | - | kHz | (21) |
| $O_{SC\text{-}F2}$ | Internal low power oscillator frequency<br>Sleep and Stop modes | - | 100 | - | kHz | (21) |
| $W_{D1}$ | Watchdog period 1<br>Normal and standby modes | 8.58 | 9.75 | 10.92 | ms | |
| $W_{D2}$ | Watchdog period 2<br>Normal and standby modes | 39.6 | 45 | 50.4 | ms | |
| $W_{D3}$ | Watchdog period 3<br>Normal and standby modes | 88 | 100 | 112 | ms | |
| $W_{D4}$ | Watchdog period 4<br>Normal and standby modes | 308 | 350 | 392 | ms | |
| $F1_{ACC}$ | Watchdog period accuracy<br>Normal and standby modes | -12 | - | 12 | % | |
| $NR_{TOUT}$ | Normal request mode timeout<br>Normal request mode | 308 | 350 | 392 | ms | |
| $WD1_{STOP}$ | Watchdog period 1 - stop<br>Stop mode | 6.82 | 9.75 | 12.7 | ms | |
| $WD2_{STOP}$ | Watchdog period 2- stop<br>Stop mode | 31.5 | 45 | 58.5 | ms | |

Notes

21. Guaranteed by design

**Table 5. Dynamic electrical characteristics (continued)**

$V_{SUP}$ From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and $T_J$ from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Symbol | Conditions | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $WD3_{STOP}$ | Watchdog period 3 - stop<br>Stop mode | 70 | 100 | 130 | ms | |
| $WD4_{STOP}$ | Watchdog period 4 - stop<br>Stop mode | 245 | 350 | 455 | ms | |
| $F2_{ACC}$ | Stop mode watchdog period accuracy<br>Stop mode | -30 | - | 30 | % | |
| CSFWU1 | Cyclic sense/FWU timing 1<br>Sleep and Stop modes | 3.22 | 4.6 | 5.98 | ms | |
| CSFWU2 | Cyclic sense/FWU timing 2<br>Sleep and Stop modes | 6.47 | 9.25 | 12 | ms | |
| CSFWU3 | Cyclic sense/FWU timing 3<br>Sleep and Stop modes | 12.9 | 18.5 | 24 | ms | |
| CSFWU4 | Cyclic sense/FWU timing 4<br>Sleep and Stop modes | 25.9 | 37 | 48.1 | ms | |
| CSFWU5 | Cyclic sense/FWU timing 5<br>Sleep and Stop modes | 51.8 | 74 | 96.2 | ms | |
| CSFWU6 | Cyclic sense/FWU timing 6<br>Sleep and Stop modes | 66.8 | 95.5 | 124 | ms | |
| CSFWU7 | Cyclic sense/FWU timing 7<br>Sleep and Stop modes | 134 | 191 | 248 | ms | |
| CSFWU8 | Cyclic sense/FWU timing 8<br>Sleep and Stop modes | 271 | 388 | 504 | ms | |
| $t_{ON}$ | Cyclic sense On time<br>Sleep and Stop modes | 200 | 300 | 400 | µs | |
| $t_{ACC}$ | Cyclic sense/FWU timing accuracy<br>Sleep and Stop mode | -30 | - | +30 | % | |
| $t_{S-HSON}$ | Delay between SPI command and HS1 turn on<br>Normal or Standby mode, $V_{SUP}$ > 9.0 V | - | - | 22 | µs | (22) |
| $t_{S-HSOFF}$ | Delay between SPI command and HS1 turn off<br>Normal or Standby mode, $V_{SUP}$ > 9.0 V | - | - | 22 | µs | (22) |
| $t_{S-V2ON}$ | Delay between SPI and V2 turn on<br>Standby mode | 9.0 | - | 25 | µs | (22) |
| $t_{S-V2OFF}$ | Delay between SPI and V2 turn off<br>Normal modes | 9.0 | - | 25 | µs | (22) |
| $t_{S-NR2N}$ | Delay between Normal Request and Normal mode, after W/D trigger command<br>Normal request mode | 15 | 35 | 70 | µs | |

Notes

22. State Machine Timing - Delay starts at rising edge of $\overline{CS}$ (end of SPI command) and start of Turn on or Turn off of HS1 or V2.

**Table 5. Dynamic electrical characteristics (continued)**

$V_{SUP}$ From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and $T_J$ from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Symbol | Conditions | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{S-CANN}$ | Delay between SPI and “CAN normal mode”<br>SBC Normal mode | - | - | 10 | µs | (23) |
| $t_{S-CANS}$ | Delay between SPI and “CAN sleep mode”<br>SBC Normal mode | - | - | 10 | µs | (23) |
| $t_{W-\overline{CS}}$ | Delay between $\overline{CS}$ wake-up ($\overline{CS}$ low to high) and SBC normal request mode ($V_{DD1}$ on & reset high)<br>SBC in Stop mode | 15 | 40 | 90 | µs | |
| $t_{W-SPI}$ | Delay between $\overline{CS}$ wake-up ($\overline{CS}$ low to high) and first accepted SPI command<br>SBC in Stop mode | 90 | - | - | µs | |
| $t_{S-1STSPI}$ | Delay between INT pulse and 1st SPI command accepted<br>In Stop mode after wake-up | 20 | - | - | µs | |
| $t2_{SPI}$ | Delay between two SPI messages addressing the same register<br>For 33889D only | 25 | - | - | µs | |
| **Input pins (L0 and L1)** | | | | | | |
| $t_{WUF}$ | Wake-up Filter Time (enable/disable option on L0 input)<br>(If filter enabled) | 8.0 | 20 | 38 | µs | |
| **Pin AC characteristics (canh, canl, rx, tx)** | | | | | | |
| $t_{SLDR}$ | CANL and CANH Slew Rates (25% to 75% CAN signal).<br>Recessive to Dominant state<br>Dominant to Recessive state | <br>2.0<br>2.0 | <br>-<br>- | <br>8.0<br>9.0 | V/µs | (24) |
| $t_{ONRX}$ | Propagation Delay<br>TX to RX Low. -40 < T ≤ 25°C.<br>TX to RX Low. 25 < T < 125°C. | <br>-<br>- | <br>1.2<br>1.1 | <br>1.6<br>1.8 | µs | (25) |
| $t_{OFFRX}$ | Propagation Delay TX to RX High. | - | 1.8 | 2.2 | µs | (25) |

Notes

23. Guaranteed by design
24. Dominant to recessive slew rate is dependant upon the bus load characteristics.
25. AC Characteristics measured according to schematic Figure 5

**Table 5. Dynamic electrical characteristics (continued)**

$V_{SUP}$ From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and $T_J$ from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Symbol | Conditions | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{LOOPRD}$ | Loop time Tx to Rx, no bus failure, MC33889D only (Figure 6) (ISO ICT test series 10)<br>Tx high to low transition (dominant edge)<br>Tx low to high transition (recessive edge) | <br>-<br>- | <br>1.15<br>1.45 | <br>1.5<br>1.5 | µs | (26) |
| $t_{LOOPRD-F}$ | Loop time Tx to Rx, with bus failure, MC33889D only (Figure 7) (ISO ICT test series 10)<br>Tx high to low transition (dominant edge)<br>Tx low to high transition (recessive edge) | <br>-<br>- | <br>-<br>- | <br>1.9<br>1.9 | µs | (26) |
| $t_{LOOPRD/DR-F+GS}$ | Loop time Tx to Rx, with bus failure and ±1.5 V gnd shift, 5 nodes network, MC33889D,(Figure 8, ISO ICT tests series 11) | | | 3.6 | µs | (27) |
| $t_{WAKE}$ | Min. Dominant Time For Wake-up On CANL or CANH (Term $V_{BAT}$; $V_{SUP}$ = 12 V) Guaranteed by design.<br>MC33889B<br>MC33889D | <br>-<br>8.0 | <br>30<br>16 | <br>-<br>30 | µs | |
| $t_{DF3}$ | Failure 3 Detection Time (Normal Mode) | 10 | 30 | 80 | µs | |
| $t_{DR3}$ | Failure 3 Recovery Time (Normal Mode) | - | 160 | - | µs | |
| $t_{DF6}$ | Failure 6 Detection Time (Normal Mode) | 50 | 200 | 500 | µs | |
| $t_{DR6}$ | Failure 6 Recovery Time (Normal Mode) | 150 | 200 | 1000 | µs | |
| $t_{DF47}$ | Failure 4, 7 Detection Time (Normal Mode) | 0.75 | 1.5 | 4.0 | ms | |
| $t_{DR47}$ | Failure 4, 7 Recovery Time (Normal Mode) | 10 | 30 | 60 | µs | |
| $t_{DF8}$ | Failure 3a, 8 Detection Time (Normal Mode) | 0.75 | 1.7 | 4.0 | ms | |
| $tT_{DR8}$ | Failure 3a, 8 Recovery Time (Normal Mode) | 0.75 | 1.5 | 4.0 | ms | |
| $t_{DR47}$ | Failure 4, 7 Detection Time, (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | 0.8 | 1.2 | 8.0 | ms | |
| $t_{DR47}$ | Failure 4, 7 Recovery Time (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | - | 1.92 | - | ms | |
| $t_{DR3}$ | Failure 3 Detection Time (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | - | 3.84 | - | ms | |
| $t_{DR3}$ | Failure 3 Recovery Time (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | - | 1.92 | - | ms | |
| $t_{DR8}$ | Failure 3a, 8Detection Time (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | - | 2.3 | - | ms | |
| $t_{DR8}$ | Failure 3a, 8 Recovery Time (Term $V_{BAT}$; $V_{SUP}$ = 12 V) | - | 1.2 | - | ms | |
| $E_{CDF}$ | Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection (Failure bit set, Normal Mode) | - | 3 | - | | |
| $E_{CDR}$ | Edge Count Difference Between CANH And CANL For Failures 1, 2, 5 Recovery (Normal Mode) | - | 3 | - | | |
| $t_{TX,D}$ | TX Permanent Dominant Timer Disable Time (Normal Mode And Failure Mode) | 0.75 | - | 4.0 | ms | |
| $t_{TX,E}$ | TX Permanent Dominant Timer Enable Time (Normal Mode And Failure Mode) | 10 | - | 60 | µs | |

Notes

26. AC characteristic according to ISO11898-3, tested per figure 5 and 6. Guaranteed by design, room temperature only.
27. AC characteristic according to ISO11898-3, tested per figure 7. Max. reported is the typical measurement under the worst condition (gnd shift, dominant/recessive edge, at source or destination node. ref to ISO test specification). Guaranteed by design, room temperature only.

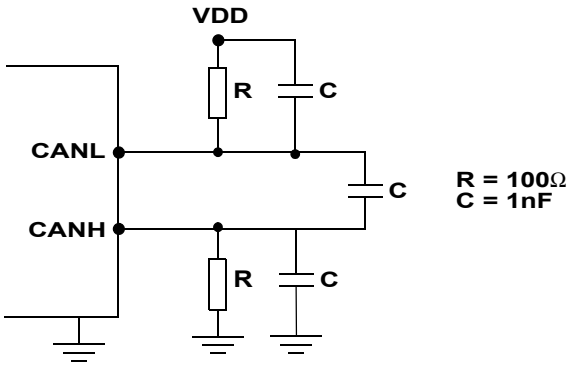
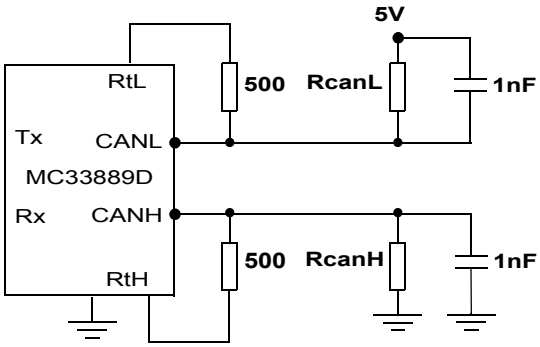
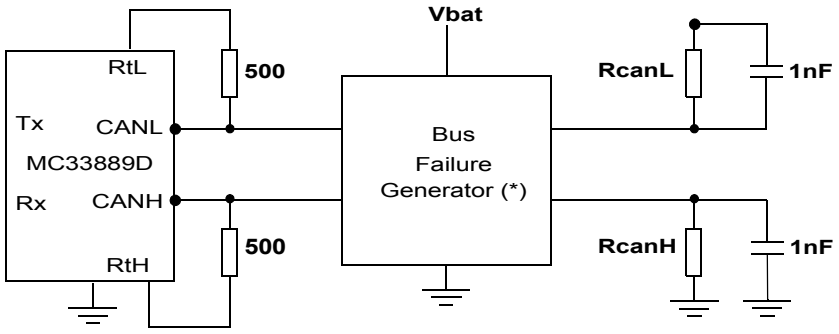



**Figure 5. Test circuit for AC characteristics**




RcanL = RcanH = 125 Ω

**Figure 6. ISO loop time without bus failure**




RcanL = RcanH = 125 Ω
except for failure CANH short to CANL
(Rcanl = 1M Ω)

(*) List of failure
CANL short to gnd, Vdd, Vbat
CANHshort to gnd, Vdd, Vbat
CANL short to CANH
CANL and CANH open

**Figure 7. ISO loop time with bus failure**

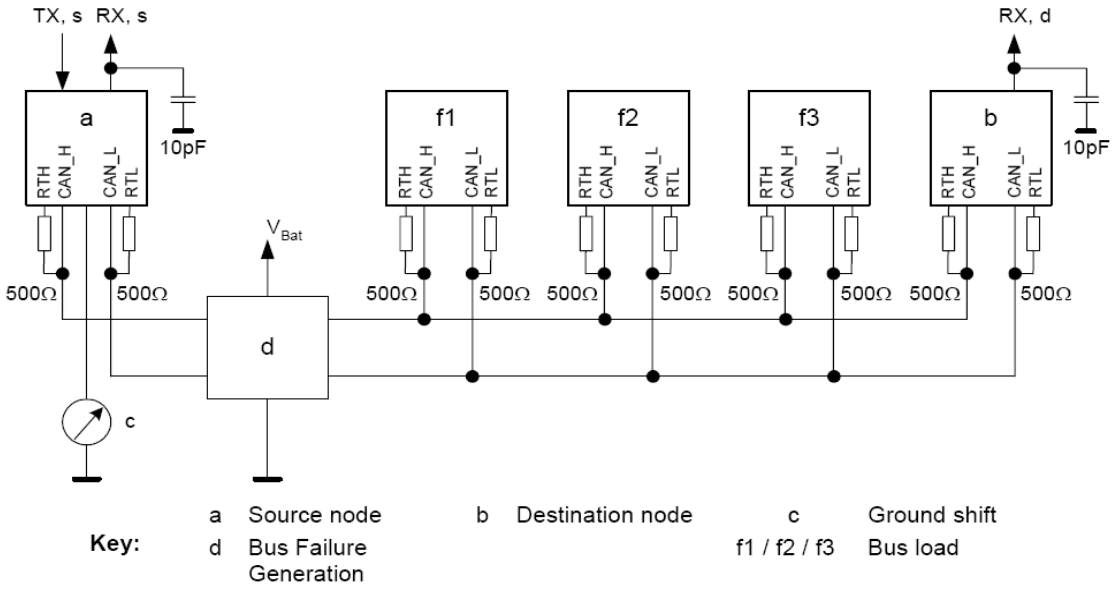



**Figure 8. Test set up for propagation delay with GND shift in a 5 node configuration**

## 4.4 Timing diagrams

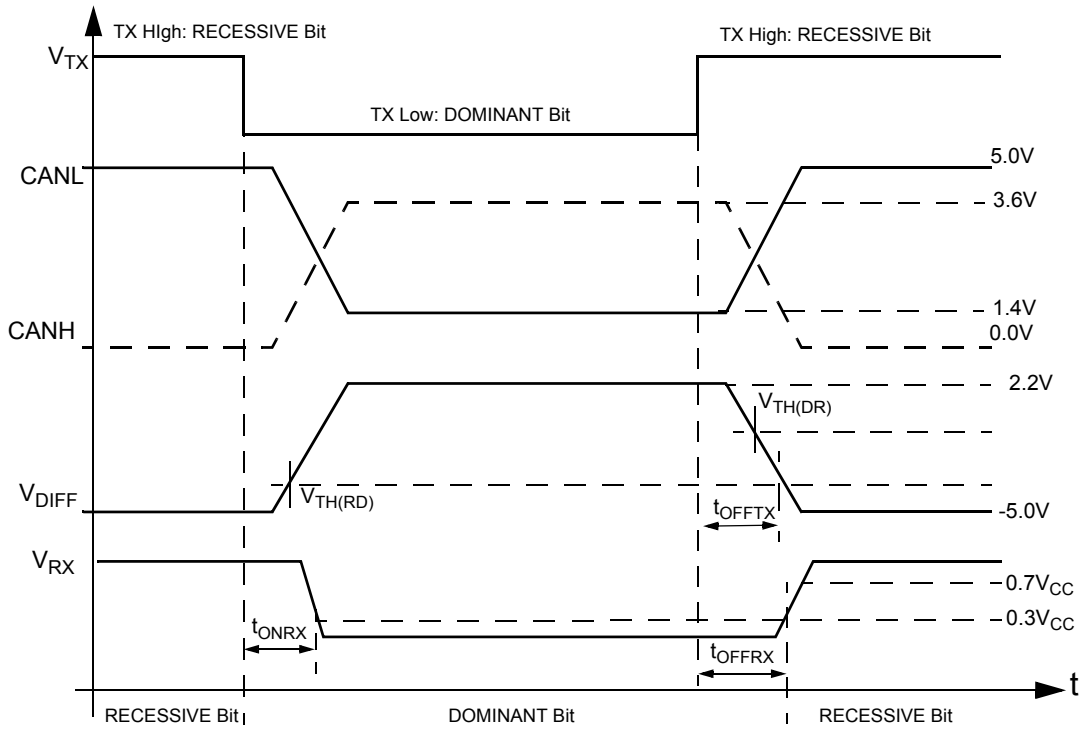



**Figure 9. Device signal waveforms**

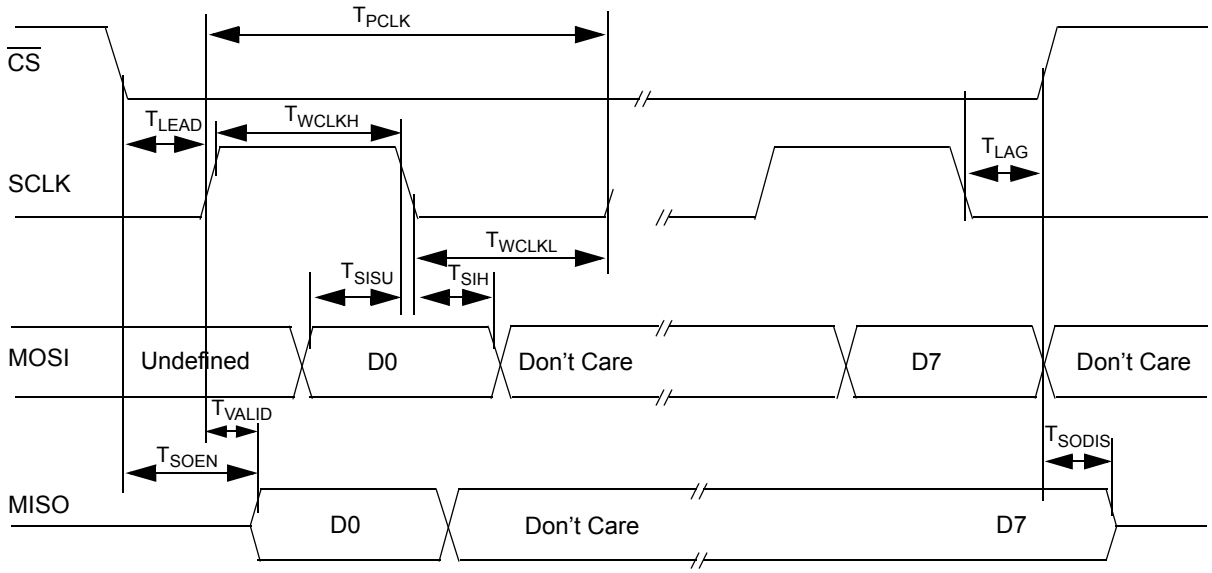



**Figure 10. Timing characteristic**

# 5 Functional description

## 5.1 Introduction

The MC33889 is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 200 mA total output current capability.
- Driver for external path transistor for V2 regulator function.
- Reset, programmable watchdog function
- Four operational modes
- Wake-up capabilities: Forced wake-up, cyclic sense and wake-up inputs, CAN and the SPI
- Can low speed fault tolerant physical interface.

## 5.2 Functional pin description

### 5.2.1 Receive and transmit data (RX and TX)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TX is an input and controls the CANH and CANL line state (dominant when TX is LOW, recessive when TX is HIGH). RX is an output and reports the bus state (RX LOW when CAN bus is dominant, HIGH when CAN bus is recessive).

### 5.2.2 Voltage regulator one (VDD1)

The VDD1 pin is the output pin of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against overcurrent and overtemperature. It includes an overtemperature prewarning flag, which is set when the internal regulator temperature exceeds 130 °C typical. When the temperature exceeds the overtemperature shutdown (170 °C typical), the regulator is turned off. VDD1 includes an undervoltage reset circuitry, which sets the $\overline{\text{RST}}$ pin LOW when VDD is below the undervoltage reset threshold.

### 5.2.3 Reset ($\overline{\text{RST}}$)

The Reset pin $\overline{\text{RST}}$ is an output that is set LOW when the device is in reset mode. The $\overline{\text{RST}}$ pin is set HIGH when the device is not in reset mode. $\overline{\text{RST}}$ includes an internal pull-up current source. When $\overline{\text{RST}}$ is LOW, the sink current capability is limited, allowing $\overline{\text{RST}}$ to be shorted to 5.0 V for software debug or software download purposes.

### 5.2.4 Interrupt ($\overline{\text{INT}}$)

The Interrupt pin $\overline{\text{INT}}$ is an output that is set LOW when an interrupt occurs. $\overline{\text{INT}}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{\text{INT}}$ stays LOW until the interrupt source is cleared. $\overline{\text{INT}}$ output also reports a wake-up event by a 10 sec. typical pulse when the device is in Stop mode.

### 5.2.5 Ground (GND)

This pin is the ground of the integrated circuit.

### 5.2.6 V2CTRL (V2CTRL)

The V2CTRL pin is the output drive pin for the V2 regulator connected to the external series pass transistor.

### 5.2.7 Voltage supply (VSUP)

The VSUP pin is the battery supply input of the device.

### 5.2.8 High-side output 1 (HS1)

The HS pin is the internal high-side driver output. It is internally protected against overcurrent and overtemperature.

### 5.2.9 Level 0-1 inputs (L0: L1)

The L0: L1 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by the SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

### 5.2.10 Voltage regulator two (V2)

The V2 pin is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the VDD output when no external series pass transistor is used. In this case, the V2CTRL pin must be left open.

### 5.2.11 RTH (RTH)

Pin for the connection of the bus termination resistor to CANH

### 5.2.12 RTL (RTL)

Pin for the connection of the bus termination resistor to CANL

### 5.2.13 CAN high and CAN low outputs (CANH and CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TXD input level, and the state of CANH and CANL is reported through RXD output.

### 5.2.14 System clock (SCLK)

SCLK is the Serial Data Clock input pin of the serial peripheral interface.

### 5.2.15 Master in/slave out (MISO

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

### 5.2.16 Master out/slave in (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

### 5.2.17 Chip select ($\overline{CS}$)

$\overline{CS}$ is the Chip Select pin of the serial peripheral interface. When this pin is LOW, the SPI port of the device is selected.

### 5.2.18 Watchdog ($\overline{WDOG}$)

The Watchdog output pin is asserted LOW to flag that the software watchdog has not been properly triggered.

## 5.3 Functional internal block description

### 5.3.1 Device supply

The device is supplied from the battery line through the VSUP pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5 V and under the jump start condition at 27 V DC. This pin sustains standard automotive voltage conditions such as load dump at 40 V. When $V_{SUP}$ falls below 3.0 V typical, the MC33889 detects it and stores the information in the SPI register, in a bit called “BATFAIL”. This detection is available in all operation modes.

### 5.3.2 VDD1 voltage regulator

VDD1 Regulator is a 5.0 V output voltage with total current capability of 200 mA. It includes a voltage monitoring circuitry associated with a reset function. The VDD1 regulator is fully protected against overcurrent, short-circuit and has overtemperature detection warning flags and shutdown with hysteresis.

### 5.3.3 V2 regulator

V2 Regulator circuitry is designed to drive an external path transistor in order to increase output current flexibility. Two pins are used: V2 and V2CTRL. Output voltage is 5.0 V and is realized by a tracking function of the VDD1 regulator. A recommended ballast transistor is the MJD32C. Other transistors might be used, however depending upon the PNP gain, an external resistor capacitor network might be connected between the emitter and base of the PNP. The use of external ballast is optional (refer to simplified typical application). The state of V2 is reported into the IOR register (if V2 is below 4.5 V typical, or in cases of overload or short-circuit).

### 5.3.4 HS1 VBAT switch output

HS1 output is a 2.0 Ω typical switch from the VSUP pin. It allows the supply of external switches and their associated pull-up or pull-down circuitry, for example, in conjunction with the wake-up input pins. Output current is limited to 200 mA and HS1 is protected against short-circuit and has an over temperature shutdown (reported into the IOR register). The HS1 output is controlled from the internal register and the SPI. It can be activated at regular intervals in sleep mode thanks to an internal timer. It can also be permanently turned on in normal or stand-by modes to drive external loads, such as relays or supply peripheral components. In case of inductive load drive, external clamp circuitry must be added.

### 5.3.5 SPI

The complete device control as well as the status report is done through an 8 bit SPI interface. Refer to the SPI paragraph.

### 5.3.6 CAN

The device incorporates a low speed fault tolerant CAN physical interface. The speed rate is up to 125 kBaud.

The state of the CAN interface is programmable through the SPI. Reference the CAN transceiver description on page 28.

### 5.3.7 Package and thermal consideration

The device is proposed in a standard surface mount SO28 package. In order to improve the thermal performances of the SO28 package, 8 pins are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

# 6 Functional device operation

## 6.1 Operational modes

### 6.1.1 Introduction

The device has four modes of operation, normal, stand-by, sleep and stop modes. All modes are controlled by the SPI. An additional temporary mode called “normal request mode” is automatically accessed by the device (refer to state machine) after wake-up events. Special mode and configurations are possible for software application debug and flash memory programming.

### 6.1.2 Normal mode

In this mode both regulators are ON, and this corresponds to the normal application operation. All functions are available in this mode (watchdog, wake-up input reading through the SPI, HS1 activation, and CAN communication). The software watchdog is running and must be periodically cleared through the SPI.

### 6.1.3 Standby mode

Only the Regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2CTRL pin. The CAN cell is not available, as powered from V2. Other functions are available: wake-up input reading through the SPI and HS1 activation. The watchdog is running.

### 6.1.4 Sleep mode

Regulators 1 and 2 are OFF. In this mode, the MCU is not powered. The device can be awakened internally by cyclic sense via the wake-up input pins and HS1 output, from the forced wake function, the CAN physical interface, and the SPI ($\overline{CS}$ pin).

### 6.1.5 Stop mode

Regulator 2 is turned OFF by disabling the V2CTRL pin. Regulator 1 is activated in a special low power mode which allows it to deliver 2.0 mA. The objective is to supply the MCU of the application while it is turned into a power saving condition (i.e stop or wait mode).

Stop mode is entered through the SPI. Stop mode is dedicated to powering the Microcontroller when it is in low power mode (stop, pseudo stop, wait etc.). In these modes, the MCU supply current is less than 1.0 mA. The MCU can restart its software application very quickly without the complete power up and reset sequence.

When the application is in stop mode (both MCU and SBC), the application can wake-up from the SBC side (ex cyclic sense, forced wake-up, CAN message, wake-up inputs) or the MCU side (key wake-up etc.).

When Stop mode is selected by the SPI, stop mode becomes active 20 μs after end of the SPI message. The “go to stop” instruction must be the last instruction executed by the MCU before going to low power mode.

In Stop mode, the Software watchdog can be “running” or “not running” depending on the selection by the SPI. Refer to the SPI description, RCR register bit WDSTOP. If the W/D is enabled, the SBC must wake-up before the W/D time has expired, otherwise a reset is generated. In stop mode, the SBC wake-up capability is identical as in sleep mode.

#### 6.1.5.1 Stop mode: wake-up from SBC side, INT pin activation

When an application is in stop mode, it can wake-up from the SBC side. When a wake-up is detected by the SBC (CAN, Wake-up input, forced wake-up, etc.), the SBC turns itself into Normal request mode and activates the VDD1 main regulator. When the main regulator is fully active, then the wake-up is signalled to the MCU through the $\overline{INT}$ pin. The $\overline{INT}$ pin is pulled low for 10 μs and then returns high. Wake-up events can be read through the SPI registers.

#### 6.1.5.2 Stop mode: wake-up from MCU side

When the application is in stop mode, the wake-up event may come to the MCU. In this case, the MCU has to signal to the SBC that it has to go into Normal mode in order for the VDD1 regulator to be able to deliver full current capability. This is done by a low to high transition of the $\overline{CS}$ pin. The $\overline{CS}$ pin low to high activation has to be done as soon as possible after the MCU. The SBC generates a pulse at the $\overline{INT}$ pin. Alternatively the L0 and L1 inputs can also be used as wake-up from the Stop mode.

#### 6.1.5.3 Stop mode current monitoring

If the current in Stop mode exceeds the $I_{DD1S-WU}$ threshold, the SBC jumps into Normal request mode, activates the VDD1 main regulator, and generates an interrupt to the MCU. This interrupt is not maskable and a not bit are set into the $\overline{INT}$ register.

#### 6.1.5.4 Software watchdog in stop mode

If the watchdog is enabled (register MCR, bit WDSTOP set), the MCU has to wake-up independently of the SBC before the end of the SBC watchdog time. In order to do this, the MCU has to signal the wake-up to the SBC through the SPI wake-up ($\overline{CS}$ pin low to high transition to activated the SPI wake-up). Then the SBC wakes up and jumps into the normal request mode. The MCU has to configure the SBC to go to either into normal or standby mode. The MCU can then choose to go back into stop mode.

If no MCU wake-up occurs within the watchdog timing, the SBC will activate the reset pin and jump into the normal request mode. The MCU can then be initialized.

#### 6.1.5.5 Normal request mode

This is a temporary mode automatically accessed by the device after a wake-up event from sleep or stop mode, or after device power up. In this mode, the VDD1 regulator is ON, V2 is off, and the reset pin is high. As soon as the device enters the normal request mode, an internal 350 ms timer is started. During these 350 ms, the microcontroller of the application must address the SBC via the SPI and configure the watchdog register (TIM1 register). This is the condition for the SBC to leave the Normal request Mode and enter the Normal mode, and to set the watchdog timer according to the configuration done during the Normal Request mode.

The “BATFAIL flag” is a bit which is triggered when $V_{SUP}$ falls below 3.0 V. This bit is set into the MCR register. It is reset by the MCR register read.

### 6.1.6 Internal Clock

This device has an internal clock used to generate all timings (reset, watchdog, cyclic wake-up, filtering time etc...).

### 6.1.7 Reset Pin

A reset output is available in order to reset the microcontroller. Reset causes are:

- $V_{DD1}$ falling out of range: if $V_{DD1}$ falls below the reset threshold (parameter $R_{ST-TH}$), the reset pin is pulled low until $V_{DD1}$ returns to the nominal voltage.
- Power on reset: at device power on or at device wake-up from sleep mode, the reset is maintained low until $V_{DD1}$ is within its operation range.
- Watchdog timeout: if the watchdog is not cleared, the SBC will pull the reset pin low for the duration of the reset duration time (parameter: RESET-DUR).

For debug purposes at 25 °C, the reset pin can be shorted to 5.0 V.

### 6.1.8 Software watchdog (selectable window or timeout watchdog)

The software watchdog is used in the SBC normal and stand-by modes for monitoring the MCU. The watchdog can be either a window or timeout. This is selectable by the SPI (register TIM, bit WDW). Default is the window watchdog. The period of the watchdog is selectable by the SPI from 5.0 to 350 ms (register TIM, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first half of the selected period, and the open window is the second half of the period. The watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. The Watchdog is cleared through the SPI by addressing the TIM register.

Refer to “table for reset pin operations” operation in mode 2.

### 6.1.9 Wake-up capabilities

Several wake-up capabilities are available for the device when it is in sleep or stop mode. When a wake-up has occurred, the wake-up event is stored into the WUR or CAN registers. The MCU can then access the wake-up source. The wake-up options are selectable through the SPI while the device is in normal or standby mode, and prior to entering low power mode (Sleep or Stop mode).

### 6.1.10 Wake-up from wake-up inputs (L0, L1) without cyclic sense

The wake-up lines are dedicated to sense external switch states, and when changes occur to wake-up the MCU (In sleep or stop modes). The wake-up pins are able to handle 40 V DC. The internal threshold is 3.0 V typical, and these inputs can be used as an input port expander. The wake-up inputs state can be read through the SPI (register WUR). L0 has a lower threshold than L1 in order to allow a connection and wake-up from a digital output such as a CAN physical interface.

### 6.1.11 Cyclic sense wake-up (cyclic sense timer and wake-up inputs L0, L1)

The SBC can wake-up from a state change of one of the wake-up input lines (L0, L1), while the external pull-up or pull-down resistor of the switches associated to the wake-up input lines are biased with HS1 VSUP switch. The HS1 switch is activated in sleep or stop mode from an internal timer. Cyclic sense and forced wake-up are exclusive. If Cyclic sense is enabled, the forced wake-up can not be enabled.

### 6.1.12 Info for cyclic sense + dual edge selection

In case the Cyclic sense and Lx both level sensitive conditions are use together, the initial value for Lx inputs are sampled in two cases:

1) When the register LPC[D3 and D0] are set and

2) At cyclic sense event, that is when device is in sleep or stop mode and HS1 is active.

The consequence is that when the device wake up by Lx transition, the new value is sampled as default, then when the device is set back into low power again, it will automatically wake up.

**The user should reset the LPC bits [D3 and D0] to 0 and set them again to the desired value prior to enter sleep or stop mode.**

### 6.1.13 Forced wake-up

The SBC can wake-up automatically after a predetermined time spent in sleep or stop mode. Forced wake-up is enabled by setting bit FWU in the LPC register. Cyclic sense and forced wake-up are exclusive. If forced wake-up is enabled, the Cyclic sense can not be enabled.

### 6.1.14 CAN wake-up

The device can wake-up from a CAN message. A CAN wake-up cannot be disabled.

### 6.1.15 SPI wake-up

The device can wake-up by the $\overline{CS}$ pin in sleep or stop mode. Wake-up is detected by the $\overline{CS}$ pin transition from a low to high level. In stop mode this correspond to the condition where the MCU and SBC are both in Stop mode, and when the application wake-up events come through the MCU.

### 6.1.16 System power up

At power up the device automatically wakes up.

### 6.1.17 Device power up, SBC wake up

After device or system power up or a wake-up from sleep mode, the SBC enters into “reset mode” then into “normal request mode”.

## 6.1.18 Battery fall early warning

This function provides an interrupt when the VSUP voltage is below the 6.1 V typical. This interrupt is maskable. A hysteresis is included. Operation is only in Normal and Stand-by modes. VBAT low state reports in the IOR register.

## 6.1.19 Reset and Wdog operation

The following figure shows the reset and watchdog output operations. Reset is active at device power up and wake-up. Reset is activated in case the VDD1 falls or the watchdog is not triggered. The $\overline{\text{WDOG}}$ output is active low as soon as the reset goes low and stays low for as long as the watchdog is not properly re-activated by the SPI.

The $\overline{\text{WDOG}}$ output pin is a push pull structure than can drive external components of the application, for instance to signal the MCU is in a wrong operation. Even if it is internally turned on (low-state), the reset pin can be forced to 5.0 V at 25 °C only, thanks to its internally limited current drive capability. The $\overline{\text{WDOG}}$ stays low until the Watchdog register is properly addressed through the SPI.

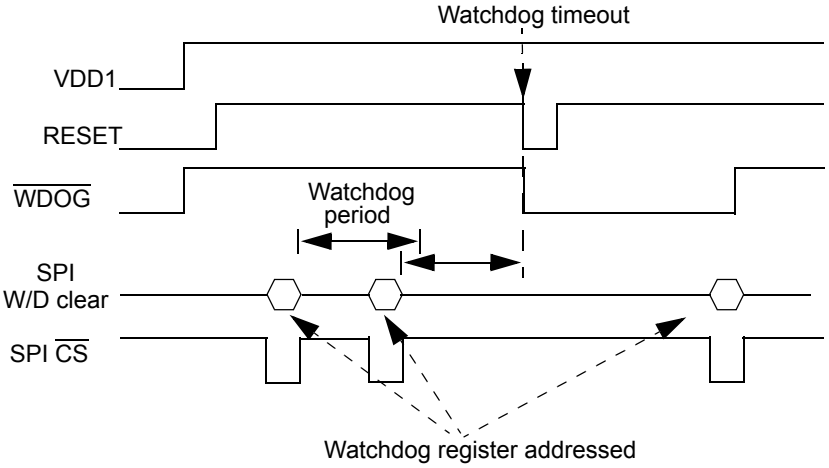



**Figure 11. Reset and $\overline{\text{WDOG}}$ function diagram**

## 6.1.20 Debug mode Application hardware and software debug with the SBC.

When the SBC is mounted on the same printed circuit board as the micro controller, it supplies both application software and the SBC with a dedicated routine that must be debugged. The following features allow the user to debug the software by disabling the SBC internal software watchdog timer.

## 6.1.21 Device power up, reset pin connected to VDD1

At SBC power up, the VDD1 voltage is provided, but if no SPI communication occurs to configure the device, a reset occurs every 350 ms. In order to allow software debugging and avoid an MCU reset, the Reset pin can be connected directly to VDD1 by a jumper.

## 6.1.22 Debug modes with software watchdog disabled though SPI (normal debug, standby debug and stop debug)

The software watchdog can be disabled through the SPI. In order to avoid unwanted watchdog disables, and to limit the risk of disabling the watchdog during an SBC normal operation, the watchdog disable has to be performed with the following sequence:

Step 1) Power down the SBC

Step 2) Power up the SBC (The BATFAIL bit is set, and the SBC enters normal request mode)

Step 3) Write to the TIM1 register to allow the SBC to enter Normal mode

Step 4) Write to the MCR register with data 0000 (this enables the debug mode). (Complete SPI byte: 000 1 0000)

Step 5) Write to the MCR register normal debug (0001 x101), stand-by debug (0001 x110), or Stop debug (0001 x111)

While in debug mode, the SBC can be used without having to clear the W/D on a regular basis to facilitate software and hardware debugging.

Step 6) To leave the debug mode, write 0000 to the MCR register.

To avoid entering the debug mode after a power up, first read the BATFAIL bit (MCR read) and write 0000 into the MCR.

Figure 12 illustrates entering the debug mode.

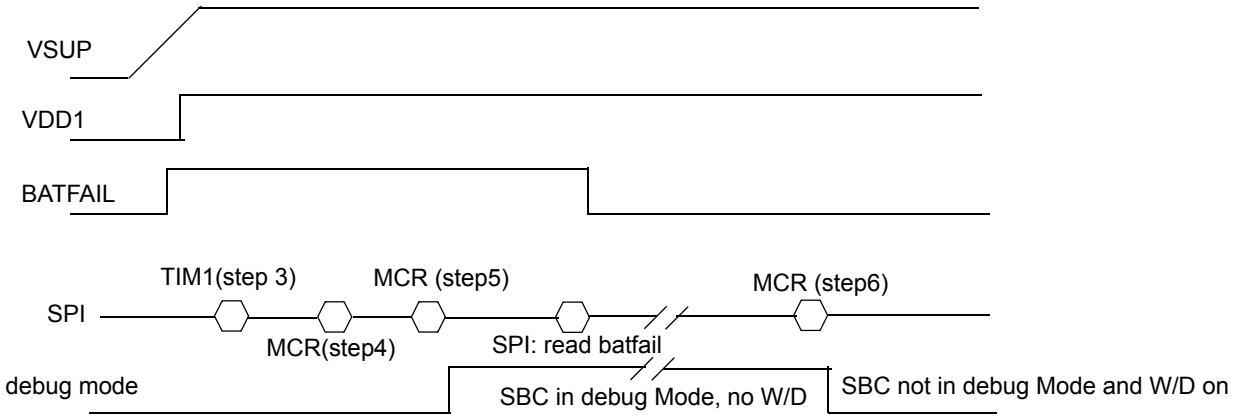



**Figure 12. Debug mode enter**

## 6.1.23 MCU flash programming configuration

To facilitate the possibility of down loading software into the application memory (MCU EEPROM or Flash), the SBC allows the following capabilities: The VDD1 can be forced by an external power supply to 5.0 V and the reset and $\overline{\text{WDOG}}$ output by external signal sources to zero or 5.0 V without damage. This supplies the complete application board with external power supply and applies the correct signal to the reset pin.

### 6.1.24 CAN transceiver description

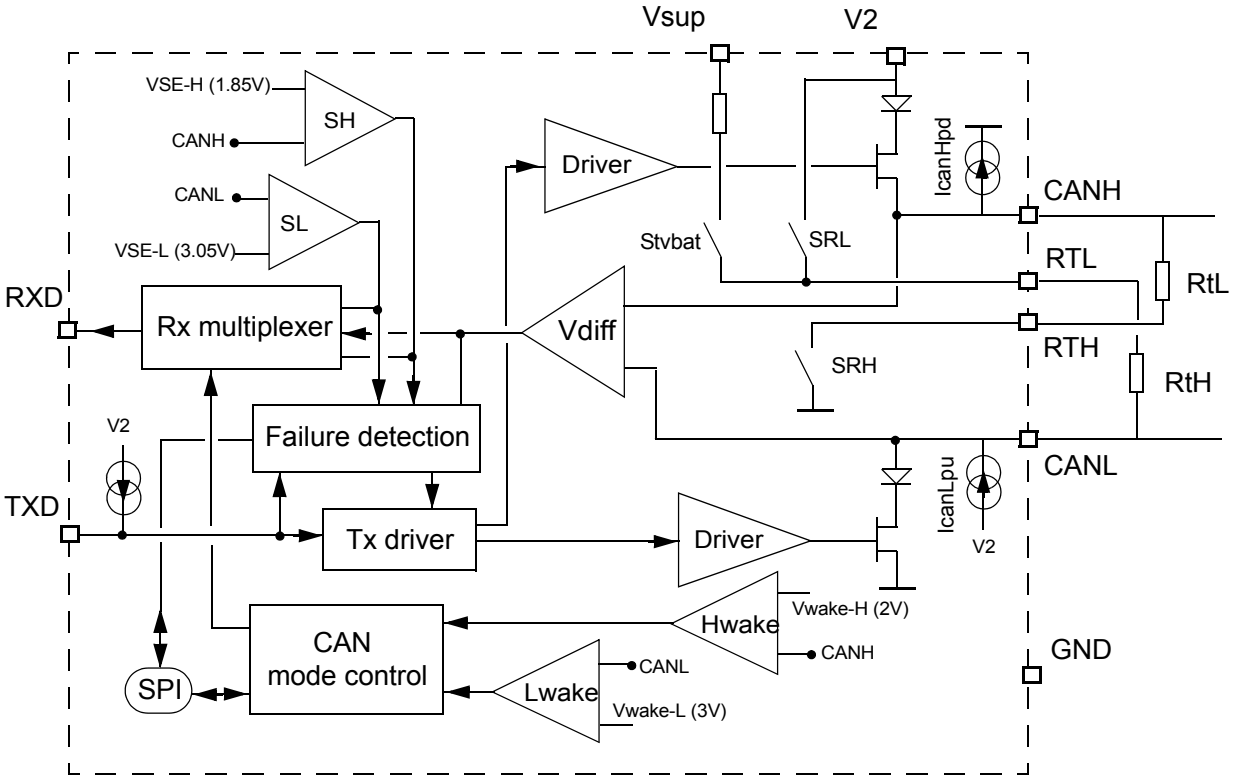



**Figure 13. Simplified block diagram of the CAN transceiver of the MC33889**

## 6.2 General description

### 6.2.1 CAN driver

The CANH driver is a “high-side” switch to the V2 voltage (5.0 V). The CANL driver is a “low-side” switch to gnd.The turn on and turn off time is controlled in order to control the slew rate, and the CANH and CANL driver have a current limitation as well as an over temperature shutdown.

The CAN H or CANL driver can be disabled in case a failure is detected on the CAN bus (ex: CANH driver is disabled in case CANH is shorted to $V_{DD}$). The disabling of one of the drivers is controlled by the CAN logic and the communication continues via the other drivers. When the failure is removed the logic detects a failure recovery and automatically reenables the associated driver.

The CAN drivers are also disabled in case of a Tx failure detection.

### 6.2.2 Bus termination

The bus is terminated by pull-up and pull-down resistors, which are connected to GND, VDD, or VBAT through dedicated RTL and RTH pins and internal switches Srh, Srl, Stvbat. Each node must have a resistor connected between CANH and RTH and between CANL and RTL. The resistor value should be between 500 and 16000 Ω.

### 6.2.3 Transmitter function

CAN bus levels are called Dominant and Recessive, and correspond respectively to Low and High states of the TX input pin.

Dominant state:

The CANH and CANL drivers are on. The voltage at CANL is <1.4 V, the voltage at CANH is >3.6 V, and the differential voltage between CANH and CANL line is >2.2 V (3.6 -1.4 V).

Recessive state:

This is a weak state, where the CANH and CANL drivers are off. The CANL line is pulled up to 5 V via the RTL pin and RTL resistor, and the CANH line is pull down via the RTH and RTH resistor. The resultant voltage at CANL is 5.0 V and 0V at CANH. The differential voltage is -5.0 V (0V - 5.0 V). The recessive state can be over written by any other node forcing a Dominant state.

### 6.2.4 Receiver function

In normal operation (no bus failures), RX is the image of the differential bus voltage. The differential receiver inputs are connected to CANH and CANL.

The device incorporates single ended comparators connected to CANH and CANL in order to monitor the bus state as well as detect bus failures. Failures are reported via the SPI.

In normal operation when no failure is present, the differential comparator is active. Under a fault condition, one of the two CANH or CANL pins can be become non-operational. The single ended comparator of either CANH or CANL is activated and continues to report a bus state to Rx pin. The device permanently monitors the bus failure and recovery, and as soon as fault disappears, it automatically switches back to differential operation.

#### 6.2.4.1 CAN interface operation mode

The CAN has 3 operation modes: TxRx (Transmit-Receive), Receive Only, and Term-VBAT (Terminated to VBAT). The mode is selected by the SPI. As soon as the MC33889 mode is sleep or stop (selected via MCR register), the CAN interface automatically enters Tem-Vbat mode.

### 6.2.5 Tx Rx mode

In this mode, the CAN drivers and receivers are enabled, and the device is able to send and receive messages. Bus failures are detected and managed, this means that in case of a bus failure, one of the CAN drivers can be disabled, but communication continues via the remaining drivers.

### 6.2.6 Receive only mode:

In this mode, the transmitter path is disabled, so the device does not drive the bus. It maintains CANL and CANH in the recessive state. The receiver function operates normally.

### 6.2.7 TermVbat mode

In this mode, the transmitter and receiver functions are disabled. The CANL pin is connected to $V_{SUP}$ through the RTL resistor and internal pull up resistor of 12.5 kΩ. In this mode, the device monitors the bus activity and if a wake up conditions is encountered on the CAN bus, it will wakes up the MC33889.

The device will enter into a normal request mode if low power mode was in sleep, or generates an INT. It enters into Normal request mode if low power mode was in stop mode. If the device was in normal or stand by mode, the Rx pin will report a wake up (feature not available on the MC33889B). See Rx pin behavior.

## 6.2.8 Bus Failure Detection

### 6.2.8.1 General description

The device permanently monitors the bus lines and detects faults in normal and receive only modes. When a fault is detected, the device automatically takes appropriate actions to minimize the system current consumption and to allow communication on the network. Depending on the type of fault, the mode of operation, and the fault detected, the device automatically switches off one or more of the following functions: CANL or CANH line driver, RTL or RTH termination resistors, or internal switches. These actions are detailed in the following table.

The device permanently monitors the faults and in case of fault recovery, it automatically switches back to normal operation and reconnects the open functions. Fault detection and recovery circuitry have internal filters and delays timing, detailed in the AC characteristics parameters.

The failure list identification and the consequence on the device operation are described in following table. The failure detection, and recovery principle, the transceiver state after a failure detected, timing for failure detection and recovery can be found in the ISO11898-3 standard.

The following table is a summary of the failure identifications and of the consequences on the CAN driver and receiver when the CAN is in Tx Rx mode.

| Bus failure identification | Description | Consequence on CAN driver | Consequence on Rx pin |
|---|---|---|---|
| | no failure | default operation: CAN H and CANL driver active, RTH and RTL termination switched ON | default operation: Report differential receiver output |
| 1 | CANH open wire | default operation | default operation |
| 5 | CANH shorted to GND | default operation | default operation |
| 8, 3a | CANH shorted to $V_{DD}$ (5.0 V) | CANH driver turn OFF. RTH termination switched OFF | Rx report CANL single ended receiver |
| 3 | CANH shorted to $V_{BAT}$ | CANH driver turn OFF. RTH termination switched OFF | Rx report CANL single ended receiver |
| 2 | CANL open wire | default operation | default operation |
| 4, 7 | CANL shorted to GND or CANL shorted to CANH | CANL driver is OFF. RTL termination switched OFF | Rx report CANH single ended receiver |
| 9 | CANL shorted to $V_{DD}$ (5.0 V) | CANL driver is ON. RTL termination active | default operation |
| 6 | CANL shorted to $V_{BAT}$ | CANL driver is OFF. RTL termination switched OFF | Rx report CANH single ended receiver |

## 6.2.9 Open wire detection operation

### 6.2.9.1 Description

The CANH and CANL open wire failures are not described in the ISO document. Open wire is only diagnostic information, as no CAN driver or receiver state will change in case of an open wire condition.

In case one of the CAN wires are open, the communication will continue through the remaining wire. In this situation the 33889 will receive information on one wire only and the consequences are as follows:

when the bus is set in dominant:

- The differential receiver will toggle
- Only one of the single ended receivers CANH or of CANL will toggle

The following figure illustrates the CAN signal during normal communication and in the example of a CANH open wire. The single ended receiver is sampled at the differential receiver switching event, in a window of 1.0 µs.

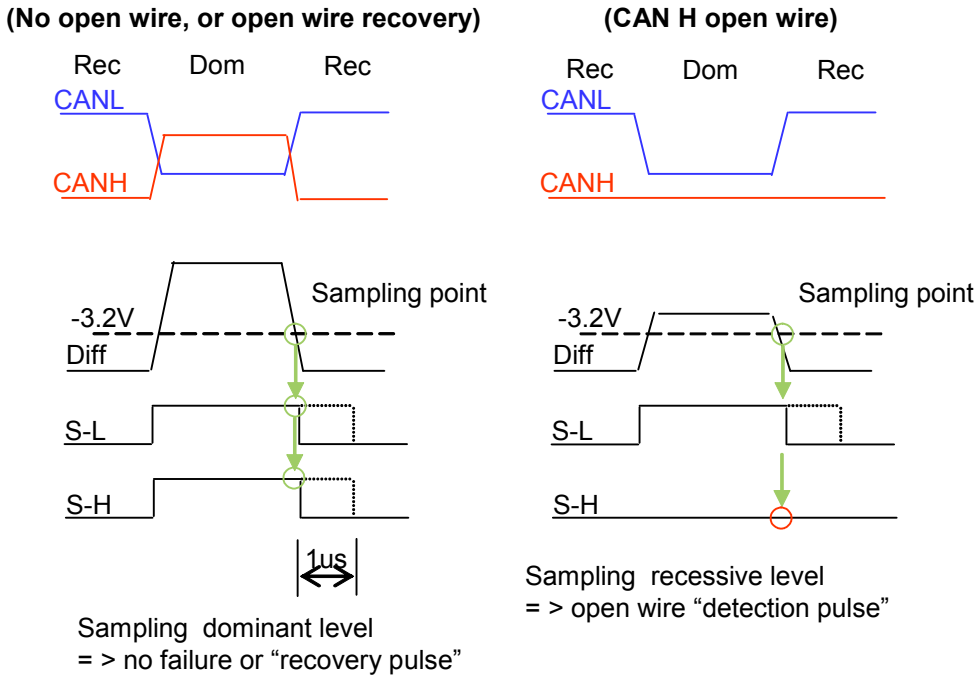



**Figure 14. CAN normal signal communication and CAN open wire**

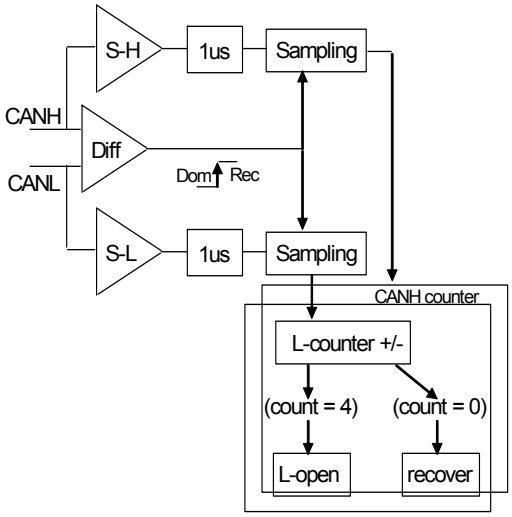



**Figure 15. Open wire detection principle**

## 6.2.10 Open wire detection, MC33889B and D

### 6.2.10.1 Failure detection

The device will detect a difference in toggling counts between the differential receiver and one of the single ended receivers. Every time a difference in count is detected a counter is incremented. When the counter reaches 4, the device detects and reports an open wire condition. The open wire detection is performed only when the device receives a message and not when it send message.

Open wire recovery:

When the open wire failure has recovered, the difference in count is reduced and the device detects the open wire recovery.

### 6.2.10.2 MC33889B

When detection is complete, the counter is no longer incremented. It can only be decremented by sampling of the dominant level on the S-H (S-L) (recovery pulse). When it reaches zero, the failure has recovered.

In application, with CAN communication, a recovery condition is detected after 4 acknowledge bits are sent by the MC33889B.

### 6.2.10.3 MC333889D

When detection is complete, the counter is decremented by sampling the dominant pulse (recovery pulse) on S-H (S-L), and incremented (up to 4) by sampling the recessive pulse (detection pulses) on S-H (S-L). It is necessary to get 4 consecutive dominant samples (recovery pulse) to get to zero. When reaching zero, the failure is recovered.

In application with real CAN communication, a recovery condition will not be detected by a single acknowledge bit send by MC33889D, but requires a complete CAN message (at least 4 dominant bits) send in dual wire mode, without reception of any bit in single wire mode.

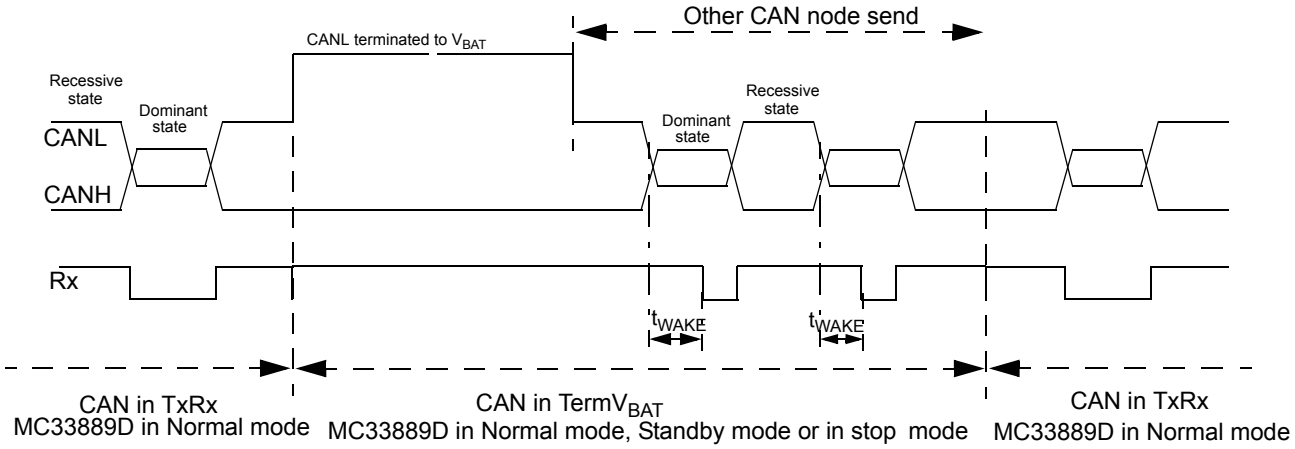
### 6.2.10.4 Tx permanent dominant detection

In addition to the previous list, the 33889 detects a permanent low state at the TX input which results in a permanent dominant bus state. If TX is low for more than 0.75-4.0 ms, the bus output driver is disabled. This avoids blocking communication between other nodes of the network. TXD is reported via the SPI (RCR register bit D1: TXFAILURE). Tx permanent dominant recovery is done with TX recessive for more than Typ. 32 µs.

### 6.2.10.5 Rx pin behavior while CAN interface is in Term$V_{BAT}$

The MC33889D is able to signal bus activity on Rx while the CAN interface is in Term$V_{BAT}$ and the SBC in normal or standby mode. When the bus is driven into a dominant state by another sending node, each dominant state is reported at Rx by a low level, after a delay of $t_{WAKE}$.

The bus state report is done through the CAN interface wake-up comparator on CANL and CANH, and thus operates also in case of bus failure. This is illustrated in Figure 16.




$t_{WAKE}$: duration of the CAN wake up filter, typ 16 µs. The MC33889D Rx dominant low level duration is the difference between the duration of the bus minus the $t_{WAKE}$, as illustrated below ($t_{RX\_DOM} = t_{BUS\_DOM} - t_{WAKE}$)

Example: A dominant duration at the bus level of 5 bits of 8us each results in a 40 µs bus dominant. This results in a 24 µs (40 µs -16 µs) dominant level at Rx of MC33889D (while the CAN of the MC33889D is in Term$V_{BAT}$).

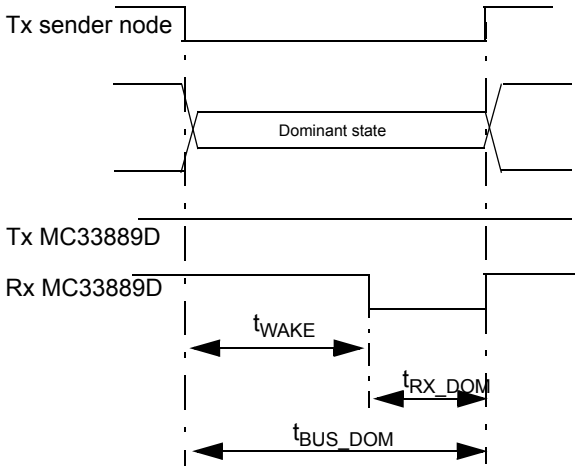



**Figure 16. Bus state report of the CAN interface wake-up comparator on CANL and CANH**

The following table summarizes the device behavior when a CAN Wake-up event occurs.

**Table 6. Summary of RX pin operations for wake-up signaling**

| SBC mode | CAN state | MC33889B | MC33889D |
|---|---|---|---|
| Normal | Term$V_{BAT}$ | no event on RX, no bit set | RX pulse (1), bit CANWU is not set |
| Standby | Term$V_{BAT}$ | no event on RX, no bit set | RX pulse (1), bit CANWU is not set |
| Sleep | Term$V_{BAT}$ | SBC mode transition to Normal request, bit CANWU set | SBC mode transition to Normal request, bit CANWU set |
| Stop | Term$V_{BAT}$ | INT pulse, bit CANWU set | Int pulse, bit CANWU set |

Notes

28. pulse duration is bus dominant duration minus $t_{WAKE}$.

## 6.2.11 GND shift detection

### 6.2.11.1 General

When normally working in two-wire operating mode, the CAN transmission can afford some ground shift between different nodes without trouble. Should a bus failure occur, the transceiver switches to single-wire operation, therefore working with less noise margin. The affordable ground shift is decreased.

The SBC provides a ground shift detection for diagnosis purpose. The four ground shift levels are selectable and the detection is stored in the IOR register which is accessible via the SPI.

### 6.2.11.2 Detection principle

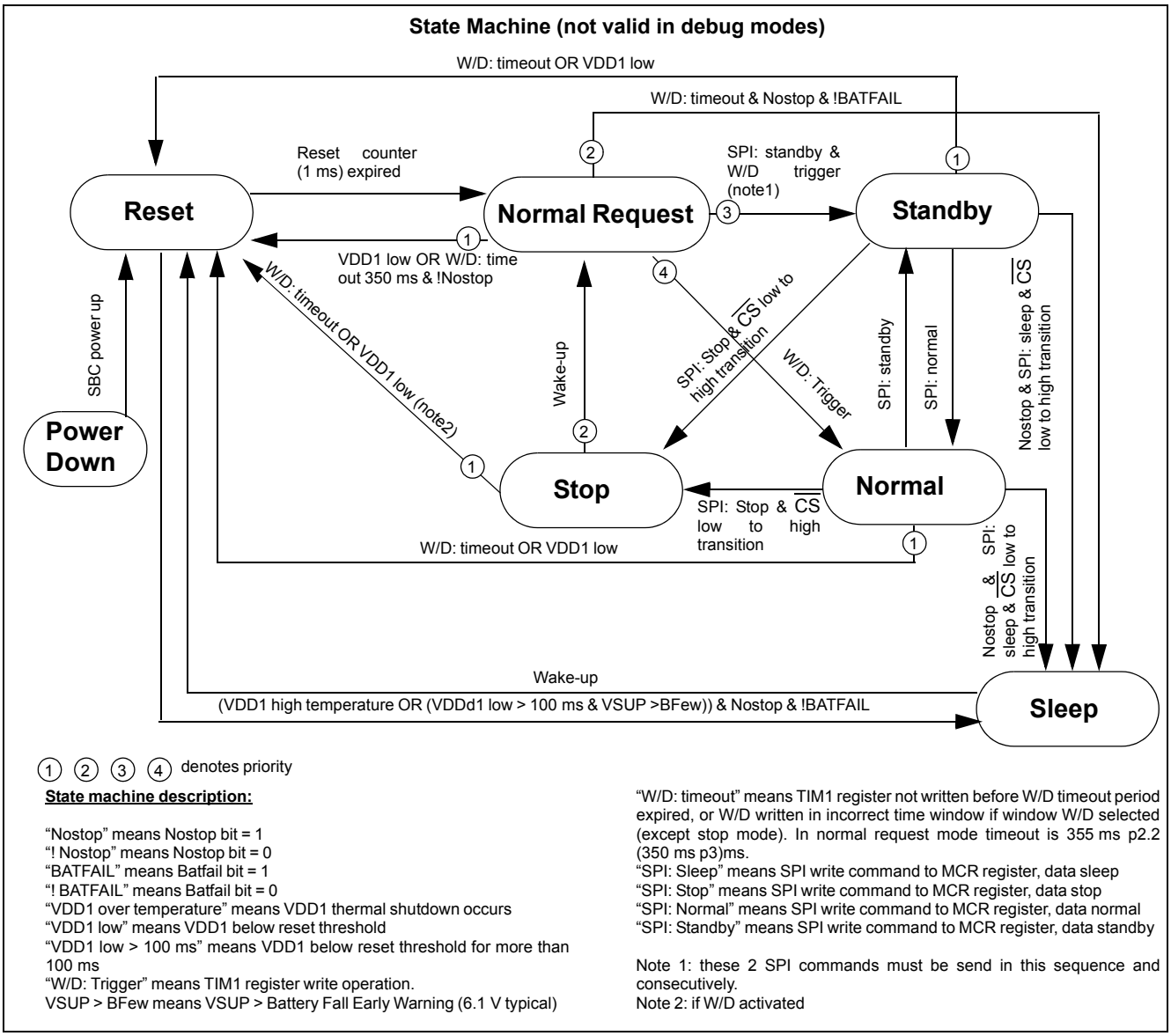
The GND shift to detect is selected via the SPI from 4 different values (-0.3 V, -0.7 V, -1.2 V, -1.7 V). At each TX falling edge (end of recessive state), the CANH voltage is sensed. If it is detected to be below the selected gnd shift threshold, the bit SHIFT is set at 1 in the IOR register. No filter is implemented. Required filtering for reliable detection should be done by software (e.g. several trials).

## 6.2.12 Device state description

**Table 7. 33889 table of operations**

The table below describes the SBC operation modes.

| Mode | Voltage regulator HS1 switch | Wake-up capabilities (if enabled) | Reset pin | INT | Software watchdog | CAN cell |
|---|---|---|---|---|---|---|
| Normal Request | VDD1: ON<br>V2: OFF<br>HS1: OFF | | Low for 1.0 ms, then high | | | term $V_{BAT}$ |
| Normal | VDD1: ON<br>V2: ON<br>HS1 controllable | | Normally high. Active low if W/D or VDD1 under voltage occur | If enabled, signal failure (VDD prewarning temp, CAN, HS1) | Running | Term $V_{BAT}$<br>Tx/Rx<br>Rec only |
| Standby | VDD1: ON<br>V2: OFF<br>HS1 controllable | | Normally high. Active low if W/D or VDD1 under voltage occur | If enabled, signal failure (VDD temp, HS1) | Running | Term $V_{BAT}$<br>Tx/Rx<br>Rec only |
| Stop | VDD1: ON<br>(limited current capability)<br>V2: OFF<br>HS1: OFF or cyclic | CAN (always enable)<br>SPI and L0,L1<br>Cyclic sense or<br>Forced Wake-up | Normally high. Active low if W/D or VDD1 under voltage occur | Signal SBC wake-up (not maskable) | - Running if enabled<br>- Not Running if disabled | Term $V_{BAT}$ |
| Sleep | VDD1: OFF<br>V2: OFF<br>HS1 OFF or cyclic | CAN (always enable<br>SPI and L0,L1<br>Cyclic sense<br>Forced Wake-up | Low | Not active | No Running | Term $V_{BAT}$ |




**State machine description:**

"Nostop" means Nostop bit = 1
"! Nostop" means Nostop bit = 0
"BATFAIL" means Batfail bit = 1
"! BATFAIL" means Batfail bit = 0
"VDD1 over temperature" means VDD1 thermal shutdown occurs
"VDD1 low" means VDD1 below reset threshold
"VDD1 low > 100 ms" means VDD1 below reset threshold for more than 100 ms
"W/D: Trigger" means TIM1 register write operation.
VSUP > BFew means VSUP > Battery Fall Early Warning (6.1 V typical)

"W/D: timeout" means TIM1 register not written before W/D timeout period expired, or W/D written in incorrect time window if window W/D selected (except stop mode). In normal request mode timeout is 355 ms p2.2 (350 ms p3)ms.
"SPI: Sleep" means SPI write command to MCR register, data sleep
"SPI: Stop" means SPI write command to MCR register, data stop
"SPI: Normal" means SPI write command to MCR register, data normal
"SPI: Standby" means SPI write command to MCR register, data standby

Note 1: these 2 SPI commands must be send in this sequence and consecutively.
Note 2: if W/D activated

**Figure 17. Simplified state machine**

33889

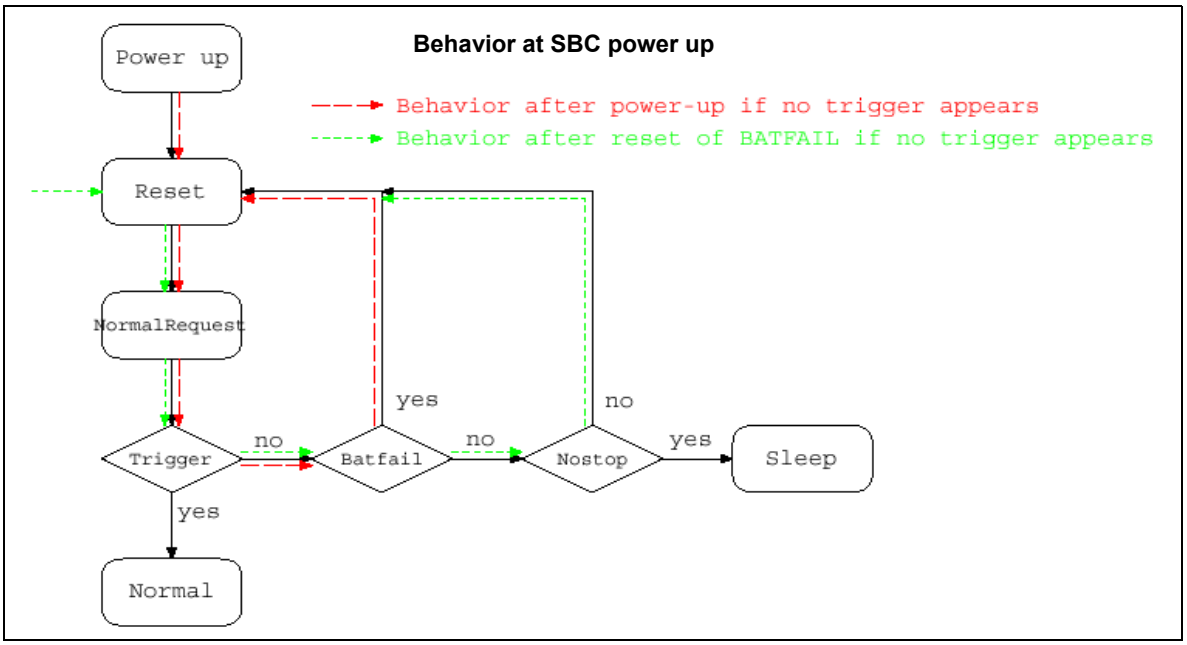



**Figure 18. Behavior at SBC power up**

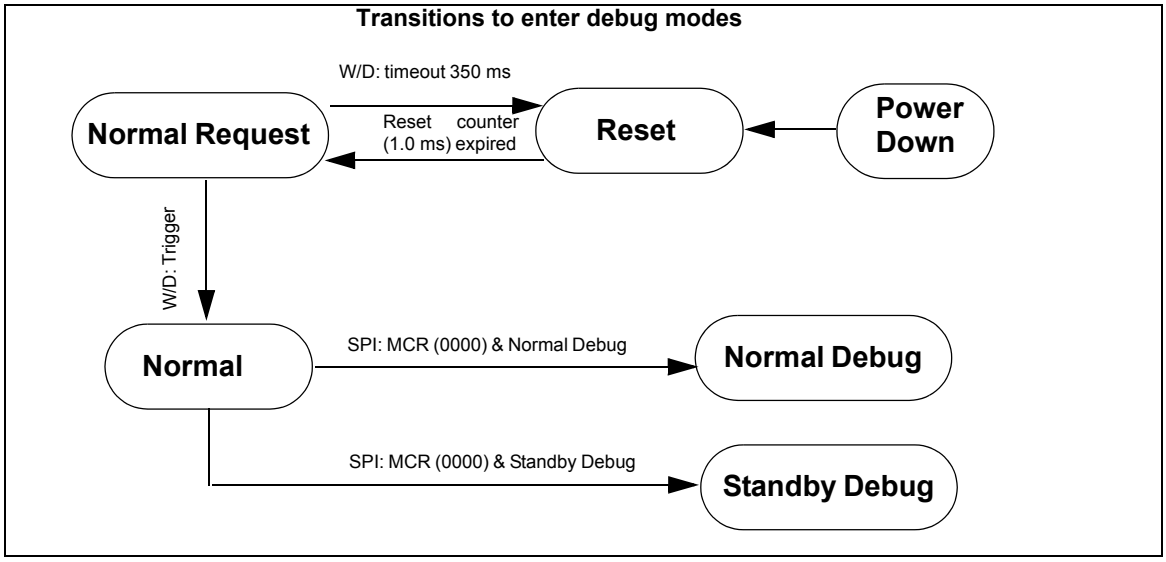



**Figure 19. Transitions to enter debug modes**

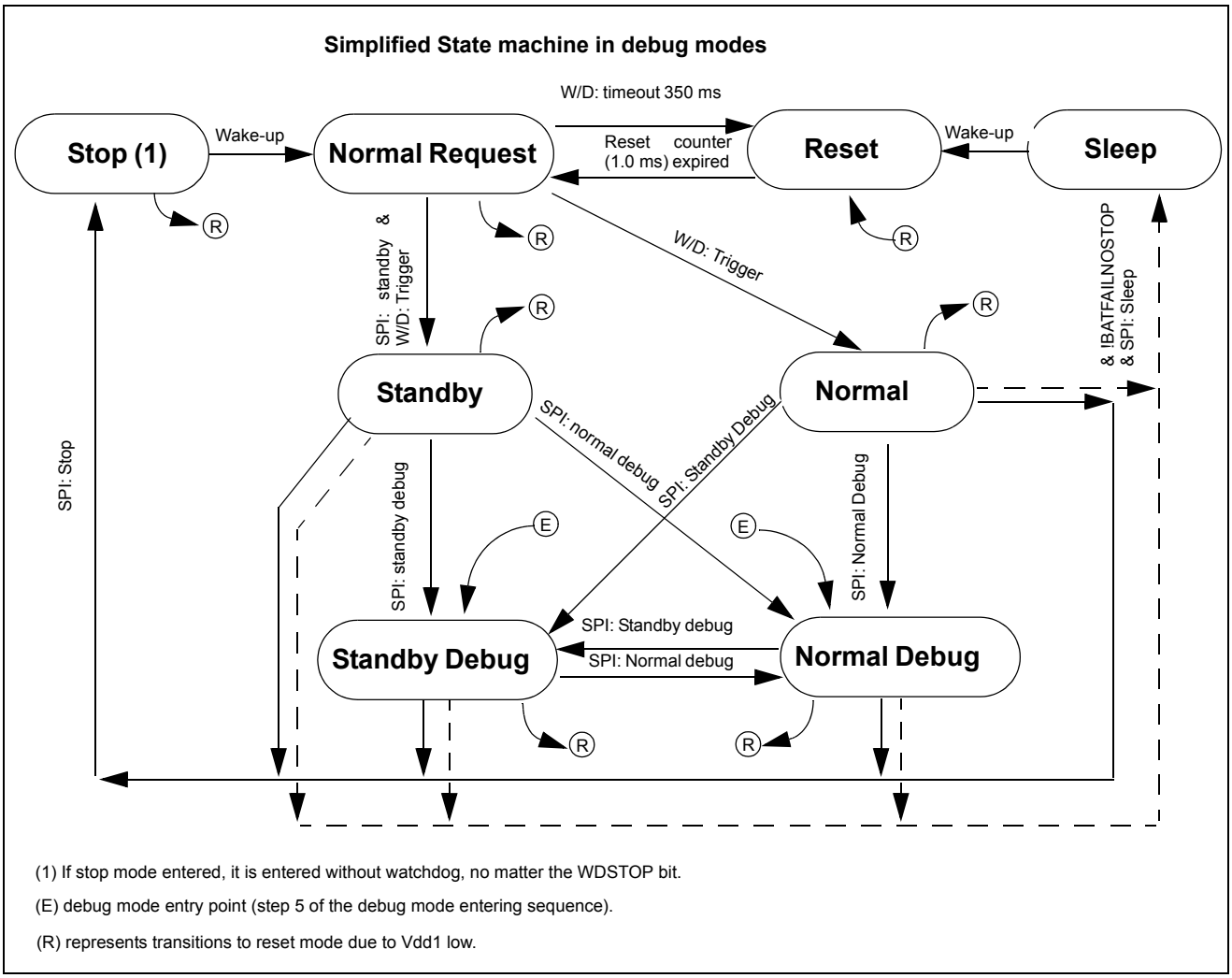



**Figure 20. Simplified state machine in debug mode**

# 6.3 Logic commands and registers

## 6.3.1 SPI interface

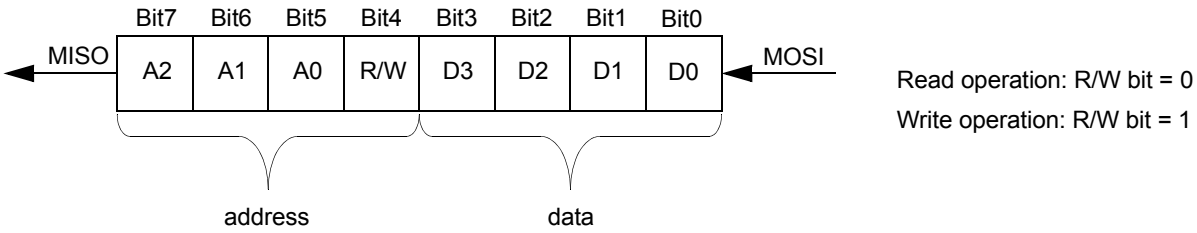



**Figure 21. Data format description**

The SPI is a 8 bit SPI. First 3 bits are used to identify the internal SBC register address, bit 4 is a read/write bit. The last 4 bits are data send from MCU to SBC or read back from SBC to MCU.

During write operation state of MISO has no signification.

During read operation only the last 4 bits at MISO have a meaning (content of the accessed register)

Following tables describe the SPI register list, and register bit meaning.

Registers “reset value” is also described, as well as the “reset condition”. reset condition is the condition which cause the bit to be set at the “reset value”.

Possible reset condition are:

Power On Reset: POR

SBC mode transition:

- NR2R - Normal Request to Reset mode
- NR2N - Normal Request to Normal mode
- N2R - Normal to Reset mode
- STB2R - Standby to Reset mode
- STO2R - Stop to Reset mode
- SBC mode:RESET - SBC in Reset mode

**Table 8. List of registers**

| Name | Address | Description | Comment and usage |
|---|---|---|---|
| MCR | $0 0 0 | Mode control register | Write: Control of normal, standby, sleep, and stop modes<br>Read: BATFAIL flag and other status bits and flags |
| RCR | $0 0 1 | Reset control register | Write: Configuration of reset voltage level, WD in stop mode, low power mode selection<br>Read: CAN wake-up event, Tx permanent dominant |
| CAN | $0 1 0 | CAN control register | Write: CAN module control: TX/RX, Rec only, term VBAT, Normal and extended modes, filter at L0 input.<br>Read: CAN failure status bits |
| IOR | $0 1 1 | I/O control register | Write: HS1 (high-side switch) control in normal and standby mode.<br>Gnd shift register level selection<br>Read: HS1 over temp bit, SHIFT bit (gnd shift above selection), $V_{SUP}$ below 6.1V, V2 below 4.0 V |
| WUR | $1 0 0 | Wake-up input register | Write: Control of wake-up input polarity<br>Read: Wake-up input, and real time LX input state |
| TIM | $1 0 1 | Timing register | Write: TIM1, Watchdog timing control, window or Timeout mode.<br>Write: TIM2, Cyclic sense and force wake-up timing selection |
| LPC | $1 1 0 | Low power mode control register | Write: HS1 periodic activation in sleep and stop modes<br>Force wake-up control |
| INTR | $1 1 1 | Interrupt register | Write: Interrupt source configuration<br>Read: INT source |

NOTE: For SPI Operation

In case a low pulse is asserted by the device on the RST output pin during a SPI message, the SPI message can be corrupted. An RST low pulse is asserted in 2 cases:

Case 1: W/D refresh issue: The MCU does not perform the SPI watchdog refresh command before the expiration of the timeout (in Normal mode or Normal Request mode and if the “Timeout watchdog” option is selected), or the SPI watchdog refresh command is performed in the closed window (in Normal mode and if “Window watchdog” option is selected).

Case 2: VDD undervoltage condition: VDD falls below the VDD undervoltage threshold.

Message corruption means that the targeted register address can be changed, and another register is written. Table 9 shows the various cases and impacts on SPI register address:

**Table 9. Possible corrupted registers in case of RST pulse during SPI communication**

| | | Resulting Written register | | | | |
|---|---|---|---|---|---|---|
| | | **Register** | **MCR** | **RCR** | **CAN** | **IOR** |
| | | **Address** | **$000** | **$001** | **$010** | **$011** |
| Target written register | Register | Address | | | | |
| | CAN | $010 | X | | | |
| | IOR | $011 | | X | | |
| | WUR | $100 | X | | | |
| | TIM1/2 | $101 | | X | | |
| | LPC | $110 | X | | X | |
| | INTR | $111 | | X | | X |

Four registers can be corrupted: MCR, RCR, CAN, and IOR registers. As examples:

- write to CAN register can end up as write to MCR register, or
- write to TIM1 register can end up as write to RCR register

To avoid the previously described behavior, it is recommended to write into the MCR, RCR, CAN, and IOR registers with the expected configuration, after each $\overline{\text{RST}}$ assertion.

In the application, a $\overline{\text{RST}}$ low pulse leads to an MCU reset and a software restart. By applying this recommendation, all registers will be written with the expected configuration.

## 6.3.2 Register description

**Table 10. MCR register**

| MCR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $000b | W | | MCTR2 | MCTR1 | MCTR0 |
| | R | BATFAIL | VDDTEMP | GFAIL | WDRST |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 11. Control bits**

| MCTR2 | MCTR1 | MCTR0 | SBC mode | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | Enter/leave debug mode | To enter debug mode, SBC must be in Normal or Standby mode and BATFAIL [29] must be still at 1. To leave debug mode, BATFAIL must be at 0. |
| 0 | 0 | 1 | Normal | |
| 0 | 1 | 0 | Standby | |
| 0 | 1 | 1 | Stop, watchdog off [30] | |
| 0 | 1 | 1 | Stop, watchdog on [30] | |
| 1 | 0 | 0 | Sleep [31] | |
| 1 | 0 | 1 | Normal | No watchdog running, debug mode |
| 1 | 1 | 0 | Standby | |
| 1 | 1 | 1 | Stop [32] | |

Notes

29. Bit BATFAIL cannot be set by SPI. BATFAIL is set when $V_{SUP}$ falls below 3V.
30. Watchdog ON or OFF depends on the RCR register bit D3.
31. Before entering sleep mode, bit NOSTOP in RCR register must be previously set to 1.
32. Stop command should be replaced by Stop Watchdog OFF. MCTR2=0, MCTR1= MCTR0=1

**Table 12. Status bits**

| Status bit | Description |
|---|---|
| GFAIL | Logic OR of CAN failure, HS1 failure, V2LOW |
| BATFAIL | Battery fail flag ($V_{SUP}$ < 3.0 V) |
| VDDTEMP | Temperature prewarning on VDD (latched) |
| WDRST | Watchdog reset occurred |

**RCR register**

| RCR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $001b | W | WDSTOP | NOSTOP | | RSTTH |
| | R | | | TXFAILURE | CANWU |
| Reset | | 1 | 0 | | 0 |
| Reset condition | | POR, RESET | POR, NR2N | | POR |

**Table 13. Control bits**

| Status bit | Bit value | Description |
|---|---|---|
| WDSTOP | 0 | No watchdog in stop mode |
| | 1 | Watchdog runs in stop mode |
| NOSTOP | 0 | Stop mode is default low power mode |
| | 1 | Sleep mode is default low power mode |
| RSTTH | 0 | Reset threshold 1 selected (typ. 4.6 V) |
| | 1 | Reset threshold 2 selected (typ. 4.2 V) |
| CANWU | 1 | Wake-rom CAN |
| TXFAILURE | 1 | Tx permanent dominant (CAN) |

**Table 14. CAN register**

| CAN | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $010b | W | FDIS | CEXT | CCTR1 | CCTR0 |
| | R | CS3 | CS2 | CS1 | CS0 |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, CAN | POR, CAN | POR, CAN | POR, CAN |

## 6.3.3 Fault tolerant CAN transceiver standard modes

The CAN transceiver standard mode can be programmed by setting CEXT to 0. The transceiver cell will then be behave as known from the 33889.

**Table 15. CAN transceiver modes**

| CEXT | CCTR1 | CCTR0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Term$V_{BAT}$ |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | RxOnly |
| 0 | 1 | 1 | RxTx |

**Table 16. CAN transceiver extended modes (CAN with CEXT bit =1 is not recommended)**

| CEXT [33] | CCTR1 | CCTR0 | Mode |
|---|---|---|---|
| 1 | 0 | 0 | $TermV_{BAT}$ |
| 1 | 0 | 1 | $TermV_{DD}$ |
| 1 | 1 | 0 | RxOnly |
| 1 | 1 | 1 | RxTx |

Notes

33. CEXT Bit should be set at 0. The CAN operation in extended mode is not recommended.

Fault tolerant CAN transceiver extended modes

By setting CEXT to 1 the transceiver cell supports sub bus communication

| FDIS | L0 Wake Input Filter (20 µs Typical) |
|---|---|
| 0 | Enable (LO wake threshold selectable by WUR register) |
| 1 | Disable (L0 wake-up threshold is low level only, no matter D0 and D1 bits set in WUR register). |

Note: if DFIS bit is set to 1, WUR register must be read before going into sleep or stop mode in order to clear the wake-up flag. During read out L0 must be at high level and should stay high when entering sleep or stop.

**Table 17. Status bits**

| CS3 | CS2 | CS1 | CS0 | Bus failure # | | Description |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | no failure | |
| 0 | 0 | 0 | 1 | 1 | CANH open wire | |
| 0 | 1 | 0 | 1 | 5 | CANH short circuit to | ground |
| 0 | 1 | 1 | 0 | 8, 3a | | VDD |
| 0 | 1 | 1 | 1 | 3 | | VBAT |
| 1 | 0 | 0 | 1 | 2 | CANL open wire | |
| 1 | 1 | 0 | 1 | 4, 7 | CANL short circuit to | ground / CANH |
| 1 | 1 | 1 | 0 | 9 | | VDD |
| 1 | 1 | 1 | 1 | 6 | | VBAT |

Comments:

CS2 bit at 0 = open failure. CS2 bit at 1 = short failure.

(CS3 bit at 0 and (CS1 = 1 or CS2 =1)) = CANH failure. CS3 bit at 1 = CANL failure.

CS1 and CS0 bits: short type failure coding (GND, VDD or VBAT).

In case of multiple failures, the last failure is reported.

**Table 18. IOR register**

| IOR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $011b | W | | HS1ON | GSLR1 | GSLR0 |
| | R | SHIFT | HS1OT | V2LOW | VSUPLOW |
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 19. Control bits**

| HS1ON | HS1 |
|---|---|
| 0 | HS1 switch turn OFF |
| 1 | HS1 switch turn ON |

**Table 20. Gnd shift selection**

| GSLR1 | GSLR0 | Typical GND shift comparator level |
|---|---|---|
| 0 | 0 | -0.3 V |
| 0 | 1 | -0.7 V |
| 1 | 0 | -1.2 V |
| 1 | 1 | -1.7 V |

| Shift | State |
|---|---|
| 0 | Gnd shift value is lower than the level selected by the GSLR1 and GSLR2 bit |
| 1 | Gnd shift value is higher than the level selected by the GSLR1 and GSLR2 bit |

**Table 21. Status bits**

| Status bit | Description |
|---|---|
| HS1OT [34] | High-side 1 overtemperature |
| SHIFT | gnd shift level selected by GSLR1 and GSLR2 bits is reached |
| V2LOW | V2 below 4.0 V typical |
| VSUPLOW | $V_{SUP}$ below 6.1 V typical |

Notes

34. Once the HS1 switch has been turned off because of overtemperature, it can be turned on again by setting the appropriate control bit to “1”.

## 6.3.4 WUR register

The local wake-up inputs L0 and L1 can be used in both normal and standby mode as port expander and for waking up the SBC in sleep or stop mode.

**Table 22. WUR register**

| WUR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $100b | W | LCTR3 | LCTR2 | LCTR1 | LCTR0 |
| | R | L1WUb | L1WUa | L0WUb | L0WUa |
| Reset | | 1 | 1 | 1 | 1 |
| Reset condition | | POR, NR2R, N2R, STB2R, STO2R | | | |

**Control bits**

| LCTR3 | LCTR2 | LCTR1 | LCTR0 | L0 configuration | L1 configuration |
|---|---|---|---|---|---|
| X | X | 0 | 0 | inputs disabled | |
| X | X | 0 | 1 | high level sensitive | |
| X | X | 1 | 0 | low level sensitive | |
| X | X | 1 | 1 | both level sensitive | |
| 0 | 0 | X | X | | inputs disabled |
| 0 | 1 | X | X | | high level sensitive |
| 1 | 0 | X | X | | low level sensitive |
| 1 | 1 | X | X | | both level sensitive |

**Table 23. Status bits**

| L0WUb | L0WUa | FDIS bit in CAN register | Description |
|---|---|---|---|
| 0 | 0 | 0 | No wake-up occurred at L0 (sleep or stop mode). Low level state on L0 (standby or normal mode) |
| 1 | 1 | 0 | Wake-up occurred at L0 (sleep or stop mode). High level state on L0 (standby or normal mode) |
| 0 | 1 | 1 | Wake-up occurred at L0 (sleep or stop mode with L0 filter disable). WUR must be set to xx00 before sleep or stop mode. |

| L1WUb | L1WUa | Description |
|---|---|---|
| 0 | 0 | No wake-up occurred at L1 (sleep or stop mode). Low level state on L1 (standby or normal mode) |
| 1 | 1 | Wake-up occurred at L1 (sleep or stop mode). High level state on L1 (standby or normal mode) |

## 6.3.5 TIM registers

Description: This register is split into 2 sub registers, TIM1 and TIM2.

TIM1 controls the watchdog timing selection as well as the window or timeout option. TIM1 is selected when bit D3 is 0.

TIM2 is used to define the timing for the cyclic sense and forced wake-up function. TIM2 is selected when bit D3 is 1.

No read operation is allowed for registers TIM1 and TIM2

## 6.3.6 TIM register

**Table 24. TIM register**

| TIM1 | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $101b | W | 0 | WDW | WDT1 | WDT0 |
| | R | | | | |
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Watchdog**

| WDW | WDT1 | WDT0 | Watchdog timing [ms] | |
|---|---|---|---|---|
| 0 | 0 | 0 | 10 | no window watchdog |
| 0 | 0 | 1 | 50 | |
| 0 | 1 | 0 | 100 | |
| 0 | 1 | 1 | 350 | |
| 1 | 0 | 0 | 10 | window watchdog enabled (window lenght is half the watchdog timing) |
| 1 | 0 | 1 | 50 | |
| 1 | 1 | 0 | 100 | |
| 1 | 1 | 1 | 350 | |

j

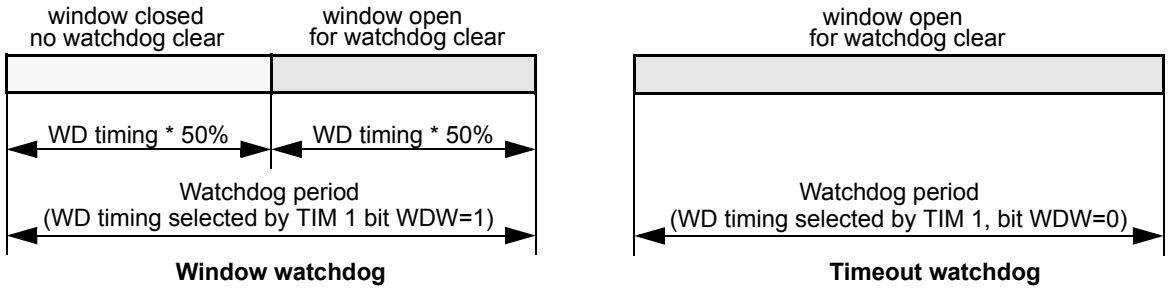



**Figure 22. Watchdog operation (window and timeout)**

## 6.3.7 TIM2 register

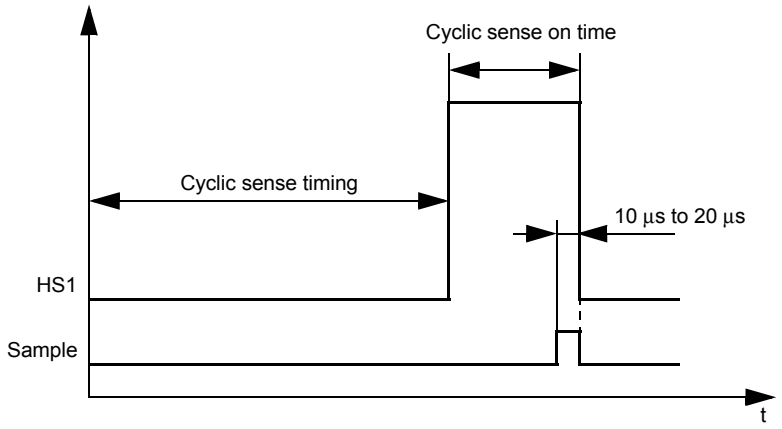
The purpose of TIM2 register is to select an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching on or off HS1

**Table 25. TIM2 register**

| TIM2 | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $101b | W | 1 | CSP2 | CSP1 | CSP0 |
| | R | | | | |
| Reset | | | 0 | 0 | 0 |
| Reset condition | | | POR, RESET | POR, RESET | POR, RESET |

**Table 26. Cyclic sense timing**

| CSP2 | CSP1 | CSP0 | Cyclic sense timing [ms] |
|---|---|---|---|
| 0 | 0 | 0 | 5 |
| 0 | 0 | 1 | 10 |
| 0 | 1 | 0 | 20 |
| 0 | 1 | 1 | 40 |
| 1 | 0 | 0 | 75 |
| 1 | 0 | 1 | 100 |
| 1 | 1 | 0 | 200 |
| 1 | 1 | 1 | 400 |




## 6.3.8 LPC register

Description: This register controls:

- The state of HS1 in Stop and Sleep mode (HS1 permanently off or HS1 cyclic)
- Enable or disable the forced wake-up function (SBC automatic wake-up after time spend in Sleep or Stop mode, time defined by the TIM2 register)
- Enable or disable the sense of the wake-up inputs (LX) at sampling point of the cyclic sense period (LX2HS1 bit).

**Table 27. LPC register**

| LPC | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $110b | W | LX2HS1 | FWU | IDDS | HS1AUTO |
| | R | | | | |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R | POR, NR2R, N2R, STB2R, STO2R |

| LX2HS1 | HS1AUTO | Wake-up inputs supplied by HS1 | Autotiming HS1 |
|---|---|---|---|
| X | 0 | | off |
| X | 1 | | On, HS1 cyclic, period defined in TIM2 register |
| 0 | X | no | |
| 1 | X | Yes, LX inputs sensed at sampling point | |

| Bit | Description |
|---|---|
| FWU | If this bit is set, and the SBC is turned into sleep or stop mode, the SBC wakes up after the time selected in the TIM2 register |
| IDDS | Bit = 0: $I_{DDS-WU1}$ selected (lowest value, typ 3.5 mA)<br>Bit = 1: $I_{DDS-WU2}$ selected (highest value, typ 14 mA) |

**Table 28. INTR register**

| INTR | | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|
| $111b | W | VSUPLOW | HS1OT-V2LOW | VDDTEMP | CANF |
| | R | VSUPLOW | HS1OT | VDDTEMP | CANF |
| Reset | | 0 | 0 | 0 | 0 |
| Reset condition | | POR, RESET | POR, RESET | POR, RESET | POR, RESET |

**Table 29. Control bits**

| Control bit | Description |
|---|---|
| CANF | Mask bit for CAN failures (OR of any CAN failure) |
| VDDTEMP | Mask bit for VDD medium temperature |
| HS1OT-V2LOW | Mask bit for HS1 over temperature OR V2 below 4.0 V |
| VSUPLOW | Mask bit for SUP below 6.1 V |

When the mask bit has been set, $\overline{INT}$ pin goes low if the appropriate condition occurs.

**Table 30. Status bits**

| Status bit | Description |
|---|---|
| CANF | CAN failure |
| VDDTEMP | VDD medium temperature |
| HS1OT | HS1 overtemperature |
| VSUPLOW | $V_{SUP}$ below 6.1 V, typical |

Notes:

If HS1OT-V2LOW interrupt is only selected (only bit D2 set in INTR register), reading INTR register bit D2 leads to two possibilities:

Bit D2 = 1: INT source is HS1OT

Bit D2 = 0: INT source is V2LOW.

Upon a wake-up condition from Stop mode due to overcurrent detection ($I_{DD1S-WU1}$ or $I_{DD1S-WU2}$), an INT pulse is generated. However, the INTR register content remains at 0000 (not bit set into the INTR register).

# 7 Typical applications

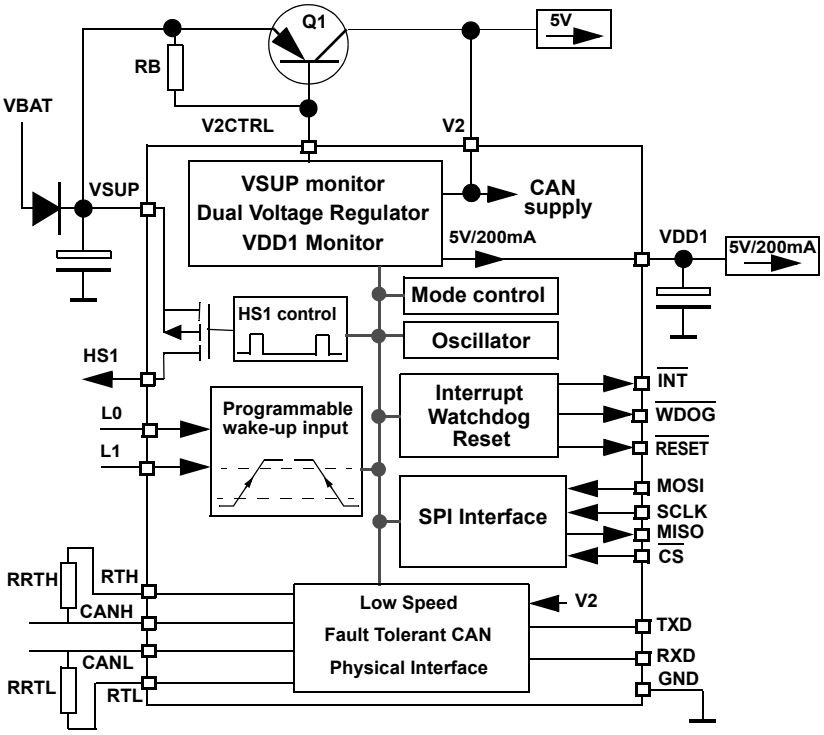



**Figure 23. 33889D/33889B simplified typical application with ballast transistor**

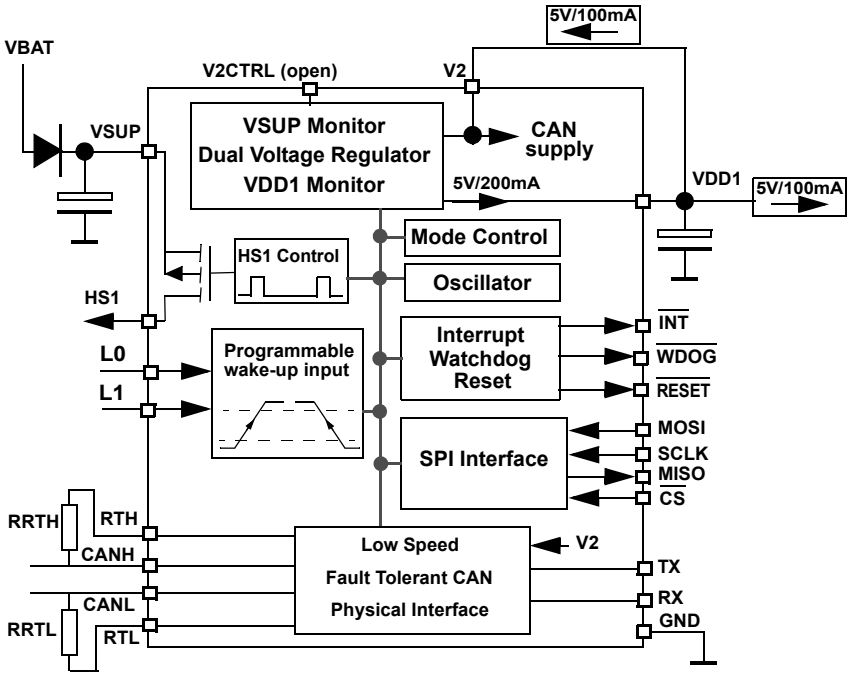
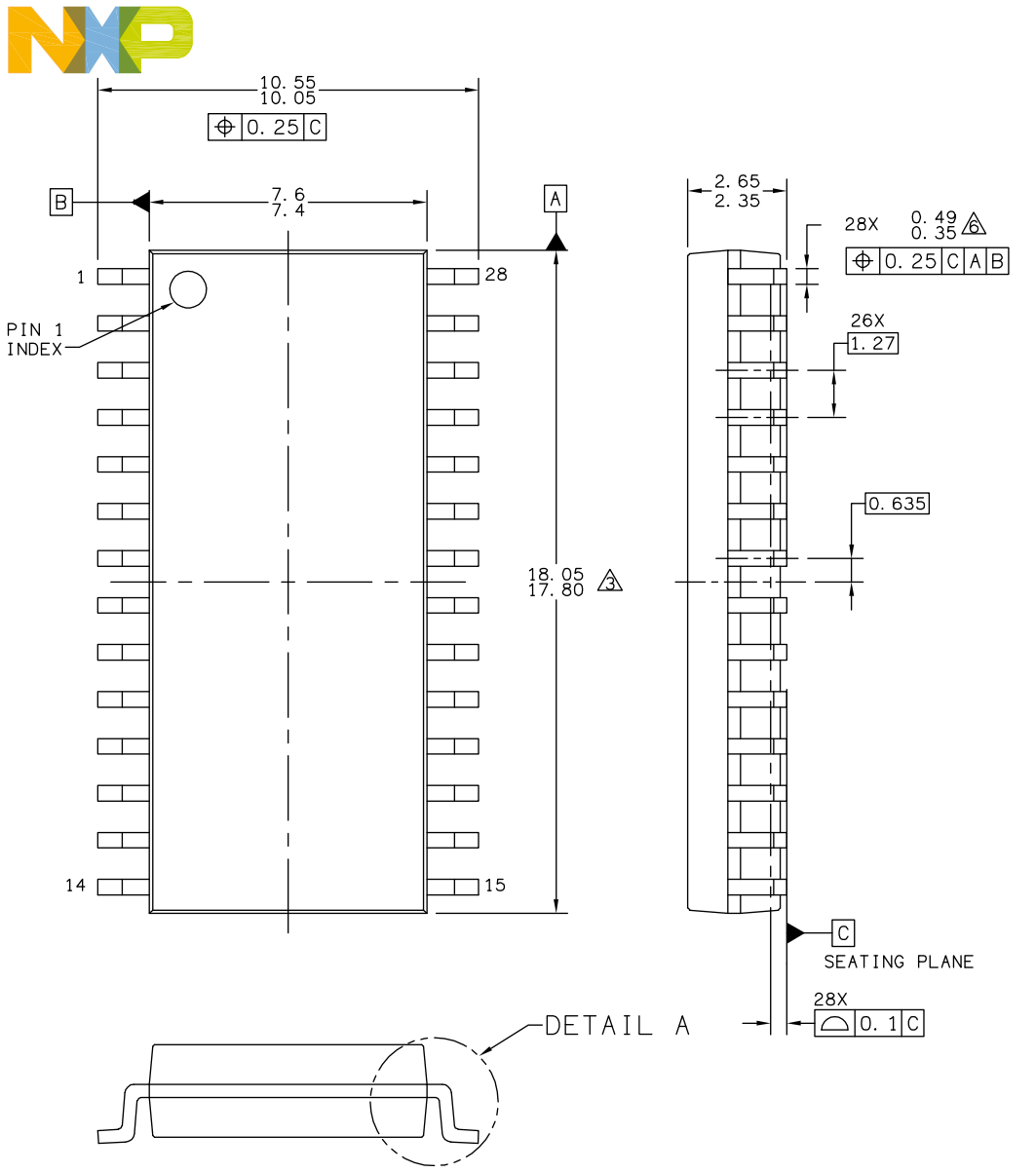



**Figure 24. 33889D/33889B simplified typical application without ballast transistor**

# 8 Packaging

## 8.1 Package dimensions

**Important** For the most current revision of the package, visit www.nxp.com and do a keyword search on the 98ASB42345B number listed below. Dimensions shown are provided for reference ONLY.

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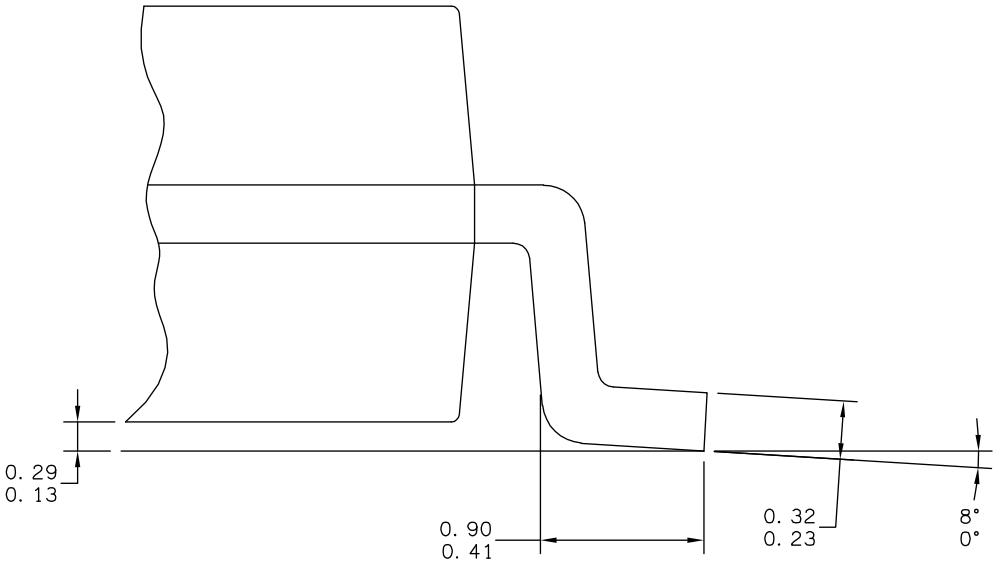
|---|---|---|
| TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | DOCUMENT NO: 98ASB42345B | REV: J |
| | STANDARD: MS-013AE | |
| | SOT136-3 | 11 APR 2016 |

**33889**




DETAIL A

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| TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | DOCUMENT NO: 98ASB42345B | REV: J |
| | STANDARD: MS-013AE | |
| | SOT136-3 | 11 APR 2016 |

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05
5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | DOCUMENT NO: 98ASB42345B REV: J |
|---|---|
| | STANDARD: MS–013AE |
| | SOT136–3 11 APR 2016 |

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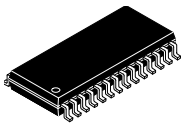
# 9 Additional documentation

## 9.1 Thermal addendum (rev 2.0)

**33889EG**

**28-PIN**
**SOICW**



**EG SUFFIX (PB-FREE)**
**98ASB42345**
**28-PIN SOICW**

**NOTE FOR PACKAGE DIMENSIONS, REFER TO THE 33889 DEVICE DATASHEET.**

### Introduction

This thermal addendum is provided as a supplement to the MC33889 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

### Packaging and thermal considerations

The MC33889 is offered in a 28 pin SOICW, single die package. There is a single heat source (P), a single junction temperature ($T_J$), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [ R_{\theta JA} ] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

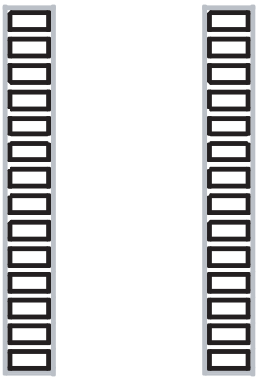
### Standards

**Table 31. Thermal performance comparison**

| Thermal Resistance | [°C/W] |
|---|---|
| $P_{\theta JA}$ (1) (2) | 42 |
| $P_{\theta JB}$ (2) (3) | 11 |
| $P_{\theta JA}$ (1) (4) | 69 |
| $P_{\theta \vartheta X}$ (5) | 23 |

Notes

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3.
5. Thermal resistance between the die junction and the package top surface; cold plate attached to the package top surface and remaining surfaces insulated.



20 Terminal SOICW
1.27 mm Pitch
18.0 mm x 7.5 mm Body

**Figure 25. Surface mount for SOIC wide body non-exposed pad**

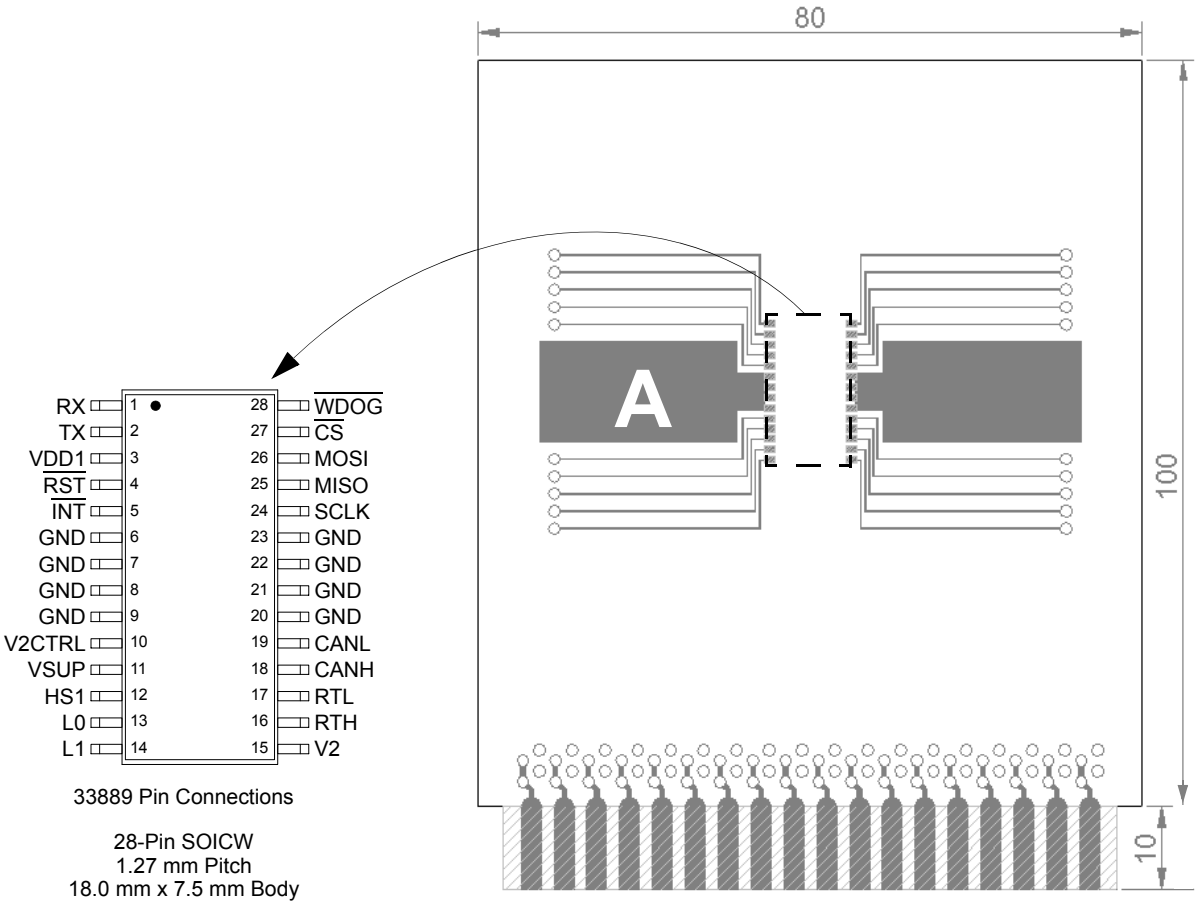



**Figure 26. Thermal** test b**oard**

**Device on thermal test board**

| | |
|---|---|
| Material: | Single layer printed circuit board<br>FR4, 1.6 mm thickness<br>Cu traces, 0.07 mm thickness |
| Outline: | 80 mm x 100 mm board area, including edge connector for thermal testing |
| Area **A**: | Cu heat-spreading areas on board surface |
| Ambient Conditions: | Natural convection, still air |

**Table 32. Thermal resistance performance**

| Thermal resistance | Area A ($mm^2$) | (°C/W) |
|---|---|---|
| $R_{\theta JA}$ | 0 | 69 |
| | 300 | 53 |
| | 600 | 48 |

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

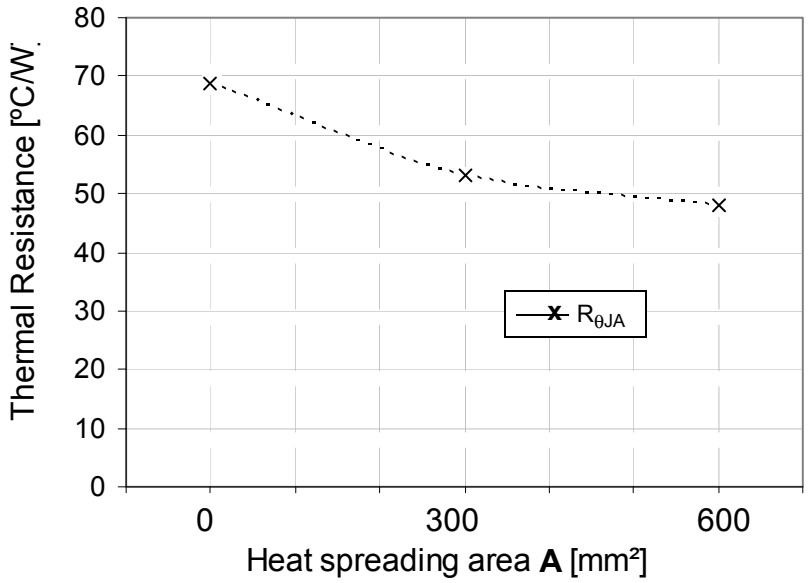



**Figure 27. Device on thermal test board $R_{\theta JA}$**

33889

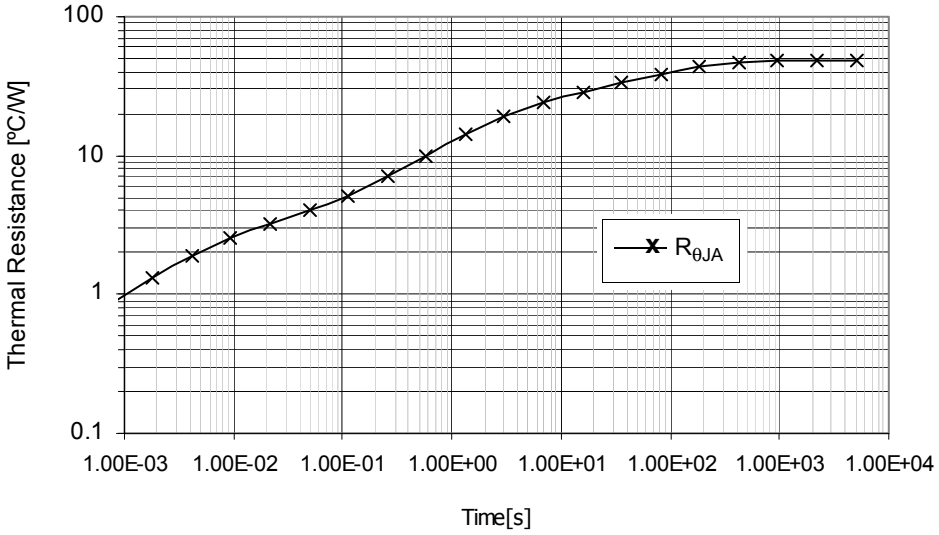



**Figure 28. Transient pin resistance $R_{\theta JA}$ device on thermal test board area A = 600 ($mm^2$)**

# 10 Revision history

| Revision | Date | Description of changes |
|---|---|---|
| 7.0 | 5/2006 | • Implemented Revision History page<br>• Added “EG” PB-Free package type<br>• Removed MC33889DW version, and added MC33889B and MC33889D versions<br>• Converted to the Freescale format, and updated to the prevailing form and style<br>• Modified Device variations between the 33889D and 33889B versions (1) on page 2<br>• Added Thermal addendum (rev 2.0) on page 51<br>• Changed the Maximum Ratings on page 6 to the standard format<br>• Added CAN transceiver description section |
| 8.0 | 6/2002 | • Corrected two instances where pin LO had an overline, and one instance where pin WDOG did not. |
| 9.0 | 8/2006 | • Removed MC33889BEG/R2 and MC33889DEG/R2 and replaced them with MCZ33889BEG/R2 and MCZ33889DEG/R2 in the ordering Information table |
| 10.0 | 9/2006 | • Replaced the label Logic Inputs with Logic Signals (RX, TX, MOSI, MISO, CS, SCLK, RST, WDOG, INT) on page 5<br>• Changed CS to $\overline{CS}$ at various places in the document |
| 11.0 | 12/2006 | • Made changes to Supply Current in Stand-by Mode on page 7 and Supply Current in Normal Mode on page 7 |
| 12.0 | 3/2007 | • Added the EG suffix to the included thermal addendum |
| 13.0 | 12/2012 | • Updated orderable part number from MCZ33889BEG to MC33889BPEG<br>• Updated orderable part number from MCZ33889DEG to MC33889DPEG<br>• Removed all DW part ordering information and documentation<br>• Updated format |
| 14.0 | 6/2013 | • Added a For SPI Operation on page 38<br>• Updated document properties |
| 15.0 | 6/2015 | • Added note (17) |
| | 8/2016 | • Updated to NXP document form and style |

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Document Number: MC33889
Rev. 15.0
8/2016

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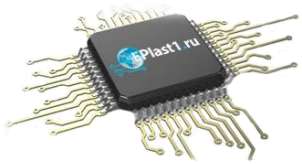


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