

Data Sheet

September 2011

Features

Internal control latches and address decoder

Short setup and hold times

Wide operating voltage: 4.5 V to 13.2 V

12 Vpp analog signal capability

• R_{ON} 65 Ω max. @ V_{DD} = 12 V, 25°C

• $\Delta R_{ON} \le 10 \Omega @ V_{DD} = 12 V, 25C$

· Full CMOS switch for low distortion

· Minimum feedthrough and crosstalk

Low power consumption ISO-CMOS technology

Internal pull-up resistor for RESET pin

Applications

- Key systems
- · PBX systems
- Mobile radio
- Test equipment/instrumentation
- · Analog/digital multiplexers
- · Audio/Video switching

Ordering Information

MT8809AP1 28 Pin PLCC* Tubes
MT8809APR1 28 Pin PLCC* Tape & Reel
MT8809AE1 28 Pin PDIP* Tubes

* Pb Free Matte Tin -40°C to +85°C

Description

The Zarlink MT8809 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

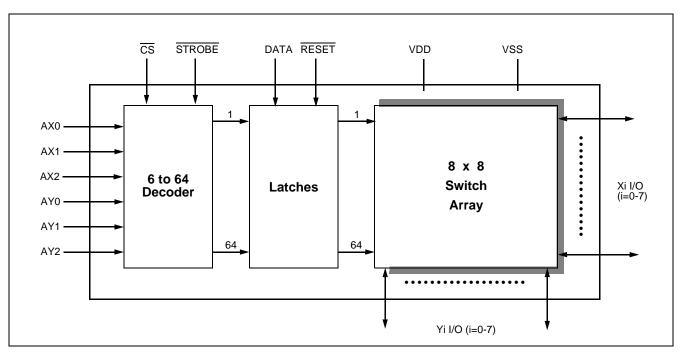


Figure 1 - Functional Block Diagram

Change Summary

Changes from the September 2005 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

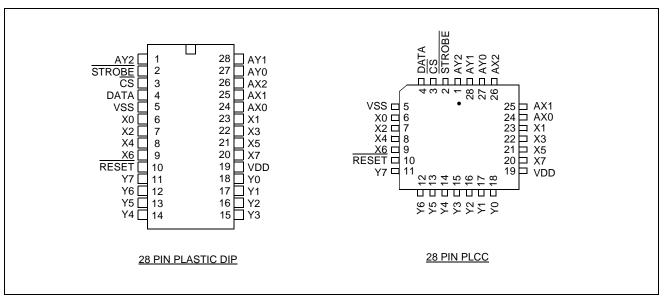


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	AY2	AY2 Address Line (Input).
2	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes low and DATA must be stable on the rising edge of STROBE. Active Low.
3	CS	Chip Select (Input): this is used to select the device. Active Low.
4	DATA	DATA (Input) : a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	V _{SS}	Ground Reference.
6-9	X0, X2, X4, X6	X0, X2, X4 and X6 Analog (Inputs/Outputs): these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	RESET	<u>Master RESET (Input)</u> : this is used to turn off all switches regardless of the condition of CS. A 100 kΩ internal pull-up resistor is also provided. This can be used in conjunction with a 0.1 μF capacitor (connected to the RESET pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	Y7 - Y0 Analog (Inputs/Outputs): these are connected to the Y0 - Y7 columns of the switch array.

Pin Description

Pin #	Name	Description
19	V_{DD}	Positive Power Supply.
20-23		X7, X5, X3 and X1 Analog (Inputs/Outputs): these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	AX0 - AX2 Address Lines (Inputs).
27, 28	AY0, AY1	AY0 and AY1 Address Lines (Inputs).

Functional Description

The MT8809 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the \overline{CS} (Chip Select) and \overline{STROBE} inputs are low and are latched on the rising edge of \overline{STROBE} . A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "0" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether \overline{CS} is high or low.

Address Decode

The six address inputs along with the \$\overline{STROBE}\$ and \$\overline{CS}\$ (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, \$\overline{RESET}\$ must be high and \$\overline{CS}\$ must go low while the address and data are set up. Then the \$\overline{STROBE}\$ input is set low and then high causing the data to be latched. The data can be changed while \$\overline{STROBE}\$ is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of \$\overline{STROBE}\$ in order for correct data to be written to the latch.

$\textbf{Absolute Maximum Ratings*-} \ \textit{Voltages are with respect to V}_{SS} \ \textit{unless otherwise stated}.$

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V _{DD} V _{SS}	-0.3 -0.3	15.0 V _{DD} +0.3	V V
2	Analog Input Voltage	V _{INA}	-0.3	V _{DD} +0.3	V
3	Digital Input Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V
4	Current on any I/O Pin	ļ		±15	mA
5	Storage Temperature	T _S	-65	+150	°C
6	Package Power Dissipation PLASTIC DIP	P _D		0.6	W

^{*} Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym.	Min.	Тур.	Max.	Units	Test Conditions
1	Operating Temperature	T _O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V _{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics † - Voltages are with respect to $V_{SS} = 0 \text{ V}$, $V_{DD} = 12 \text{ V}$ unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Quiescent Supply Current	I _{DD}		1	100	μА	All digital inputs at V _{IN} = V _{SS} V _{DD} except RESET = V _{DD} .
				120	400	μΑ	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} except RESET = V_{SS} .
				0.5	1.6	mA	All digital inputs at $V_{IN} = 2.4 \text{ V}$, $V_{DD} = 5.0 \text{ V}$
				5	15	mA	All digital inputs at V _{IN} = 3.4 V
2	Off-state Leakage Current (See G.9 in Appendix)	l _{OFF}		±1	±500	nA	$IV_{Xi} - V_{Yj}I = V_{DD} - V_{SS}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V _{IH}	3.0			V	
6	Input Leakage (digital pins)	I _{LEAK}		0.1	10	μΑ	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} ; RESET = V_{DD}

[†] DC Electrical Characteristics are over recommended temperature range. ‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym.	25	5°C	70	°C	85°C		85°C		Units	Test Conditions
			Тур.	Max.	Тур.	Max.	Тур.	Max.				
1	On-state V_{DD} =12 V Resistance V_{DD} =10V V_{DD} = 5V (See G.1, G.2, G.3 in Appendix)	R _{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS} = 0 \text{ V,V}_{DC} = V_{DD}/2,$ IV_{Xi} - $V_{Yj}I = 0.4 \text{ V}$ See Appendix, Fig. A.2		
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR _O N	5	10		10		10	Ω	$\begin{aligned} &V_{DD} = 12 \text{ V, } V_{SS} = 0, \\ &V_{DC} = V_{DD}/2, \\ &IV_{Xi^-}V_{Yj}I = 0.4 \text{ V} \\ &\text{See Appendix, Fig. A.2} \end{aligned}$		

AC Electrical Characteristics † - Crosspoint Performance- V_{DC} is the external DC offset at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Switch I/O Capacitance	Cs		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C _F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V _{OUT} /V _{Xi})=-3 dB	F _{3dB}		45		MHz	Switch is "ON"; $V_{INA} = 2 \text{ Vpp}$ sinewave; $R_L = 1 \text{ k}\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA} = 2 \text{ Vpp}$ sinewave f = 1 kHz; $R_L = 1 \text{ k}\Omega$
5	Feedthrough Channel "OFF" Feed.=20LOG (V _{OUT} /V _{Xi}) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sinewave f = 1 kHz; R_L = 1 k Ω . See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and	X _{talk}		-45		dB	V_{INA} = 2Vpp sinewave f = 10 MHz; R_L = 75 Ω
	Xj-Yj. Xtalk=20LOG (V _{Yi} /V _{Xi}).			-90		dB	V_{INA} = 2Vpp sinewave f = 10kHz; R _L = 600 Ω .
	(See G.7 in Appendix).			-85		dB	V_{INA} =2Vpp sinewave f = 10 kHz; R _L = 1 kΩ.
				-80		dB	V_{INA} = 2Vpp sinewave f = 1 kHz; R _L = 10 kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t _{PS}			30	ns	$R_L = 1 \text{ k}\Omega; C_L = 50 \text{ pF}$

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

AC Electrical Characteristics † - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions		
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX _{talk}		30		mVpp	V_{IN} =3V+ V_{DC} squarewave; R_{IN} =1 k Ω , R_{L} =1 k Ω . See Appendix, Fig. A.6		
2	Digital Input Capacitance	C _{DI}		10		pF	f = 1 MHz		
3	Switching Frequency	F _O			20	MHz			
4	Setup Time DATA to STROBE	t _{DS}	10			ns	R_L = 1 kΩ, C_L = 50 pF ; Å		
5	Hold Time DATA to STROBE	t _{DH}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$		
6	Setup Time Address to STROBE	t _{AS}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$		
7	Hold Time Address to STROBE	t _{AH}	10			ns	R_L = 1 kΩ, C_L = 50 pF Å;		
8	Setup Time CS to STROBE	t _{CSS}	10			ns	R_L = 1 kΩ, C_L = 50 pF Å;		
9	Hold Time CS to STROBE	t _{CSH}	10			ns	R_L = 1 kΩ, C_L = 50 pF \dot{c} Å		
10	STROBE Pulse Width	t _{SPW}	20			ns	R_L = 1 kΩ, C_L = 50 pF \dot{c} Å		
11	RESET Pulse Width	t _{RPW}	40			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$		
12	STROBE to Switch Status Delay	t _S		40	100	ns	R_L = 1 kΩ, C_L =50 pF Å;		
13	DATA to Switch Status Delay	t _D		50	100	ns	R_L = 1 kΩ, C_L = 50 pF Å;		
14	RESET to Switch Status Delay	t _R		35	100	ns	R_L = 1 kΩ, C_L = 50 pF ¿Å		

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details. Digital Input rise time (tr) and fall time (tf) = 5 ns. ‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing. ſRefer to Appendix, Fig. A.7 for test circuit.

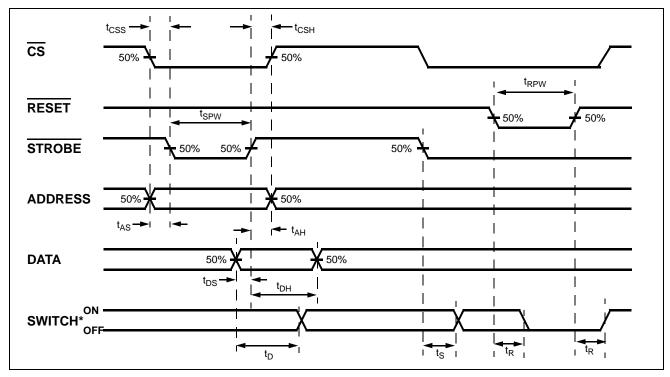


Figure 3 - Control Memory Timing Diagram

^{*} See Appendix, Fig. A.7 for switching waveform

AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 1 0 1	X0 Y0 X1 Y0 X2 Y0 X3 Y0	1 1 1	0 0 0	0 0 0	0 0 0 0	0 0 1 1	0 1 0 1	X0 Y4 X1 Y4 X2 Y4 X3 Y4
0 0 0	0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	X4 Y0 X5 Y0 X6 Y0 X7 Y0	1 1 1 1	0 0 0	0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	X4 Y4 X5 Y4 X6 Y4 X7 Y4
0 0 0	0 0 0	1 1 1	0 0 0	0 0 1	0 1 0	X0 Y1 X1 Y1 X2 Y1	1 1 1	0 0 0	1 1 1	0 0 0	0 0 1	0 1 0	X0 Y5 X1 Y5 X2 Y5
0 0 0	0 0 0	1 1 1 1	0 1 1 1	1 0 0 1	1 0 1 0	X3 Y1 X4 Y1 X5 Y1 X6 Y1	1 1 1 1	0 0 0	1 1 1	0 1 1 1	1 0 0 1	1 0 1 0	X3 Y5 X4 Y5 X5 Y5 X6 Y5
0	0 1 1	0 0	0 0	0 0	0	X7 Y1 X0 Y2 X1 Y2	1 1 1	0 1 1	0 0	0 0	0 0	0	X7 Y5 X0 Y6 X1 Y6
0 0 0 0	1 1 1	0 0 0	0 0 0 1	1 1 0	0 1 0	X2 Y2 X3 Y2 X4 Y2	1 1 1	1 1 1	0 0 0	0 0 0 1	1 1 0	0 1 0	X2 Y6 X3 Y6 X4 Y6
0 0 0	1 1 1	0 0 0	1 1 1	0 1 1	1 0 1	X5 Y2 X6 Y2 X7 Y2	1 1 1	1 1 1	0 0 0	1 1 1	0 1 1	1 0 1	X5 Y6 X6 Y6 X7 Y6
0 0 0	1 1 1	1 1 1	0 0 0	0 0 1	0 1 0	X0 Y3 X1 Y3 X2 Y3	1 1 1	1 1 1	1 1 1	0 0 0	0 0 1	0 1 0	X0 Y7 X1 Y7 X2 Y7
0 0 0	1 1 1 1	1 1 1 1	0 1 1 1	1 0 0 1	1 0 1 0	X3 Y3 X4 Y3 X5 Y3 X6 Y3	1 1 1 1	1 1 1 1	1 1 1 1	0 1 1 1	1 0 0 1	1 0 1 0	X3 Y7 X4 Y7 X5 Y7 X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table



Data Sheet

September 2005

Features

- Internal control latches and address decoder
- Short setup and hold times
- Wide operating voltage: 4.5 V to 13.2 V
- 12 Vpp analog signal capability
- R_{ON} 65 Ω max. @ V_{DD} = 12 V, 25°C
- $\Delta R_{ON} \le 10 \ \Omega$ @ $V_{DD} = 12 \ V$, 25C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology
- Internal pull-up resistor for RESET pin

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

MT8809AE 28 Pin PDIP Tubes 28 Pin PLCC Tubes MT8809AP MT8809APR 28 Pin PLCC Tape & Reel MT8809AP1 28 Pin PLCC* Tubes 28 Pin PLCC* MT8809APR1 Tape & Reel 28 Pin PDIP* MT8809AE1 Tubes

> * Pb Free Matte Tin -40°C to +85°C

Description

ISO-CMOS

The Zarlink MT8809 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

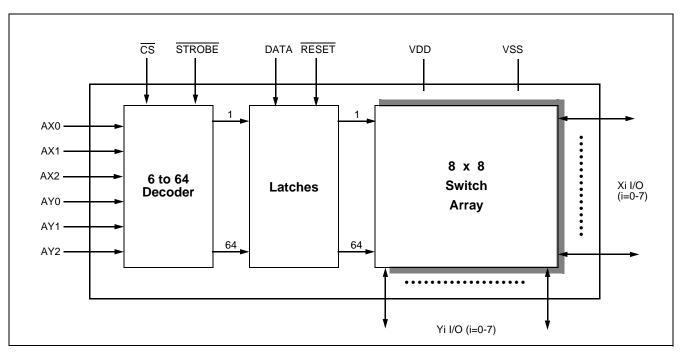


Figure 1 - Functional Block Diagram

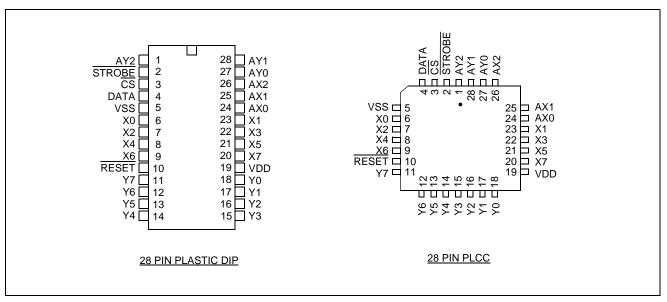


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	AY2	AY2 Address Line (Input).
2	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes low and DATA must be stable on the rising edge of STROBE. Active Low.
3	CS	Chip Select (Input): this is used to select the device. Active Low.
4	DATA	DATA (Input) : a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	V _{SS}	Ground Reference.
6-9	X0, X2, X4, X6	X0, X2, X4 and X6 Analog (Inputs/Outputs): these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	RESET	<u>Ma</u> ster RESET (Input): this is used to turn off all switches regardless of the condition of \overline{CS} . A 100 kΩ internal pull-up resistor is also provided. This can be used in conjunction with a 0.1 μF capacitor (connected to the RESET pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	Y7 - Y0 Analog (Inputs/Outputs): these are connected to the Y0 - Y7 columns of the switch array.
19	V _{DD}	Positive Power Supply.
20-23	X7, X5, X3, X1	X7, X5, X3 and X1 Analog (Inputs/Outputs): these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	AX0 - AX2 Address Lines (Inputs).
27, 28	AY0, AY1	AY0 and AY1 Address Lines (Inputs).

Functional Description

The MT8809 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the \overline{CS} (Chip Select) and \overline{STROBE} inputs are low and are latched on the rising edge of \overline{STROBE} . A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "0" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether \overline{CS} is high or low.

Address Decode

The six address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be high and CS must go low while the address and data are set up. Then the STROBE input is set low and then high causing the data to be latched. The data can be changed while STROBE is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of STROBE in order for correct data to be written to the latch.

$\textbf{Absolute Maximum Ratings*-} \ \textit{Voltages are with respect to V}_{SS} \ \textit{unless otherwise stated}.$

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD} V_{SS}	-0.3 -0.3	15.0 V _{DD} +0.3	V V
2	Analog Input Voltage	V _{INA}	-0.3	V _{DD} +0.3	V
3	Digital Input Voltage	V _{IN}	V _{SS} -0.3	V _{DD} +0.3	V
4	Current on any I/O Pin	I		±15	mA
5	Storage Temperature	T _S	-65	+150	°C
6	Package Power Dissipation PLASTIC DIP	P_{D}		0.6	W

^{*} Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

$\textbf{Recommended Operating Conditions} \text{ - Voltages are with respect to V}_{SS} \text{ unless otherwise stated}.$

	Characteristics	Sym.	Min.	Тур.	Max.	Units	Test Conditions
1	Operating Temperature	T _O	-40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V _{IN}	V _{SS}		V _{DD}	V	

DC Electrical Characteristics[†]- Voltages are with respect to $V_{SS} = 0 \text{ V}$, $V_{DD} = 12 \text{ V}$ unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Quiescent Supply Current	I _{DD}		1	100	μΑ	All digital inputs at $V_{IN} = V_{SS}$ V_{DD} except RESET = V_{DD} .
				120	400	μΑ	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} except RESET = V_{SS} .
				0.5	1.6	mA	All digital inputs at V_{IN} = 2.4 V, V_{DD} = 5.0 V
				5	15	mA	All digital inputs at V _{IN} = 3.4 V
2	Off-state Leakage Current (See G.9 in Appendix)	I _{OFF}		±1	±500	nA	$IV_{Xi} - V_{Yj}I = V_{DD} - V_{SS}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V _{IL}			0.8	V	
4	Input Logic "1" level	V _{IH}	3.0			V	
6	Input Leakage (digital pins)	I _{LEAK}		0.1	10	μΑ	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} ; RESET = V_{DD}

[†] DC Electrical Characteristics are over recommended temperature range.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

$\textbf{DC Electrical Characteristics-Switch Resistance} \text{ -} V_{DC} \text{ is the external DC offset applied at the analog I/O pins.}$

	Characteristics	Sym.	25	5°C	70	°C	85°C		Units	Test Conditions
			Тур.	Max.	Тур.	Max.	Тур.	Max.		
1	On-state V_{DD} =12 V Resistance V_{DD} =10V V_{DD} = 5V (See G.1, G.2, G.3 in Appendix)	R _{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS} = 0 \text{ V,V}_{DC} = V_{DD}/2,$ $IV_{Xi}-V_{Yj}I = 0.4 \text{ V}$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR _O N	5	10		10		10	Ω	$\begin{split} &V_{DD}=12~\text{V},~V_{SS}=0,\\ &V_{DC}=V_{DD}/2,\\ &IV_{Xi^{-}}V_{Yj}I=0.4~\text{V}\\ &\text{See Appendix, Fig. A.2} \end{split}$

AC Electrical Characteristics † - Crosspoint Performance- V_{DC} is the external DC offset at the analog I/O pins. Voltages are with respect to $V_{DD} = 5$ V, $V_{DC} = 0$ V, $V_{SS} = -7$ V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Switch I/O Capacitance	C _S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C _F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V _{OUT} /V _{Xi})=-3 dB	F _{3dB}		45		MHz	Switch is "ON"; $V_{INA} = 2 \text{ Vpp}$ sinewave; $R_L = 1 \text{ k}\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA} = 2 \text{ Vpp}$ sinewave f = 1 kHz; $R_L = 1 \text{ k}\Omega$
5	Feedthrough Channel "OFF" Feed.=20LOG (V _{OUT} /V _{Xi}) (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA} = 2Vpp sinewave f = 1 kHz; R_L = 1 k Ω . See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and	X _{talk}		-45		dB	V_{INA} = 2Vpp sinewave f = 10 MHz; R _L = 75 Ω.
	Xj-Yj. Xtalk=20LOG (V _{Yi} /V _{Xi}).			-90		dB	V_{INA} = 2Vpp sinewave f = 10kHz; R _L = 600 Ω.
	(See G.7 in Appendix).			-85		dB	V_{INA} =2Vpp sinewave f = 10 kHz; R _L = 1 kΩ.
				-80		dB	V_{INA} = 2Vpp sinewave f = 1 kHz; R _L = 10 kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t _{PS}			30	ns	$R_L = 1 \text{ k}\Omega; C_L = 50 \text{ pF}$

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

AC Electrical Characteristics † - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to V_{DD} = 5 V, V_{DC} = 0 V, V_{SS} = -7 V, unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX _{talk}		30		mVpp	V_{IN} =3V+ V_{DC} squarewave; R_{IN} =1 k Ω , R_{L} =1 k Ω . See Appendix, Fig. A.6
2	Digital Input Capacitance	C _{DI}		10		pF	f = 1 MHz
3	Switching Frequency	F _O			20	MHz	
4	Setup Time DATA to STROBE	t _{DS}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF}$; Å
5	Hold Time DATA to STROBE	t _{DH}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$
6	Setup Time Address to STROBE	t _{AS}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$
7	Hold Time Address to STROBE	t _{AH}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}_{\dot{c}}$
8	Setup Time CS to STROBE	t _{CSS}	10			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}_{\dot{c}}$
9	Hold Time CS to STROBE	t _{CSH}	10			ns	R_L = 1 kΩ, C_L = 50 pF ¿Å
10	STROBE Pulse Width	t _{SPW}	20			ns	R_L = 1 kΩ, C_L = 50 pF ¿Å
11	RESET Pulse Width	t _{RPW}	40			ns	$R_L = 1 \text{ k}\Omega$, $C_L = 50 \text{ pF Å}$
12	STROBE to Switch Status Delay	t _S		40	100	ns	R_L = 1 kΩ, C_L =50 pF Å;
13	DATA to Switch Status Delay	t _D		50	100	ns	R_L = 1 kΩ, C_L = 50 pF Å;
14	RESET to Switch Status Delay	t _R		35	100	ns	R_L = 1 kΩ, C_L = 50 pF ¿Å

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details. Digital Input rise time (tr) and fall time (tf) = 5 ns. ‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing. Å¿Refer to Appendix, Fig. A.7 for test circuit.

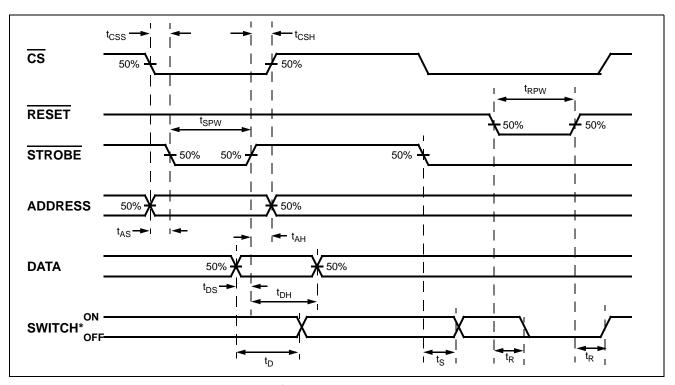
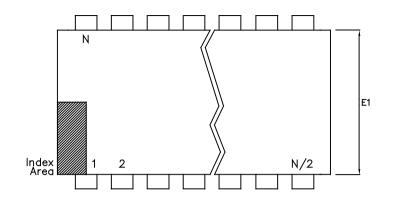


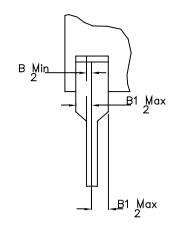
Figure 3 - Control Memory Timing Diagram

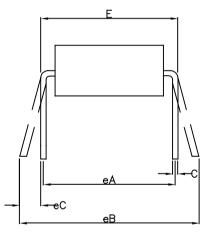
^{*} See Appendix, Fig. A.7 for switching waveform

AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0	0	0	0	0	0	X0 Y0	1	0	0	0	0	0	X0 Y4
0	0	0	0	0	1	X1 Y0	1	0	0	0	0	1	X1 Y4
0	0	0	0	1	0	X2 Y0	1	0	0	0	1	0	X2 Y4
0	0	0	0	1	1	X3 Y0	1	0	0	0	1	1	X3 Y4
0	0	0	1	0	0	X4 Y0	1	0	0	1	0	0	X4 Y4
0	0	0	1	0	1	X5 Y0	1	0	0	1	0	1	X5 Y4
0	0	0	1	1	0	X6 Y0	1	0	0	1	1	0	X6 Y4
0	0	0	1	1	1	X7 Y0	1	0	0	1	1	1	X7 Y4
0	0	1	0	0	0	X0 Y1	1	0	1	0	0	0	X0 Y5
0	0	1	0	0	1	X1 Y1	1	0	1	0	0	1	X1 Y5
0	0	1	0	1	0	X2 Y1	1	0	1	0	1	0	X2 Y5
0	0	1	0	1	1	X3 Y1	1	0	1	0	1	1	X3 Y5
0	0	1	1	0	0	X4 Y1	1	0	1	1	0	0	X4 Y5
0	0	1	1	0	1	X5 Y1	1	0	1	1	0	1	X5 Y5
0	0	1	1	1	0	X6 Y1	1	0	1	1	1	0	X6 Y5
0	0	1	1	1	1	X7 Y1	1	0	1	1	1	1	X7 Y5
0	1	0	0	0	0	X0 Y2	1	1	0	0	0	0	X0 Y6
0	1	0	0	0	1	X1 Y2	1	1	0	0	0	1	X1 Y6
0	1	0	0	1	0	X2 Y2	1	1	0	0	1	0	X2 Y6
0	1	0	0	1	1	X3 Y2	1	1	0	0	1	1	X3 Y6
0	1	0	1	0	0	X4 Y2	1	1	0	1	0	0	X4 Y6
0	1	0	1	0	1	X5 Y2	1	1	0	1	0	1	X5 Y6
0	1	0	1	1	0	X6 Y2	1	1	0	1	1	0	X6 Y6
0	1	0	1	1	1	X7 Y2	1	1	0	1	1	1	X7 Y6
0	1	1	0	0	0	X0 Y3	1	1	1	0	0	0	X0 Y7
0	1	1	0	0	1	X1 Y3	1	1	1	0	0	1	X1 Y7
0	1	1	0	1	0	X2 Y3	1	1	1	0	1	0	X2 Y7
0	1	1	0	1	1	X3 Y3	1	1	1	0	1	1	X3 Y7
0	1	1	1	0	0	X4 Y3	1	1	1	1	0	0	X4 Y7
0	1	1	1	0	1	X5 Y3	1	1	1	1	0	1	X5 Y7
0	1	1	1	1	0	X6 Y3	1	1	1	1	1	0	X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table







	Min	Max	Min	Max				
	mm	mm	<u>Inches</u>	<u>Inches</u>				
Α		6.35		0.250				
A1	0.38		0.015					
A2	3.18	4.95	0.125	0.195				
В	0.36	0.56	0.014	0.022				
B1	0.76	1.78	0.030	0.070				
С	0.20	0.38	0.008	0.015				
D	35.05	39.75	1.380	1.565				
D1	0.13		0.005					
E	15.24	15.88	0.600	0.625				
E1	12.32	14.73	0.485	0.580				
е	2.54	BSC	0.100	BSC				
eА	15.24	BSC	0.600) BSC				
eВ		17.78		0.700				
L	2.92	5.08	0.115	0.200				
N	2	8	28					
Confo	Conforms to Jedec MS-011AB ISS.B							

Notes:

Base Plane Seating Plane

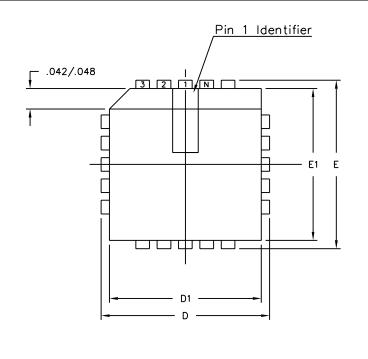
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

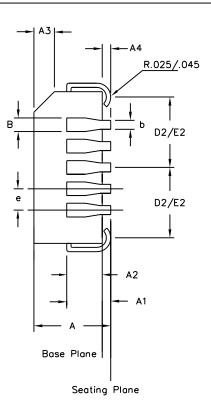
[A1

© Zarlink Semiconductor 2005. All rights reserved.									
ISSUE	3	4							
ACN	7010	213102	CDCA						
DATE	20Apr95	25Nov97	15Jul02	02Dec05					
APPRD.									



		Package Code DA
· ·	Previous package codes	Package Outline for 28 lead 600mils PDIP
		GPD00072





	Control Di	imensions	Altern. Dimensions				
Symbol	in inc	hes	in milli	metres			
	MIN	MAX	MIN	MAX			
Α	0.165	0.180	4.19	4.57			
A1	0.090	0.120	2.29	3.05			
A2	0.062	0.083	1.57	2.11			
А3	0.042	0.056	1.07	1.42			
A4	0.020	_	0.51	-			
D	0.485	0.495	12.32	12.57			
D1	0.450	0.456	11.43	11.58			
D2	0.191	0.219	4.85	5.56			
E	0.485	0.495	12.32	12.57			
E1	0.450	0.456	11.43	11.58			
E2	0.191	0.219	4.85	5.56			
В	0.026	0.032	0.66	0.81			
b	0.013	0.021	0.33	0.53			
е	0.050	BSC	1.27	BSC			
		Pin fed	atures				
ND	7						
NE	7						
N	28						
Note	ote Square						
Confor	ms to J	EDEC MS	-018AB	Iss. A			

Notes:

- 1. All dimensions and tolerances conform to ANSI Y14.5M-1982
- 2. Dimensions D1 and E1 do not include mould protrusions.
 Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
- 3. Controlling dimensions in Inches.
- 4. "N" is the number of terminals.
- 5. Not To Scale
- 6. Dimension R required for 120° minimum bend.

© Zarlink S	Semiconducto	2002 All right	s reserved.			Package Code () A
ISSUE	1	2	3		Previous package codes	Package Outline for
ACN	5958	207469	212422	ZARLINK SEMICONDUCTOR	HP / P	28 Tead PLCC
DATE	15Aug94	10Sep99	22Mar02	SEMICONDUCTOR	,	
APPRD.						GPD00002



For more information about all Zarlink products visit our Web Site at www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов:
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001:
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: <u>org@eplast1.ru</u>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина,

дом 2, корпус 4, литера А.