

CBTU04082

1.8 V, wide bandwidth, 4 differential channel,
2 : 1 multiplexer/demultiplexer switch with single enable

Rev. 2 — 13 July 2010

Product data sheet

1. General description

CBTU04082 is an 8-to-4 differential channel multiplexer/ demultiplexer switch. The CBTU04082 can switch four differential signals to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimizes the channel-to-channel skew as well as channel-to-channel crosstalk, as required by the high-speed serial interface.

2. Features and benefits

- 4 differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching; 5.0 Gbit/s
- Low intra-pair skew: 10 ps maximum (between positive and negative bits)
- Low crosstalk: -23 dB at 3 GHz
- Low off-state isolation: -23 dB at 3 GHz
- V_{DD} operating range: 1.8 V \pm 10 %
- ESD tolerance:
 - ◆ 6 kV HBM
 - ◆ 1 kV CDM
- Low inter-pair skew: 35 ps maximum
- Fit, form and function compatible to PI2PCIE2412
- HVQFN42 package

3. Applications

- Routing of high-speed differential signals with low signal attenuation
 - ◆ PCIe Gen2
 - ◆ DisplayPort 1.1a
 - ◆ LVDS
 - ◆ SATA 3 Gbit/s



4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
CBTU04082BS	HVQFN42	plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 × 9 × 0.85 mm	SOT1144-1

5. Functional diagram

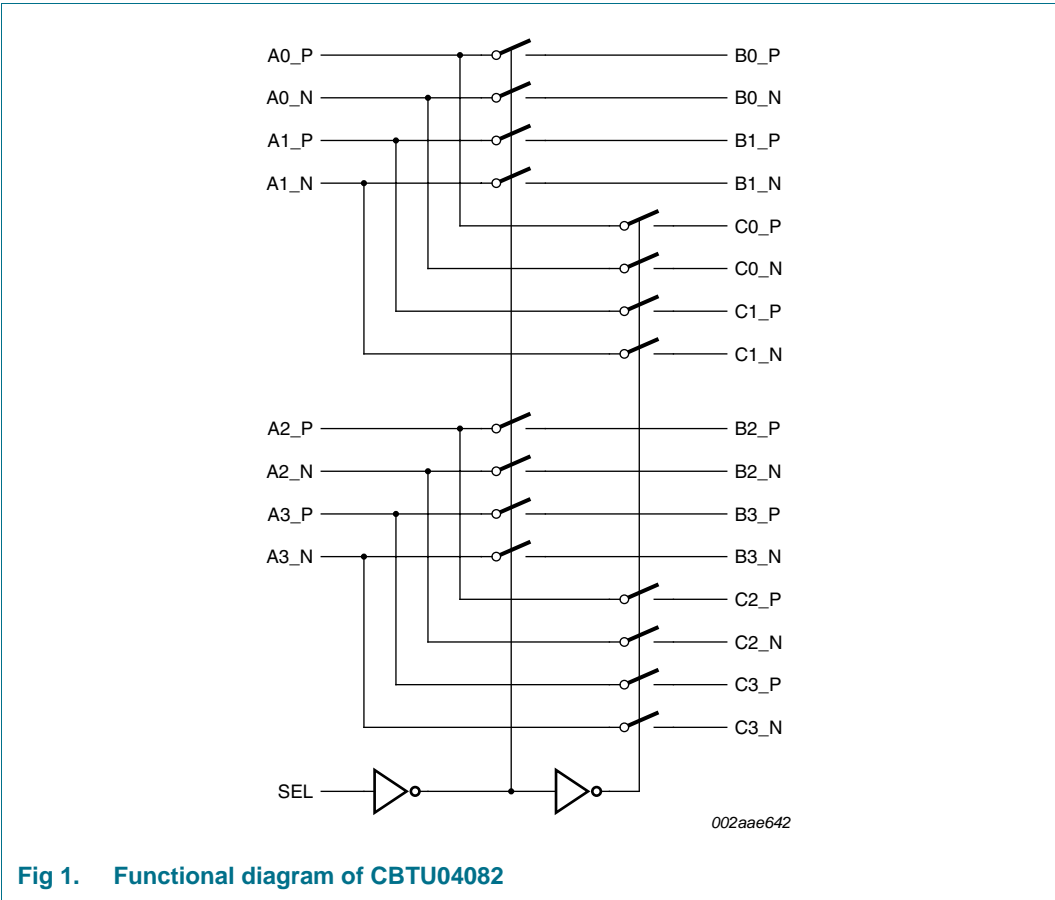


Fig 1. Functional diagram of CBTU04082

Transparent top view

Fig 2. Pin configuration for HVQFN42

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0_P	2	I/O	channel 0, port A differential signal input/output
A0_N	3	I/O	
A1_P	6	I/O	channel 1, port A differential signal input/output
A1_N	7	I/O	
A2_P	11	I/O	channel 2, port A differential signal input/output
A2_N	12	I/O	
A3_P	15	I/O	channel 3, port A differential signal input/output
A3_N	16	I/O	
B0_P	38	I/O	channel 0, port B differential signal input/output
B0_N	37	I/O	
B1_P	36	I/O	channel 1, port B differential signal input/output
B1_N	35	I/O	
B2_P	29	I/O	channel 2, port B differential signal input/output
B2_N	28	I/O	
B3_P	27	I/O	channel 3, port B differential signal input/output
B3_N	26	I/O	
C0_P	34	I/O	channel 0, port C differential signal input/output
C0_N	33	I/O	
C1_P	32	I/O	channel 1, port C differential signal input/output
C1_N	31	I/O	
C2_P	25	I/O	channel 2, port C differential signal input/output
C2_N	24	I/O	
C3_P	23	I/O	channel 3, port C differential signal input/output
C3_N	22	I/O	
SEL	9	CMOS single-ended input	operation mode select SEL = 0: A → B SEL = 1: A → C
V _{DD}	5, 8, 13, 18, 20, 30, 40, 42	power	positive supply voltage, 1.8 V to 2.0 V (± 0.1 V)
GND	1, 4, 10, 14, 17, 19, 21, 39, 41, center pad	power	supply ground

7. Functional description

Refer to [Figure 1 “Functional diagram of CBTU04082”](#).

7.1 Function selection

Table 3. Function selection

SEL	Function
L	An to Bn
H	An to Cn

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	referenced to GND	-0.5	+2.5	V
V_I	input voltage		-0.5	V_{DD}	V
I_O	output current		-	120	mA
P	power dissipation		-	0.5	W
T_{stg}	storage temperature		-65	+150	°C

9. Static characteristics

Table 5. Static characteristics

$V_{DD} = 1.8\text{ V} \pm 10\%$; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{DD}	supply current	$V_{DD} = \text{max.}; V_I = \text{GND or } V_{DD}$	-	-	4	mA
I_{IH}	HIGH-level input current	$V_{DD} = \text{max.}; V_I = V_{DD}$	-	-	± 5 ^[2]	μA
I_{IL}	LOW-level input current	$V_{DD} = \text{max.}; V_I = \text{GND}$	-	-	± 5 ^[2]	μA
V_{IH}	HIGH-level input voltage	guaranteed HIGH level	$0.65V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	guaranteed LOW level	-0.5	-	$0.15V_{DD}$	V
V_{IK}	input clamping voltage	$V_{DD} = \text{max.}; I_I = -18\text{ mA}$	-	-0.7	-1.2	V

[1] Typical values are at $V_{DD} = 1.8\text{ V}$, $T_{amb} = 25\text{ °C}$, and maximum loading.

[2] Input leakage current is $\pm 50\text{ }\mu\text{A}$ if differential pairs are pulled to HIGH and LOW.

10. Dynamic characteristics

Table 6. Dynamic characteristics

$V_{DD} = 1.8 \text{ V} \pm 10 \%$; $T_{amb} = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
α_{ct}	crosstalk attenuation	$f = 3 \text{ GHz}$	-	-23	-	dB
		$f = 100 \text{ MHz}$	-	-58	-	dB
$\alpha_{iso(off)}$	off-state isolation	$f = 3 \text{ GHz}$	-	-23	-	dB
		$f = 100 \text{ MHz}$	-	-58	-	dB
DDIL	differential insertion loss	$f = 3 \text{ GHz}$	-	-2	-	dB
B_{-3dB}	-3 dB bandwidth		-	4.1	-	GHz
t_{PD}	propagation delay	from left-side port to right-side port, or vice versa	-	80	-	ps

Switching characteristics

t_{PZH}	OFF-state to HIGH propagation delay		-	-	8.0	ns
t_{PZL}	OFF-state to LOW propagation delay		-	-	8.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay		-	-	8.0	ns
t_{PLZ}	LOW to OFF-state propagation delay		-	-	8.0	ns
$t_{sk(dif)}$	differential skew time	intra-pair	-	-	10	ps
t_{sk}	skew time	inter-pair	-	-	35	ps

[1] Typical values are at $V_{DD} = 1.8 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$, and maximum loading.

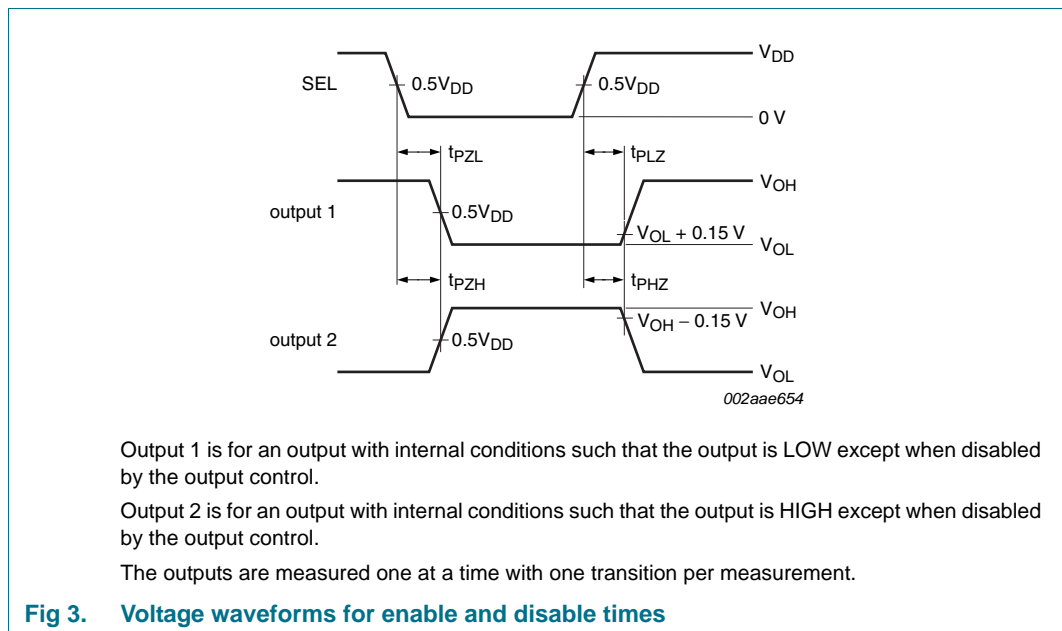


Fig 3. Voltage waveforms for enable and disable times

11. Test information

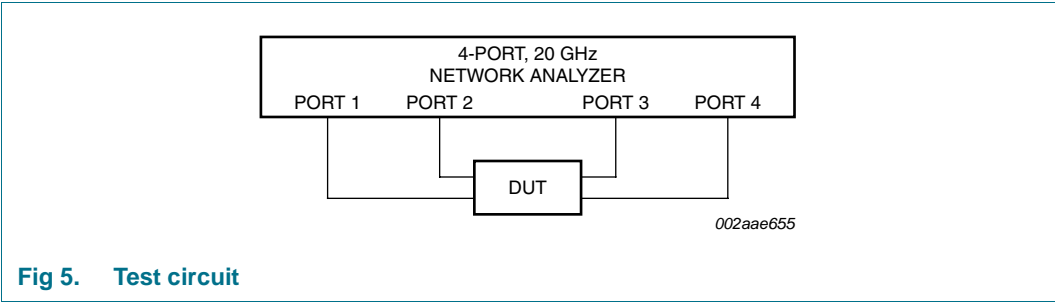
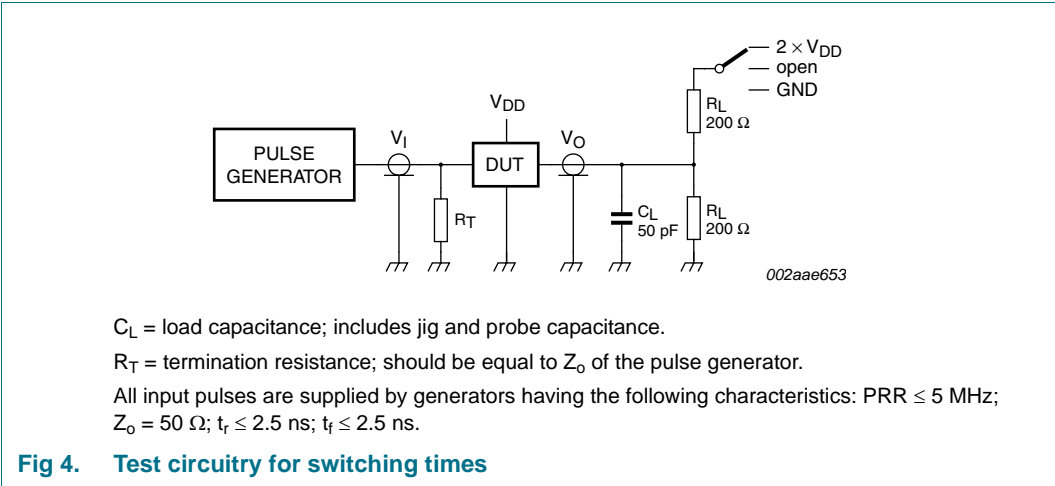


Table 7. Test data

Test	Load		Switch
	C_L	R_L	
t_{PLZ} , t_{PZL} (output on B side)	50 pF	200 Ω	$2 \times V_{DD}$
t_{PHZ} , t_{PZH} (output on B side)	50 pF	200 Ω	GND
t_{PD}	50 pF	200 Ω	open

12. Package outline

HVQFN42: plastic thermal enhanced very thin quad flat package; no leads;
 42 terminals; body 3.5 x 9 x 0.85 mm

SOT1144-1

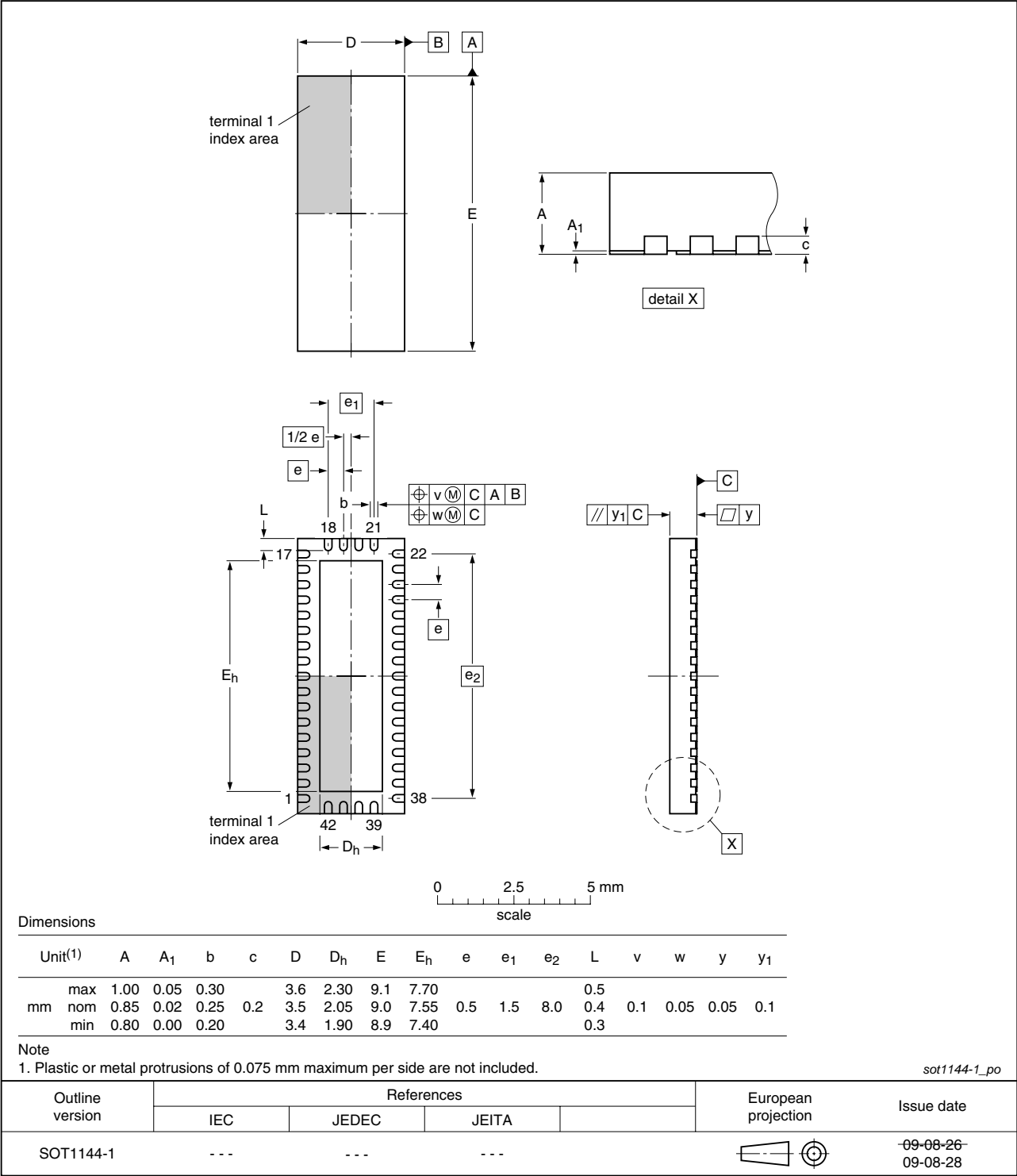


Fig 6. Package outline SOT1144-1 (HVQFN42)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 7](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020C)

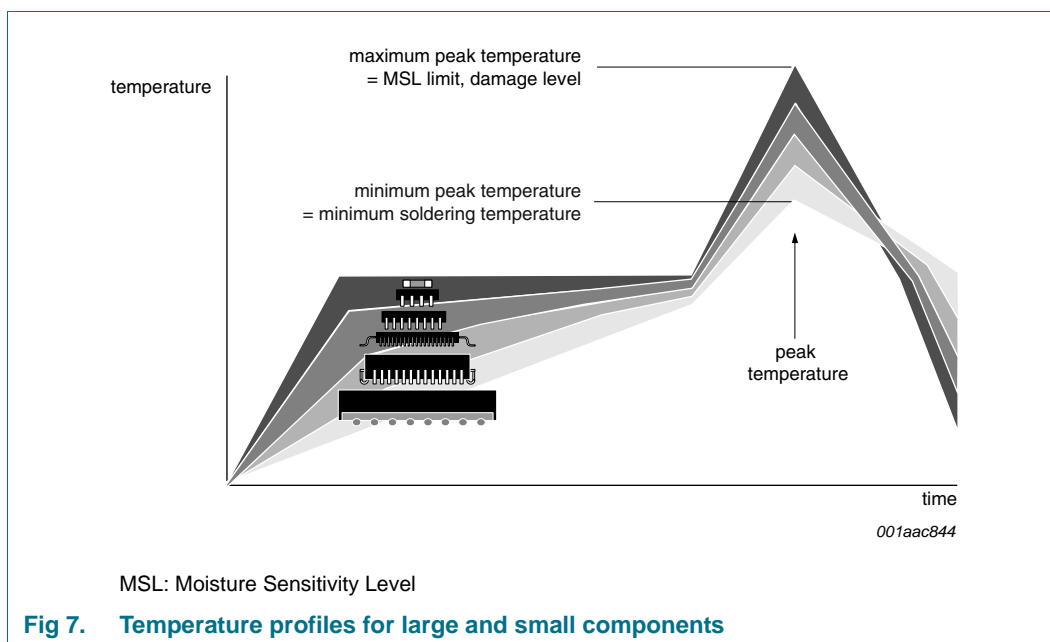
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 7](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
LVDS	Low-Voltage Differential Signalling
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PRR	Pulse Repetition Rate
SATA	Serial Advanced Technology Attachment
USB	Universal Serial Bus

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTU04082 v2	20100713	Product data sheet	-	CBTU04082 v1
Modifications:	<ul style="list-style-type: none">• Section 2 "Features and benefits", third sub-bullet: changed from "7 ps maximum" to "10 ps maximum"• Section 3 "Applications": deleted third sub-bullet "USB 3.0"• Table 5 "Static characteristics": V_{IL} Max value changed from "$0.35V_{DD}$" to "$0.15V_{DD}$"• Table 6 "Dynamic characteristics": t_{PD} Typ value changed from "180 ps" to "80 ps"			
CBTU04082 v1	20100215	Product data sheet	-	-

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