Enpirion® Power Datasheet
ES1030QI Power Rail Sequencer

Features

- Four enable outputs
- Four power good feedback signals
- Can be chained with additional devices to achieve >16 sequenced rails
- Precise, adjustable qualification time for sequenced supplies (33us to 8.04ms)
- Aggregate PG signal for the logical AND of the individual PG signals
- Wide 1.8 V to 5.0 V nominal voltage range
- Low power consumption
- Pb-free/ RoHS compliant
- Halogen-free
- STQFN-20 package

Description

The ES1030QI Power Rail Sequencer is a low-power and small-form factor device ideal for establishing the power sequencing pattern in small to large multi-rail power systems (please refer to Figure 6). The part provides nested sequencing of four outputs per device, with the ability to attach additional devices in a sequencing chain for at least 16 outputs. A simple resistor divider establishes a precise qualification time window by determining if each power rail is valid at the correct time. The part uses power good signals from the regulators to provide feedback of valid power. Separate fault I/O signals and aggregate PG signals further enhance the utility of this device. The sequencer is available in a 2mm x 3mm STQFN package, optimal for use in dense systems.

Pin Assignments

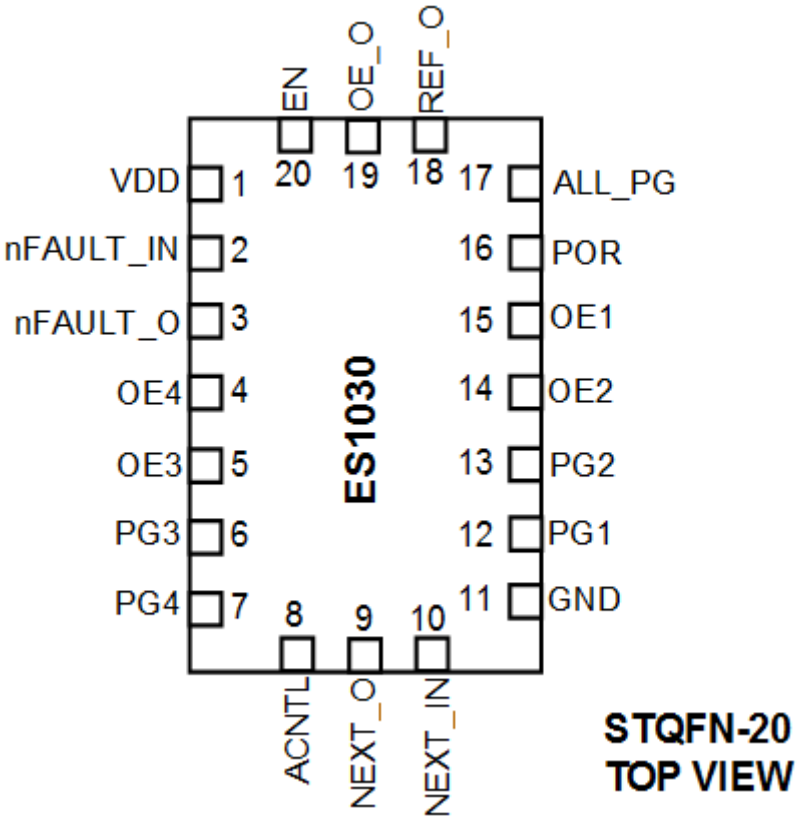


Figure 1: ES1030QI Pin Assignments

Ordering Information

PART NUMBER	PACKAGE MARKINGS	$T_{AMBIENT}$ RATING (°C)	PACKAGE DESCRIPTION
ES1030QI	S1030	-40 to +85	20-pin (2mm x 3mm x 0.55 mm) QFN T&R (3000)
EVB-ES1030QI			QFN evaluation board

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Description

PIN	NAME	TYPE	FUNCTION
1	VDD	PWR	Supply voltage
2	nFAULT_IN	Digital input	Digital input without Schmitt Trigger Input
3	nFAULT_O	Digital output	Open-drain NMOS
4	OE4	Digital output	Push pull
5	OE3	Digital output	Push pull
6	PG3	Digital input	Digital input without Schmitt Trigger Input
7	PG4	Digital input	Digital input without Schmitt Trigger Input
8	ACNTL	Analog input/output	Analog input/output
9	NEXT_O	Digital output	Push pull
10	NEXT_IN	Digital input	Digital input with Schmitt Trigger Input
11	GND	GND	Ground
12	PG1	Digital input	Digital input without Schmitt Trigger Input
13	PG2	Digital input	Digital input without Schmitt Trigger Input
14	OE2	Digital output	Push pull
15	OE1	Digital output	Push pull
16	POR	Digital output	Push pull
17	ALL_PG	Digital output	Push pull
18	REF_O	Analog input/output	Analog input/output
19	OE_O	Digital output	Push pull
20	EN	Digital input	Digital input without Schmitt Trigger Input

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	MIN	MAX	UNITS	NOTES
V_{HIGH} to GND	-0.3	7	V	Open Drain output nFLT_O.
Voltage at input pins	-0.3	7	V	
Current at input pin	-1.0	1.0	mA	
Storage temperature range	-65	150	°C	
Junction temperature	--	150	°C	

Electrical Characteristics

Unless otherwise noted: Ta = 25°C. **Boldface limits apply over the operating temperature range, T_A within -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		**1.71**	3.3	**5.5**	V
Operating temperature	T_A	Ambient temperature with the chip mounted on a typical PCB	**-40**	25	**85**	°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent current	I_Q	Static inputs and outputs	—	300	—	µA
Maximal voltage applied to any PIN in high-impedance state	V_O		—	—	**VDD**	V
Maximal average or DC current[1]	I_O	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	—	—	90	mA
High-level input voltage	V_{IH}	Logic Input, at VDD=1.8V	**0.98**	—	**VDD**	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	**1.15**	—	**VDD**	
		Logic Input, at VDD=3.3V	**1.75**	—	**VDD**	
		Logic Input with Schmitt Trigger, at VDD=3.3V	**1.99**	—	**VDD**	
		Logic Input, at VDD=5.0V	**2.88**	—	**VDD**	
		Logic Input with Schmitt Trigger, at VDD=5.0V	**3.21**	—	**VDD**	
Low-level input voltage	V_{IL}	Logic Input, at VDD=1.8V	—	—	**0.77**	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	—	—	**0.60**	
		Logic Input, at VDD=3.3V	—	—	**1.43**	
		Logic Input with Schmitt Trigger, at VDD=3.3V	—	—	**1.39**	
		Logic Input, at VDD=5.0V	—	—	**2.33**	
		Logic Input with Schmitt Trigger, at VDD=5.0V	—	—	**2.33**	
High-level input current	I_{IH}	Logic input PINs; V_{IN} = VDD	-1.0	—	1.0	µA
Low-level input current	I_{IL}	Logic input PINs; V_{IN} = 0V	-1.0	—	1.0	µA
High-level output Voltage[1]	V_{OH}	Push pull, I_{OH} = 100uA, at VDD=1.8 V	**1.67**	1.789	—	V
		Push pull, I_{OH} = 3mA, at VDD=3.3 V	**2.71**	3.10	—	
		Push pull, I_{OH} = 5mA, at VDD=5.0 V	**4.15**	4.75	—	
Low-level output Voltage[1]	V_{OL}	Push pull, I_{OL} = 100uA, at VDD=1.8 V	—	0.010	**0.014**	V
		Open drain, I_{OL} = 100uA, at VDD=1.8 V	—	0.007	**0.012**	
		Push pull, I_{OL} = 3mA, at VDD=3.3 V	—	0.148	**0.179**	
		Open drain, I_{OL} = 3mA, at VDD=3.3 V	—	0.061	**0074**	
		Push pull, I_{OL} = 5mA, at VDD=5.0 V	—	0.189	**0.225**	
		Open drain, I_{OL} = 5mA, at VDD=5.0 V	—	0.079	**0.097**	
High-level output current [1]	I_{OH}	Push pull, V_{OH} = V_{DD}-0.2, at VDD=1.8 V	**1.01**	1.78	—	mA
		Push pull, V_{OH} = 2.4 V, at VDD=3.3 V	**5.55**	10.8	—	
		Push pull, V_{OH} = 2.4 V, at VDD=5.0 V	**20.1**	30.0	—	

[1] Guaranteed by design.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Low-level output current [1]	I_{OL}	Push pull, V_{OL} =0.15V, at VDD=1.8 V	**1.18**	1.66	—	mA
		Open drain, V_{OL} =0.15V, at VDD=1.8 V	**2.88**	4.08	—	
		Push pull, V_{OL} =0.4V, at VDD=3.3 V	**5.06**	7.80	—	
		Open drain, V_{OL} =0.4V, at VDD=3.3 V	**12.0**	18.9	—	
		Push pull, V_{OL} =0.4V, at VDD=5.0 V	**6.78**	10.4	—	
		Open drain, V_{OL} =0.4V, at VDD=5.0 V	**15.6**	25.0	—	
Internal pull up resistance	R_{PULL_UP}	Pull up on PINs 6, 7, 12, 13	**85**	106	**127**	kΩ
		Pull up on PINs 3, 20	**869**	1060	**1275**	
REF_O output voltage	Vref	(R1+R2)>100k	—	1050	—	mV
Delay, ACTRL/REF_O = 0	TDelay0	Ta = 25 C (R1+R2)>100k	0.0288	0.033	0.0368	ms
		-40°C to +85°C (R1+R2)>100k	**0.0283**		**0.0373**	
Delay, ACTRL/ REF_O = 0.5	TDelay0.5	Ta = 25 C (R1+R2)>100k	3.36	3.85	4.32	ms
		-40°C to +85°C (R1+R2)>100k	**3.36**		**4.39**	
Delay, ACTRL/ REF_O = 1	TDelay1.0	Ta = 25 C (R1+R2)>100k	7.04	8.04	9.06	ms
		-40°C to +85°C (R1+R2)>100k	**7.03**		**9.19**	
Start-up time	T_{SU}	From VDD rising past 1.6V to first transition on OE1	--	2.0	**2.5**	ms

Functional Block Diagram

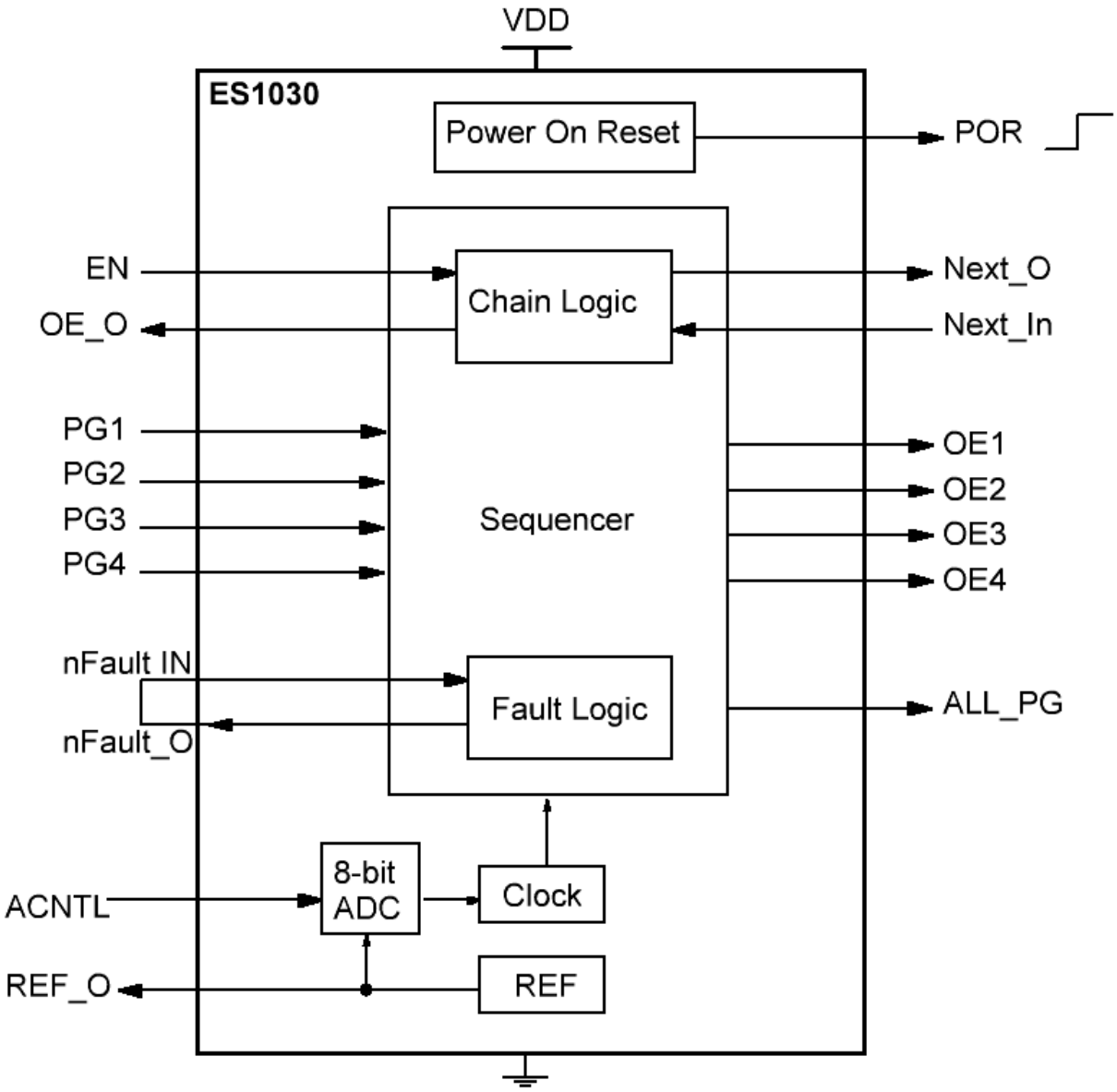


Figure 2: Functional Block Diagram

Typical Application Circuits

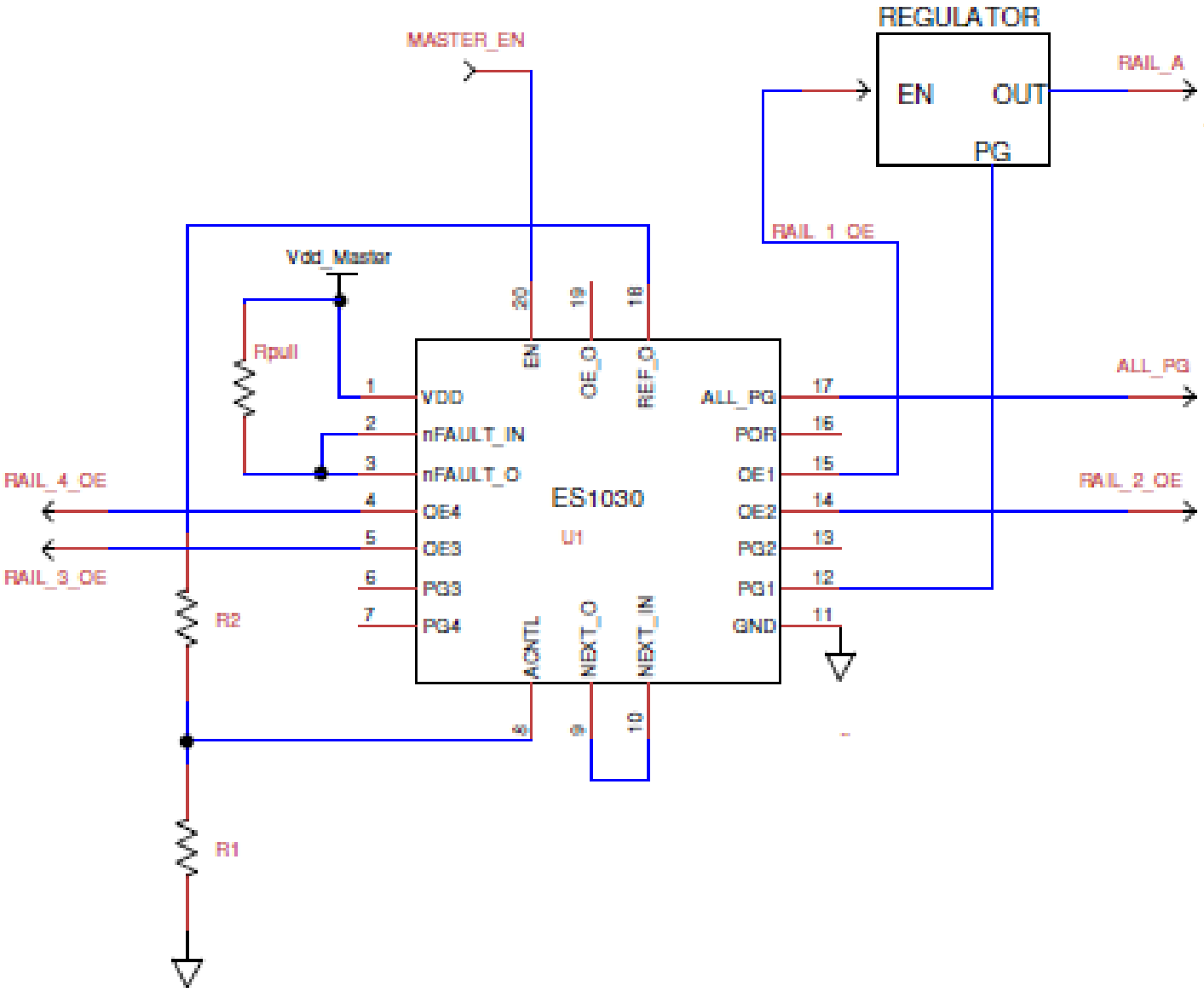


Figure 3: Stand Alone Operation

Notes to **Figure 3**:

1. Unused PG pins may be floated or tied to VDD.
2. ACNTL controls delays based on voltage ratio relative to REF_O: full scale delay (ACTRL at REF_O) is 8.04ms; minimum delay (ACTRL at GND) is 33us.
3. For single device, connect NEXT_O to NEXT_IN.
4. Tie all nFAULT_x pins of all chained devices together. When fault is detected in any device, the device pulls the nFAULT line low, triggering sequential power down starting with the end device. This is released by EN low until FAULT is cleared.
5. ALL_PG is a push-pull output for logical AND of all PG_x signals.

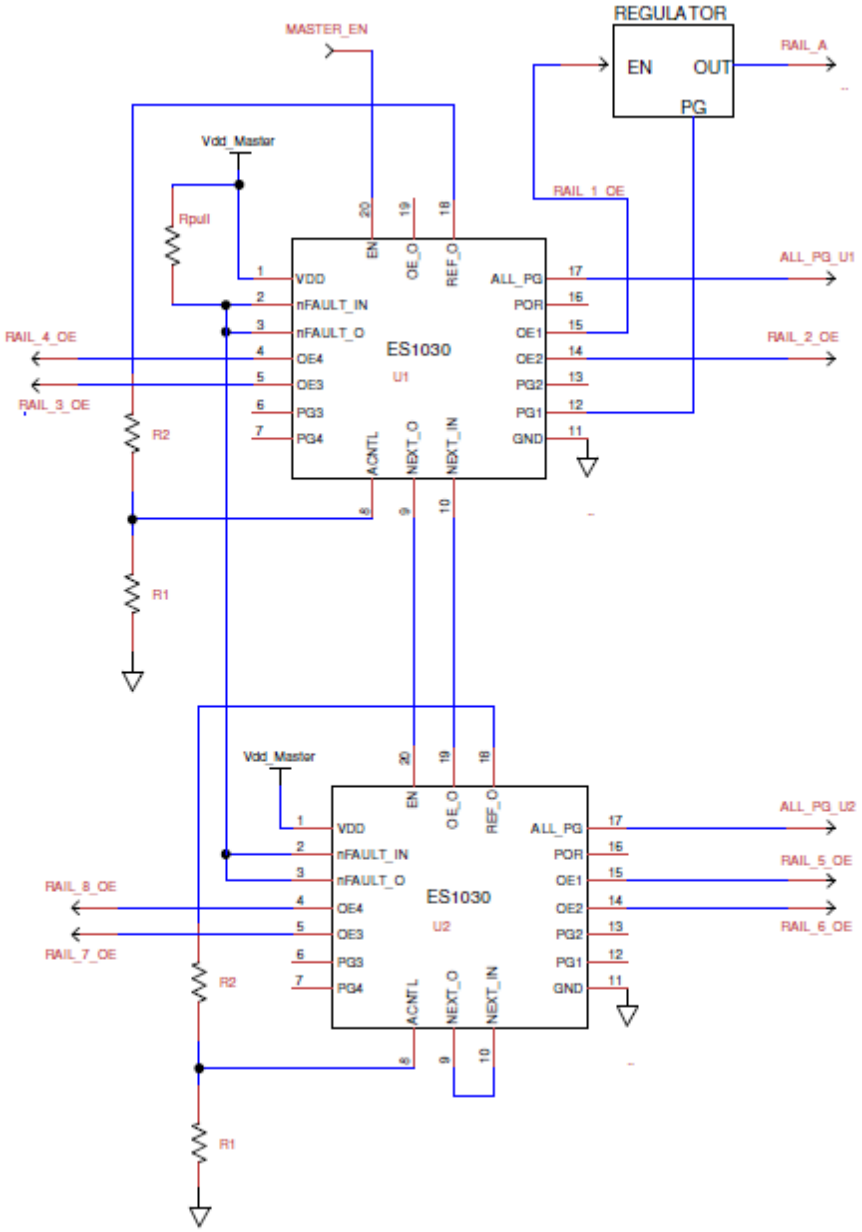


Figure 4: Chained Operation

Notes to **Figure 4**:

1. Connect NEXT_O to NEXT_IN on device at end of chain.
2. Tie all nFAULT_x pins of all chained devices together. When fault is detected in any device, the device pulls the nFAULT line low, triggering sequential power down starting with the end device. This is released by EN low until FAULT is cleared.
3. Tie NEXT_O to EN of following device. Tie NEXT_IN to OE_O of following device.

Application Information

Nested Sequencing

For many integrated circuits with multiple power supply domains, the manufacturer establishes a prescribed voltage sequencing order for both power-up and power-down. The sequencing order ensures the safety of the device and prevents potentially damaging currents from flowing from one power domain to another through parasitic junctions in the device. The ES1030QI uses the most common pattern of sequencing, *nested sequencing*, where power domains are activated in a certain order (such as 1-2-3-4) and then removed in the reverse order (4-3-2-1). Nested sequencing is illustrated in the waveforms shown in Figures 5 through 7.

Four-Channels with Qualification Window

The ES1030QI allows nested sequencing of four power channels per ES1030QI device. After the master enable (EN) signal goes high to start the sequence, each output enable (OEx) signal transitions high in the prescribed 1-2-3-4 order. A resistor divider from the REF_O output to the ACNTL input pin determines a precision time delay between successive OEx outputs. During this time delay, or *qualification window*, the ES1030QI pauses for a transition of the PGx signal corresponding to the OEx signal to indicate the enabled power supply has a valid output. Successive outputs are enabled with the same qualification window.

The power supplies are sequenced down in the reverse order if any of these events are true:

1. Negation of the EN signal.
2. Failure of any PGx to become true within its corresponding qualification window.
3. Any other fault (such as from chained ES1030QI parts) introduced into the nFAULT_IN input. This input is negative logic to allow open-drain wired OR configurations.

Precision Delay

Unlike other sequencing solutions which rely on poorly-specified current sources and wide-tolerance capacitors, the ES1030QI generates a precision delay using precision resistors and mixed-signal techniques. An internal reference produces an output voltage which sources 1.05 V on the REF_O pin. The voltage divider you select from REF_O divides the voltage to any value between 20 mV and 1.05 V. The divider impedance (R1+R2) should be kept >100k ohms for accurate delay settings.

The ACNTL pin samples the divided voltage with an internal analog to digital (A/D) converter. The resulting digital value is the divider for an internal clock, resulting in a precision time delay. The delay is scaled to range from 33 µs to 8.04 ms according to the formula:

```
Tdelay=(N/255)*8.04ms, where
N=(Vacntl/1.05V)*255 quantized to
8-bit values (0-255)
```

To limit the potential timing error to less than 20% of the set value, delays for N=5 or less should not be used. The delay time is the same for all intervals between successive outputs, and for both sequence up and sequence down directions.

Chaining Functions

Use the ES1030QI in multiple instances to extend the number of power rails sequenced up to at least 16 rails. You can accomplish this by connecting the NEXT_O, NEXT_IN, EN, OE_O, nFAULT_O, nFAULT_IN, and ALL_PG signals as shown in the chaining application circuit in Figure 4. This connection extends the behavior of the nested sequencing function to an additional four channels per each ES1030QI added to the chain. Each ES1030QI has its own time delay generator, and the delay values do not need to be the same for all instances of the part.

Convenience Logic Functions

The ES1030QI allows additional logic functions to make system application of the part much easier. Since the individual regulator PGx signals must remain distinct to satisfy the qualification windows during sequencing, an additional signal ALL_PG is introduced as the logical AND of the individual PGx signals.

The nFAULT_IN signal is a negative logic signal driven by the open-drain nFAULT_O signal, allowing connection to other open-drain nFAULT signals on the same connection. With this connection, other recognized faults in the system can trigger the system to sequence down in an orderly way.
The negative logic (nFAULT_O) signal asserts when the qualification windows for any of the PGx signals fail. In addition to its function as a chaining signal, OE_O going LOW indicates that the sequence down

of all devices connected to this part has completed.

Voltage Levels and Power-On Reset (POR)

The internal circuitry of the ES1030QI is functional over the VDD voltage range from 1.71 V to 5.5 V, allowing operation from standard logic voltages from 1.8 V to 5 V.

There is an internal initialization time of up to 2.5 ms while the device is preparing for operation. All I/O signals on the ES1030QI are in a high-impedance state during the hardware initialization time. The POR output indicates by transition to HIGH that the sequencer initialization is complete.

The sequencer accepts EN inputs before, during, or after internal initialization, and the outputs begin sequencing in the correct order after the initialization is complete. To avoid additional delay on the first OE, the sequencer should be powered up at least 2.5 ms before the first transition on EN.

The PGx signal inputs provide internal pull-ups (~100k ohms) to VDD. External pull ups on the PG signals from the regulator should only be needed if there is significant capacitive loading or leakage current on the PG signals. Logic levels are dependent on the VDD for the ES1030QI as shown in the Electrical Characteristics table. The nFAULT_IN and NEXT_IN signals should have external pull ups to VDD. Transitions on the PGx, nFAULT_IN, and NEXT_IN signals are ignored during the initialization period.

The OEx and ALL_PG output drive signals are push-pull active drivers after initialization. Therefore, the output logic drive level is the same as the VDD supply to the ES1030QI.

Functionality Waveforms

WAVEFORM DEFINITIONS FOR FIGURES 5 TO 9	
WAVE	**PIN**
D0	Pin 20 (EN)
D1	Pin 15 (OE1)
D2	Pin 14 (OE2)
D3	Pin 5 (OE3)
D4	Pin 4 (OE4)
D5	Pin 12 (PG1)
D6	Pin 13 (PG2)
D7	Pin 6 (PG3)
D8	Pin 7 (PG4)
D9	Pin 17 (ALL_PG)
D10	Pin 3 (nFAULT_O)
Channel 1 (yellow)	Pin 8 (ACNTL)

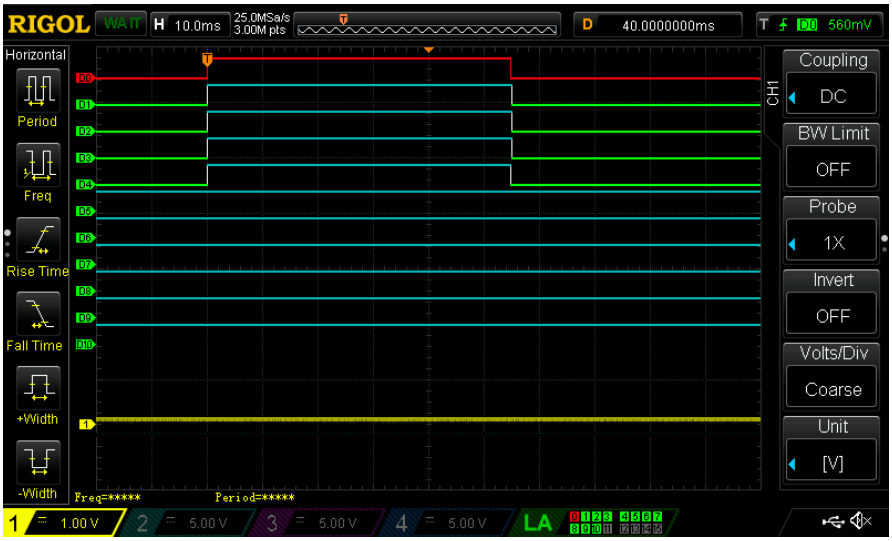


Figure 5: Normal operation, ACNTL = 0 mV

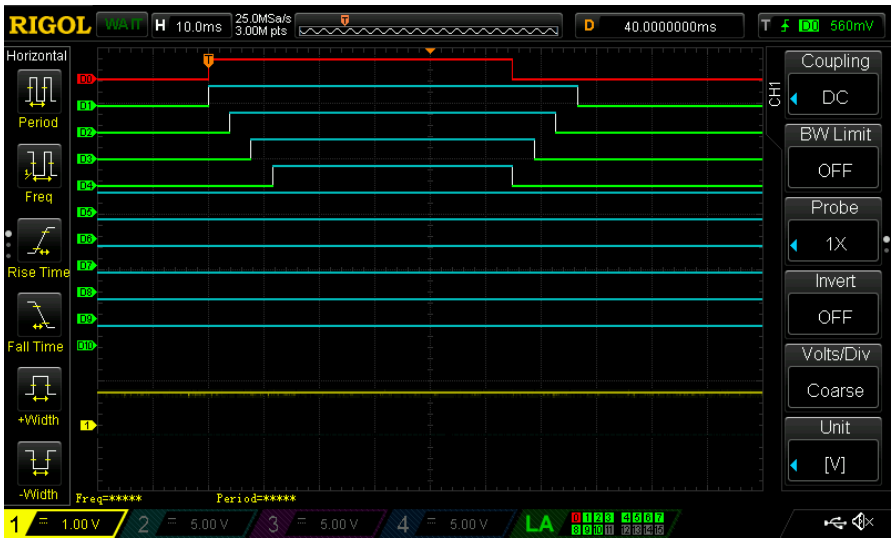


Figure 6: Normal operation, ACNTL = 500 mV

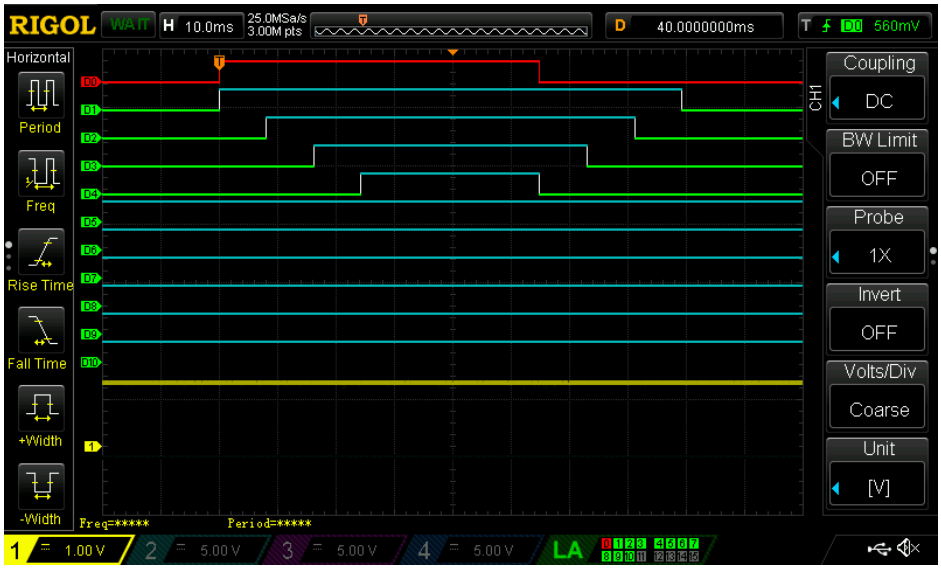


Figure 7: Normal operation, ACNTL = 1000 mV

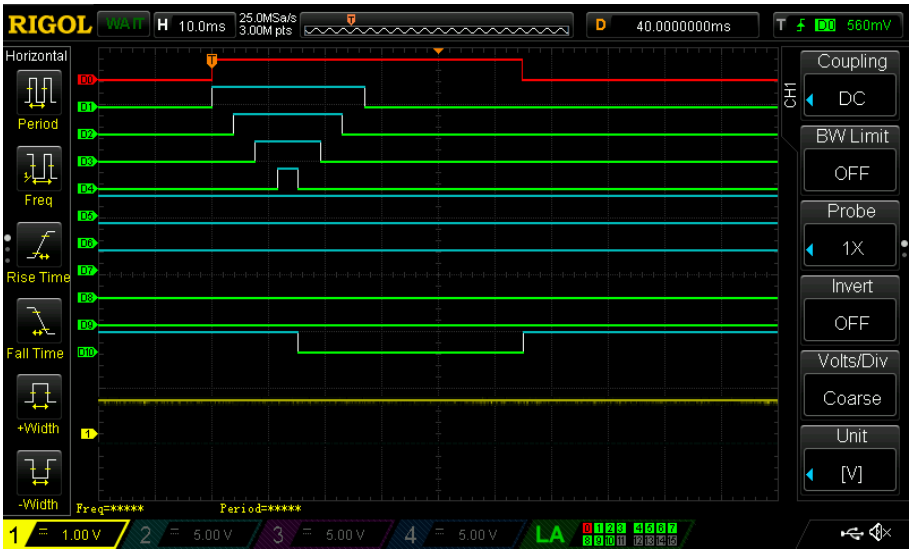


Figure 8: FAULT: No response from PG4

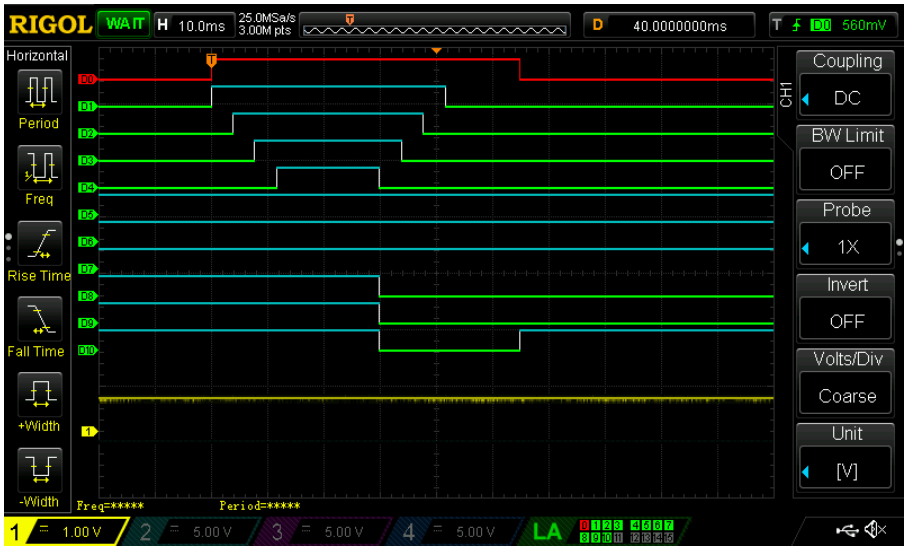


Figure 9: Fault on PG4

WAVEFORM DEFINITIONS FOR FIGURES 10 TO 12	
WAVE	**PIN**
D0	Pin 20 (EN – chip 1)
D1	Pin 15 (OE1 – chip 1)
D2	Pin 14 (OE2 – chip 1)
D3	Pin 5 (OE3 – chip 1)
D4	Pin 4 (OE4 – chip 1)
D5	Pin 15 (OE1 – chip 2)
D6	Pin 14 (OE2 – chip 2)
D7	Pin 5 (OE3 – chip 2)
D8	Pin 4 (OE4 – chip 2)
D9	Pin 3 (nFAULT_O)
D10	Pin 16 (POR)
D11	Pin 7 (PG4 – chip 2)
Channel 1 (yellow)	Pin 1 (VDD)
Channel 1 (blue)	Pin 8 (ACNTL)

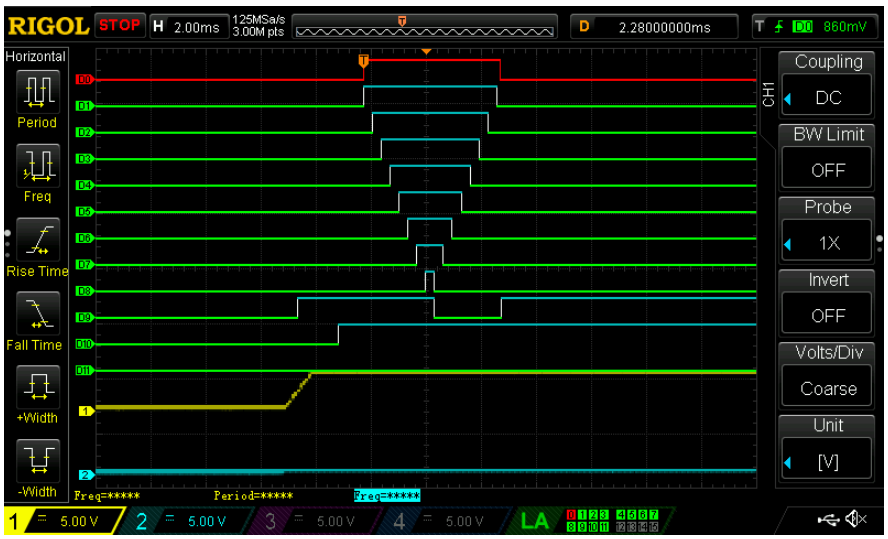


Figure 10: Chaining Example – No Response from PG4 (Chip 2)

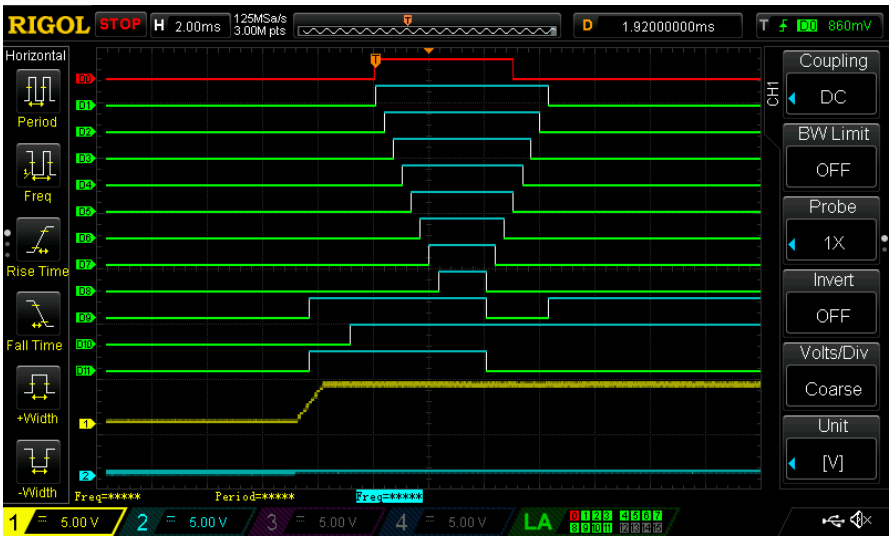


Figure 11: Chaining Example – Fault on PG4 (Chip 2)

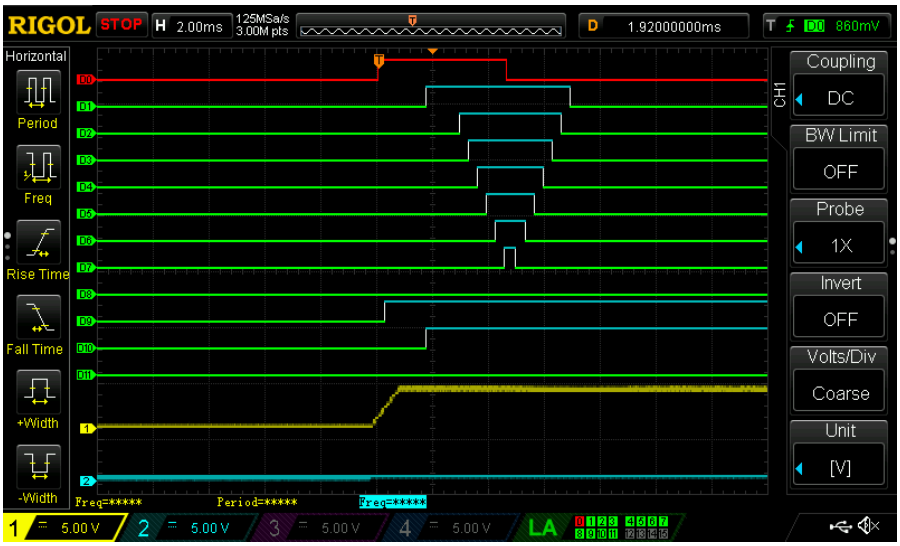


Figure 12: EN Activated During Initialization

Package Information

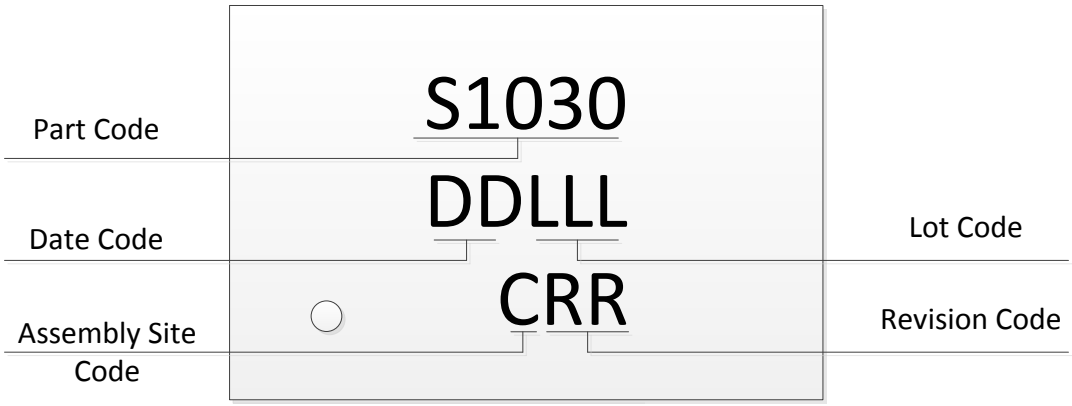
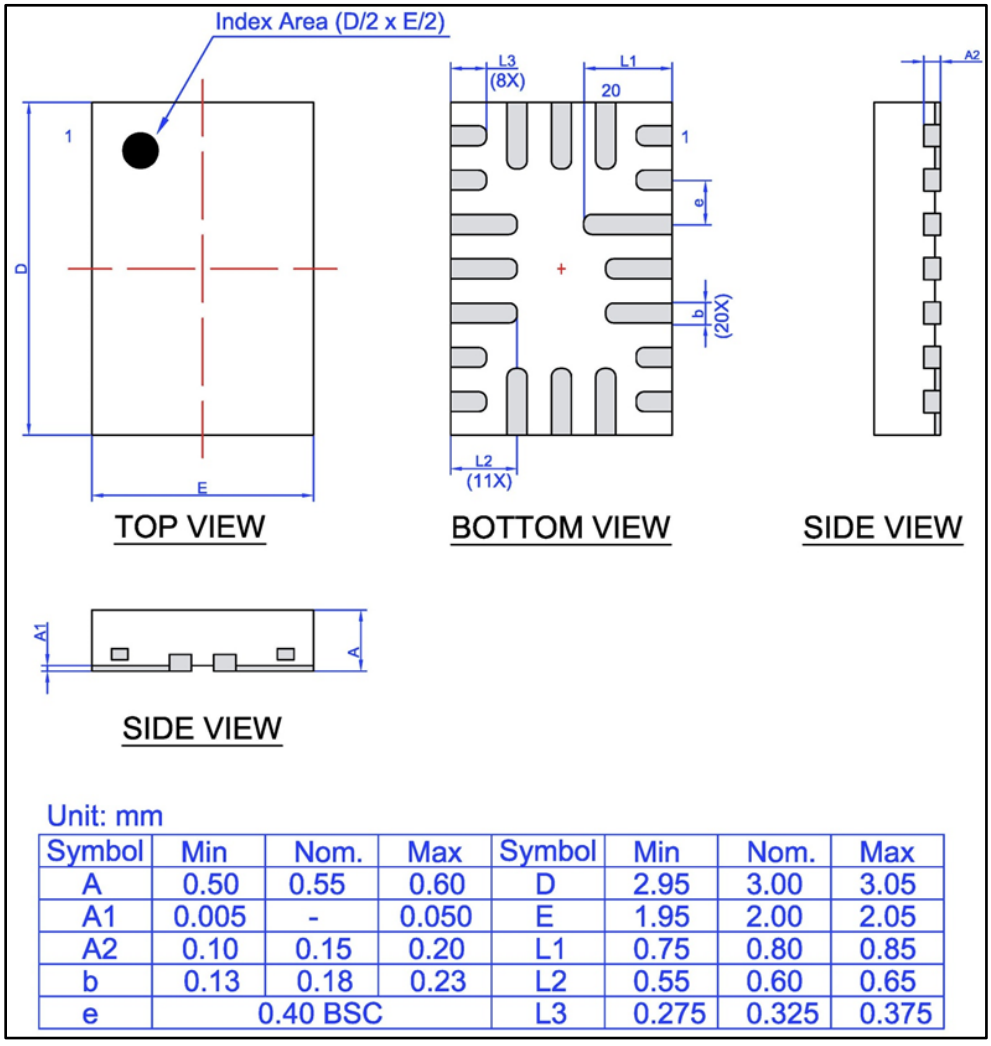


Figure 13: Package Top Marking



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Figure 14: Package Drawing and Dimensions (20 Lead STQFN Package JEDEC MO-220, Variation WECE)

Tape and Reel Specification

PACKAGE TYPE	NO. OF PINS	NOMINAL PACKAGE SIZE (mm)	MAX UNITS		REEL AND HUB SIZE (mm)	TRAILER A		LEADER B		POCKET (mm)	
			PER REEL	PER BOX		POCKETS	LENGTH (mm)	POCKETS	LENGTH (mm)	WIDTH	PITCH
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

PACKAGE TYPE	POCKET BTM LENGTH (mm)	POCKET BTM WIDTH (mm)	POCKET DEPTH (mm)	INDEX HOLE PITCH (mm)	POCKET PITCH (mm)	INDEX HOLE DIAMETER (mm)	INDEX HOLE TO TAPE EDGE (mm)	INDEX HOLE TO POCKET CENTER (mm)	TAPE WIDTH (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

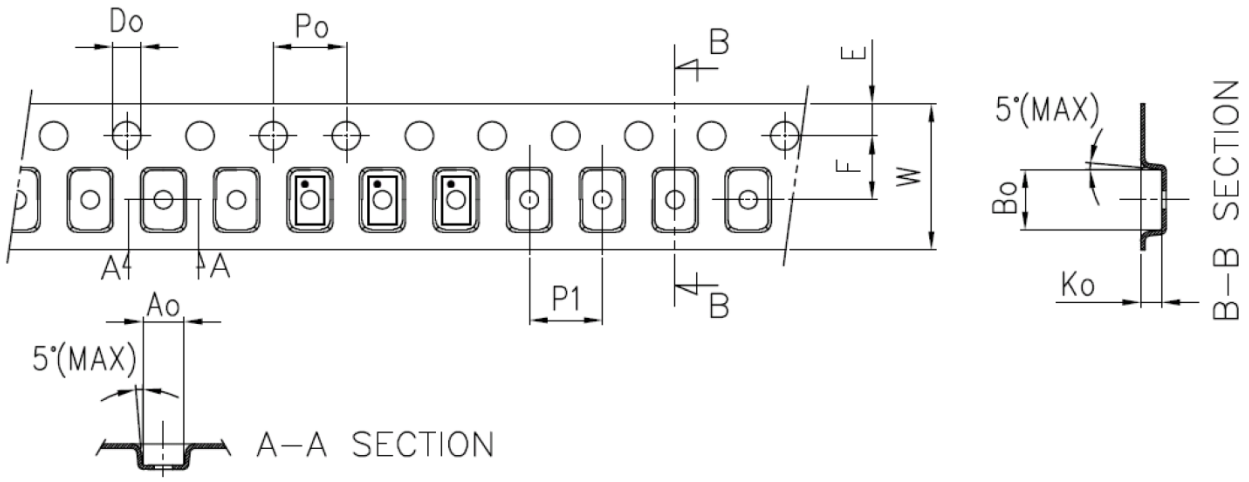


Figure 15: Carrier Tape Drawing and Dimensions

Recommended Reflow Soldering Profile

Please see the latest revision of IPC/JEDEC J-STD-020 for the reflow profile based on a package volume of 3.3 mm^3 (nominal). For more information, visit www.jedec.org.

Document Revision History

DATE	DOCUMENT VERSION	CHANGES
April 2015	2.0	Electrical Characteristics values, Applications text, Figures 10-12 waveform labels, Figures 3-4
February 2015	1.0	Initial release.

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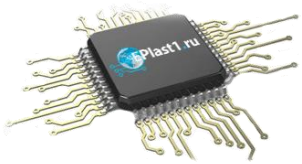
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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