FAIRCHILD SEMICONDUCTOR™

April 1988
Revised September 2000

74F125
Quad Buffer (3-STATE)

Features

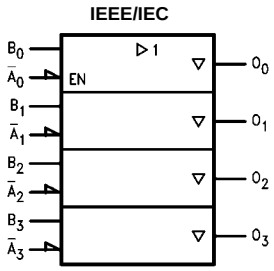
■ High impedance base inputs for reduced loading

Ordering Code:

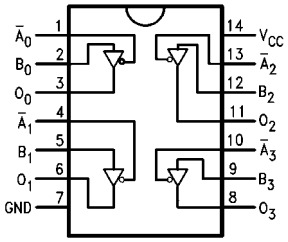
Order Number	Package Number	Package Description
74F125SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F125PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{A}_n$, B_n	Inputs	1.0/0.033	20 µA/–20 µA
O_n	Outputs	600/106.6 (80)	–12 mA/64 mA (48 mA)

Function Table

Inputs		Output
$\overline{A}_n$	B_n	O
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

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Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

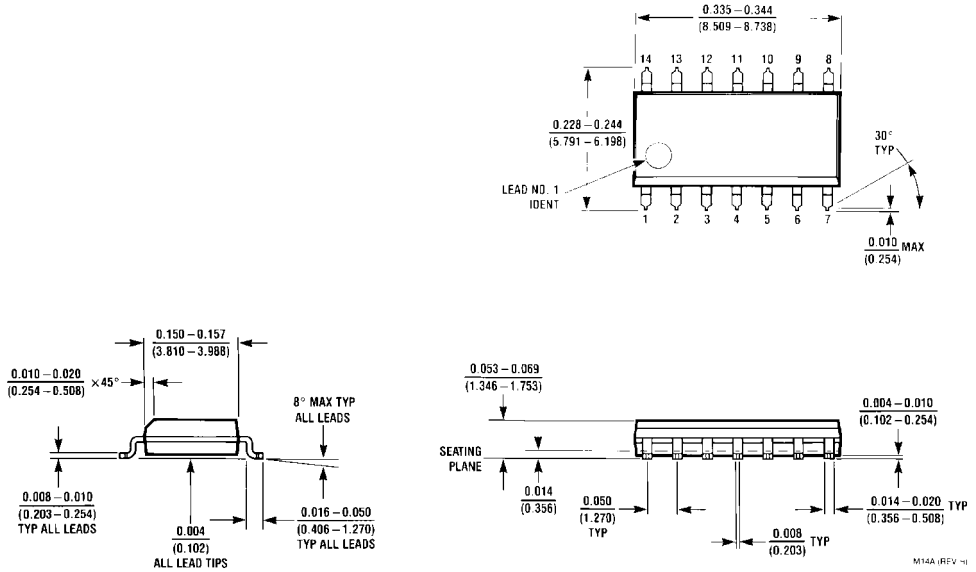
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.4			V	Min	I_{OH} = −3 mA
		10% V_{CC}	2.0					I_{OH} = −12 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
		5% V_{CC}	2.0					I_{OH} = −15 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				20	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	µA	0.0V	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−20.0	µA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Buss Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			18.5	24.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			31.7	40.0	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			27.6	35.0	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

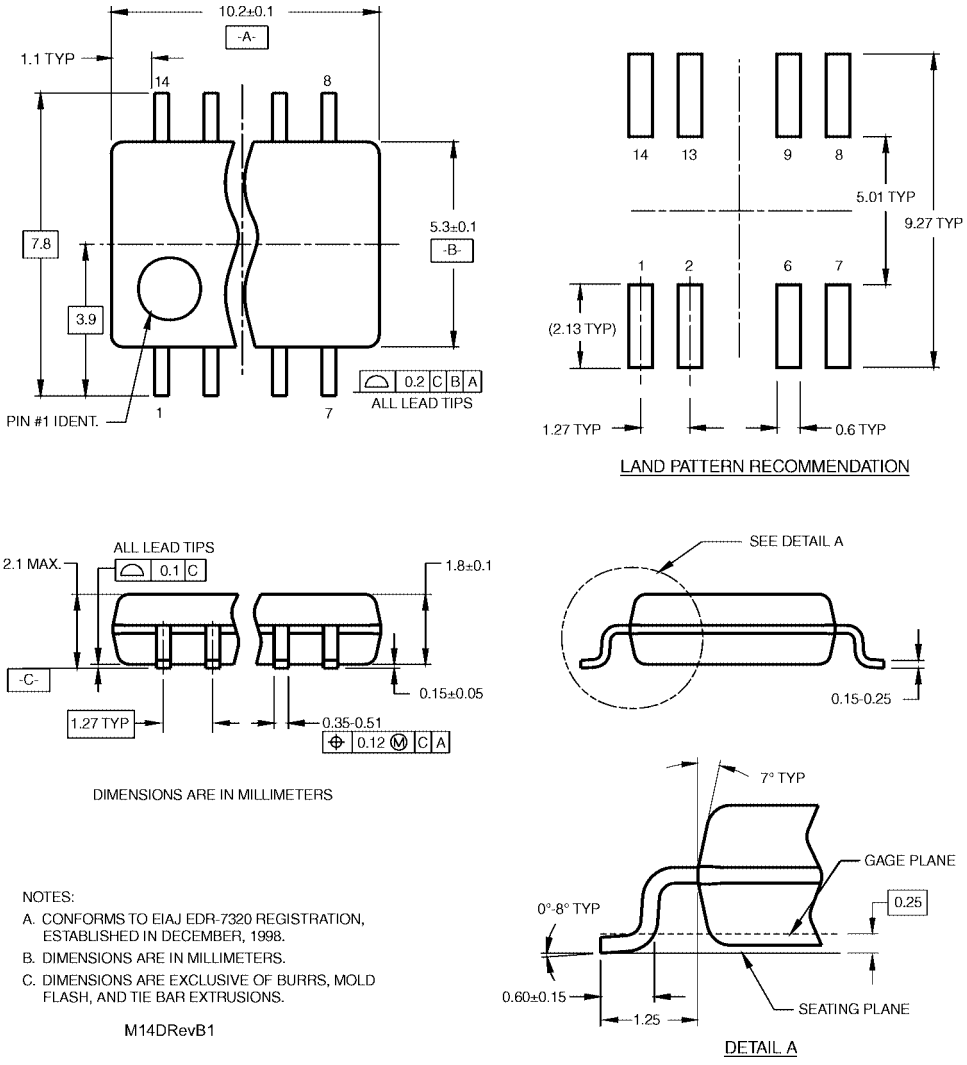
Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = 0°C to +70°C, V_{CC} = +5.0V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.0	4.0	6.0	2.0	6.5	ns
t_{PHL}		3.0	4.6	7.5	3.0	8.0	
t_{PZH}	Output Enable Time	3.5	4.7	7.5	3.0	8.5	ns
t_{PZL}		3.5	5.3	8.0	3.5	9.0	
t_{PHZ}	Output Disable Time	1.5	3.9	5.5	1.5	6.0	ns
t_{PLZ}		1.5	4.0	6.0	1.5	6.5	

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

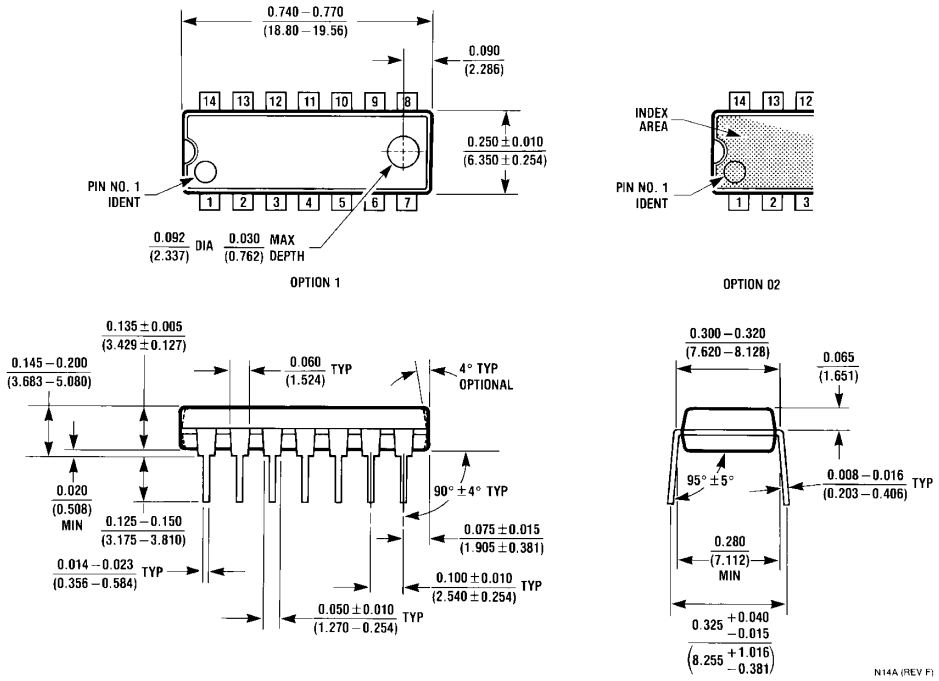
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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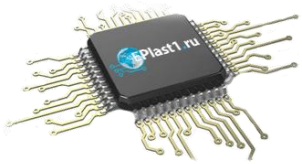
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- Подбор аналогов;
- Консультации по применению компонента;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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