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Product data sheet

Industrial CompactFlash™ Card

C-300 Longevity Series

up to UDMA4 / MDMA4 / PIO6

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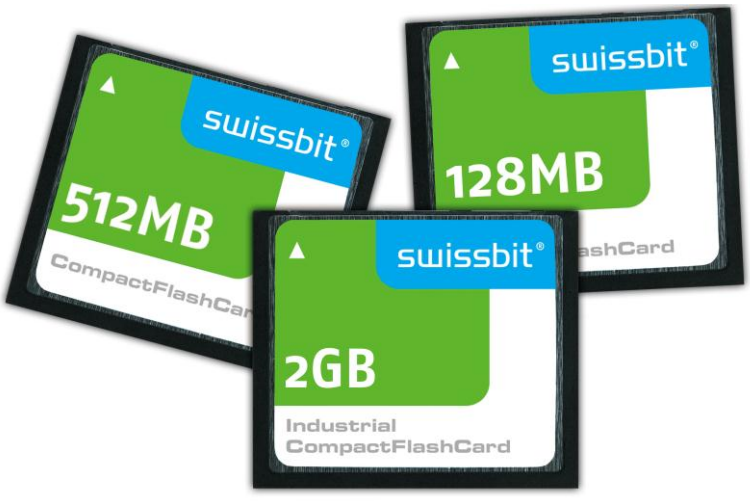
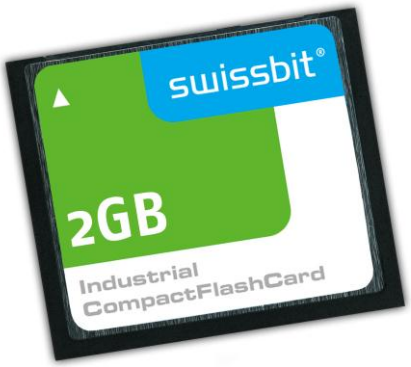


C-300 Longevity Series – UDMA CompactFlash™ Card, 128MByte up to 8GByte, 3.3/5V Supply



1 Main Features

- Highly-integrated memory controller
  - Fully compliant with CompactFlash™ specification 3.0, compatible with specification 4.1
  - Fully compatible with PCMCIA specification
  - PC Card ATA Interface supported
  - True IDE mode compatible
  - Up to PIO mode 6 supported
  - Up to MDMA4 supported
  - Up to UDMA4 supported
  - Hardware RS-code ECC (4 Bytes/528 Bytes correction)
  - Fix drive (IDE mode) & removable drive (PCMCIA mode) as default in the same card
- Small form factor
  - CFC Type I: 36.4mm x 42.8mm x 3.3mm
- Low-power CMOS technology
- 3.3V or 5.0V power supply
- Power saving mode (with automatic wake-up)
- S.M.A.R.T. support by *-SMA product type
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Data Retention: 10 year (JESD47)
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 16/32 sectors data loss (old data kept) for 2k/4k Page flash respectively
  - All data written to the flash if card status is ready after write command
- High reliability
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF: > 3,000,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of insertions: > 10,000
- Hot swappable in PCMCIA modes
- High performance
  - Up to 66MB/s burst transfer rate in UDMA4
  - optimized for random access 150kB/s
  - Sustained Read/Write performance: up to 38/20MB/s (UDMA4)
- Available densities
  - 128MB to 8GBytes
  - 1 or 2 channel cards are available depends at the application requirement
- Operating System support
  - Standard Software Drivers operation CompactFlash
- Controlled BOM
- RoHS compliant
- Long term support

on request

2 Table of Contents

3 Order Information

3.1 General part numbers

IDE-FIX & PCMCIA-Removable / PIO, DMA & UDMA support

Density	Part Number	Comment
128MB	SFCF0128HxBK1MT-t-MS-5y3-SMA	
256MB	SFCF0256HxBK1MT-t-MS-5y3-SMA	
512MB	SFCF0512HxBK1MT-t-MS-5y3-SMA	
1GB	SFCF1024HxBK2MT-t-MO-5y3-SMA	
2GB	SFCF2048HxBK1MT-t-QT-5y3-SMA	
4GB	SFCF4096HxBK2MT-t-QP-5y3-SMA	
8GB	SFCF8192HxBK4MT-t-QT-5y3-SMA	

Table 1: Standard and industrial product list

x= depends on product generation
y= firmware generation
t= C commercial temperature; =I industrial temperature

3.2 Standard part numbers 0°C to 70°C

IDE-FIX & PCMCIA-Removable / PIO, DMA & UDMA support

Density	Part Number	SAP
128MB	SFCF0128H1BK1MT-C-MS-553-SMA	604722
256MB	SFCF0256H1BK1MT-C-MS-553-SMA	604723
512MB	SFCF0512H1BK1MT-C-MS-553-SMA	604742
1GB	SFCF1024H1BK2MT-C-MO-553-SMA	604744
2GB	SFCF2048H1BK1MT-C-QT-553-SMA	604745
4GB	SFCF4096H1BK2MT-C-QP-553-SMA	604750
8GB	SFCF8192H1BK4MT-C-QT-553-SMA	604753

Table 2: Commercial Temp. Order Information

3.3 Standard part numbers -40°C to 85°C

IDE-FIX & PCMCIA-Removable / PIO, DMA & UDMA support

Density	Part Number	SAP
128MB	SFCF0128H1BK1MT-I-MS-553-SMA	604721
256MB	SFCF0256H1BK1MT-I-MS-553-SMA	604724
512MB	SFCF0512H1BK1MT-I-MS-553-SMA	604741
1GB	SFCF1024H1BK2MT-I-MO-553-SMA	604743
2GB	SFCF2048H1BK1MT-I-QT-553-SMA	604746
4GB	SFCF4096H1BK2MT-I-QP-553-SMA	604749
8GB	SFCF8192H1BK4MT-I-QT-553-SMA	604754

Table 3: Industrial Temp. Order Information

3.4 Offered OEM options

- Disabling MDMA and/or UDMA modes
- Customer specified card size and card geometry (C/H/S – cylinder/head/sector)
- Customer specified CIS and drive ID strings
- Preload service (also images with any file system)
- Customized front label
- ROM mode (write protected with preloaded software)
- Special Firmware solutions for additional customer requirements
- ...

4 Product Specification

The CompactFlash is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in three basic modes:

- PC card ATA I/O mode
- PC card ATA memory mode
- True IDE mode

The CompactFlash also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.
Standard cards are shipped as max. PIO6 and MDMA4 (80ns) and UDMA4 (30ns).
If the cards should be used in extended speed modes, they should be qualified on the target system and the system should fulfill the requirements listed below.
It conforms to the PCMCIA Card Specification 2.1 when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash™ Cards can be used with passive adapters in a PC-Card Type II or Type III socket.
The Card has an internal intelligent controller which manages interface protocols, data storage and retrieval as well as hardware RS-code Error Correction Code (ECC), defect handling, diagnostics and clock control.
The wear leveling mechanism assures an equal usage of the Flash memory cells to extend the life time.
Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware RS-code ECC allows to detect and correct 4 symbols per 528 Bytes.
The Card has a voltage detector and a powerful power-loss management feature to prevent data corruption after power-down.

The specification has been realized and approved by the CompactFlash Association (CFA).
This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design. The system highlights are shown in Table 4 ... Table 10.

Related Documentation:

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994
- CF+ and CompactFlash Specification Revision 3.0

4.1 System Performance

Table 4: System Performance

Parameter		Typ.	Max.	Unit
Sleep to write			5	ms
Sleep to read			5	
Power up to Ready		<500	1000	
Reset to Ready (PCMCIA/IDE Master)		200	500	
Data transfer Rate (UDMA4 burst)			66	MB/s
Sustained Read (measured)	128MB to 4GB	20	22	MB/s
	8GB	34	38	
Sustained Write (measured)	128MB to 4GB	8.5	10	
	8GB	17	20	
Random Read 4kB (measured)	128MB to 4GB	10000 (2500)	12000 (3000)	kB/s (IOPs)
	8GB	12000 (3000)	13000 (3250)	
Random Write 4kB (measured)	128MB to 4GB	180 (45)	200 (50)	
	8GB	155 (39)	170 (42)	
Command to DRQ	Read	100	2000	µs
	Write	30	1000	
Access Time	Read	0.22		ms

1. All values refer to Micron Flash chips
   CompactFlash Card in UDMA mode 4, cycle time 30ns in True-IDE mode with Sequential write/read test with 128kB/command.
   The number of flash and flash manufacturer is decoded in the part number, also the flash page size is depicted in this table.
   The densities are the current standard products.
   Sustained Speed depends on flash type and number, file size, and burst speed

Requirements for using extended speed (PIO 5, 6/ MDMA 3, 4)
(CompactFlash Specification 3.0; section 4.3.7)

The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:

1. Only one CF device shall be attached to the CF Bus.
2. The host shall not present a load of more than 40pF to the device for all signals, including any cabling.
3. The maximum cable length is 0.05 m (2 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported.
4. The –WAIT and IORDY signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes.

Ultra DMA Electrical Requirements
(CompactFlash Specification 3.0; section 4.3.8)

Operation in Ultra DMA mode requires careful attention to cabling, printed circuit board (PCB) trace routing and termination for reliable operation. These requirements are described in the following sections.

Host and Card signal capacitance limits for Ultra DMA operation
The host interface signal capacitance at the host connector shall be a maximum of 25pF for each signal as measured at 1 MHz.
The card interface signal capacitance at the card connector shall be a maximum of 20pF for each signal as measured at 1 MHz.

Series termination required for Ultra DMA operation
Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. The CF specification describes typical values for series termination at the host and the device.

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

Table 5: CF Card Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage (5V)	4.5V to 5.5V – 5.0V ±10%
Power Supply VCC Voltage (3.3V)	2.97V to 3.63V – 3.3V ±10%

Table 6: Current consumption (1)

Current Consumption (type)	3.3V	5V	Unit
Read (typ/max) 1ch	70 / 90	80 / 160(2)	mA
Write (typ/max) 1ch	70 / 90	70 / 80(2)	
Read (typ/max) 2ch	100 / 140	120 / 260(2)	mA
Write (typ/max) 2ch	80 / 130	100 / 140(2)	
Idle Mode (typ/max)	0.5 / 1.5	1 / 5(2)	

1. All values are typical at 25° C and nominal supply voltage and refer to 512MByte (1ch) or 4GByte (2ch) CompactFlash Card.
   Max values are for 256MB (1ch) and 4GB (2ch) cards in UDMA4 mode in IDE mode.
   The card goes to Sleep/idle mode 20ms (default) after last host command.
2. The card drives the lines with the applied voltage. Depending on the host interface current can flow to the host through the lines and the host clamb diodes, if the host inputs are supplied with 3.3V.

4.2.2 Recommended Storage Conditions

Table 7: CF Card Recommended Storage Conditions

Parameter	Value
Storage Temperature	-50°C to 100°C

4.2.3 Shock, Vibration, and Humidity

Table 8: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20 G peak, 20-2000Hz, 4 per direction (JEDEC JESD22, method B103) 5.35G RMS, 15 min per plane (IEC 68-2-6)
Shock	1.5k G peak, 0.5ms 5 times (JEDEC JESD22, method B110) 30 G, 11ms 1 time (IEC 68-2-27)

4.3 Physical Dimensions

Table 9: Physical Dimensions

Parameter	Value	Unit
Width	42.8	mm
Height	36.4	
Thickness	3.3	
Weight (typ.)	10	g

4.4 Reliability

Table 10: System Reliability and Maintenance

Parameter	Value
MTBF @ 25°C	> 3,000,000 hours (1)
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read (1)
Data Retention	10 years (JESD47)

(1) Dependent on final system qualification data.

4.5 Drive Geometry / CHS Parameter

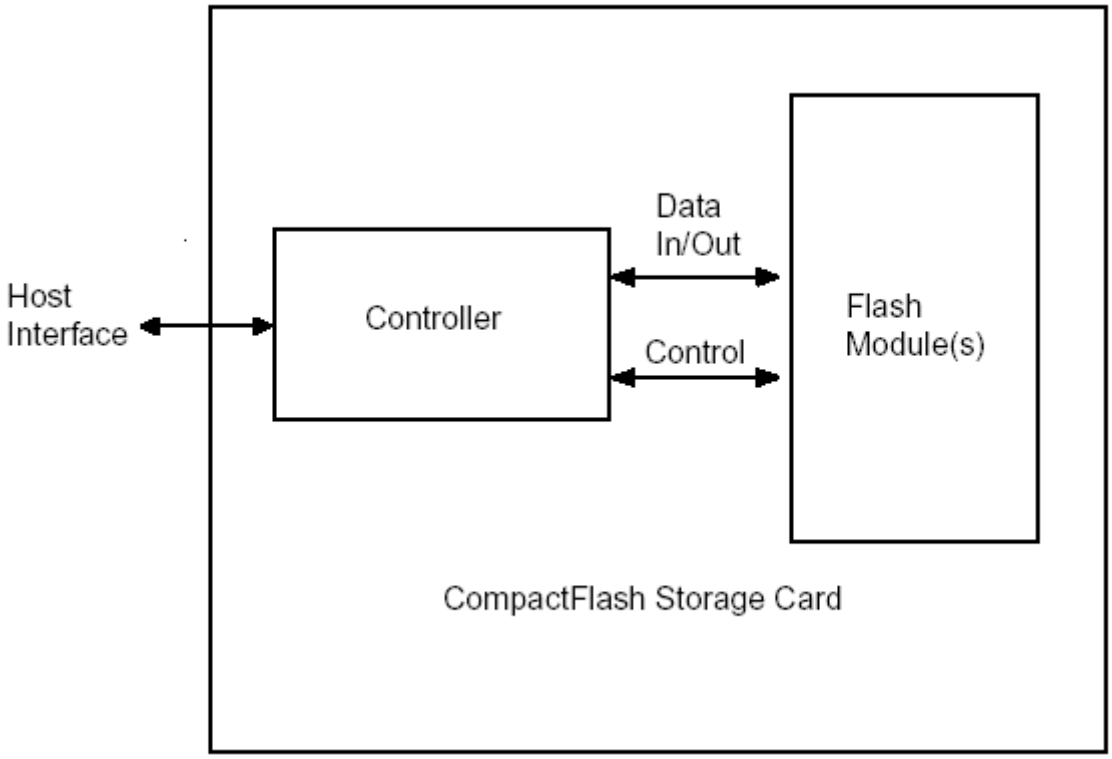
Table 11: CF capacity specification

Capacity	Cylinders	Heads	Sectors / track	Sectors	Total addressable capacity (Byte)
128MB	937	8	32	239,872	122,814,464
256MB	980	16	32	501,760	256,901,120
512MB	993	16	63	1,000,944	512,483,328
1GB	1,986	16	63	2,001,888	1,024,966,656
2GB	3,970	16	63	4,001,760	2,048,901,120
4GB	7,964	16	63	8,027,712	4,110,188,544
8GB	15,880	16	63	16,007,040	8,195,604,480

4.6 Physical description

The CompactFlash Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 shows the Block Diagram of the CompactFlash Memory Card.
The Card is offered in a Type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27mm) centers. Figure 21 shows Type I Card Dimensions.

Figure 1: CompactFlash Memory Card Block Diagram



5 Electrical interface

5.1 Electrical description

The CompactFlash Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode with MWDMA and UDMA, which is compatible with most disk drives

The signal/pin assignments are listed in Table 12 Low active signals have a '–' prefix. Pin types are Input, Output or Input/Output.
The configuration of the Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the memory card.

Table 13 describes the I/O signals. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.
All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

Table 12: Pin Assignment and Pin Type

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10[2]	I	I1Z
9[1]	-OE	I	I3U	-OE	I	I3U	-ATASEL	I	I3U
10	A09	I	I1Z	A09	I	I1Z	A09[2]	I	I1Z
11	A08	I	I1Z	A08	I	I1Z	A08[2]	I	I1Z
12	A07	I	I1Z	A07	I	I1Z	A07[2]	I	I1Z
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A06	I	I1Z	A06	I	I1Z	A06[2]	I	I1Z
15	A05	I	I1Z	A05	I	I1Z	A05[2]	I	I1Z
16	A04	I	I1Z	A04	I	I1Z	A04[2]	I	I1Z
17	A03	I	I1Z	A03	I	I1Z	A03[2]	I	I1Z
18	A02	I	I1Z	A02	I	I1Z	A02	I	I1Z
19	A01	I	I1Z	A01	I	I1Z	A01	I	I1Z
20	A00	I	I1Z	A00	I	I1Z	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3
24	WP	O	OT3	-IOIS16	O	OT3	-IOIS16	O	ON3
25	-CD2	O	Ground	-CD2	O	Ground	-CD2	O	Ground
26	-CD1	O	Ground	-CD1	O	Ground	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	D11[1]	I/O	I1Z,OZ3	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	D12[1]	I/O	I1Z,OZ3	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	D13[1]	I/O	I1Z,OZ3	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	-CE2[1]	I	I3U	-CS1[1]	I	I3Z
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I3U	-IORD	I	I3U	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z
35	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR[7] STOP[8][9]	I	I3Z
36	-WE	I	I3U	-WE	I	I3U	-WE[3]	I	I3U
37	READY	O	OT1	-IREQ	O	OT1	INTRQ	O	OZ1
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL[5]	I	I2Z	-CSEL[5]	I	I2Z	-CSEL	I	I2U

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode[4]		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
40	-VS2	O	OPEN	-VS2	O	OPEN	-VS2	O	OPEN
41	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
42	-WAIT	O	OT1	-WAIT	O	OT1	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1
43	-INPACK	O	OT1	-INPACK	O	OT1	DMARQ	O	OZ1
44	-REG	I	I3U	-REG	I	I3U	-DMACK[6]	I	I3U
45	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
47	D08[1]	I/O	I1Z,OZ3	D08[1]	I/O	I1Z,OZ3	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z,OZ3	D09[1]	I/O	I1Z,OZ3	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

1. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. The signal should be grounded by the host.
3. The signal should be tied to VCC by the host.
4. The mode is required for CompactFlash Storage Cards.
5. The –CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6. **If DMA operations are not used, the signal must be held high or tied to VCC by the host, also for read registers.**
7. Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9. Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. The signal should be grounded by the host.

Table 13: Signal Description

Signal Name	Dir.	Pin	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 to A0 (True IDE Mode)			In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
–STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
–PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
–SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
–DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15-D00 (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15-D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)		1, 50	Ground.
GND (PC Card I/O Mode)			Same for all modes.
GND (True IDE Mode)			Same for all modes.
–INPACK (PC Card Memory Mode)	0	43	This signal is not used in this mode.
–INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU.

Signal Name	Dir.	Pin	Description
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
–IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
–IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface.
–IORD (True IDE Mode)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.
HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
–CD1, –CD2 (PC Card Memory Mode)	O	26, 25	These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card or is fully inserted into its socket.
–CD1, –CD2 (PC Card I/O Mode)			This signal is the same for all modes.
–CD1, –CD2 (True IDE Mode)			This signal is the same for all modes.
–CE1, –CE2 (PC Card Memory Mode)	I	7, 32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 33, Table 41, Table 42Table 43, and Table 44.
–CE1, –CE2 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
–CS0, –CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
–CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.

Signal Name	Dir.	Pin	Description
–CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
–CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
–IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
–IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
–OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage in Memory Mode and to read the CIS and configuration registers.
–OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
–ATASEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
–IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
–REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
–REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
–DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
–RESET (True IDE Mode)			In the True IDE Mode, this input pin is the **active low** hardware reset from the host.
Vcc (PC Card Memory Mode)		13, 38	+5V, +3.3V power.
Vcc (PC Card I/O Mode)			Same for all modes.
Vcc (True IDE Mode)			Same for all modes.
–VS1, –VS2 (PC Card Memory Mode)	0	33, 40	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
–VS1, –VS2 (PC Card I/O Mode)			This signal is the same for all modes.
–VS1, –VS2 (True IDE Mode)			This signal is the same for all modes.
–WAIT (PC Card Memory Mode)	0	42	The –WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
–WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
–DDMARDY (True IDE Mode – Ultra DMA Write Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
DSTROBE (True IDE Mode – Ultra DMA Read Mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
–WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
–WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
–WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	0	24	Memory Mode – The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (–IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
–IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

5.2 Electrical Specification

Table 14 defines the DC Characteristics for the CompactFlash Memory Card. Unless otherwise stated, conditions are:

- Vcc = 5V ± 10%
- Vcc = 3.3V ± 10%
- 0 °C to +85 °C

Table 14 shows that the Card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.
The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 14.
Table 15 shows the Input Leakage Current, Table 16 the Input Characteristics, Table 17 the Output Drive Type and Table 18 the Output Drive Characteristics.

Table 14: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V
Voltage on any pin except VCC with respect to GND	V	-0.5V to VCC +0.5V

Table 15: Input Leakage current(1)

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	V_{IH} =Vcc V_{IL} = GND	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50		500	kOhm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50		500	kOhm

1. x refers to the characteristics described in Table 16 For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 16: Input characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			Vcc = 3.3V			Vcc = 5.0V			
1	Input Voltage CMOS	V_{IH}	2.0		3.6	2.0		5.3	V
		V_{IL}	-0.3		0.6	-0.3		0.8	
2	Input Voltage CMOS	V_{IH}	2.0		3.6	2.0		5.3	V
		V_{IL}	-0.3		0.6	-0.3		0.8	
3	Input Voltage CMOS Schmitt Trigger	V_{TH}	2.0		3.6	2.0		5.3	V
		V_{TL}	-0.3		0.6	-0.3		0.8	

Table 17: Output Drive Type(1)

Type	Output Type	Valid Conditions
Otx	Totempole	I_{OH} & I_{OL}
Ozx	Tri-State N-P Channel	I_{OH} & I_{OL}
Opx	P-Channel Only	I_{OH} only
Onx	N-Channel Only	I_{OL} only

1. x refers to the characteristics described in Table 16 For example, OT3 refers to totem pole output with a type 3 output drive characteristic.

Table 18: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
2	Output Voltage	V_{OH}	I_{OH} = -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
3	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
	Tri-State	I_{OZ}	V_{OL}= Gnd	-10		10	µA
X	Leakage Current		V_{OH} = Vcc				

5.3 Additional requirements for CompactFlash Advanced Timing mode

When operating in a CompactFlash Advanced timing mode, the following conditions must be respected:

- **Only one CompactFlash Card must be connected to the CompactFlash bus.**
- The load capacitance (cable included) for all signals must be lower than 40pF.
- The cable length must be **lower than 0.15m** (6 inches). The cable length is measured from the Card connector to the host controller. **0.46m (18 inches) cables are not supported**.

6 Command Interface

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. Two types of bus cycles are also available in True IDE interface type: PIO transfer and Multi-Word DMA transfer.

Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, and Table 26 show the read and write timing parameters. Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 and Figure 9 show the read and write timing diagrams.

In order to set the card mode, the –OE (-ATASEL) signal must be set and kept stable before applying VCC until the reset phase is completed. To place the card in Memory mode or I/O mode, -OE (-ATASEL) must be driven High, while it must be driven Low to place the card in True IDE mode.

6.1 Attribute Memory Read and Write

Figure 2: Attribute Memory Read waveforms

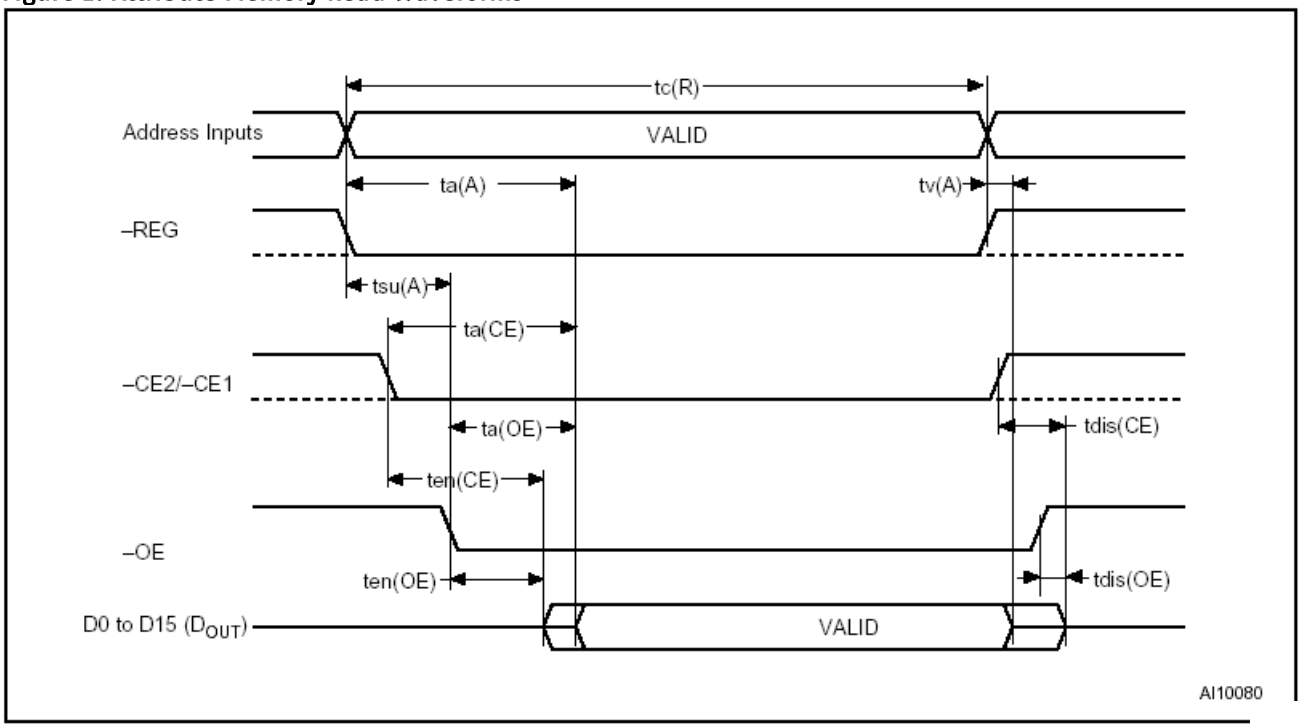
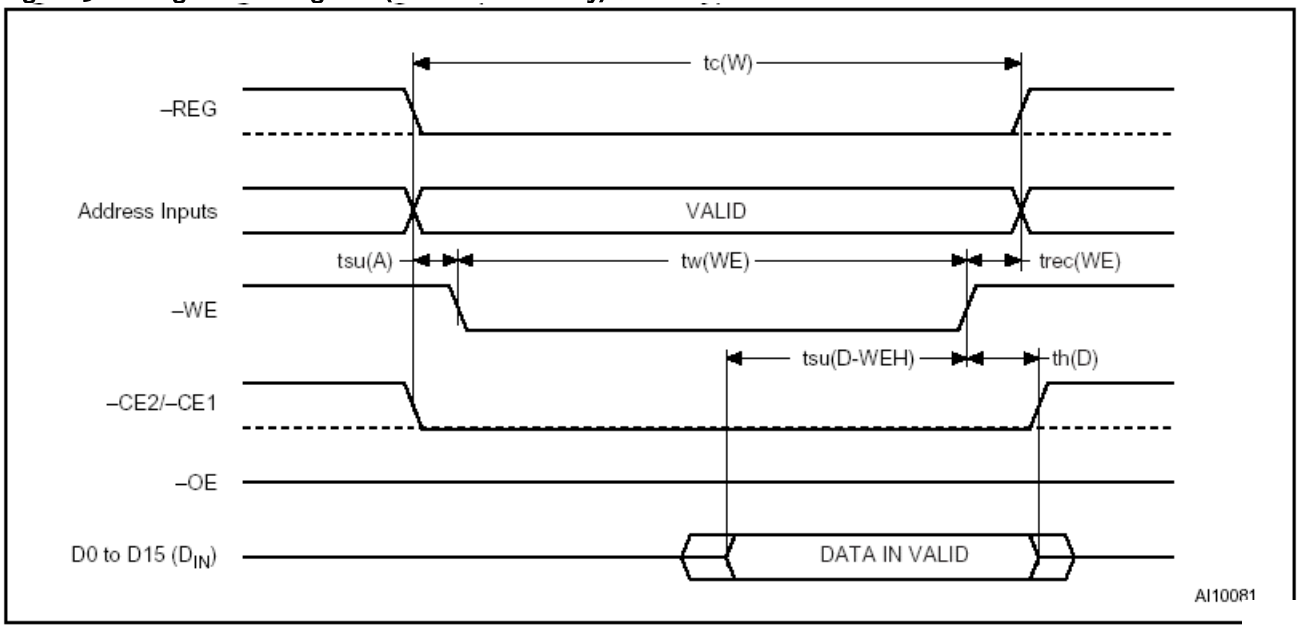


Table 19: Attribute Memory Read timing

Speed version			300ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Read Cycle Time	tcl	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Setup Time	tsu(A)	tAVWL	30	

Figure 3: Configuration Register (Attribute Memory) Write waveforms



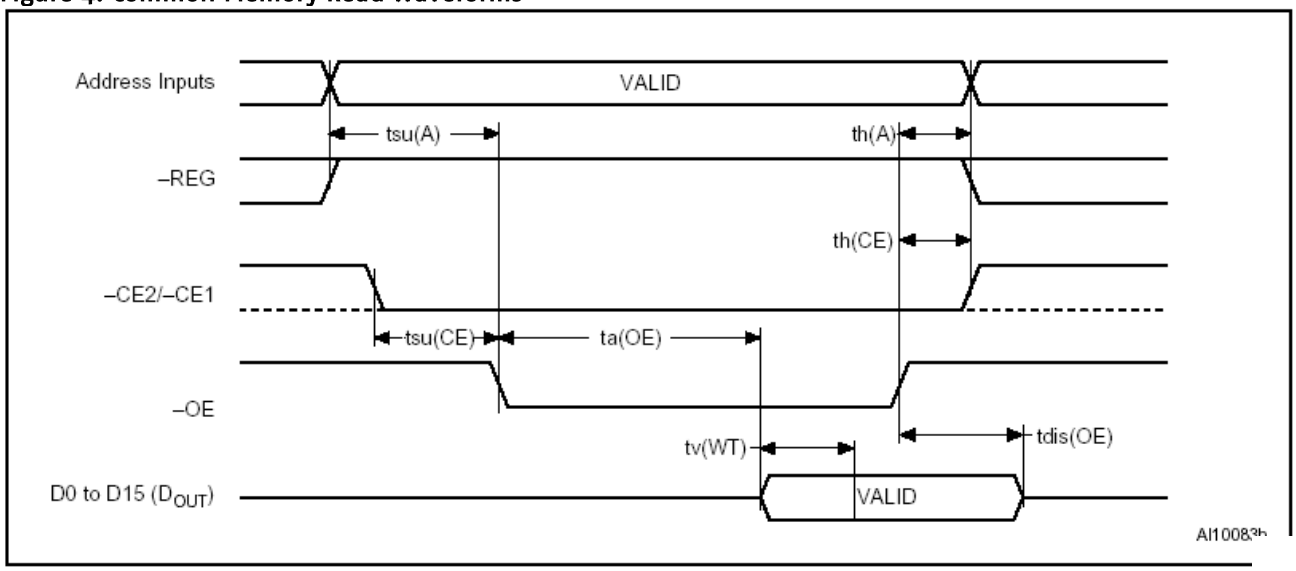
16 D_{IN} signifies data provided by the system to the CompactFlash Card.

Table 20: Configuration Register (Attribute Memory) Write timing

Speed Version			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	

6.2 Common Memory Read and Write

Figure 4: Common Memory Read waveforms



17 D_{OUT} means data provided by the CompactFlash Memory Card to the system.

Table 21: Common Memory Read timing (1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	

18 Swissbit CF does not assert the WAIT signal.

Figure 5: Common Memory Write Waveforms

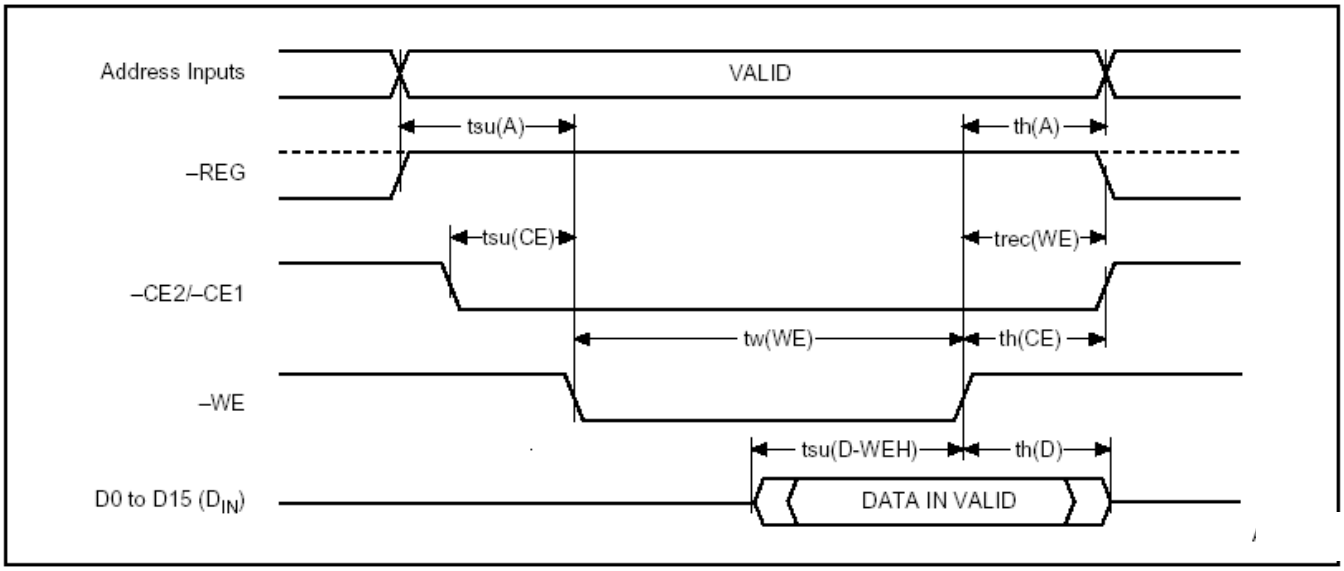


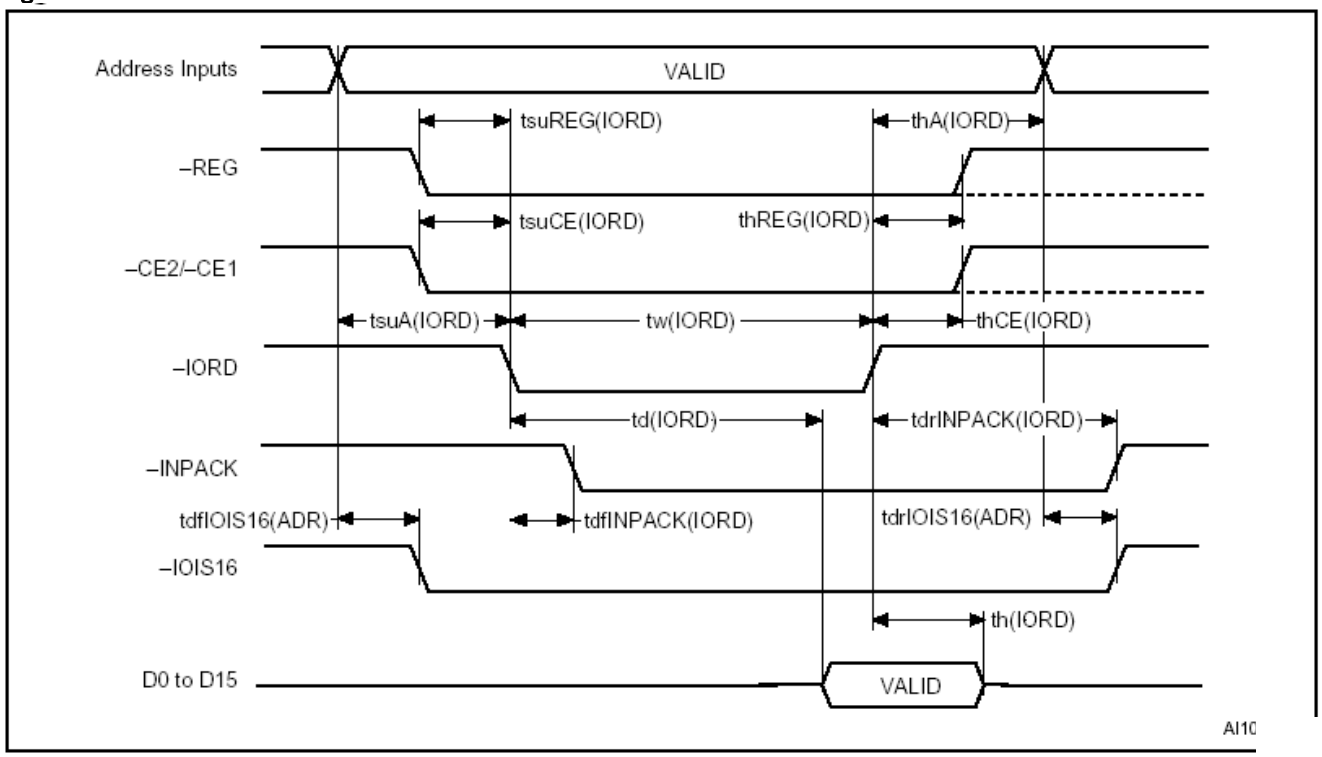
Table 22: Common Memory Write Timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tIWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	

19 Swissbit CF does not assert the WAIT signal.

6.3 I/O Read and Write

Figure 6: I/O Read waveforms



20 DOUT signifies data provided by the CompactFlash Memory Card or to the system.

Table 23: I/O Read timing(1)

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	0	NA(2)	0	NA(2)	0	NA(2)
NPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45		NA(2)		NA(2)		NA(2)
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35						
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35						

1. Swissbit CF does not assert the WAIT signal.
2. –IOIS16 is not supported in this mode.

Figure 7: I/O Write waveforms

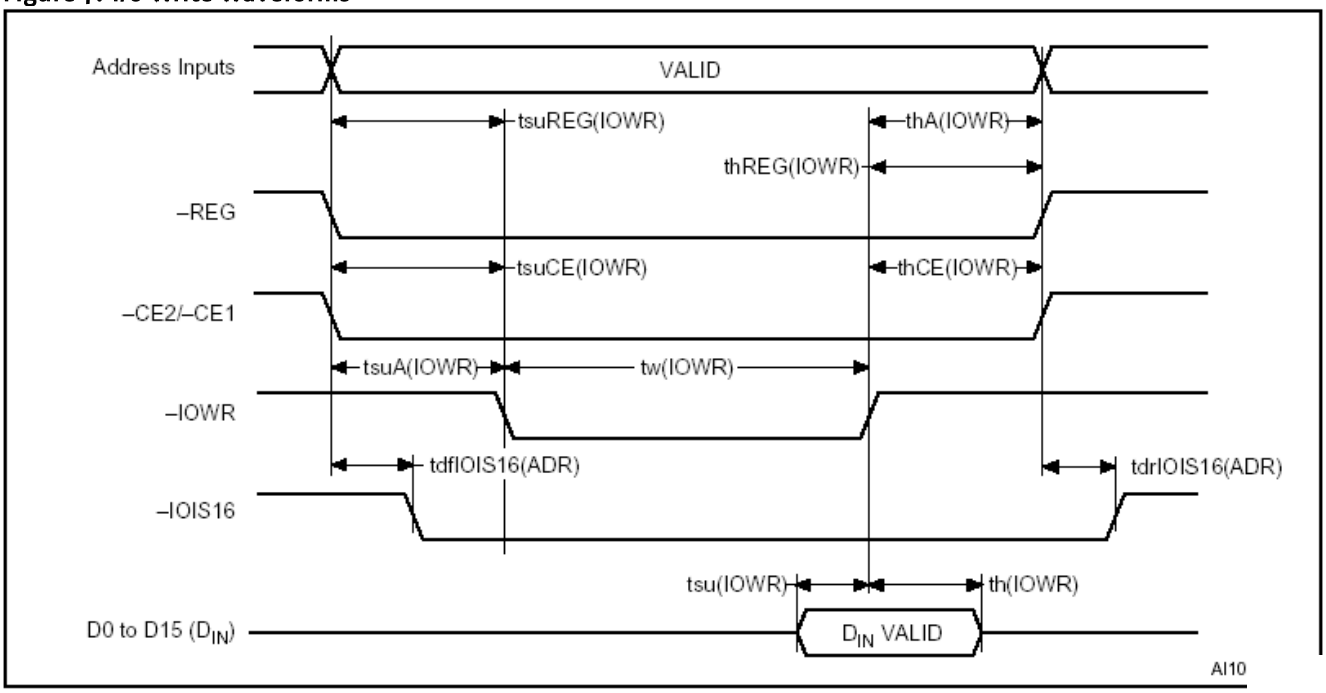


Table 24: I/O write timing

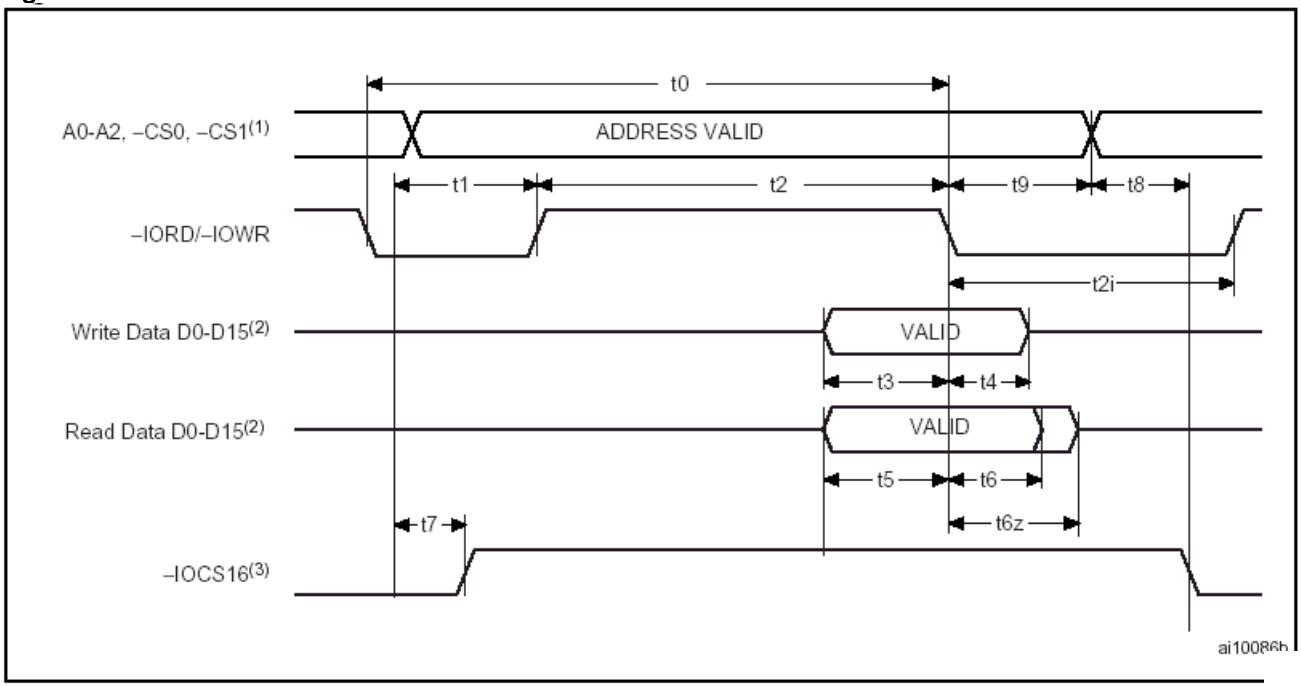
Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Addr.	tdfIOIS16(ADR)	tAVISL		35		NA(2)		NA(2)		NA(2)
IOIS16 Delay Rising from Addr.	tdrIOIS16(ADR)	tAVISH		35		NA(2)		NA(2)		NA(2)

1. D_{IN} signifies data provided by the system to the CompactFlash Memory Card.
2. –IOIS16 and –INPACK are not supported in this mode.

6.4 True IDE Mode

The timing waveforms for True IDE mode and True IDE DMA mode of operation in this section are drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the waveforms inverted from their electrical states on the bus.

Figure 8: True IDE PIO mode Read/Write waveforms



1. The device addresses consists of –CS0, –CS1, and A2–A0.
2. The Data I/O consist of D15–D0 (16–bit) or D7–D0 (8 bit).
3. –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

Table 25: True IDE PIO mode Read/Write timing(1)

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)	5(5) (ns)	6(5) (ns)
Cycle time (min)	t_0(2)	600	383	240	180	120	100	80
Address Valid to –IORD/–IOWR setup (min)	t_1	70	50	30	30	25	15	10
–IORD/–IOWR (min)	t_2(2)	165	125	100	80	70	65	55
–IORD/–IOWR (min) Register (8 bit)	t_2(2)	290	290	290	80	70	65	55
–IORD/–IOWR recovery time (min)	t_{2i}(2)	–	–	–	70	25	25	20
–IOWR data setup (min)	t_3	60	45	30	30	20	20	15
–IOWR data hold (min)	t_4	30	20	15	10	10	5	5
–IORD data setup (min)	t_5	50	35	20	20	20	15	10
–IORD data hold (min)	t_{6z}(3)	5	5	5	5	5	5	5
–IORD data tri–state (max)	t_7(4)	30	30	30	30	30	20	20
Address valid to –IOCS16 assertion (max)	t_8(4)	90	50	40	NA	NA	NA	NA
Address valid to –IOCS16 released (max)	t_7	60	45	30	NA	NA	NA	NA
–IORD/–IOWR to address valid hold	t_9	20	15	10	10	10	10	10

1. The maximum load on –IOCS16 is 1 LSTTL with a 50pF total load.
2. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements of to, t_2, and t_{2i} have to be met. The requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can ensure that to is equal to or greater than the value reported in the devices identify drive Card implementation should support any legal host implementation.
3. This parameter specifies the time from the falling edge of –IORD to the moment when the CompactFlash Memory Card (tri–state).
4. t_7 and t_8 apply only to modes 0, 1 and 2. The –IOCS16 signal is not valid for other modes.

Figure 9: True IDE Multi-Word DMA Mode Read/Write waveforms

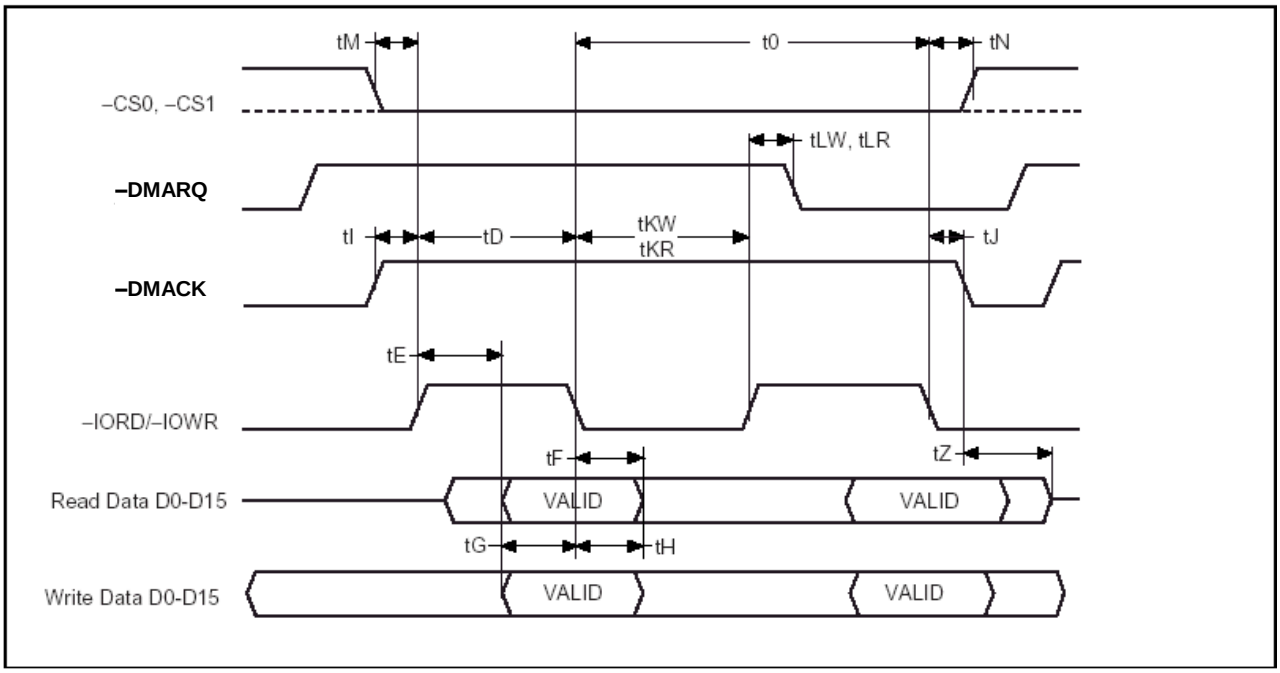


Table 26: True IDE Multi-Word DMA Mode Read/Write timing

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)
Cycle time (min)	t_0 (1)	480	150	120	100	80
-IORD / -IOWR asserted width (min)	t_D (1)	215	80	70	65	55
-IORD data access (max)	t_E	150	60	50	50	45
-IORD data hold (min)	t_F	5	5	5	5	5
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10
-IOWR data hold (min)	t_H	20	15	10	5	5
DMACK to –IORD/-IOWR setup (min)	t_I	0	0	0	0	0
-IORD / -IOWR to –DMACK hold (min)	t_J	20	5	5	5	5
-IORD Low width (min)	t_{KR} (1)	50	50	25	25	20
-IOWR Low width (min)	t_{KW} (1)	215	50	25	25	20
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35
CS(1:0) valid to –IORD / -IOWR	t_M	50	30	25	10	5
CS(1:0) hold	t_N	15	10	10	10	10
-DMACK	t_Z	20	25	25	25	25

1. t_0 is the minimum total cycle time. T_D is the minimum command active time. T_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles, respectively. The actual cycle time is the sum of the actual command active time and the actual command inactive time. The timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be respected. T_0 is higher than t_D + t_{KR} or t_D + t_{KW}, for input and output cycles respectively. This means the host can lengthen either t_D or t_{KR}/t_{KW}, or both, to ensure that t_0 is equal to or higher than the value reported in the devices identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

6.5 Ultra DMA Mode

6.5.1 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).
Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 27: Ultra DMA Signal Usage In Each Interface Mode

Table 27: Ultra DMA Signal Usage In Each Interface Mode

UDMA Signal	Type	Pin # (Non UDMA MEM MODE)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	43 (-INPACK)	-DMARQ	-DMARQ	DMARQ
DMACK	Input	44 (-REG)	-DMACK	DMACK	-DMACK
STOP	Input	35 (-IOWR)	STOP [1]	STOP [1]	STOP [1]
HDMARDYI HSTROBE(W)	Input	34 (-IORD)	-HDMARDYI [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDYI [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDYI [1, 2] HSTROBE(W) [1, 3, 4]
DDMARDY(W) DSTROBEI	Output	42 (-WAIT)	-DDMARDY(W) [1, 3] DSTROBEI [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBEI [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBEI [1. 2. 4]
DATA	Bidir	… (D[15:00])	D[15:00]	D[15:00]	D[15:00]
ADDRESS	Input	… (A[10:00])	A[10:00]	A[10:00]	A[02:00] [5]
CSEL	Input	39 (-CSEL)	-CSEL	-CSEL	-CSEL
INTRQ	Output	37 (READY)	READY	-INTRQ	INTRQ
Card Select	Input	7 (-CE1) 31 (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

1. The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2. The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3. The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4. The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5. Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume these definitions when:

1. an Ultra DMA mode is selected, and
2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3. the device asserts (-)DMARQ, and
4. the host asserts –DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of –DMACK by the host at the termination of an Ultra DMA burst.
With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst. During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.
Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.
An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.
Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE – If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

6.5.2 Restrictions and Considerations During Ultra DMA Commands

There are number of important restrictions and considerations for the implementation and use of Ultra DMA commands in CompactFlash devices. These are highlighted in the subsections below.
Additional restrictions on specific modes of operation are given in sections 5.3 and 6.5.3

6.5.2.1 System Restrictions for Ultra DMA modes 3 and above

Ultra DMA modes 3 and above are valid only for systems that meet the requirements of section 5.3

6.5.2.2 UDMA Address and Card Enable Signals

The Card Enable signals (-CE1 / -CS0 and –CE2 / -CS1) shall remain negated during Ultra DMA data bursts.
The Address bus (A[10:00]) shall not transition unnecessarily during the UDMA command and shall remain fixed during an Ultra DMA data burst. In True IDE mode, the address lines (A[02:00]) shall be held to all zeros. This will reduce unnecessary noise during the UDMA command.

6.5.2.3 Task File registers shall not be written during an Ultra DMA command

The task file registers shall not be written after an Ultra DMA command is issued by the host and before the command completes. Writing to the device control register is permitted between bursts, but is expected to occur only to reset the card after an unrecoverable protocol error.

6.5.2.4 Ultra DMA transfers shall be 16 bits wide

All transfers during an Ultra DMA data burst are 16 bit wide transfers. The Set Features command that controls the bus width for PIO transfers does not affect the width of Ultra DMA transfers.

6.5.2.5 No Access to Memory or I/O Space during an Ultra DMA Data Burst

No access to common or attribute memory or to I/O space on the device is permitted during an Ultra DMA data burst.

6.5.3 Specific rules for PC Card Memory Mode Ultra DMA

In addition to the general restrictions for all Ultra DMA operations, these additional considerations exist for PC Card Memory Mode Ultra DMA operations.

6.5.3.1 No Access to Attribute Memory during PC Card Memory Mode DMA Commands

The host shall not attempt to access Attribute Memory space during a PC Card Memory Mode DMA command either before, between or within Ultra DMA data bursts.

6.5.3.2 READY signal handling during DMA commands in PC Card Memory Mode

In PC Card Memory Mode, the READY signal shall be negated (made BUSY) by the device upon receipt of a DMA command and shall remain negated until the command has completed at which time it shall be re-asserted. This treatment allows the host to receive a single interrupt at the end of the command and avoids the extra overhead that would be associated with processing busy to ready transitions for each sector transferred as is the case when the READY toggles at the end of every sector of PIO Memory Mode transfers.
The BSY bit in the status register is permitted to be negated in the status register at any time that the DRQ bit in the status register is asserted. The only restriction is that either DRQ or BSY or both must remain asserted while the command is in progress.

6.5.4 Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see: 6.5.4.4 , for the detailed protocol descriptions for each of these phases. Table 28: Ultra DMA Data Burst Timing Requirements and Table 29: Ultra DMA Data Burst Timing Descriptions define the specific timing requirements). In the following rules –DMARDY is used in cases that could apply to either –DDMARDY or –HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA burst is defined as the period from an assertion of –DMACK by the host to the subsequent negation of –DMACK.
2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 6, 5, 4, or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

6.5.4.1 Ultra DMA Burst Initiation Phase Rules

1. An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
2. An Ultra DMA burst shall always be requested by a device asserting DMARQ.
3. When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting –DMACK.
4. A host shall never assert –DMACK without first detecting that DMARQ is asserted.
5. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that –DMACK is asserted, STOP negated, and –HDMARDY is asserted.
6. After asserting DMARQ or asserting –DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
7. After negating STOP or asserting –HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

6.5.4.2 Ultra DMA Data transfer phase rules

1. The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
2. A recipient pauses an Ultra DMA burst by negating –DMARDY and resumes an Ultra DMA burst by reasserting –DMARDY.
3. A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate –DMARDY and wait the required period before signaling a termination request.
5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

6.5.4.3 Ultra DMA Burst Termination Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA burst.
2. Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.
3. An Ultra DMA burst shall be paused before a recipient requests a termination.
4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
7. A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.
8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

6.5.4.4 Ultra DMA Data Transfers Timing

Table 28 and Table 29 define the timings associated with all phases of Ultra DMA bursts.

Table 28: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes:

1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.
3. The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4. The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
5. The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.
6. See the AC Timing requirements in Table 29: Ultra DMA Data Burst Timing Descriptions.

Table 29: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until –DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from –DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
T_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
T_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from –DMACK to STOP and –HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating –DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for –DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1. The parameters t_{UI}, t_{MLI} (in Figure 13: Ultra DMA Data-In Burst Device Termination Timing and Figure 14: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. T_{UI} is an unlimited interlock that has no maximum time value. T_{MLI} is a limited time-out that has a defined minimum. T_{LI} is a limited time-out that has a defined maximum.
2. 80-conductor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.
3. Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4. For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5. The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Table 30: Ultra DMA Sender and Recipient IC Timing Requirements

Name	Comments	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0		9.0		9.0	

Notes:

1. All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.
2. The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
3. The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 31: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:

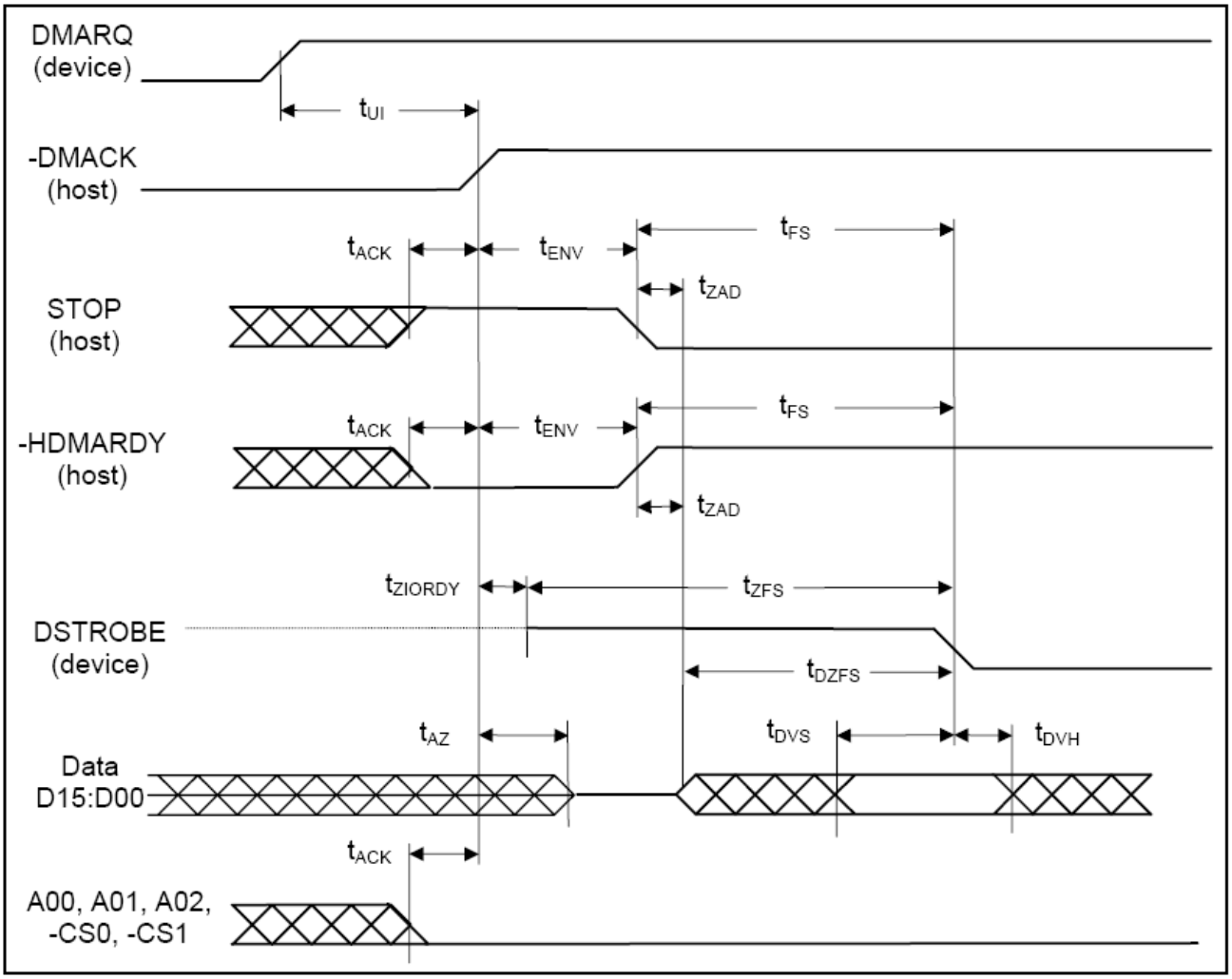
1. The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.
   The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.
   Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 ns apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

6.5.4.4.1 Initiating an Ultra DMA Data-In Burst

a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 10: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.
b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:
c) The host shall keep –DMACK in the negated state before an Ultra DMA burst is initiated.
d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
e) Steps I, (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
f) The host shall negate –HDMARDY.
g) The host shall negate –CS0, -CS1, DA2, DA1, and DA0. The host shall keep –CS0, -CS1, DA2, DA1, and DA0 negated until after negating –DMACK at the end of the burst.
h) Steps I, (d), and (e) shall have occurred at least t_{ACK} before the host asserts –DMACK. The host shall keep –DMACK asserted until the end of an Ultra DMA burst.
i) The host shall release D[15:00] within t_{AZ} after asserting –DMACK.

j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted –DMACK. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated –DMACK at the end of an Ultra DMA burst.
k) The host shall negate STOP and assert –HDMARDY within t_{ENV} after asserting –DMACK. After negating STOP and asserting –HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
l) The device shall drive D[15:00] no sooner than t_{ZAD} after the host has asserted –DMACK, negated STOP, and asserted –HDMARDY.
m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).
n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted –HDMARDY. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto D[15:00].

Figure 10: Ultra DMA Data-In Burst Initiation Timing



Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and –IOWR:STOP signal lines are not in effect until DMARQ and –DMACK are asserted.

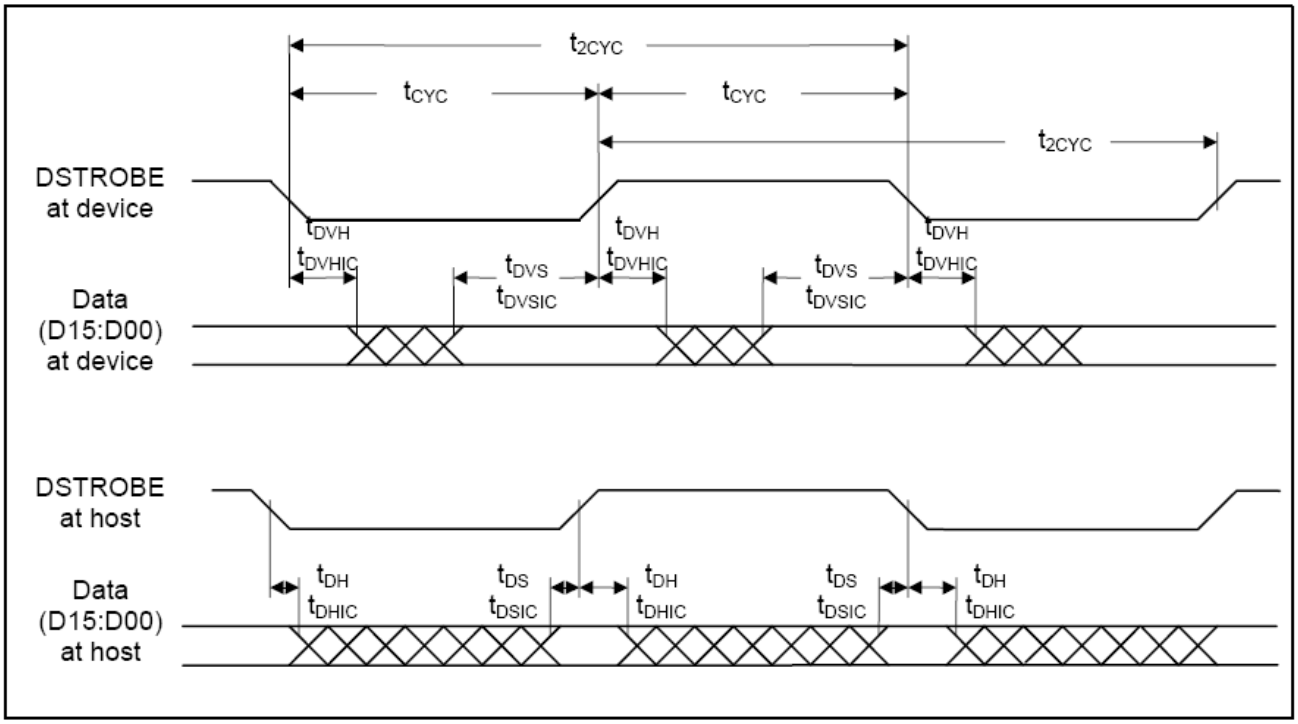
6.5.4.4.2 Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 11: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].
b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.
c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.
d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

Figure 11: Sustained Ultra DMA Data-In Burst Timing



Notes: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

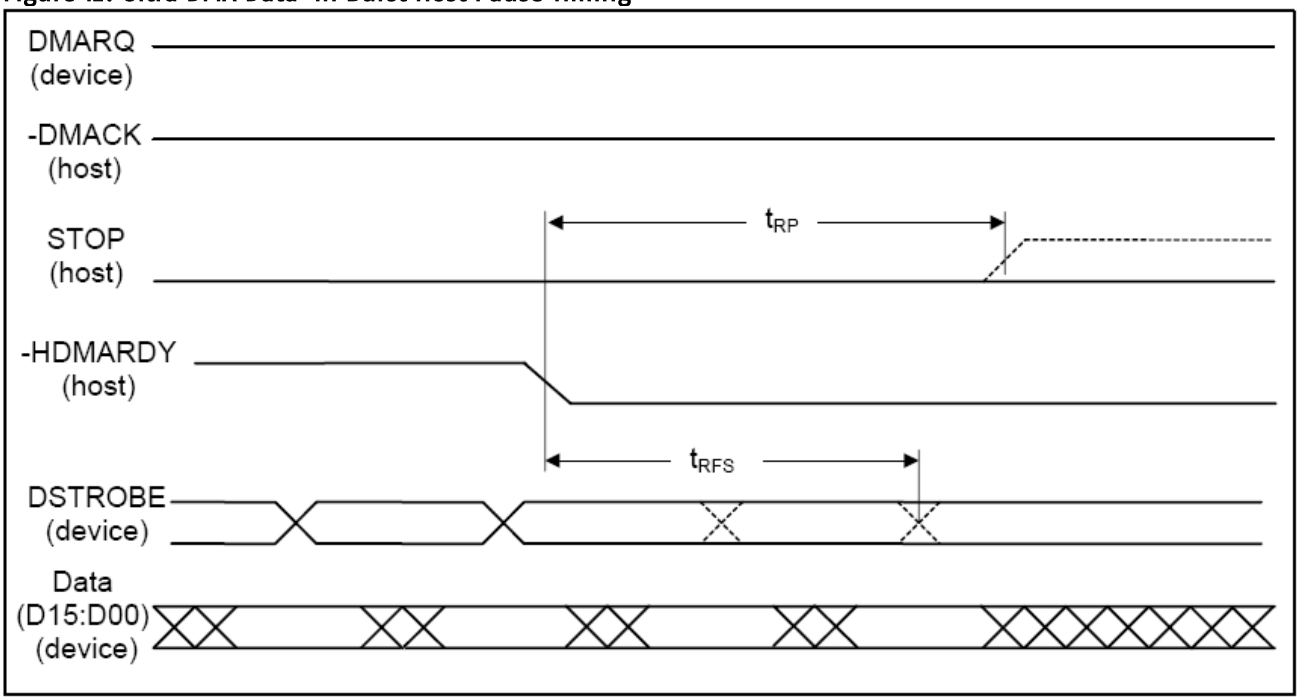
6.5.4.4.3 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 12: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall pause an Ultra DMA burst by negating –HDMARDY.
c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating –HDMARDY.
d) If the host negates –HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates –HDMARDY greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
e) The host shall resume an Ultra DMA burst by asserting –HDMARDY.

Figure 12: Ultra DMA Data-In Burst Host Pause Timing



Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after –HDMARDY is negated.
2. After negating –HDMARDY, the host may receive zero, one, two, or three more data words from the device.

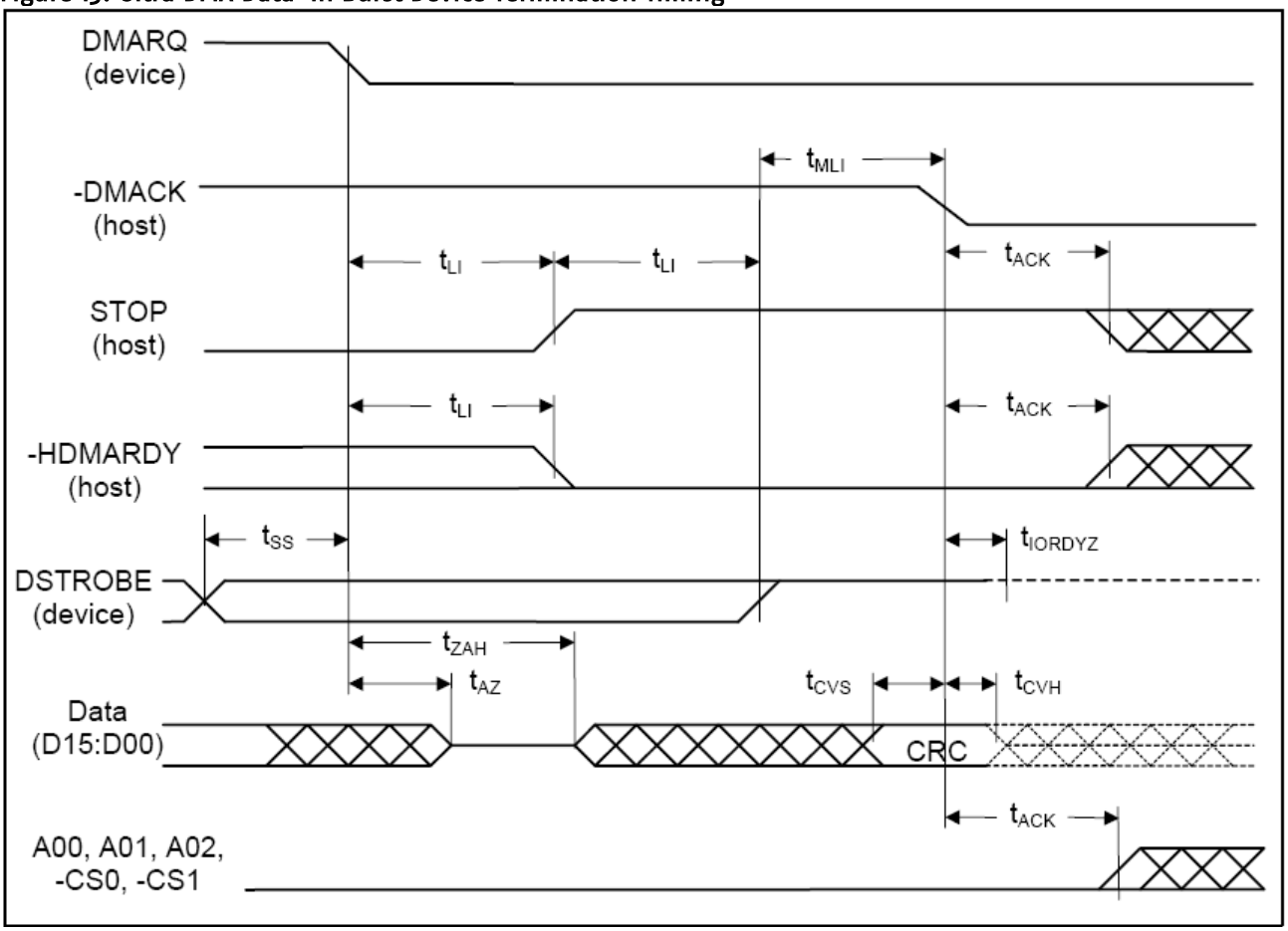
6.5.4.4.4 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 13: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra
b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.
c) NOTE – The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate
d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

Figure 13: Ultra DMA Data-In Burst Device Termination Timing



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.5.4.4.5 Host Terminating an Ultra DMA Data-In Burst

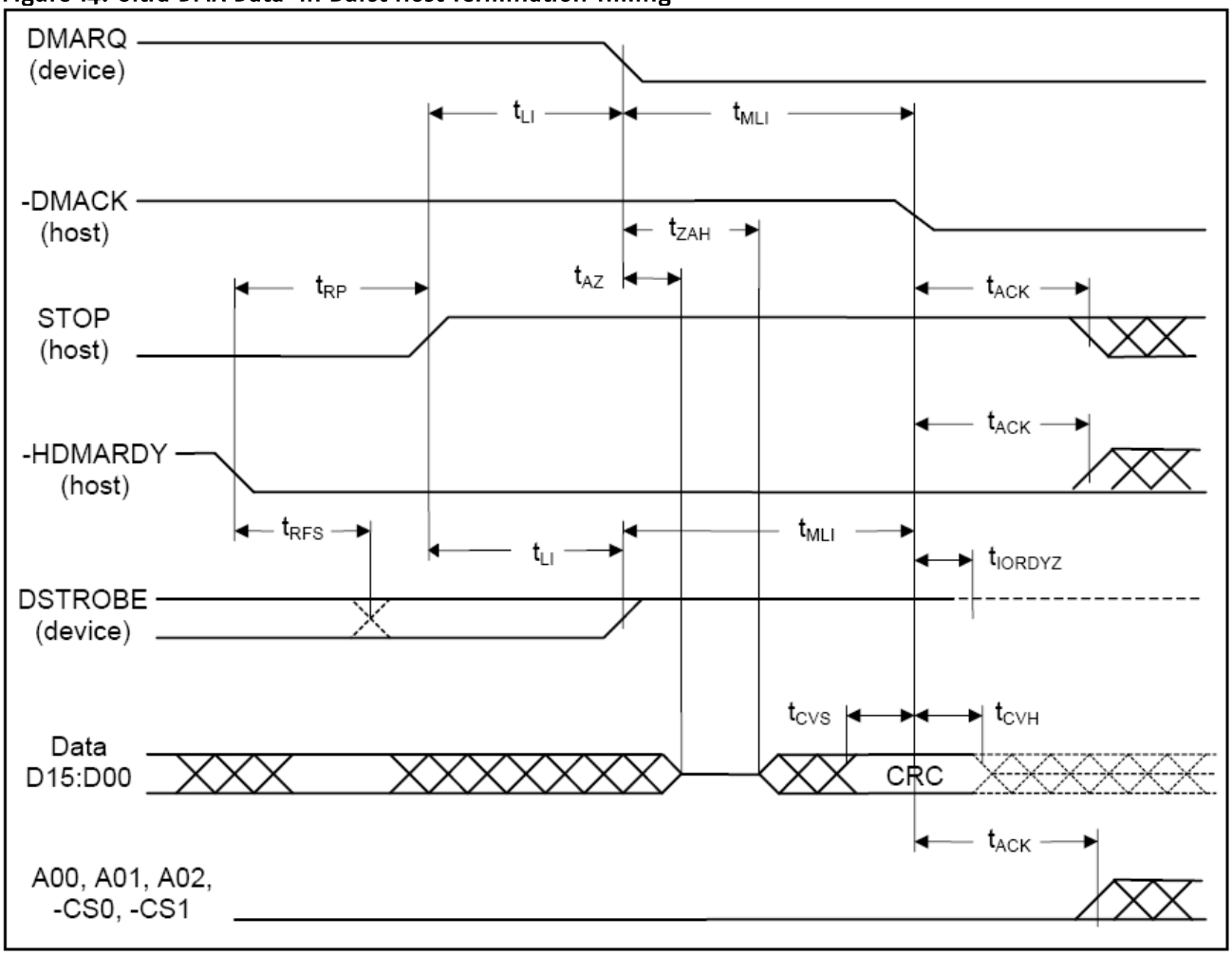
The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 14: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall initiate Ultra DMA burst termination by negating –HDMARDY. The host shall continue to negate –HDMARDY until the Ultra DMA burst is terminated.
c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating –HDMARDY
d) If the host negates –HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDYgreater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
e) The host shall assert STOP no sooner than t_{RP} after negating –HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.
i) The host shall drive DD D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation (see 6.5.4.5).

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00] (see 6.5.4.5).
k) The host shall negate –DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated –HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].
l) The device shall latch the host's CRC data from D[15:00] on the negating edge of –DMACK.
m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 6.5.4.5).
n) The device shall release DSTROBE within t_{IORDYZ} after the host negates –DMACK.
o) The host shall neither negate STOP nor assert –HDMARDY until at least t_{ACK} after the host has negated –DMACK.
p) The host shall not assert –IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

Figure 14: Ultra DMA Data-In Burst Host Termination Timing



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

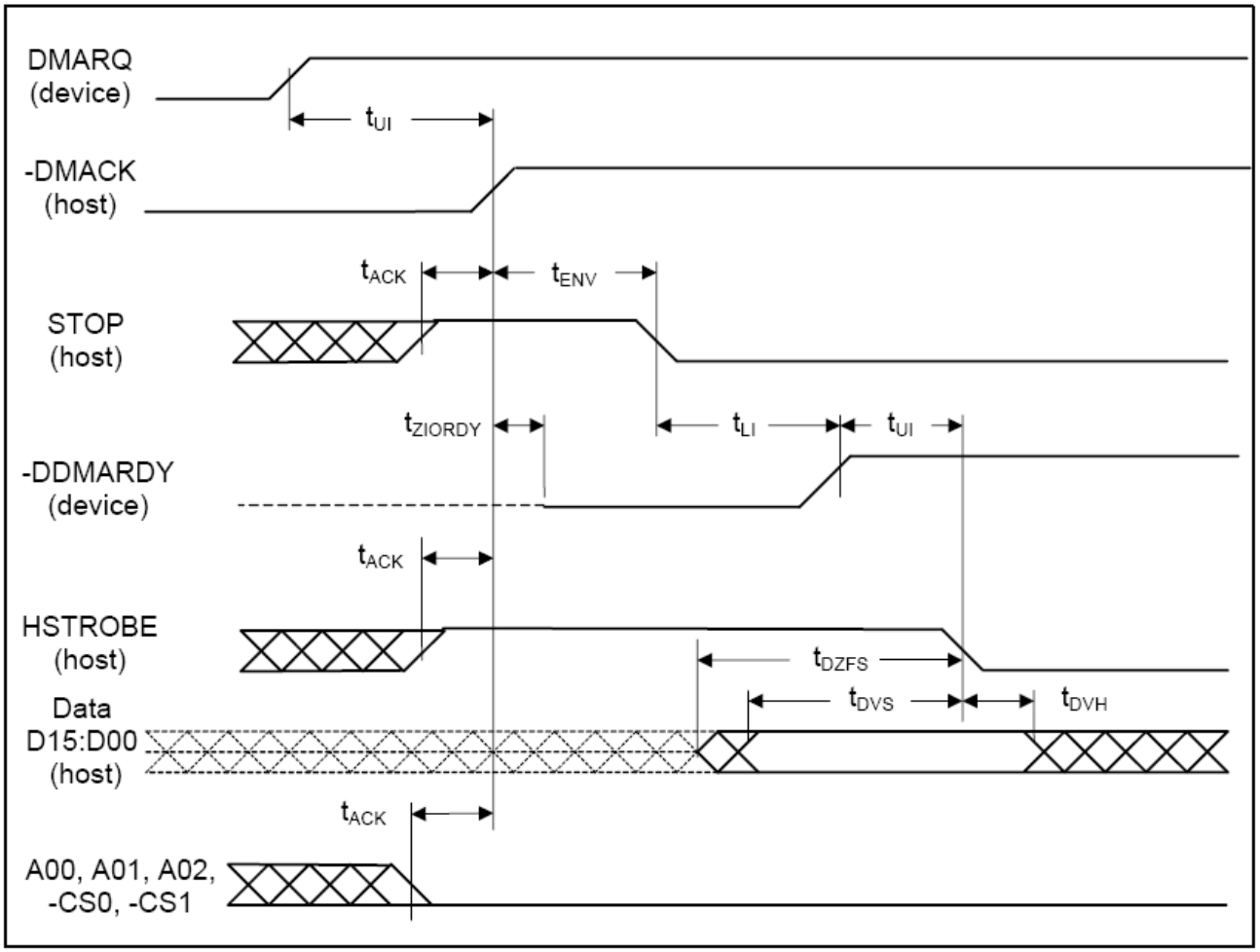
6.5.4.4.6 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 15: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:
a) The host shall keep –DMACK in the negated state before an Ultra DMA burst is initiated.
b) The device shall assert DMARQ to initiate an Ultra DMA burst.
c) Steps I, (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
d) The host shall assert HSTROBE.

e) The host shall negate –CS0, -CS1, DA2, DA1, and DA0. The host shall keep –CS0, -CS1, DA2, DA1, and DA0 negated until after negating –DMACK at the end of the burst.
f) Steps I, (d), and (e) shall have occurred at least t_{ACK} before the host asserts –DMACK. The host shall keep –DMACK asserted until the end of an Ultra DMA burst.
g) The device may negate –DDMARDY t_{ZIORDY} after the host has asserted –DMACK. Once the device has negated –DDMARDY, the device shall not release –DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
h) The host shall negate STOP within t_{ENV} after asserting –DMACK. The host shall not assert STOP until after the first negation of HSTROBE.
i) The device shall assert –DDMARDY within t_{LI} after the host has negated STOP. After asserting DMARQ and –DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.
k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted –DDMARDY. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto D[15:00].

Figure 15: Ultra DMA Data-Out Burst Initiation Timing



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

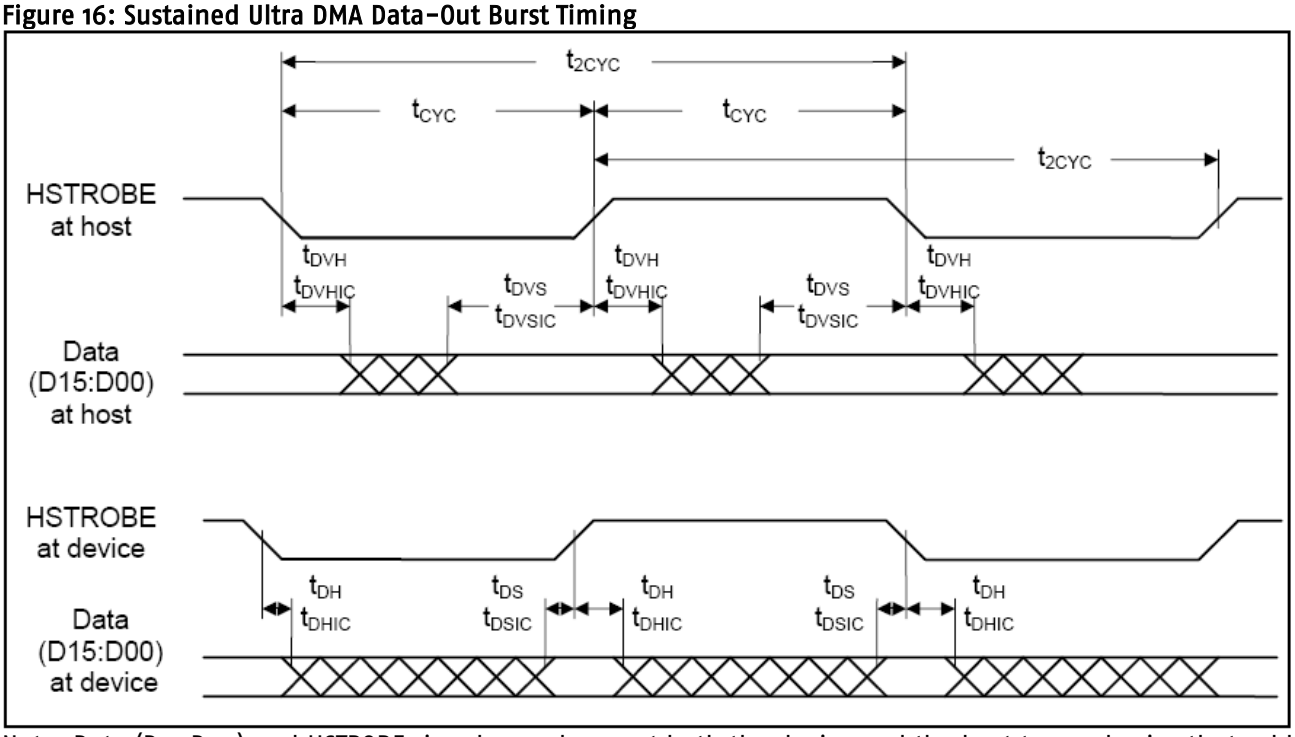
6.5.4.4.7 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 16: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:
a) The host shall drive a data word onto D[15:00].

b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than $2t_{CYC}$ for the selected Ultra DMA mode.
c) The host shall not change the state of D[15:00] until at least t_{DVH} after generating an HSTROBE edge to latch the data.
d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

Figure 16: Sustained Ultra DMA Data-Out Burst Timing



Note: Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

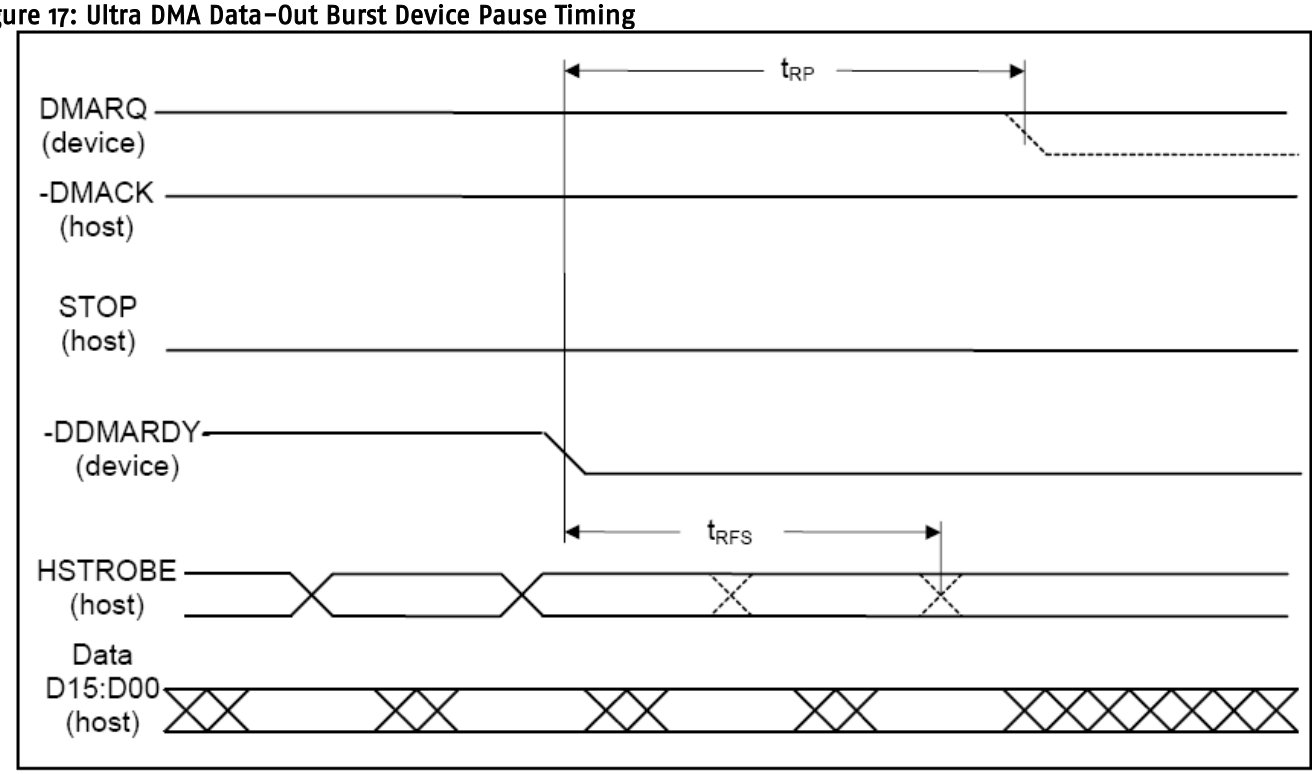
6.5.4.4.8 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 17: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall pause an Ultra DMA burst by negating –DDMARDY.
c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating –DDMARDY.
d) If the device negates –DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates –DDMARDY greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
e) The device shall resume an Ultra DMA burst by asserting –DDMARDY.

Figure 17: Ultra DMA Data-Out Burst Device Pause Timing



Notes:

1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after -DDMARDY is negated.
2. After negating –DDMARDY, the device may receive zero, one, two, or three more data words from the host.

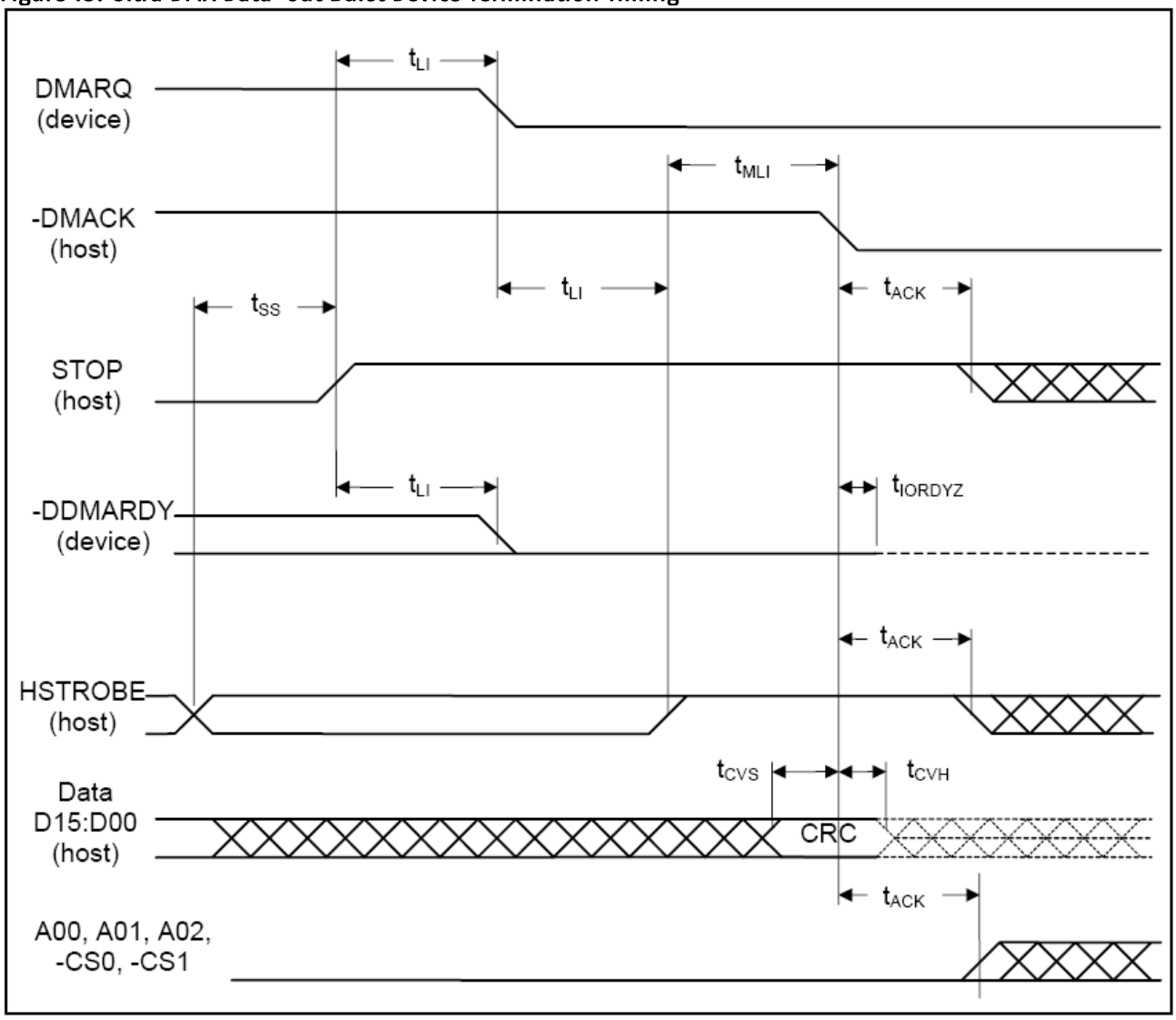
6.5.4.4.9 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 18: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall initiate Ultra DMA burst termination by negating –DDMARDY.
c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating –DDMARDY.
d) If the device negates –DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates –DDMARDY greater than t_{SR} after the host has generated anHSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.
e) The device shall negate DMARQ no sooner than t_{RP} after negating –DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
g) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) The host shall place the result of its CRC calculation on D[15:00] (see 6.5.4.5).
i) The host shall negate –DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and –DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].
j) The device shall latch the host's CRC data from D[15:00] on the negating edge of –DMACK.
k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command.

Figure 18: Ultra DMA Data-Out Burst Device Termination Timing



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.5.4.4.10 Host Terminating an Ultra DMA Data-Out Burst

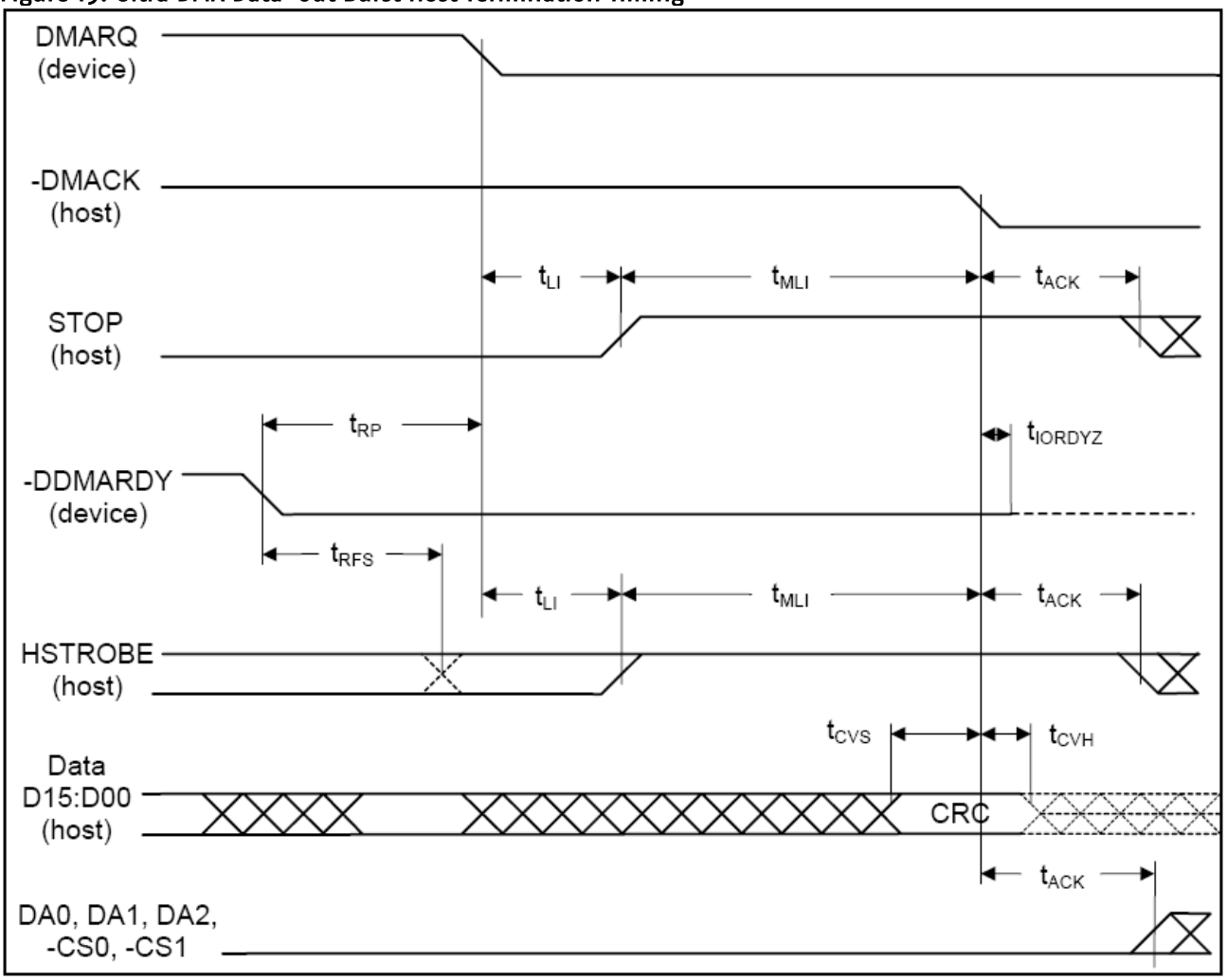
Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 19: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 28: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 29: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
b) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
c) The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
d) The device shall negate –DDMARDY within t_{LI} after the host has negated STOP. The device shall not assert –DDMARDY again until after the Ultra DMA burst termination is complete.
e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
f) The host shall place the result of its CRC calculation on D[15:00] (see 6.5.4.5).
g) The host shall negate –DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and –DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

h) The device shall latch the host's CRC data from D[15:00] on the negating edge of –DMACK.
i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 6.5.4.5).
j) The device shall release –DDMARDY within t_{IORDYZ} after the host has negated –DMACK.
k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating –DMACK.
l) The host shall not assert –IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating -DMACK.

Figure 19: Ultra DMA Data-Out Burst Host Termination Timing



Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.5.4.5 Ultra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

1. Both the host and the device shall have a 16-bit CRC calculation function.
2. Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
3. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
4. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
5. At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of –DMACK.

6. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
7. For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands:
   When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the "Interface CRC Error" bit. The host shall respond to this error by re-issuing the command.
8. For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command):
   When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
9. For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.
   NOTE – If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.
10. A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.
11. 11. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 32 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).
    NOTE – Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

Table 32: Equations for parallel generation of an Ultra DMA CRC

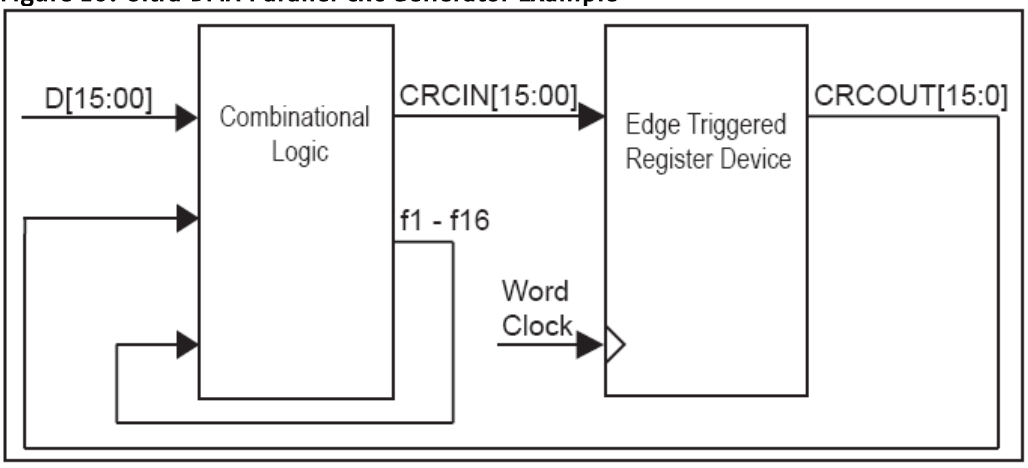
CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:

1. f=feedback
2. D[15:0] = Data to or from the bus
3. CRCOUT = 16-bit edge triggered result (current CRC)
4. CRCOUT[15:0] are sent on matching order bits of D[15:00]

An example of a CRC generator implementation is provided below in Figure 20: Ultra DMA Parallel CRC Generator Example.

Figure 20: Ultra DMA Parallel CRC Generator Example



7 Card Configuration

The CompactFlash Memory Card is identified by information in the Card Information Structure (CIS). The Card has four configuration registers (Table 33and Table 34).

- Configuration Option Register
- Pin Replacement Register
- Card Configuration and Status Register
- Socket and Copy Register

They are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, in I/O Card mode these registers provide a method for accessing status information that would normally appear on dedicated pins in Memory Card mode.
The base address of the card configuration registers is 200h in the Attribute Memory space.
No write operation should be performed to the attribute memory area except for the configuration register addresses. All other attribute memory locations are reserved. See 7.5 *Attribute Memory Function.*

Table 33: CompactFlash Memory Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Register Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D7 to D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D15 to D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit – D15 to D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Register Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7 to D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D15 to D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit – D15 to D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Write)

Table 34: CompactFlash Memory Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8~A4	A3	A2	A1	A0	Selected Space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read(200h)
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write(200h)
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read (202h)
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write (202h)
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read (204h)
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write (204h)
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read (206h)
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write (206h)

Note: The location of the Card Configuration Registers should always be read from the CIS since these locations may vary in future products. No Writes should be performed to the Card Attribute Memory except to the Card Configuration Register Addresses. All other attribute memory locations are reserved.

7.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the Card's interface, address decoding and interrupt to the Card (see Table 35).

7.1.1 SRESET

Setting the SRESET bit to '1' and returning the bit '0' places the CompactFlash Storage Card in the Reset state. Setting this bit to '1' is equivalent to asserting the RESET signal except that the SRESET bit is not cleared. Returning the SRESET bit to '0' leaves the CompactFlash Storage Card in the same un-configured Reset state as after a power-up and hardware reset.

This bit is set to '0' at power-up and taking the Card through a hardware reset.

7.1.2 LevlREQ

This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) after Power Up.

7.1.3 Conf5 – Conf0 (Configuration Index)

These bits are used to select the operation mode of the Card as shown in Table 36. This bit is set to '0' after Power Up.

Table 35: Configuration Option Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 36: CompactFlash Memory Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Mapping Mode	Card Mode	Task File Register Address
0	0	0	0	0	0	Memory	Memory	0h – Fh, 400h – 7FFh
0	0	0	0	0	1	Contiguous I/O	I/O	xx0h – xxFh
0	0	0	0	1	0	Primary I/O	I/O	1F0h – 1F7h, 3F6h – 3F7h
0	0	0	0	1	1	Secondary I/O	I/O	170h – 177h, 376h – 377h

7.2 CompactFlash Memory Card Configurations

The Card Configuration and Status Register contains information about the Card's status (see Table 37).

7.2.1 Changed

Indicates that one or both of the Pin Replacement register (CRDY, or CWProt) bits are set to '1'. When the Changed bit is set, -STSCHG (Pin 46) is held Low and if the SigChg bit is '1' the Card is configured for the I/O interface.

7.2.2 SigChg

This bit is set and reset by the host to enable and disable a state-change signal from the Status Register (issued on Status Changed pin 46). If no state change signal is desired, this bit should be set '0' and pin 46 (-STSCHG) will be held High while the Card is configured for I/O.

7.2.3 Iois8

The host sets this bit to '1' if the Card is to be configured in 8 bit I/O Mode. The Card is always configured for both 8 and 16 bit I/O, so this bit is ignored.

7.2.4 PwrDwn

This bit indicates whether the Card is in the power saving mode or active mode. When the PwrDwn bit is set to '1', the Card enters power down mode. When set to '0', the Card enters active mode. The READY value on Pin Replacement Register becomes BUSY when this bit is changed. READY will not become Ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.

7.2.5 Int

This bit represents the internal state of the interrupt request. It is available whether or not the I/O interface has been configured. It remains valid until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is '0'.

Table 37: Card Configuration and Status Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOIS8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOIS8	0	0	PwrDwn	0	0

7.3 Pin Replacement Register (204h in Attribute Memory)

This register contains information on the state of the READY signal when configured in memory mode and the IREQ signal in I/O mode. See Table 38 and Table 39.

7.3.1 Cready

This bit is set to '1' when the bit Rready changes state. This bit can also be written by the host.

7.3.2 CWProt

This bit is set to '1' when the bit RWProt changes state. This bit can also be written by the host.

7.3.3 Rready

This bit is used to determine the internal state of the Ready signal. In I/O mode it is used as an interrupt request. When written, this bit acts as a mask (Mready) for writing the corresponding bit Cready.

7.3.4 Wprot

This bit is always '0' since the CompactFlash Memory Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding CWProt bit.

7.3.5 Mready

This bit acts as a mask for writing the corresponding Cready bit.

7.3.6 MWProt

This bit when written acts as a mask for writing the corresponding CWProt bit.

Table 38: Pin Replacement Register (default value: 0Ch)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	Cready	CWProt	1	1	Rready	Wprot
Write	0	0	Cready	CWProt	0	0	Rready	MWProt

Table 39: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of 'C' Status	Written by Host		Final 'C' Bit	Comments
	'C' Bit	'M' Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

7.4 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information which identifies the Card from other cards. This register is always written by the system before writing the Configuration Option Register (see Table 40).

7.4.1 Drive

This value can be used to address two different cards in the case of twin card configuration.

7.4.2 X

The socket number is ignored by the Card.

Table 40: Socket and Copy Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

7.5 Attribute Memory Function

Attribute memory is a space where identification and configuration information are stored. Only 8 bit wide accesses at even addresses can be performed in this area. The Card configuration registers are also located in the Attribute Memory area, at base address 200h. Attribute memory is not accessible in True IDE mode of operation. For the Attribute Memory Read function, signals –REG and –OE must be active and –WE inactive during the cycle. As in the Main Memory Read functions, the signals –CE1 and –CE2 control the even and odd Byte address, but only the even Byte data is valid during the Attribute Memory access. Refer to Table 41 for signal states and bus validity.

Table 41: Attribute Memory Function

Function Mode	-REG	-CE2[1]	-CE1[1]	A10	A9	A0	-OE[1]	-WE[1]	D15 to D8	D7 to D0
Standby	X	H	H	X	X	X	X	X	High-Z	High-Z
Read Byte Access CIS (8 bits)	L	H	L	L	L	L	L	H	High-Z	Even Byte
Write Byte Access CIS (8 bits) Invalid	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	L	H	L	L	H	High-Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	L	H	High-Z	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) Invalid	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte

21 The –CE signal or both the –OE signal and the –WE signal must be de-asserted between consecutive cycle operations.

7.6 I/O Transfer Function

The I/O transfer to or from the Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the –IOIS16 signal is asserted by the Card, otherwise it is de-asserted. When a 16 bit transfer is attempted, and the –IOIS16 signal is not asserted, the system must generate a pair of 8 bit references to access the Word's even and odd Bytes. The Card permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS16 is asserted for all addresses (see Table 42).

Table 42: I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd Byte	Even Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd Byte	Even Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd Byte	Don't Care

7.7 Common Memory Transfer Function

The Common Memory transfer to or from the Card permits both 8 or 16 bit access to all of the Common Memory addresses (see Table 43).

Table 43: Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd Byte	Even Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd Byte	Don't Care

7.8 True IDE Mode I/O Function

The Card can be configured in a True IDE Mode of operation. It is configured in this mode only when the –OE signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed.

No Memory or Attribute Registers are accessible to the host. The Set Feature Command can be used to put the device in 8 bit Mode (see Table 44).
Removing and reinserting the Card while the host computer's power is on will reconfigure the Card to PC Card ATA mode.

Table 44: True IDE Mode I/O Function

Function Code	-CS1	-CS0	A2 to A0	-DMACK	-IORD	-IOWR	D15 to D8	D7 to D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1h-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1h-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	L	X	L	H	L	Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alternate Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

7.9 Host Configuration Requirements for Master/Slave or New Timing Modes

The CF Advanced Timing modes include PCMCIA PC Card style I/O modes that are faster than the original 250 ns cycle time. These modes are not supported by the PCMCIA PC Card specification nor CF by cards based on revisions of the CF specification before Revision 3.0. Hosts shall ensure that all cards accessed through a common electrical interface are capable of operation at the desired, faster than 250 ns, I/O mode before configuring the interface for that I/O mode.
Advanced Timing modes are PCMCIA PC Card style I/O modes that are 100 ns or faster, PC Card Memory modes that are 100ns or faster, True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. These modes are permitted to be used only when a single card is present and the host and card are connected directly, without a cable exceeding 0.15m in length. Consequently, the host shall not configure a card into an Advanced Timing Mode if two cards are sharing I/O lines, as in Master/Slave operation, nor if it is constructed such that a cable exceeding 0.15 meters is required to connect the host to the card.
The load presented to the Host by cards supporting Ultra DMA is more controlled than that presented by other CompactFlash cards. Therefore, the use of a card that does not support Ultra DMA in a Master/Slave arrangement with a Ultra DMA card can affect the critical timing of the Ultra DMA transfers. The host shall not configure a card into Ultra DMA mode when a card not supporting Ultra DMA is also present on the same interface
When the use of two cards on an interface is otherwise permitted, the host may use any mode that is supported by both cards, but to achieve maximum performance it should use its highest performance mode that is also supported by both cards.

8 Software interface

8.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Memory Card can be configured as a high performance I/O device through:

- Standard PC-AT disk I/O address spaces
  - 1F0h-1F7h, 3F6h-3F7h (primary);
  - 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16 Byte I/O block using any available IRQ.
- Memory space.

Communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four-register mapping methods. Table 45: I/O Configurations is a detailed description of these methods:

Table 45: I/O Configurations

Standards Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	xx0h-xxFh	I/O Mapped 16 Continuous Registers
2	I/O	1F0-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170-177h, 376h-377h	Secondary I/O Mapped

8.2 Memory Mapped Addressing

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2Kbytes as shown in Table 46: Memory Mapped Decoding. This window accesses the Data Register FIFO. It does not allow random access to the data buffer within the Card.
Register 0 is accessed with −CE1 and −CE2 Low, as a Word register on the combined Odd and Even Data Bus (D15 to D0). It can also be accessed with −CE1 Low and −CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with −CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to address 0 with −CE1 High and −CE2 Low accesses the Error (read) or Feature (write) register.
Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even then odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.
Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 kByte memory window to the data register is provided so that hosts can perform memory-to-memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory-to-memory block move instruction. Some PCMCIA socket adapters also have embedded auto incrementing address logic.
A Word access to address at offset 8 will provide even data on the least significant Byte of the data bus, along with odd data at offset 9 on the most significant Byte of the data bus.

Table 46: Memory Mapped Decoding

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0
1	0	X	0	0	0	0	0h	Even Data Register	Even Data Register
1	0	X	0	0	0	1	1h	Error Register	Feature Register
1	0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
1	0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
1	0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
1	0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
1	0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
1	0	X	0	1	1	1	7h	Status Register	Command Register
1	0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
1	0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
1	0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register
1	0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
1	0	X	1	1	1	1	Fh	Drive Address Register	Reserved
1	1	X	X	X	X	0	8h	Even Data Register	Even Data Register
1	1	X	X	X	X	1	9h	Odd Data Register	Odd Data Register

8.3 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the Card, the registers are accessed in the block of I/O space decoded by the system as shown in Table 47.
As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.
Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even than odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.

Table 47: Contiguous I/O Decoding

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0
0	X	0	0	0	0	0h	Even Data Register	Even Data Register
0	X	0	0	0	1	1h	Error Register	Feature Register
0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
0	X	0	1	1	1	7h	Status Register	Command Register
0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register
0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
0	X	1	1	1	1	Fh	Drive Address Register	Reserved

8.4 I/O Primary and Secondary Address Configurations

When the system decodes the Primary and Secondary Address Configurations, the registers are accessed in the block of I/O space as shown in Table 48.
As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.

Table 48: Primary and Secondary I/O Decoding

-REG	A9 to A4	A3	A2	A1	A0	-IORD=0	-IOWR=0
0	1F(17)h	0	0	0	0	Even Data Register	Even Data Register
0	1F(17)h	0	0	0	1	Error Register	Feature Register
0	1F(17)h	0	0	1	0	Sector Count Register	Sector Count Register
0	1F(17)h	0	0	1	1	Sector Number Register	Sector Number Register
0	1F(17)h	0	1	0	0	Cylinder Low Register	Cylinder Low Register
0	1F(17)h	0	1	0	1	Cylinder High Register	Cylinder High Register
0	1F(17)h	0	1	1	0	Select Card/Head Register	Select Card/Head Register
0	1F(17)h	0	1	1	1	Status Register	Command Register
0	3F(37)h	0	1	1	0	Alternate Status Register	Device Control Register
0	3F(37)h	0	1	1	1	Drive Address Register	Reserved

8.5 True IDE Mode Addressing

When the Card is configured in the True IDE Mode, the I/O decoding is as shown in Table 49.

Table 49: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0
1	0	0	0	0	1	PIO RD Data	PIO WR Data
1	1	X	X	X	0	DMA RD Data	DMA WR Data
1	0	0	0	1	1	Error Register	Features
1	0	0	1	0	1	Sector Count	Sector Count
1	0	0	1	1	1	Sector No.	Sector No.
1	0	1	0	0	1	Cylinder Low	Cylinder Low
1	0	1	0	1	1	Cylinder High	Cylinder High
1	0	1	1	0	1	Select Card/Head	Select Card/Head
1	0	1	1	1	1	Status	Command
0	1	1	1	0	1	Alt Status	Control Register

9 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the Card. These registers are collectively referred to as the 'task file'.
In accordance with the PCMCIA specification, each register that is located at an odd offset address can be accessed in the PC Card Memory or PC Card I/O modes. The register can be addressed in two ways:

- Using the normal register address.
- Using the corresponding even address (normal address -1) when –CE1 is High and –CE2 Low, unless –IOIS16 is High (not asserted by the card) and an I/O cycle is in progress. Register data are input or output on data bus lines D15-D8.

In True IDE mode, the size of the transfer is based solely on the register being addressed. All registers are 8-bit only except for the Data Register, which is normally 16 bits. However, they can be configured to be accessed in 8-bit mode for non-DMA operations, by using a Set Features command (see *Section 10.20*).

9.1 Data Register

The Data register is located at address 1F0h [170h], offset 0h, 8h, and 9h.
The Data Register is a 16 bit register used to transfer data blocks between the Card data buffer and the Host. This register overlaps the Error Register. Table 50 and Table 51 describe the combinations of Data register access and explain the overlapped Data and Error/Feature Registers. Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for Word (-CE2 and –CE1 set to '0') operations, and are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed.

Table 50: Data Register Access (Memory and I/O mode)

Data Register	-CE2	-CE1	A0	-REG[22]	Offset	Data Bus
Word Data Register	0	0	X	-	0h, 8h, 9h	D15 to D0
Even Data Register	1	0	0	-	0h, 8h	D7 to D0
Odd Data Register	1	0	1	-	9h	D7 to D0
Odd Data Register	0	1	X	-	8h, 9h	D15 to D8
Error/Feature Register	1	0	1	-	1h, Dh	D7 to D0
Error/Feature Register	0	1	X	-	1h	D15 to D8
Error/Feature Register	0	0	X	-	Dh	D15 to D8

22 –REG signal is mode dependent. It must be Low when the Card operates in I/O Mode and High when it operates in Memory Mode.

Table 51: Data Register Access (True IDE mode)

Data Register	-CS1	-CS0	A0	-DMACK	Offset	Data Bus
PIO Word Data Register	1	0	0	1	0h	D15 to D0
DMA Word Data Register	1	1	X	0	X	D15 to D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0h	D7 to D0

9.2 Error Register

The Error register is a read-only register, located at address 1F1h [171h], offset 1h, 0Dh.
This read only register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined in Table 52 This register is accessed on data bits D15 to D8 during a write operation to offset 0 with –CE2 Low and –CE1 High.

9.2.1 Bit 7 (BBK)

This bit is set when a Bad Block is detected.

9.2.2 Bit 6 (UNC)

This bit is set when an Uncorrectable Error is encountered.

9.2.3 Bit 5

This bit is '0'.

9.2.4 Bit 4 (IDNF)

This bit is set if the requested sector ID is in error or cannot be found.

9.2.5 Bit 3

This bit is '0'.

9.2.6 Bit 2 (Abort)

This bit is set if the command has been aborted because of a Card status condition (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

9.2.7 Bit 1

This bit is '0'.

9.2.8 Bit 0 (AMNF)

This bit is set when there is a general error.

Table 52: Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

9.3 Feature Register

The Feature register is a write-only register, located at address 1F1h [171h], offset 1h, Dh.
This write-only register provides information on features that the host can utilize. It is accessed on data bits D15 to D8 during a write operation to Offset 0 with –CE2 Low and –CE1 High.

9.4 Sector Count Register

The Sector Count register is located at address 1F2h [172h], offset 2h.
This register contains the number of sectors of data to be transferred on a read or write operation between the host and Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request. The default value is 01h.

9.5 Sector Number (LBA 7-0) Register

The Sector Number register is located at address 1F3h [173h], offset 3h.
This register contains the starting sector number or bits 7 to 0 of the Logical Block Address (LBA), for any data access for the subsequent sector transfer command.

9.6 Cylinder Low (LBA 15-8) Register

The Cylinder Low register is located at address 1F4h [174h], offset 4h.
This register contains the least significant 8 bits of the starting cylinder address or bits 15 to 8 of the Logical Block Address.

9.7 Cylinder High (LBA 23-16) Register

The Cylinder High register is located at address 1F5h [175h], offset 5h.
This register contains the most significant bits of the starting cylinder address or bits 23 to 16 of the Logical Block Address.

9.8 Drive/Head (LBA 27-24) Register

The Driver/Head register is located at address 1F6h [176h], offset 6h.
The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined in Table 53.

9.8.1 Bit 7

This bit is set to '1'.

9.8.2 Bit 6 (LBA)

LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA is set to '0', Cylinder/Head/Sector mode is selected. When LBA is set to'1', Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

- LBA7–LBA0: Sector Number Register D7 to D0
- LBA15–LBA8: Cylinder Low Register D7 to D0
- LBA23–LBA16: Cylinder High Register D7 to D0
- LBA27–LBA24: Drive/Head Register bits HS3 to HS0

9.8.3 Bit 5

This bit is set to '1'.

9.8.4 Bit 4 (DRV)

DRV is the drive number. When DRV is '0', drive/card 0 is selected (Master). When DRV is '1', drive/card 1 is selected (Slave). The Card is set to Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

9.8.5 Bit 3 (HS3)

When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

9.8.6 Bit 2 (HS2)

When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

9.8.7 Bit 1 (HS1)

When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

9.8.8 Bit 0 (HS0)

When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Table 53: Drive/Head Register

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

9.9 Status & Alternate Status Registers

The Status & Alternate Status registers are located at addresses 1F7h [177h] and 3F6h [376h], respectively. Offsets are 7h and Eh.
These registers return the Card status when read by the host.
Reading the Status Register clears a pending interrupt. Reading the Auxiliary Status Register does not clear a pending interrupt.
The Status Register should be accessed in Byte mode; in Word mode it is recommended that Alternate Status Register is used. The status bits are described as follows

9.9.1 Bit 7 (BUSY)

The busy bit is set when only the Card can access the command register and buffer, The host is denied access. No other bits in this register are valid when this bit is set to '1'.

9.9.2 Bit 6 (RDY)

This bit indicates whether the device is capable of performing CompactFlash Memory Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.

9.9.3 Bit 5 (DWF)

When set this bit indicates a Write Fault has occurred.

9.9.4 Bit 4 (DSC)

This bit is set when the Card is ready.

9.9.5 Bit 3 (DRQ)

The Data Request is set when the Card requires information be transferred either to or from the host through the Data register. The bit is cleared by the next command.

9.9.6 Bit 2 (CORR)

This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

9.9.7 Bit 1 (IDX)

This bit is always set to '0'.

9.9.8 Bit 0 (ERR)

This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. In case of read or write access commands that end with an error, the address of the first sector with an error is in the command block registers. This bit is cleared by the next command.

Table 54: Status & Alternate Status Register

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

9.10 Device Control Register

The Device Control register is located at address 3F6h [376h], offset Eh.
This Write-only register is used to control the CompactFlash Memory Card interrupt request and to issue an ATA soft reset to the Card. This register can be written even if the device is BUSY. The bits are defined as follows:

9.10.1 Bit 7 to 3

Don't care. The host should reset this bit to '0'.

9.10.2 Bit 2 (SW Rst)

This bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This clears Status Register and writes Diagnostic Code in Error register after a Write or Read Sector error. The Card remains in Reset until this bit is reset to '0.'

9.10.3 Bit 1 (-Ien)

When the Interrupt Enable bit is set to '0', -IREQ interrupts are enabled. When the bit is set to '1', interrupts from the Card are disabled. This bit also controls the Int bit in the Card Configuration and Status Register. It is set to '0' at Power On.

9.10.4 Bit 0

This bit is set to '0'.

Table 55: Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	SW Rst	-Ien	0

9.11 Card (Drive) Address Register

The Card (Drive) Address register is located at address 3F7h [377h], offset Fh.
This read-only register is provided for compatibility with the AT disk drive interface and can be used for confirming the drive status. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

9.11.1 Bit 7

This bit is don't care.

9.11.2 Bit 6 (-WTG)

This bit is '0' when a write operation is in progress; otherwise, it is '1'.

9.11.3 Bit 5 (-HS3)

This bit is the negation of bit 3 in the Drive/Head register.

9.11.4 Bit 4 (-HS2)

This bit is the negation of bit 2 in the Drive/Head register.

9.11.5 Bit 3 (-HS1)

This bit is the negation of bit 1 in the Drive/Head register.

9.11.6 Bit 2 (-HS0)

This bit is the negation of bit 0 in the Drive/Head register.

9.11.7 Bit 1 (-nDS1)

This bit is '0' when drive 1 is active and selected.

9.11.8 Bit 0 (-nDS0)

This bit is '0' when the drive 0 is active and selected.

Table 56: Card (Drive) Address Register

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

10 CF-ATA command description

This section defines the software requirements and the format of the commands the Host sends to the Card. Commands are issued to the Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Card is not busy (BSY is '0').

- **Class 1:** Upon receipt of a Class 1 command, the Card sets BSY within 400ns.
- **Class 2:** Upon receipt of a Class 2 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3:**Upon receipt of a Class 3 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 57 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 57: CF-ATA Command Set(1)

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h					D	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Execute Drive Diagnostic	90h					D	
1	Flush cache	E7h					D	
2	Format track	50h		Y		Y	Y	Y
1	Identify Drive	Ech					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read DMA	C8		Y	Y	Y	Y	Y
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read native max address	F8h					D	
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
1	Set max address	F9h		Y	Y	Y	Y	Y
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	S.M.A.R.T.	B0h	Y	Y		Y	D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	E0h or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
1	Wear Level	F5h					Y	
2	Write Buffer	E8h					D	
2	Write DMA	CA		Y	Y	Y	Y	Y
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

1. FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use), Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Memory Card and head parameters are used. D – only the Compact Flash Memory Card parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

10.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Card is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Card is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 58 defines the Byte sequence of the Check Power Mode command.

Table 58: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.2 Erase Sector(s) (C0h)

This command is used to pre-erase and condition data sectors prior to a Write Sector without Erase command or a Write Multiple Without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur. Table 59 defines the Byte sequence of the Erase Sector command.

Table 59: Erase Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to erase							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to erase							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

10.3 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Card.
In PCMCIA configuration, this command only runs on the Card which is addressed by the Drive/Head register when the command is issued. This is because PCMCIA Card interface does not allow for direct inter-drive communication.
In True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 60 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 61 are returned in the Error Register at the end of the command.

Table 60: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 61: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

10.4 Flush Cache (E7h)

This command causes the card to complete writing data from its cache. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache command, the Compact Flash Storage Card shall return command aborted.

Table 62: Flush Cache

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E7h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.5 Format track (50h)

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Table 63: Format track

Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count (LBA only)							
FEATURES	nu							

10.6 Identify Device (Ech)

The Identify Device command enables the host to receive parameter information from the Card. This command has the same protocol as the Read Sector(s) command. Table 64 defines the Identify Device command Byte sequence. All reserved bits or Words are zero.

Identify Device table shows the definition of each field in the Identify Drive Information.

Table 64: Identify Device

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 65: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	**848Ah***	2	General Configuration (REMOVABLE, signature of the CompactFlash Memory Card) In PCMCIA mode the HxBK cards have normally the value 848Ah but other configurations are possible
	045Ah*	2	Alternate Configuration FIX, In IDE mode the HxBK cards have normally the value 045Ah but other configurations are possible
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0200h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per Card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Reserved
23-26	**aaaa***	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	**aaaa***	40	Model number in ASCII (right justified) Big Endian Byte Order in Word ("SFCFxxxxHxBKxxx-x-xx-xxx-xxx")
47	800Xh	2	Maximum number of sectors on Read/Write Multiple command X=1 for cards with 1 flash, X=2 for cards with more flash
48	0000h	2	Reserved
49	**0F00h*** **0E00h***	2	Capabilities with DMA without DMA (also in PCMCIA mode)
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	**0007h***	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved.
63	**0007h*** **0000h***	2	Multi-Word DMA transfer. In PCMCIA mode, this value is '0000h'.
64	0003h	2	Advanced PIO modes supported
65	**0078h*** **0000h***	2	Minimum Multi-Word DMA transfer cycle time per Word. In PCMCIA mode, this value is '0000h'.
66	**0078h*** **0000h***	2	Recommended Multi-Word DMA transfer cycle time. In PCMCIA mode, this value is '0000h'.
67	**0078h***	2	Minimum PIO transfer cycle time without flow control
68	**0078h***	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	22	Reserved
80-81	0020h 0000h	4	ATA version 5
82 -84	7409h* 5004h* 4000h*	6	Features/command sets supported
85-87	7409h* 1004h* 4000h*	6	Features/command sets enabled
88	**101Fh***	2	Ultra DMA Mode Supported and Selected 0,1,2,3,4 (changes in operation)
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92-127	0000h*	72	Reserved
128	0000h	2	Security status
129-159	0000h	62	vendor unique bytes

Word Address	Default Value	Total Bytes	Data Field Type Information
160	**A064h***	2	Power requirement description (max. 100mA)*
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	**0012h*** **0000h***	2	CF Advanced True IDE Timing Mode Capability and Setting (PIO6/MDMA4)* In PCMCIA mode, this value is '0000h'.
164	**001Bh*** **0000h***	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability In PCMCIA mode, this value is '0000h'.
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

* Standard values for full functionality, depending on Configuration
XXXX Depending on Card capacity and drive geometry

10.6.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **848Ah**. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices.
Alternate Configuration Values for Word 0 is **045Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the Card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a CompactFlash Card in True IDE mode. To support this requirement and provide capability for any future removable media cards, alternate value of Word 0 is set in True IDE Mode of operation.

10.6.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

10.6.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

10.6.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

10.6.5 Word 7-8: Number of Sectors per Card

This field contains the number of sectors per Card. This double Word value is also the first invalid address in LBA translation mode.

10.6.6 Word 10-19: Memory Card Serial Number

The contents of this field are right justified and padded without spaces (20h).

10.6.7 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

10.6.8 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

10.6.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

10.6.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 11: IORDY Supported
  If bit 11 is set to 1 then this CompactFlash Storage Card supports IORDY operation.
  If bit 11 is set to 0 then this CompactFlash Storage Card may support IORDY operation.

- Bit 10: IORDY may be disabled
  Bit 10 shall be set to 0, indicating that IORDY may not be disabled.
- Bit 9 LBA support: CompactFlash Memory Cards support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

10.6.11 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15-8: are set to 02H.

10.6.12 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported True IDE UDMA

10.6.13 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

10.6.14 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

10.6.15 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

10.6.16 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Card in LBA mode only.

10.6.17 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the CompactFlash Storage Card to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
Selection of Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163 as described in Word 163.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the Multiword DMA modes it is capable of supporting.
Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 2, 1 and 0.
Support for Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163 as described in Word 163.

10.6.18 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the CompactFlash Memory Card to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the CompactFlash Memory Card supports PIO mode 4.
- Bit 0 is set to '1' to indicate that the CompactFlash Memory Card supports PIO mode 3.

Support for PIO modes 5 and above are specific to CompactFlash are reported in word 163 as described in Word 163.

10.6.19 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

10.6.20 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the CompactFlash Storage Card will need to negate the DMARQ signal during the transfer of a sector.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

10.6.21 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer without utilization of flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

10.6.22 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the CompactFlash Storage Card supports while performing data transfers while utilizing IORDY flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the CompactFlash Storage Card.
If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

10.6.23 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

- If bit 0 of word 82 is set to one, the SMART feature set is supported.
- If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
- Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
- If bit 5 of word 82 is set to one, write cache is supported.
- If bit 6 of word 82 is set to one, look-ahead is supported.
- Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

- Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
- Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 82 is obsolete.
- Bit 12 of word 82 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.
- Bit 13 of word 82 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.
- Bit 14 of word 82 shall be set to one; the CompactFlash Storage Card supports the NOP command.
- Bit 15 of word 82 is obsolete.

- Bit 0 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.
- Bit 1 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.
- Bit 2 of word 83 shall be set to one; the CompactFlash Storage Card supports the CFA feature set.
- If bit 3 of word 83 is set to one, the CompactFlash Storage Card supports the Advanced Power Management feature set.
- Bit 4 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

10.6.24 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

- If bit 0 of word 85 is set to one; the SMART feature set is enabled.
  Bit 0 can be changed by the host and is not reset after power cycle
- If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security
- Set Password command.
- Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
- If bit 5 of word 85 is set to one, write cache is enabled.
- If bit 6 of word 85 is set to one, look-ahead is enabled.
- Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
- Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
- Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 85 is obsolete.
- Bit 12 of word 85 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.
- Bit 13 of word 85 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.
- Bit 14 of word 85 shall be set to one; the CompactFlash Storage Card supports the NOP command.
- Bit 15 of word 85 is obsolete.
- Bit 0 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.
- Bit 1 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.
- If bit 2 of word 86 shall be set to one, the CompactFlash Storage Card supports the CFA feature set.
- If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
- Bit 4 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

10.6.25 Word 88: True IDE Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be

selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device is not in True IDE mode or if it does not support UDMA in True IDE Mode.

- Bit 15: Reserved
- Bit 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7: Reserved
- Bit 6: 1 = Ultra DMA mode 6 and below are supported. Bits 0-5 shall be set to 1.
- Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 shall be set to 1.
- Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
- Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
- Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
- Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0: 1 = Ultra DMA mode 0 is supported

10.6.26 Word 160: Power Requirement Description

This word is required for CompactFlash Storage Cards that support power mode 1.

- Bit 15: VLD
  If set to 1, indicates that this word contains a valid power requirement description.
  If set to 0, indicates that this word does not contain a power requirement description.
- Bit 14: RSV
  This bit is reserved and shall be 0.
- Bit 13: -XP
  If set to 1, indicates that the CompactFlash Storage Card does not have Power Level 1 commands.
  If set to 0, indicates that the CompactFlash Storage Card has Power Level 1 commands
- Bit 12: -XE
  If set to 1, indicates that Power Level 1 commands are disabled.
  If set to 0, indicates that Power Level 1 commands are enabled.
- Bit 0-11: Maximum current
  This field contains the CompactFlash Storage Card's maximum current in mA.

10.6.27 Word 163: Advanced True IDE Timing mode capabilities and settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.

Notice! The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host as indicated in section 5.3 : Additional Requirements for CF Advanced Timing Modes.

There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes. The older modes are reported in words 63 and 64.

- Bits 2-0: Advanced True IDE PIO Mode Support
  Indicates the maximum True IDE PIO mode supported by the card.
  0 Specified in word 64
  1 PIO Mode 5
  2 PIO Mode 6
  3-7 Reserved
- Bits 5-3: Advanced True IDE Multiword DMA Mode Support
  Indicates the maximum True IDE Multiword DMA mode supported by the card.
  0 Specified in word 63
  1 Multiword DMA Mode 3
  2 Multiword DMA Mode 4
  3-7 Reserved

- Bits 8-6: Advanced True IDE PIO Mode Selected
  Indicates the current True IDE PIO mode selected on the card.
  0 Specified in word 64
  1 PIO Mode 5
  2 PIO Mode 6
  3-7 Reserved

- Bits 11-9: Advanced True IDE Multiword DMA Mode Selected
  Indicates the current True IDE Multiword DMA Mode Selected on the card.
  0 Specified in word 63
  1 Multiword DMA Mode 3
  2 Multiword DMA Mode 4
  3-7 Reserved

- Bits 15-12 are reserved.

10.6.28 Word 164: Advanced PCMCIA I/O and Memory Timing modes capabilities and settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PC Card I/O interface.

Notice! The use of PC Card I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host as indicated in section 5.3 : Additional Requirements for CF Advanced Timing Modes.

- Bits 2-0: Maximum Advanced PC Card I/O Mode Support
  Indicates the maximum I/O timing mode supported by the card.
  0 255 ns Cycle PC Card I/O Mode
  1 120 ns Cycle PC Card I/O Mode
  2 100 ns Cycle PC Card I/O Mode
  3 80 ns Cycle PC Card I/O Mode
  4-7 Reserved

- Bits 5-3: Maximum Memory timing mode supported
  Indicates the Maximum Memory timing mode supported by the card.
  0 250 ns Cycle Memory Mode
  1 120 ns Cycle Memory Mode
  2 100 ns Cycle Memory Mode
  3 80 ns Cycle Memory Mode
  4-7 Reserved

- Bits 8-6: Maximum PC Card I/O UDMA timing mode supported
  Indicates the Maximum PC Card I/O UDMA timing mode supported by the card when bit 15 is set.
  PC Card I/O UDMA mode 0 supported
  PC Card I/O UDMA mode 1 supported
  2 PC Card I/O UDMA mode 2 supported
  3 PC Card I/O UDMA mode 3 supported
  4 PC Card I/O UDMA mode 4 supported
  5 PC Card I/O UDMA mode 5 supported
  6 PC Card I/O UDMA mode 6 supported
  7 Reserved

- Bits 11-9: Maximum PC Card Memory UDMA timing mode supported
  Indicates the Maximum PC Card Memory UDMA timing mode supported by the card when bit 15 is set.
  0 PC Card Memory UDMA mode 0 supported
  1 PC Card Memory UDMA mode 1 supported
  2 PC Card Memory UDMA mode 2 supported
  3 PC Card Memory UDMA mode 3 supported
  4 PC Card Memory UDMA mode 4 supported
  5 PC Card Memory UDMA mode 5 supported
  6 PC Card Memory UDMA mode 6 supported
  7 Reserved

- Bits 14-12: PC Card Memory or I/O UDMA timing mode selected
  Indicates the PC Card Memory or I/O UDMA timing mode selected by the card.
  0 PC Card I/O UDMA mode 0 selected
  1 PC Card I/O UDMA mode 1 selected
  2 PC Card I/O UDMA mode 2 selected
  3 PC Card I/O UDMA mode 3 selected
  4 PC Card I/O UDMA mode 4 selected
  5 PC Card I/O UDMA mode 5 selected
  6 PC Card I/O UDMA mode 6 selected
  7 Reserved

- Bit 15: PC Card Memory and IO Modes Supported

10.7 Idle (97h or E3h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. If no Idle command is performed, the card goes to sleep mode after 20ms. Table 66 defines the Byte sequence of the Idle command.

Table 66: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

10.8 Idle Immediate (95h or E1h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 67 defines the Idle Immediate command Byte sequence.

Table 67: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.9 Initialize Drive Parameters (91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command. Table 68 defines the Initialize Drive Parameters command Byte sequence.

Table 68: Initialize Drive Parameters

Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Number of Sectors per Track							
FEATURES	nu							

10.10 NOP (00h)

This command always fails with the CompactFlash Memory Card returning command aborted. Table 69 defines the Byte sequence of the NOP command.

Table 69: NOP

Task File Register	7	6	5	4	3	2	1	0
COMMAND	00h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.11 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Card's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 70 defines the Read Buffer command Byte sequence.

Table 70: Read buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.12 Read DMA (C8h)

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and
asserts –IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled
by the Set Features command, the Card shall return the Aborted error.

Table 71: Read DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.13 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error.
Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.
Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 72 defines the Read Multiple command Byte sequence.

Table 72: Read Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.14 Read Native max address (F8h)

The Read Native max address command reads the max native address of the drive. It is related to the Host protected Area feature set. Table 73 defines the Read max native address command Byte sequence.

Table 73: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.
The native drive size is given in Drive/Head, Cyl Hi, Cyl Low and Sector num register as LBA value.

10.15 Read Sector(s) (20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 74 defines the Read Sector command Byte sequence.

Table 74: Read sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h or 21h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.16 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Card sets BSY. When the requested sectors have been verified, the Card clears BSY and generates an interrupt.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.
Table 75 defines the Read Verify Sector command Byte sequence.

Table 75: Read Verify Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h or 41h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.17 Recalibrate (1Xh)

This command is effectively a NOP command to the Card and is provided for compatibility purposes. Table 76 defines the Recalibrate command Byte sequence.

Table 76: Recalibrate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	1Xh							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.18 Request Sense (03h)

This command requests extended error information for the previous command. Table 77 defines the Request Sense command Byte sequence. Table 78 defines the valid extended error codes. The extended error code is returned to the host in the Error Register.

Table 77: Request sense

Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 78: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

10.19 Seek (7Xh)

This command is effectively a NOP command to the Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range. Table 79 shows the Seek command Byte sequence.

Table 79: Seek

Task File Register	7	6	5	4	3	2	1	0
COMMAND	7Xh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

10.20 Set Features (Efh)

Table 80: Set Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Efh							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Config							
FEATURES	Feature							

Table 81: Features Supported

Feature	Operation
01h/81h	Enable/Disable 8-bit data transfers.
02h/82h	Enable/Disable write cache.
03h	Set transfer mode based on value in Sector Count register.
05h/85h	Enable/Disable advance power management.
09h/89h	Enable/Disable extended power operations.
0Ah/8Ah	Enable/Disable power level 1 commands.
55h/Aah	Disable/Enable Read Look Ahead.
66h/CCh	Disable/Enable Power On Reset (POR) established of defaults at Soft Reset.
69h	NOP Accepted for backward compatibility.
96h	NOP Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows trade-off between current drawn and read/write speed.
BBh	4 bytes of data apply on Read/Write Long commands

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the –IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.
Features 02h and 82h allow the host to enable or disable write cache in CompactFlash Storage Cards that implement write cache. When the subcommand disable write cache is issued, the CompactFlash Storage Card shall initiate the sequence to flush cache to non-volatile memory before command completion.
Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 82: Transfer Mode Values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode(1)
Reserved	00010b	N/A
Multi-Word DMA mode	00100b	Mode(1)
Ultra DMA mode	01000b	Mode(1)
Reserved	1000b	N/A

(1)Mode = transfer mode number

Notes: Multiword DMA is not permitted for devices configured in the PC Card Memory or the PC Card I/O interface mode.

If a CompactFlash Storage Card supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the CompactFlash Storage Card supports disabling of IORDY, then the CompactFlash Storage Card shall set its default PIO mode and disable IORDY. A CompactFlash Storage Card shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported. Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A CompactFlash Storage Card reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported. Note that Multiword DMA shall not be supported while PC Card interface modes are selected.
A CompactFlash Storage Card reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.
If an Ultra DMA mode is enabled, any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device.
Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of Feh.
Table 83: Advanced power management levels shows these values.

Table 83: Advanced power management levels

Level	Sector Count Value
Maximum performance	Feh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

In the current version the advanced power management levels are accepted, but don't influence performance and power consumption.
Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to Feh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.
Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.
Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the CF+ CompactFlash Storage Card with extended power as they require Power Level 1 to perform their full set of functions.
Power Enhanced CF Storage Cards are required to power up and execute all supported commands and protocols in Power Level 0, their default feature shall be 8Ah: Disable Power Level 1 Commands. No commands are actually excluded for such cards in Power Level 0 because no commands require Power Level 1. The 8Ah default allows the cards to restrict their operating power to Power Level 0 limits for compatibility with hosts that do not recognize or support the extended power capabilities of Power Enhanced CF Storage Cards. It also allows hosts that support extended power to take advantage of it by setting the feature to 0Ah: Enable Power Level 1 Commands.
Features 55h and BBh are the default features for the CompactFlash Storage Card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.
Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.
Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

10.21 Set max address (F9h)

The Set max address command sets the max address of the drive. It is related to the Host protected Area feature set. Table 84 defines the Set max address command Byte sequence.

Table 84: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	Set max LBA (27:24)			
CYLINDER HI	Set max LBA (23:16)							
CYLINDER LOW	Set max LBA (15:8)							
SECTOR NUM	Set max LBA (7:0)							
SECTOR COUNT	nu							VV
FEATURES	Feature							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

Prerequisites
DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.
VV =Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.

The set max address can be locked/unlocked and secured by password with following features:

Table 85: Set max features

Feature register	Command
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05-FFh	Reserved

Typical use of the Set max address (F9h) and Read native max address (F8h) commands would be:

On reset
BIOS receives control after a system reset;

1. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
2. BIOS issues a SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
3. BIOS reads configuration data from the highest area on the disk;
4. BIOS issues a READ NATIVE MAX ADDRESS command followed by a SET MAX ADDRESS command to reset the device to the size of the file system.

On save to disk

1. BIOS receives control prior to shut down;
2. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
3. BIOS issues a volatile SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
4. Memory is copied to the reserved area;
5. Shut down completes;
6. On power-on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low-level boot time process.
Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should return command aborted if a subsequent non-volatile SET MAX ADDRESS command is received after a power-on or hardware reset.

10.22 Set Multiple Mode (C6h)

This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Card sets BSY and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on the default mode is Read and Write Multiple disabled, unless it is disabled by a Set Feature command. Table 86 defines the Set Multiple Mode command Byte sequence.

Table 86: Set Multiple Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.23 Set Sleep Mode (99h or E6h)

This command causes the CompactFlash Memory Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command. Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 20 milliseconds. Note that this time base (5ms) is different from the ATA Specification. Table 87 defines the Set Sleep Mode command Byte sequence.

Table 87: Set Sleep Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h or E6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.24 S.M.A.R.T. (Boh)

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE data (Word 82 bit 0).

Table 88: S.M.A.R.T. Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Boh							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	XXh							
FEATURES	Feature							

Details of S.M.A.R.T. features are described in Section 11.

10.25 Standby (96h or E2)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 89 defines the Standby command Byte sequence.

Table 89: Standby

Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h or E2h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.26 Standby Immediate (94h or E0h)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.
Recovery from Sleep mode is accomplished by issuing another command. Table 90 defines the Standby Immediate Byte sequence.

Table 90: Standby Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	94h or E0h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.27 Translate Sector (87h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a '00h' indicating Translate Sector is not needed.
Table 91 defines the Translate Sector command Byte sequence.

Table 91: Translate Sector

Task File Register	7	6	5	4	3	2	1	0
COMMAND	87h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

10.28 Wear Level (F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 'ooh' indicating Wear Level is not needed.

Table 92 defines the Wear Level command Byte sequence.

Table 92: Wear level

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Completion Status							
FEATURES	nu							

10.29 Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes. Table 93 defines the Write Buffer command Byte sequence.

Table 93: Write Buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.30 Write DMA (Cah)

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Table 94: Write DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Cah							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.31 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Card sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.
DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.
When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.
Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.
The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.
Note: The current revision of the CompactFlash Memory Card only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.
Table 95 defines the Write Multiple command Byte sequence.

Table 95: Write Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.32 Write Multiple without Erase (CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. Table 96 defines the Write Multiple without Erase command Byte sequence.

Table 96: Write Multiple without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	CDh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.33 Write Sector(s) (30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Card sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.
For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 97 defines the Write Sector(s) command Byte sequence.

Table 97: Write Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h or 31h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.34 Write Sector(s) without Erase (38h)

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased a normal write sector operation will occur. Table 98 defines the Write Sector(s) without Erase command Byte sequence.

Table 98: Write Sector(s) without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	38h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.35 Write Verify (3Ch)

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command. Table 99 defines the Write Verify command Byte sequence.

Table 99: Write Verify

Task File Register	7	6	5	4	3	2	1	0
COMMAND	3Ch							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

11 S.M.A.R.T Functionality

The C-300 CF cards support the following SMART commands, determined by the Feature Register value.

Table 100: S.M.A.R.T. Features Supported

Feature	Operation
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute
D8h	SMART Enable Operations
D9h	Autosave SMART Disable Operations
DAh	SMART Return Status

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

11.1 S.M.A.R.T. Enable / Disable operations

This command enables / disables access to the SMART capabilities of the CF card.
The state of SMART (enabled or disabled) is preserved across power cycles.

Table 101: S.M.A.R.T. Enable / Disable operations (Feature D8h / D9h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D8h / D9h							

11.2 S.M.A.R.T. Enable / Disable Attribute Autosave

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the CF card.

Table 102: S.M.A.R.T. Enable / Disable Attribute Autosave (Feature D0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	00h or F1h							
FEATURES	D2h							

11.3 S.M.A.R.T. Read data

This command returns one sector of SMART data.

Table 103: S.M.A.R.T. read data (Feature D0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D0h							

The data structure returned is:

Table 104: S.M.A.R.T. Data Structure

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	00h	
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	0002h	SMART Swissbit Structure Version
388..391		"Commit" counter
392..395		Wear Level Threshold
396		Global Bad Block management active
397		Global Wear Leveling active
398..510	00h	
511		Data structure checksum

There are six attributes that are defined in the CF card. These return their data in the attribute section of the SMART data, using a 12 byte data field.
The field at offset 386 gives a version number for the contents of the SMART data structure. In version 0, the spare block counts (offsets 4 to 11) in the Spare Block Count attribute need to be byte-swapped.
In versions 0 and 1, the information at offsets 396 and 397 is not available.
The byte at offset 396 is 0 if the wear leveling has not yet started its global operation, and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold (typically 100000).
The byte at offset 397 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

11.3.1 Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Table 105: Spare Block Count Attribute

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1..2	0003h	Flags – Pre-fail type, value is updated during normal operation
3		Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips (100 × current spare blocks / initial spare blocks)
4..5		initial number of spare blocks of the flash chip that has been used for the attribute value calculation
6..7		current number of spare blocks of the flash chip that has been used for the attribute value calculation
8..9		sum of the initial number of spare blocks for all flash chips
10..11		sum of the current number of spare blocks for all flash chips

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

11.3.2 Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

Table 106: Erase Count Attribute

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block.
4..11		Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

11.3.3 Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 107: Total ECC Errors Attribute

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC errors (correctable and uncorrectable)
8..11		-

11.3.4 Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 108: Correctable ECC Errors Attribute

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of correctable ECC errors
8..11		-

11.3.5 Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Table 109: Total Number of Reads Attribute

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..11		Total number of flash read commands

11.3.6 UDMA CRC Errors Attribute

This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 110: UDMA CRC Errors Attribute

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of UDMA CRC errors
8..11		-

11.4 S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute thresholds.

Table 111: S.M.A.R.T. read data (Feature D1h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D1h							

The data structure returned is:

Table 112: S.M.A.R.T. Data Structure

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute threshold entries 1 to 30 (12 bytes each)
362..379	00h	Reserved
380..510	00h	-
511		Data structure checksum

Table 113: Spare Block Count Attribute Threshold

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1		Spare Block Count Threshold
2..11	00h	Reserved

Table 114: Erase Count Attribute Threshold

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1		Erase Count Threshold
2..11	00h	Reserved

Table 115: Total ECC Errors Attribute Threshold

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1	00h	No threshold for the Total ECC Errors Attribute
2..11	00h	Reserved

Table 116: Correctable ECC Errors Attribute

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the Correctable ECC Errors Attribute
2..11	00h	Reserved

Table 117: Total Number of Reads Attribute

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1	00h	No threshold for the Total Number of Reads Attribute
2..11	00h	Reserved

Table 118: UDMA CRC Errors Attribute

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1	00h	No threshold for the UDMA CRC Errors Attribute
2..11	00h	Reserved

11.5 S.M.A.R.T. Return Status

This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

Table 119: S.M.A.R.T. read data (Feature D1h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	Dah							

12 CIS information (typical)

```
0000: Code 01, link 03
D9 01 FF
```

- Device Info Tuple
- Link is 3 bytes
- I/O Device, No WPS, speed=250ns if no wait
- (One) 2 Kilobytes of address space
- End of CISTPL_DEVICE

```
000A: Code 1C, link 04
02 D9 01 FF
```

- Other Conditions Info Tuple
- Link is 4 bytes
- Conditions: 3V operation is allowed, and WAIT is used
- I/O Device, No WPS, speed = 250 ns if no wait
- (One) 2 Kilobytes of address space
- End of CISTPL_DEVICE

```
0016: Code 18, link 02
DF 01
```

- JEDEC programming info Tulpe
- Link is 2 bytes
- Device Manufactor ID
- Manufacturer specific info

```
001E: Code 20, link 04
00 00 00 00
```

- Manufacturer ID tuple
- Link length is 4 bytes
- PC Card manufacturer code
- Manufacturer specific info

```
002A: Code 21, link 02
04 01
```

- Function ID tuple
- Link length is 2 bytes
- Fixed disk drive
- R=0: no expansion ROM; P=1: configure at POST

```
0032: Code 22, link 02
01 01
```

- Function Extension tuple
- Link length is 2 bytes
- Disk interface information
- PC card ATA interface

```
003A: Code 22, link 03
02 04 07
```

- Function Extension tuple
- Link length is 3 bytes
- PC card ATA basic features
- D=0:single drive on card; U=0: no unique serial number; S=1: silicon device; V=0: no VPP required

- I=0: twin IOIS16# unspecified; E=0: index bit not emulated; N=0: I/0 includes 0x3F7; P=7: sleep, standby, idle supported

0044: Code 1A, link 05
01 07 00 02 0F

- Configuration Tuple
- Link length is 5 bytes
- RFS: reserved; RMS: 1 byte register mask; RAS: 2 bytes base address
- Last configuration entry is 07H
- Configuration registers are located at 0200h
- Configuration registers 0 to 3 are present

0052: Code 1B, link 0B
C0 C0 A1 27 55 4D 5D 75 08 00 21

- Configuration tuple
- Link length is 11 bytes
- Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
- W=1: wait required; R=1: ready/busy active; P=0: WP not used;B=0: BVD1, BVD2 not used; Type=0: Memory interface
- M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current;PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info;NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- Length of memory space is 2 Kbyte
- X=0: no more misc fields; P=1: power-down supported; RO=0:read/write media; A=0: audio not supported; T=1: max twins is 1

006C: Code 1B, link 06
00 01 21 B5 1E 4D

- Configuration tuple
- Link length is 6 bytes
- Memory mapped configuration, index=0
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

007C: Code 1B, link 0D
C1 41 99 27 55 4D 5D 75 64 F0 FF FF 21

- Configuration tuple
- Link length is 11 bytes
- Memory mapped configuration, index=0; I=1: Interface byte follows; D=1: Default entry
- W=1: wait required; R=1: ready/busy active; P=0: WP not used;B=0: BVD1, BVD2 not used; Type=0: Memory interface
- M=1: misc info present; MS=1: 2 byte memory length; IR=0: no interrupt is used; IO=0: no I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current;PI=1: peak current info; AI: no average current info; SI: no static current info; HV=1: max voltage info; LV=1: min voltage info;NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- Length of memory space is 2 Kbyte

- X=0: no more misc fields; P=1: power-down supported; RO=0:read/write media; A=0: audio not supported; T=1: max twins is 1

009A: Code 1B, link 06
01 01 21 B5 1E 4D

- Configuration tuple
- Link length is 6 bytes
- I/O mapped, index=1
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

00AA: Code 1B, link 12
C2 41 99 27 55 4D 5D 75 EA 61 F0 01 07 F6 03 01 EE 21

- Configuration tuple
- Link length is 18 bytes
- I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
- W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=1: I/O interface
- M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP
- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static; current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; IO=10: 10 lines decoded
- LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
- Address range 1 0x1F0 to 0x1F7
- Address range 2 0x3F6 to 0x3F7
- S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported; M=0: masks V..N not present; IRQN=14: use interrupt 14
- X=0: no more misc fields; P=1: power-down supported; RO=0:read/write media; A=0: audio not supported; T=1: max twins is 1

00D2: Code 1B, link 06
02 01 21 B5 1E 4D

- Configuration tuple
- Link length is 6 bytes
- I/O mapped, index=2
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

00E2: Code 1B, link 12
C3 41 99 27 55 4D 5D 75 EA 61 70 01 07 76 03 01 EE 21

- Configuration tuple
- Link length is 18 bytes
- I/O mapped, index=2; I=1: Interface byte follows; D=1: Default entry
- W=0: wait not required; R=1: ready/busy active; P=0: WP not used; B=0: BVD1, BVD2 not used; Type=1: I/O interface
- M=1: misc info present; MS=0: no memory space info; IR=1: interrupt is used; IO=1: I/O space is used; T=0: no timing info specified; Power=1: VCC info, no VPP

- DI: no power-down current; PI=1: peak current info; AI: no average current info; SI: no static; current info; HV=1: max voltage info; LV=1: min voltage info; NV=1: nominal voltage info
- Nominal voltage 5.0V
- Minimum voltage 4.5V
- Maximum voltage 5.5V
- Peak current 80 mA
- R=1: range follows; S=1: support 16 bit hosts; E=1: support 8 bit hosts; IO=10: 10 lines decoded
- LS=1: 1 byte length; AS=2: 2 byte address; NR=1: 2 address ranges
- Address range 1 0x170 to 0x177
- Address range 2 0x376 to 0x377
- S=1: interrupt sharing logic; P=1: pulse mode supported; L=1: level mode supported; M=0: masks V..N not present; IRQN=14: use interrupt 14
- X=0: no more misc fields; P=1: power-down supported; RO=0:read/write media; A=0: audio not supported; T=1: max twins is 1

010A: Code 1B, link 06
03 01 21 B5 1E 4D

- Configuration tuple
- Link length is 6 bytes
- I/O mapped, index=3
- Power=1: VCC info, no VPP
- PI=1: peak current info; NV=1: nominal voltage info
- X=1: extension byte present
- Nominal voltage 3.30V
- Peak current 45 mA

011A: Code 1B, link 04
07 00 28 D3

- Configuration tuple
- Link length is 4 bytes
- I/O mapped, index=7
- No feature descriptions follow
- Swissbit specific data
- Swissbit specific data

0126: Code 14, link 00

- No link control tuple
- Link length is 0 bytes

012A: Code 15, link ***14*)***
04 01 ***53 77 69 73 73 62 69 74 00 43 46 20 43 61 72 64*** 00 FF *)

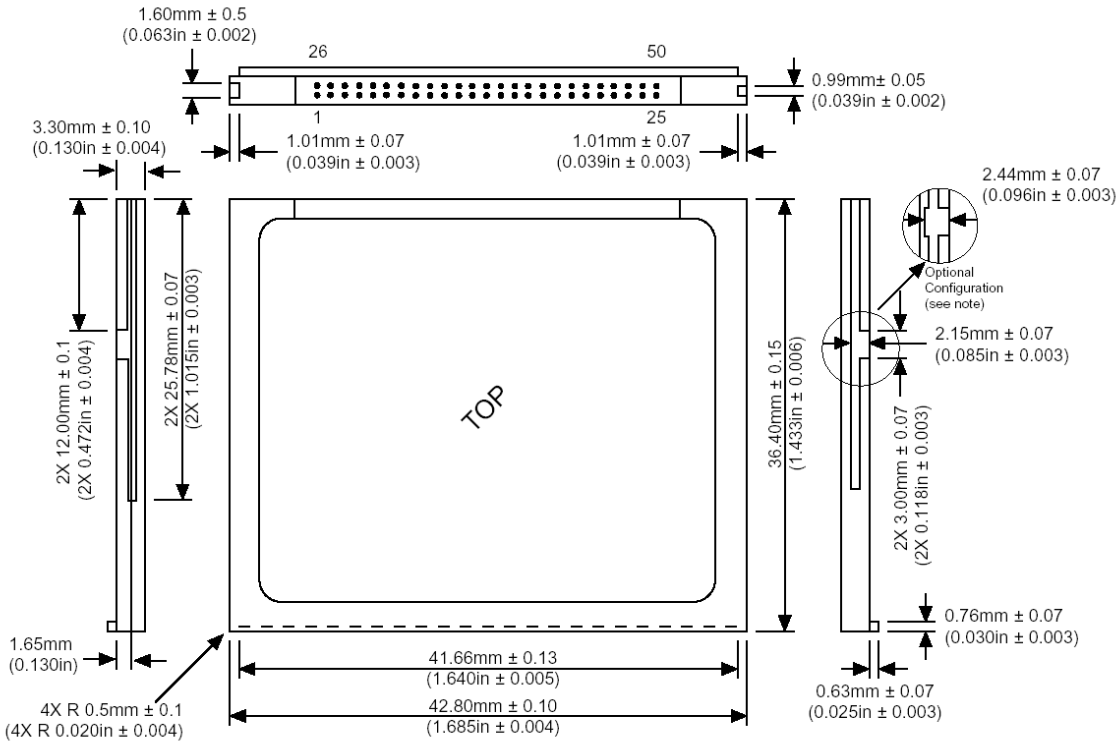
- Level 1 version/product info
- Link length is 21 bytes
- PCMCIA2.0/JEIDA4.1
- PCMCIA2.0/JEIDA4.1
- Product name: "***Swissbit***" "***CF Card***" *) can vary in different configurations
- ***The length of the strings will affect the following start addresses***

0156: Code FF, link FF

- End of CISTPL_VERS_1
- End of CIS

Package mechanical

Figure 21: Type I CompactFlash Memory Card Dimensions



13 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that CompactFlash Cards must comply with both Directives in order for them to be sold on the European market:

- **RoHS** – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2012/19/EU)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty»
(WEEE Directive 2012/19/EU)

When does the WEEE Directive take effect?

The Directive came into effect internationally on July 04, 2012.

What is RoHS (2011/65/EU)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of June 08, 2011, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

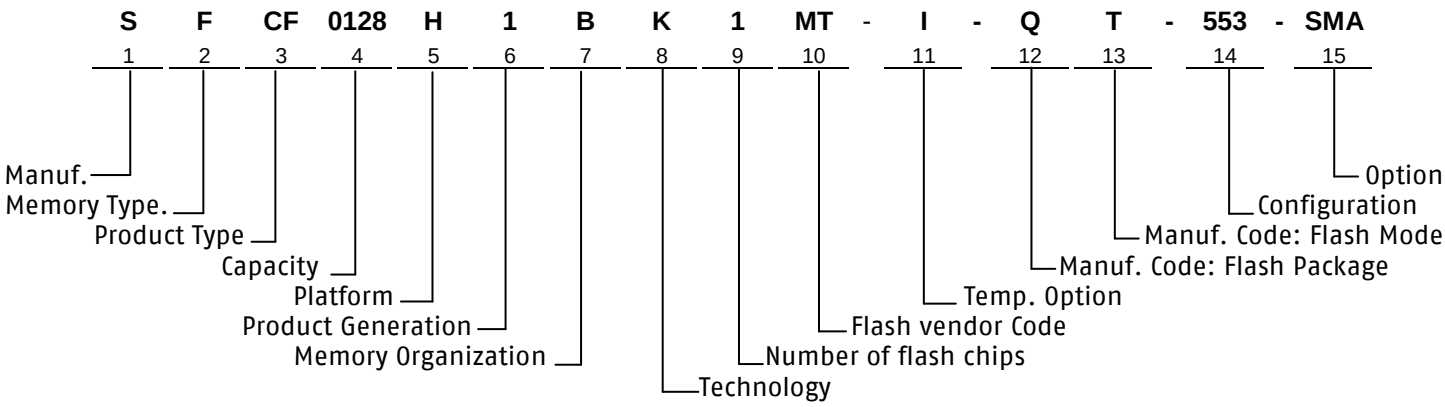
Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

Contact details:
Swissbit AG
Industriestrasse 4
CH 9552 Bronschhofen
Tel: +41 71 913 03 03 – Fax: +41 71 913 03 15
E-mail: info@swissbit.com – Website: www.swissbit.com

14 Part Number Decoder



14.1 Manufacturer

Swissbit code	S

14.2 Memory Type

Flash	F

14.3 Product Type

Compact Flash	CF

14.4 Capacity

64 MByte	0064
128 MByte	0128
256 MByte	0256
512 MByte	0512
1 GByte	1024
2 GByte	2048
4 GByte	4096
8 GByte	8192
16 GByte	16GB
32 GByte	32GB

14.5 Platform

Compact Flash	H

14.6 Product Generation

14.7 Memory Organization

x8	B

14.8 Controller type

C-300 Series	CF Card	K

14.9 Number of Flash Chip

1 Flash	1
2 Flash	2
4 Flash	4

14.10 Flash Code

Micron	MT

14.11 Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Standard Temp Range 0°C – 70°C	C

14.12 DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q

14.13 PIN Mode

	Normal	2chips at 1 channel
Normal nCE & R/nB	S	O
Dual nCE & Dual R/nB	T	P

14.14 Compact Flash XYZ

X→ CFC Mode

Removable/fix		PIO	DMA support	X
True IDE Mode	PC Card Mode			
Removable		yes	yes	1
Fix		yes	yes	2
Fix		yes	-	3
Removable		yes	-	4
Fix	*Removable*	*yes*	*yes*	*5**
Fix	Removable	yes	-	6

**default: autosense*

Y → Firmware revision per product generation

FW Revision	Y
Version 1	1
Version 2	2
Version 3	3
Version 4	4
Version 5	5

Z → max performance index

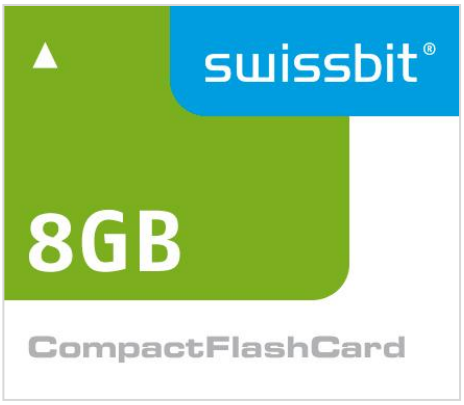
Max PIO Mode / CIS	Z
PIO4 (MDMA2 if enabled)	1
PIO6 (MDMA4 if enabled)	2
UDMA4 (PIO6, MDMA4)	3

14.15 Option

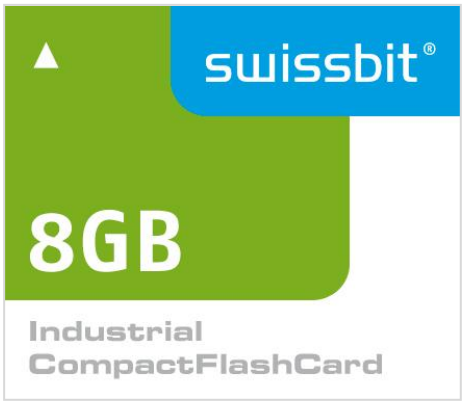
Swissbit without S.M.A.R.T. (on request)	STD
Swissbit S.M.A.R.T. features enabled	SMA

15 Swissbit CF Label specification

15.1 Front side label



Commercial Temperature CFC



Industrial Temperature CFC

15.2 Back side label

15.2.1 Label content:

- Swissbit logo
- CF logo
- Part number (defined by the data sheet)
- Barcode as lot code number (Code128)
- CE logo
- RoHS logo
- WEEE logo
- Manufacturing Date (MFG)
- "Made in Germany" string

16 Revision History

Table 120: Document Revision History

Date	Revision	Type	Revision Details
01-December-2013	0.80	initial	first preliminary release for C-300 longevity series
23-April-2014	1.00	release	Update title page, part number and performance value

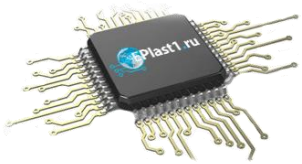
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.