

N-channel 100 V 3.9 mΩ standard level MOSFET in D2PAK Rev. 2 — 29 February 2012 Product data s

Product data sheet

Product profile 1.

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1.1 General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	<u>[1]</u> _	-	120	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	306	W
Tj	junction temperature		-55	-	175	°C
Static cha	aracteristics					
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	5.9	6.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	3.28	3.9	mΩ
Dynamic	characteristics					
Q _{GD}	gate-drain charge	V_{GS} = 10 V; I_{D} = 75 A; V_{DS} = 50 V;	-	49	-	nC
Q _{G(tot)}	total gate charge	see Figure 14; see Figure 15	-	170	-	nC
Avalanch	e ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ V_{GS} = 10 \text{ V}; \text{T}_{j(init)} = 25 \text{ °C}; \text{I}_{\text{D}} = 120 \text{ A}; \\ V_{sup} \leq 100 \text{ V}; \text{R}_{\text{GS}} = 50 \Omega; \text{ Unclamped} $	-	-	537	mJ

[1] Continuous current is limited by package.

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2. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		-
2	D	drain ^[1]	mb	
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3.Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R8-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

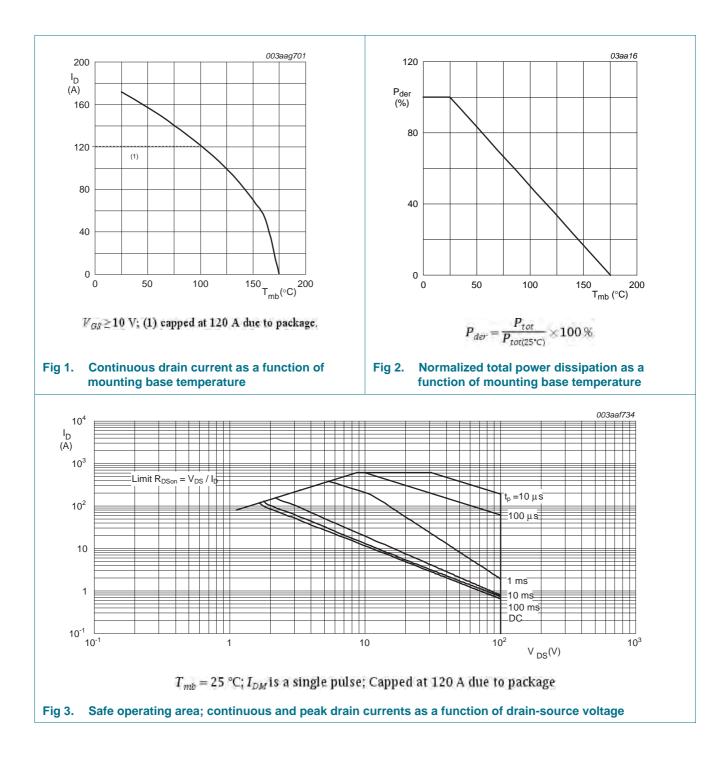
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	100	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V_{GS} = 10 V; T _j = 100 °C; see <u>Figure 1</u>	<u>[1]</u> _	120	А
		V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u>	<u>[1]</u> _	120	А
I _{DM}	peak drain current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$; see Figure 3	-	680	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	306	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain	diode				
I _S	source current	T _{mb} = 25 °C	<u>[1]</u> _	120	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	680	А
Avalanche rug	ggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 120 A; $V_{sup} \le 100$ V; R_{GS} = 50 Ω ; Unclamped	-	537	mJ

[1] Continuous current is limited by package.

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5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.49	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

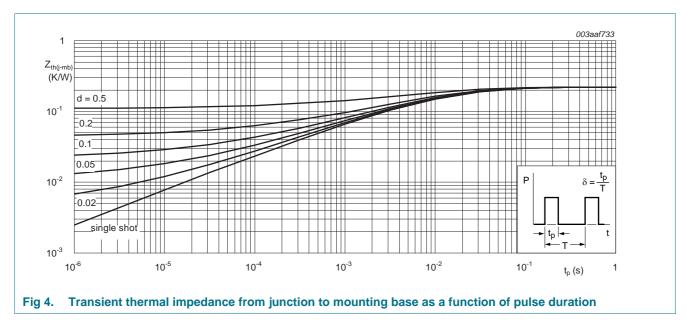


Table 5. Thermal characteristics

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6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source breakdown	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^\circ C$	100	-	-	V
	voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^\circ C$	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ see Figure 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see Figure 11; see Figure 10	2	3	4	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.08	10	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	250	500	μA
IGSS	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _i = 25 °C	-	10	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12; see Figure 13	-	9	10.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	5.9	6.9	mΩ
		$V_{GS} = 10 \text{ V}; \text{ I}_{D} = 25 \text{ A}; \text{ T}_{j} = 25 \text{ °C};$ see Figure 12; see Figure 13	-	3.28	3.9	mΩ
R _G	gate resistance	f = 1 MHz	-	0.9	-	Ω
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 75 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14; see Figure 15	-	170	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	140	-	nC
Q _{GS}	gate-source charge	$I_D = 75 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 15; see Figure 14	-	48	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	$I_D = 75 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14; see Figure 15	-	31	-	nC
Q _{GS(th} -pl)	post-threshold gate-source charge		-	17.3	-	nC
Q _{GD}	gate-drain charge		-	49	-	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 50 V; see <u>Figure 14;</u> see <u>Figure 15</u>	-	5.1	-	V
C _{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	9900	-	pF
C _{oss}	output capacitance	$T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 16}{100}$	-	660	-	pF
C _{rss}	reverse transfer capacitance		-	381	-	pF
d(on)	turn-on delay time	V_{DS} = 50 V; R_{L} = 0.67 Ω; V_{GS} = 10 V;	-	45	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \ \Omega; \ I_D = 75 \ A; \ T_j = 25 \ ^{\circ}C$	-	91	-	ns
t _{d(off)}	turn-off delay time		-	122	-	ns
t _f	fall time		-	63	-	ns

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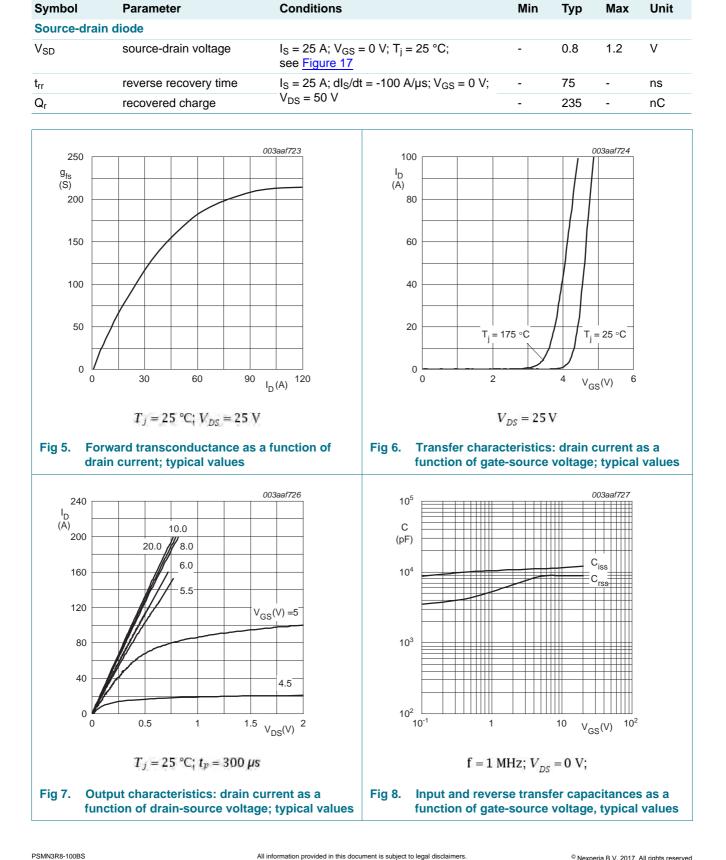
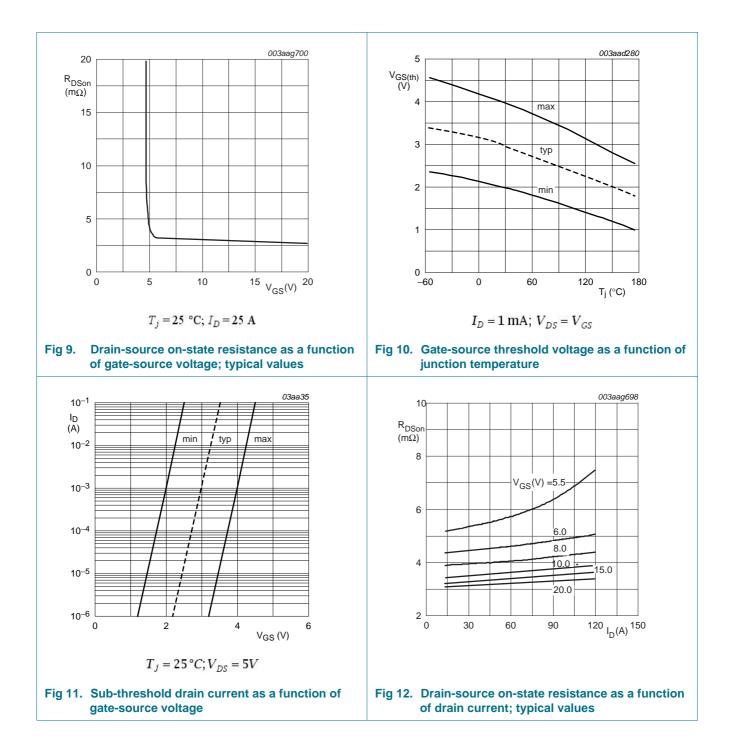


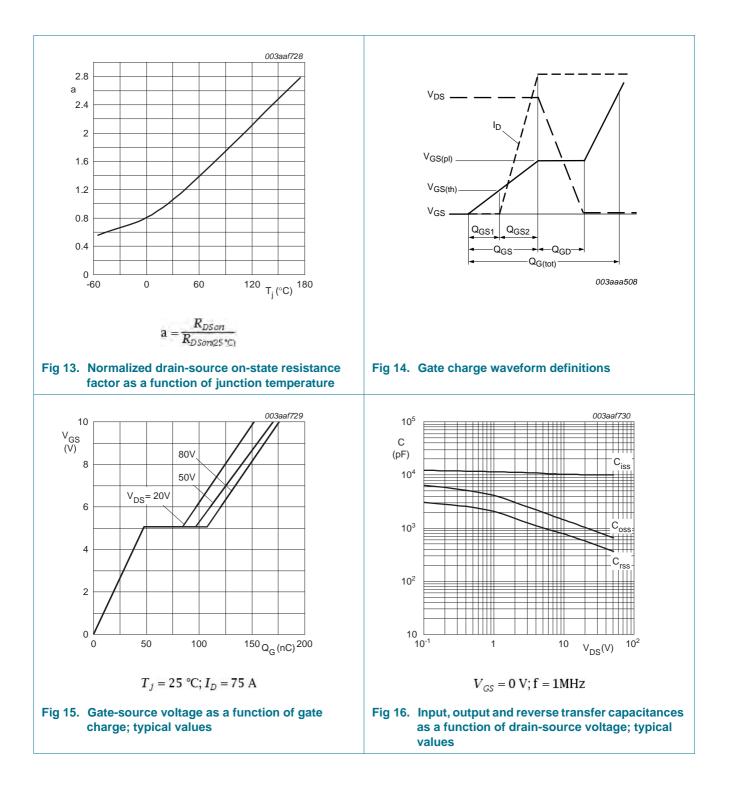
Table 6. Characteristics ...continued

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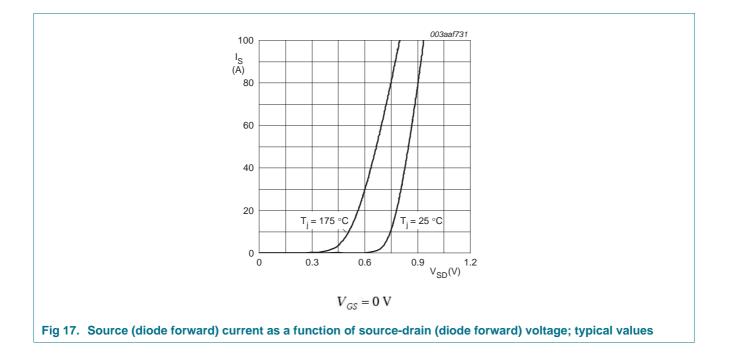
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7. Package outline

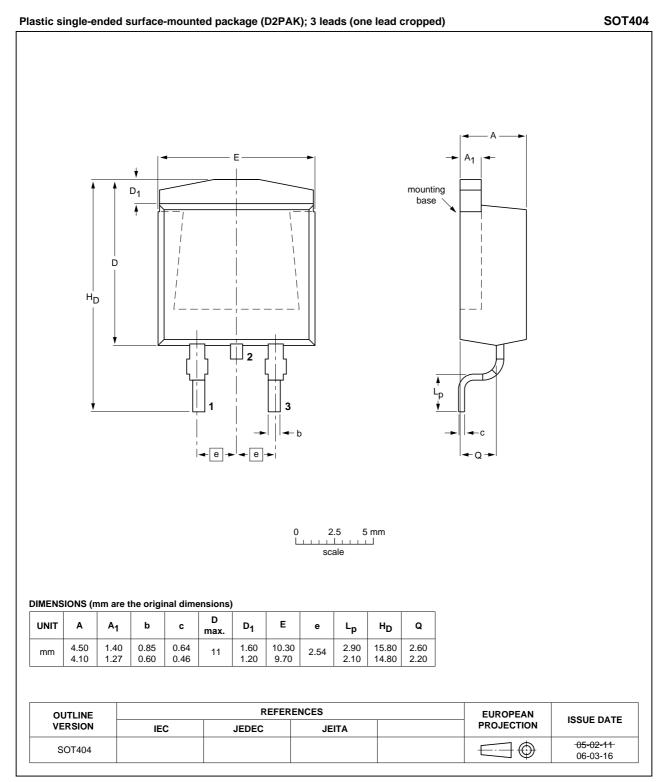


Fig 18. Package outline SOT404 (D2PAK)

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8. Revision history

Table 7. Revision history	able 7.	Revision history
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Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R8-100BS v.2	20120229	Product data sheet	-	PSMN3R8-100BS v.1
Modifications:	Status changed	from objective to product.		
	 Various changes 	s to content.		
PSMN3R8-100BS v.1	20110829	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Product data sheet

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