



## 2.5V/3.3V 1.5GHz PRECISION LVPECL PROGRAMMABLE DELAY WITH FINE TUNE CONTROL

Precision Edge®  
SY89296U

### FEATURES

- Precision LVPECL programmable delay line
- Guaranteed AC performance over temperature and voltage:
  - > 1.5GHz  $f_{MAX}$
  - < 160ps rise/fall times
- Low jitter design:
  - < 10ps<sub>pp</sub> total jitter
  - < 2ps<sub>RMS</sub> cycle-to-cycle jitter
  - < 1ps<sub>RMS</sub> random jitter
- Programmable delay range: 3.2ns to 14.8ns in 10ps increments
- Increased monotonicity over the MC100EP195
- ±10% of LSB INL
- $V_{BB}$  output reference voltage
- Parallel inputs accepts LVPECL or CMOS/LVTTL
- 40ps/V fine tuning range
- Low voltage operation: 2.5V ±5% and 3.3V ±10%
- Industrial -40°C to +85°C temperature range
- Available in 32-pin (5mm × 5mm) MLF® package or 32-pin TQFP package



Precision Edge®

### DESCRIPTION

The SY89296U is a programmable delay line that delays the input signal using a digital control signal. The delay can vary from 3.2ns to 14.8ns in 10ps increments. Further, the delay may be varied continuously in about 40ps range by setting the voltage at the FTUNE pin. In addition, the input signal is LVPECL, uses either a 2.5V ±5% or 3.3V ±10% power supply, and is guaranteed over the full industrial temperature range (-40°C to +85°C).

The delay varies in discrete steps based on a control word. The control word is 10-bits long and controls the delay in 10ps increments. The eleventh bit is D[10] and is used to simultaneously cascade the SY89296U for a larger delay range. In addition, the input pins IN and /IN default to an equivalent low state when left floating. Further, for maximum flexibility, the control register interface accepts CMOS or TTL level signals.

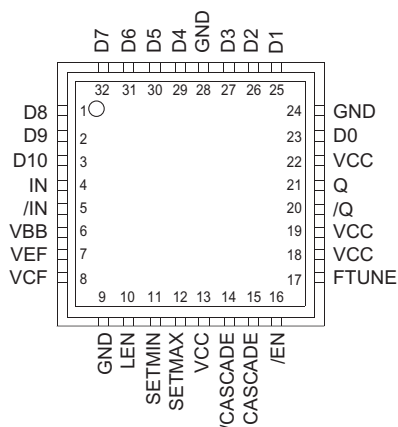
For applications that do not require an analog delay input, see the SY89295U. The SY89295U and SY89296U are part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's website at [www.micrel.com](http://www.micrel.com).

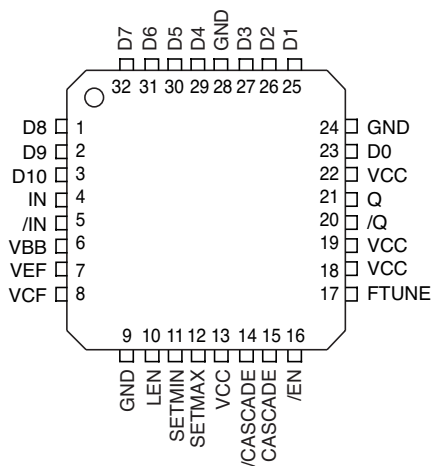
### APPLICATIONS

- Clock de-skewing
- Timing adjustments
- Aperture centering

**PACKAGE/ORDERING INFORMATION**



**32-Pin MLF™ (MLF-32)**



**32-Pin TQFP (T32-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89296UMI	MLF-32	Industrial	SY89296U	Sn-Pb
SY89296UMITR <sup>(2)</sup>	MLF-32	Industrial	SY89296U	Sn-Pb
SY89296UTI	T32-1	Industrial	SY89296U	Sn-Pb
SY89296UTITR <sup>(2)</sup>	T32-1	Industrial	SY89296U	Sn-Pb
SY89296UMG <sup>(3)</sup>	MLF-32	Industrial	SY89296U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89296UMGTR <sup>(2, 3)</sup>	MLF-32	Industrial	SY89296U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89296UTG <sup>(3)</sup>	T32-1	Industrial	SY89296U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89296UTGTR <sup>(2, 3)</sup>	T32-1	Industrial	SY89296U with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**TRUTH TABLES**

**Input/Output**

Inputs		Outputs	
IN	/IN	OUT	/OUT
0	1	0	1
1	0	1	0

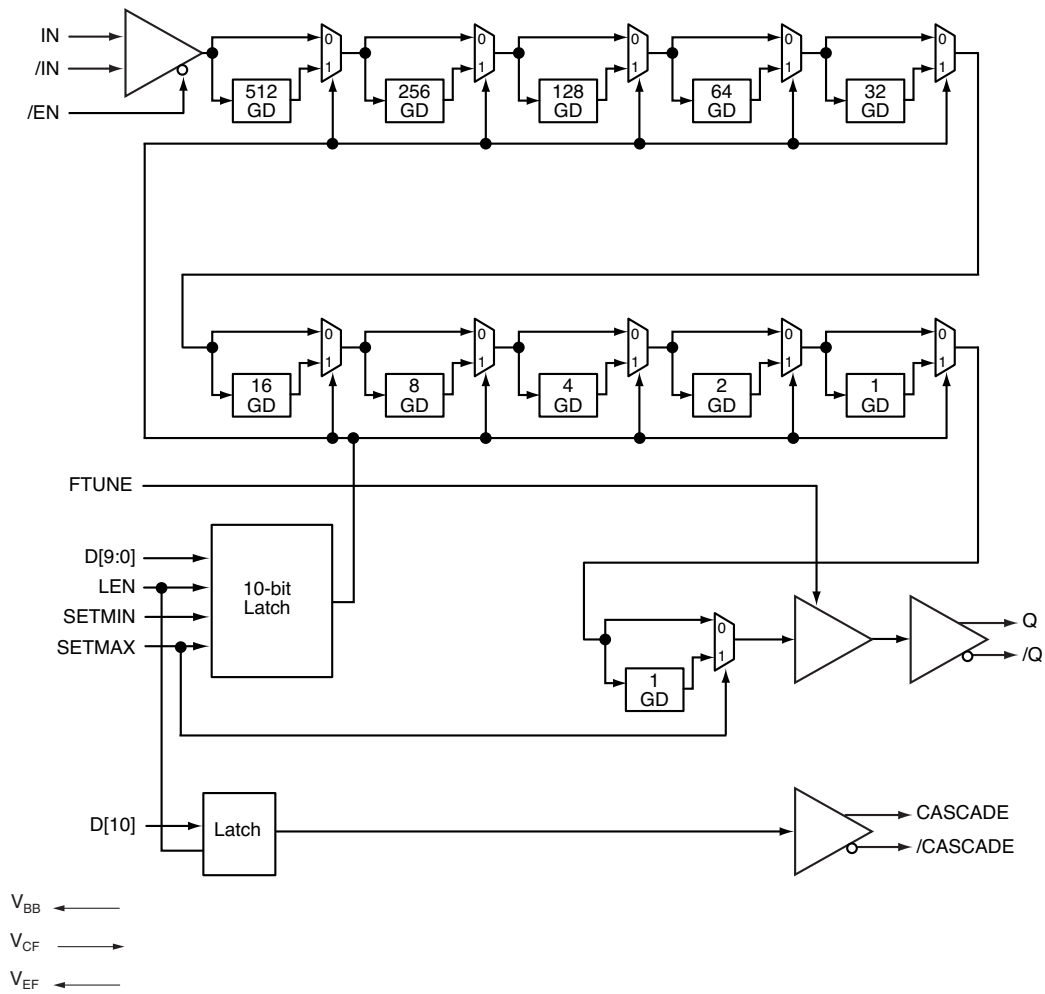
**Digital Control Latch**

LEN	Latch Action
0	Pass Through D[10:0]
1	Latched D[10:0]

**Input Enable**

/EN	Q, /Q
0	IN, /IN Delayed
1	Latched D[10:0]

**FUNCTIONAL BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function	
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[9:0]	CMOS, ECL, or TTL Control Bits: These control signals adjust the delay from IN to Q. See “AC Electrical Characteristics” for delay values. In addition, see “Interface Applications” section which illustrates the proper interfacing techniques for different logic standards. D[9:0] contains pull-downs and defaults LOW when left floating. D0 (LSB), and D9 (MSB). See “Typical Operating Characteristics” for delay information.	
3	D10	CMOS, ECL, or TTL Control Bit: This bit is used to cascade devices for an extended delay range. In addition, it drives CASCADE and /CASCADE. Further, D[10] contains a pull-down and defaults LOW when left floating.	
4, 5	IN, /IN	LVPECL/ECL Signal Input: Input signal to be delayed. IN contains a 75kΩ pull-down and will default to a logic LOW if left floating.	
6	VBB <sup>(1)</sup>	Reference Voltage Output: When using a single-ended input signal source to IN or /IN, connect the unused input of the differential pair to this pin. This pin can also be used to rebias AC-coupled inputs to IN and /IN. When used, de-couple to V <sub>CC</sub> using a 0.01μF capacitor, otherwise leave floating if not used. Maximum sink/source is ±0.5mA.	
7	VEF	Reference Voltage Output: Connect this pin to V <sub>CF</sub> when D[9:0], and D[10] is ECL.	
		<b>Logic Standard</b>	<b>V<sub>CF</sub> Connects to</b>
		LVPECL	V <sub>EF</sub> <sup>(1)</sup>
		CMOS	No Connect
		TTL	1.5V Source
8	VCF	Reference Voltage Input: The voltage driven on V <sub>CF</sub> sets the logic transition threshold for D[9:0], and D[10].	
9, 24, 28	GND, Exposed Pad <sup>(2)</sup>	Negative Supply: For MLF™ package, exposed pad must be connected to a ground plane that is the same potential as the ground pin.	
10	LEN	ECL Control Input: When HIGH latches the D[9:0] and D[10] bits. When LOW, the D[9:0] and D[10] latches are transparent.	
11	SETMIN	ECL Control Input: When HIGH, D[9:0] registers are reset. When LOW, the delay is set by SETMAX or D[9:0] and D[10]. SETMIN contains a pull-down and defaults LOW when left floating.	
12	SETMAX	ECL Control Input: When SETMAX is set HIGH and SETMIN is set LOW, D[9:0] = 111111111. When SETMAX is LOW, the delay is set by SETMIN or D[9:0] and D[10]. SETMAX contains a pull-down and defaults LOW when left floating.	
13, 18, 19, 22	VCC	Positive Power Supply: Bypass with 0.1μF and 0.01μF low ESR capacitors.	
14, 15	/Cascade, Cascade	LVPECL Differential Output: The outputs are used when cascading two or more SY89296U to extend the delay range.	
16	/EN	LVPECL Single-Ended Control Input: When LOW, Q is delayed from IN. When HIGH, Q is a differential LOW. /EN contains a pull-down and defaults LOW when left floating.	
20, 21	/Q, Q	LVPECL Differential Output: Q is a delayed version of IN. Always terminate the output with 50Ω to V <sub>CC</sub> – 2V. See “Output Interface Applications” section.	
17	FTUNE	Voltage Control Input: By varying the voltage, the delay is fine tuned, see the graph, “Propagation Delay vs. FTUNE Voltage.” Leave pin floating if not used.	

**Notes:**

1. Single-ended operation is only functional at 3.3V.
2. MLF™ package only.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20 sec.)	+260°C
Storage Temperature Range ( $T_S$ )	-65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ )	+2.375V to +3.6V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance <sup>(3)</sup>	
MLF™ ( $\theta_{JA}$ )	
Still-Air	35°C/W
MLF™ ( $\psi_{JB}$ )	
Junction-to-Board	28°C/W
TQFP ( $\theta_{JA}$ )	
Still-Air	28°C/W
TQFP ( $\psi_{JB}$ )	
Junction-to-Board	20°C/W

## DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply	$V_{CC} = 2.5\text{V}$	2.375	2.5	2.625	V
		$V_{CC} = 3.3\text{V}$	3	3.3	3.6	V
$I_{EE}$	Power Supply Current	No load, max $V_{CC}$			220	mA
$V_{IN}$	Input Voltage Swing (IN, /IN)	See Figure 1a.	150		1200	mV
$V_{DIFF\_IN}$	Differential Input Voltage Swing (IN, /IN)	See Figure 1b.	300		2400	mV
$V_{IHCMR}$	Input High Common Mode Range	IN, /IN	$V_{EE}+1.2$		$V_{CC}$	V

$V_{CC} = 3.3\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage (IN, /IN)		2.075		2.420	V
$V_{IL}$	Input Low High Voltage (IN, /IN)		1.355		1.675	V
$V_{BB}$	Output Voltage Reference		1.775	1.875	1.975	V
$V_{EF}$	Mode Connection		1.9	2.0	2.1	V
$V_{CF}$	Input Select Voltage		1.55	1.65	1.75	V

$V_{CC} = 2.5\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage (IN, /IN)		1.275		1.62	V
$V_{IL}$	Input Low High Voltage (IN, /IN)		0.555		0.875	V
$V_{BB}$	Output Voltage Reference		0.925	1.075	1.175	V
$V_{EF}$	Mode Connection		1.10	1.20	1.30	V
$V_{CF}$	Input Select Voltage		1.15	1.25	1.35	V

**Notes:**

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance on MLF™ packages assumes exposed pad is soldered (or equivalent) to the device most negative potential (GND).
4. The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. Input and output parameters vary 1:1 with  $V_{CC}$ , with the exception of  $V_{CF}$ .

**LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>**

$V_{CC} = 3.3V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}-2V$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage (Q, /Q)		2.155	2.280	2.405	V
$V_{OL}$	Output LOW Voltage (Q, /Q)		1.355	1.480	1.605	V
$V_{OUT}$	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1.1	1.6		V

**LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>**

$V_{CC} = 2.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}-2V$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage (Q, /Q)		1.355	1.48	1.605	V
$V_{OL}$	Output LOW Voltage (Q, /Q)		0.555	0.680	0.805	V
$V_{OUT}$	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1.1	1.6		V

**LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS<sup>(6)</sup>**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current				40	$\mu A$
$I_{IL}$	Input LOW Current		-300			$\mu A$

**Notes:**

- The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.  $V_{OH}$  and  $V_{OL}$  parameters vary 1:1 with  $V_{CC}$ .
- The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

**AC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>**

T<sub>A</sub> = -40°C to +85°C; unless otherwise stated.

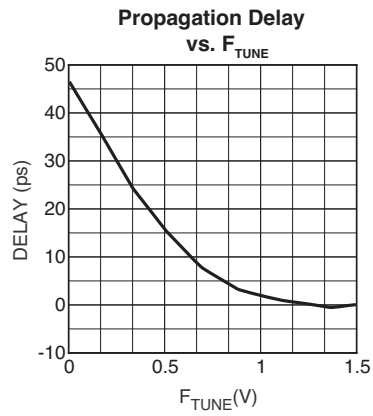
Symbol	Parameter	Condition	Min	Typ	Max	Units
f <sub>MAX</sub>	Maximum Operating Frequency	Clock	1.5			GHz
t <sub>pd</sub>	Propagation Delay IN to Q; D[0-10]=0 IN to Q; D[0-10]=1023 /EN to Q; D[0-10]=0 D10 to CASCADE		3200		4200	ps
			11500		14800	ps
			3400		4400	ps
			350		670	ps
t <sub>RANGE</sub>	Programmable Range t <sub>pd</sub> (max) – t <sub>pd</sub> (min)		8300			ps
t <sub>SKEW</sub>	Duty Cycle Skew t <sub>PHL</sub> – t <sub>PLH</sub>	<b>Note 8</b>			25	ps
Δt	Step Delay	D0 High		10		ps
		D1 High		15		ps
		D2 High		35		ps
		D3 High		70		ps
		D4 High		145		ps
		D5 High		290		ps
		D6 High		575		ps
		D7 High		1150		ps
		D8 High		2300		ps
		D9 High D0-D9 High		4610 9220		ps ps
INL	Integral Non-Linearity	<b>Note 9</b>	-10		+10	%LSB
t <sub>S</sub>	Setup Time	D t+o LEN	200			ps
		D to IN	350			ps
		/EN to IN	300			ps
t <sub>H</sub>	Hold Time	LEN to D	200			ps
		IN to /EN	400			ps
t <sub>R</sub>	Release Time	/EN to IN	500			ps
		SETMAX to LEN	500			ps
		SETMIN to LEN	450			ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter	<b>Note 13</b>			2	ps <sub>RMS</sub>
	Total Jitter	<b>Note 14</b>			10	ps <sub>PP</sub>
	Random Jitter	<b>Note 15</b>			1	ps <sub>RMS</sub>
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	20% to 80% (Q)	50	85	160	ps
		20% to 80% (CASCADE)	90		300	ps
	Duty Cycle		45		55	%
f <sub>T</sub>	FTUNE	0 ≤ FTUNE ≤ 1.25V		47	52	ps/V

**Notes:**

- High frequency AC electricals are guaranteed by design and characterization
- Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the crosspoint of the output.
- INL (Integral Non-Linearity) is defined from its corresponding point on the ideal delay versus D[9:0] curve as the deviation from its ideal delay. The maximum difference is the INL. Theoretical Ideal Linearity (TIL) = (measured maximum delay – measured minimum delay) ÷ 1024. INL = measured delay – measured minimum delay + (step number × TIL).
- This setup time defines the amount of time prior to the input signal. The delay tap of the device must be set.
- This setup time defines the amount of the time that /EN must be asserted prior to the next transition of IN, /IN to prevent an output response greater than ±75mV to the IN, /IN transition.
- Hold time is the minimum time that /EN must remain asserted after a negative going IN or a positive going /IN to prevent an output response greater than ±75mV to that IN, /IN transition.
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles over a random sample of adjacent cycle pairs.  
T<sub>jitter\_cc</sub> = T<sub>n</sub> – T<sub>n+1</sub>, where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input, no more than one output edge in 10<sup>12</sup> output edges will deviate by more than the specified peak-to-peak jitter value.
- Random jitter definition: jitter that is characterized by a Gaussian distribution, unbounded and is quantified by its standard deviation and mean. Random jitter is measured with a K28.7 comma defect pattern, measured at 1.5Gbps.

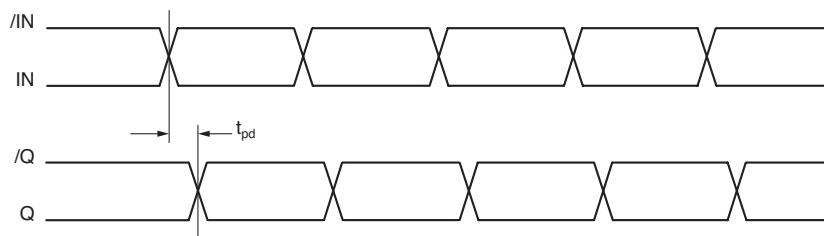
**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3V$ ,  $GND = 0$ ,  $D_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.





**TIMING DIAGRAM**



**SINGLE-ENDED AND DIFFERENTIAL SWINGS**

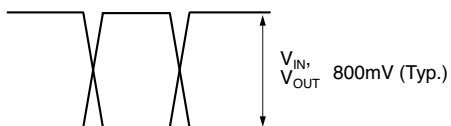


Figure 1a. Single-Ended Voltage Swing

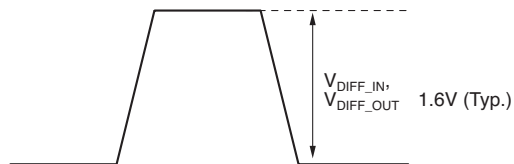


Figure 1b. Differential Voltage Swing

**INPUT AND OUTPUT STAGES**

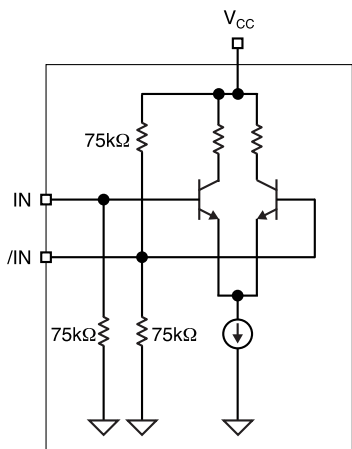


Figure 2a. Differential Input Stage

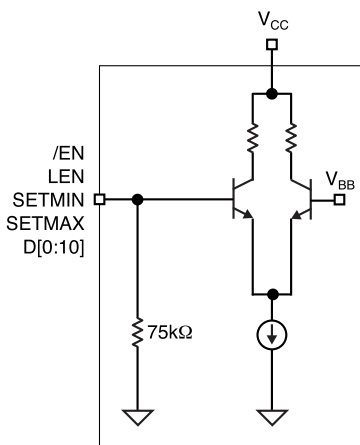


Figure 2b. Single-Ended Input Stage

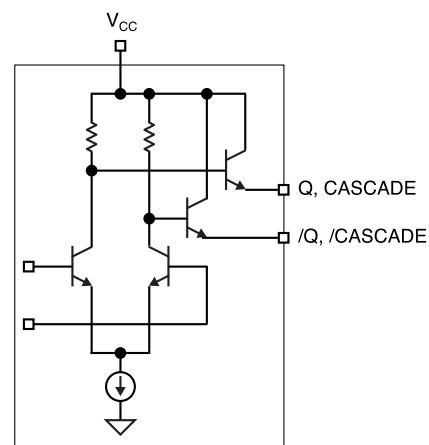
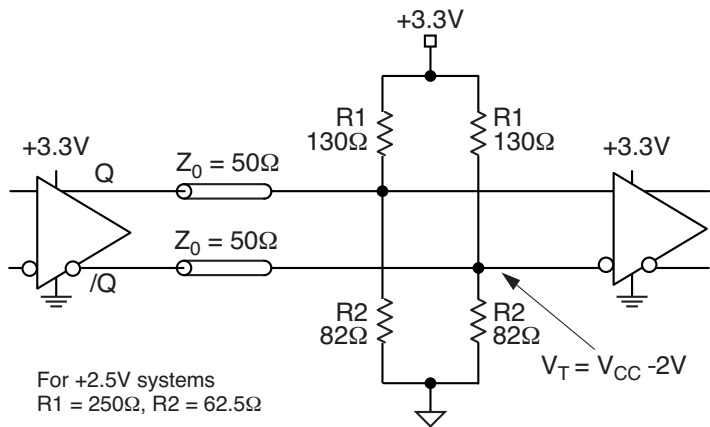
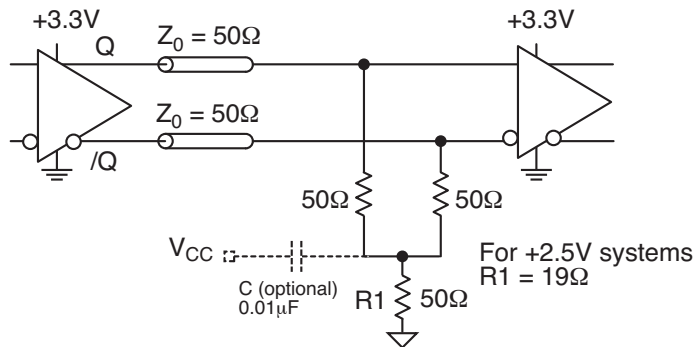


Figure 3. LVPECL Output Stage

**OUTPUT INTERFACE APPLICATIONS**



**Figure 4. Parallel Termination**



**Figure 5. Y-Termination**



**Figure 6. Terminating Unused I/O**

**APPLICATIONS INFORMATION**

For best performance, use good high frequency layout techniques, filter  $V_{CC}$  supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY89296U data inputs and outputs.

**$V_{BB}$  Reference**

The  $V_{BB}$  pin is an internally generated reference and is available for use only by the SY89296U. When unused, this pin should be left unconnected. The two common uses for  $V_{BB}$  are to handle a single-ended PECL input, and to re-bias inputs for AC-coupling applications.

If either IN or /IN is driven by a single-ended output,  $V_{BB}$  is used to bias the unused input. Please refer to Figure 10. The PECL signal driving the SY89296U may optionally be inverted in this case.

When the signal is AC-coupled,  $V_{BB}$  is used, as shown in Figure 13, to re-bias IN and/or /IN. This ensures that SY89296U inputs are within acceptable common mode range.

In all cases,  $V_{BB}$  current sinking or sourcing must be limited to 0.5mA or less.

**Setting D Input Logic Thresholds**

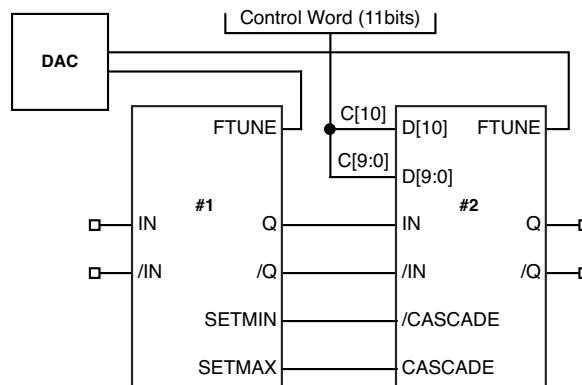
In all designs where the SY89296U GND supply is at zero volts, the D inputs can accommodate CMOS and TTL level signals, as well as PECL or LVPECL. Figures 11, 12, and 14 show how to connect  $V_{CF}$  and  $V_{EF}$  for all possible cases.

**Cascading**

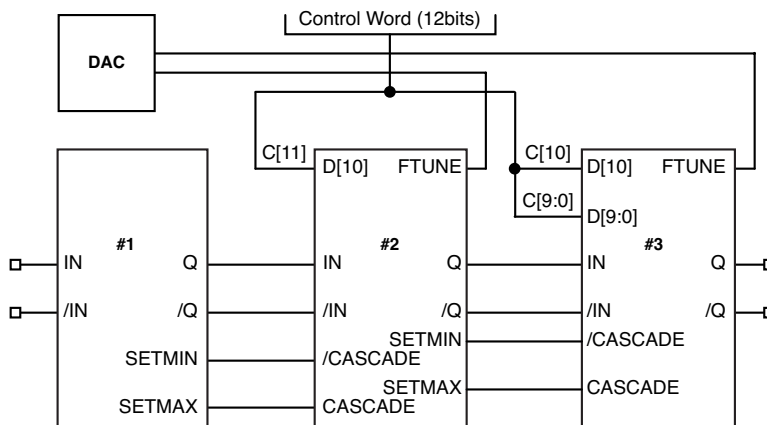
Two or more SY89296U may be cascaded in order to extend the range of delays permitted. Each additional SY89296U adds about 3.2ns to the minimum delay and adds another 10240ps to the delay range.

Internal cascade circuitry has been included in the SY89296U. Using this internal circuitry, the SY89296U may be cascaded without any external gating.

Examples of cascading 2, 3, or 4 SY89296U appear in Figures 7, 8, and 9.



**Figure 7. Cascading Two SY89296U**



**Figure 8. Cascading Three SY89296U**

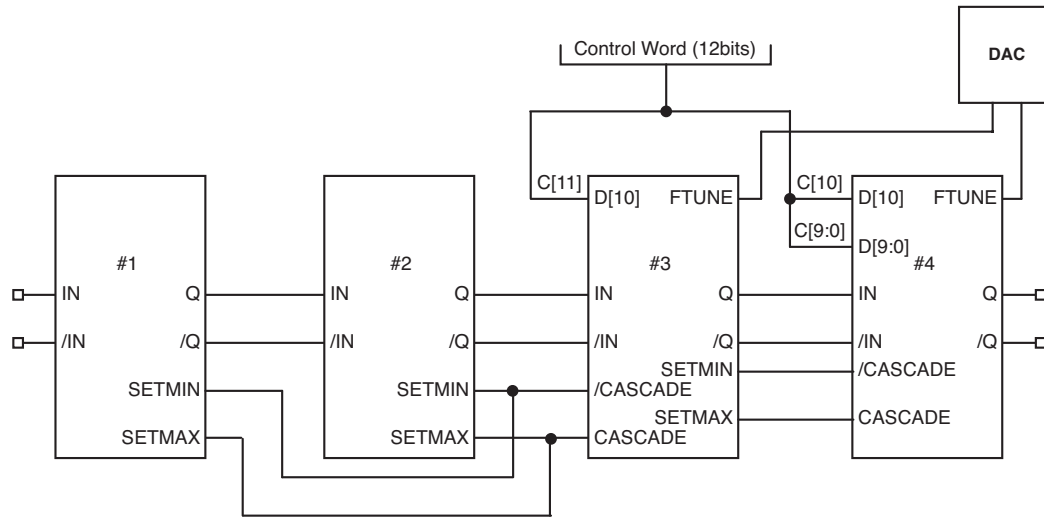
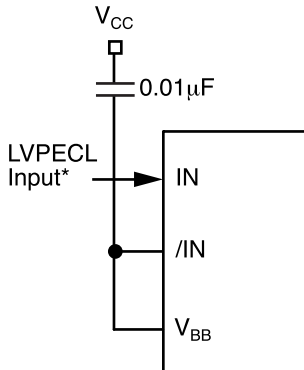


Figure 9. Cascading Four SY89296U

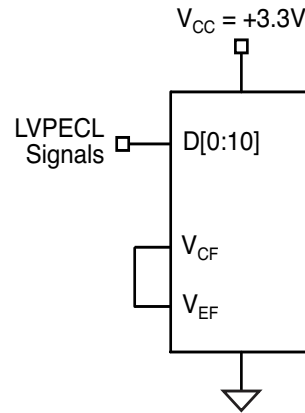
**INTERFACE APPLICATIONS**



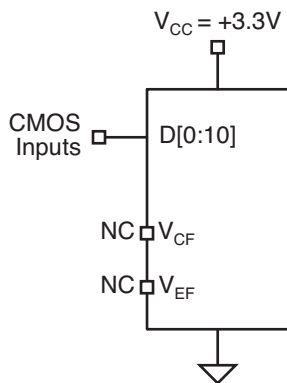
\* 3.3V single-ended only, 2.5V, single-ended is not functional.

**Figure 10. Interfacing to a Single-Ended LVPECL Signal**

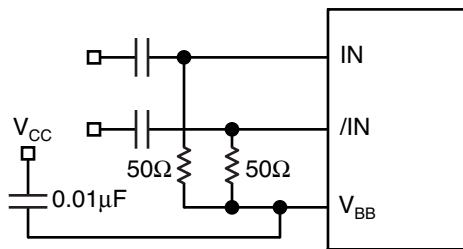
To invert the signal, connect the LVPECL input to /IN and connect VCC to IN.



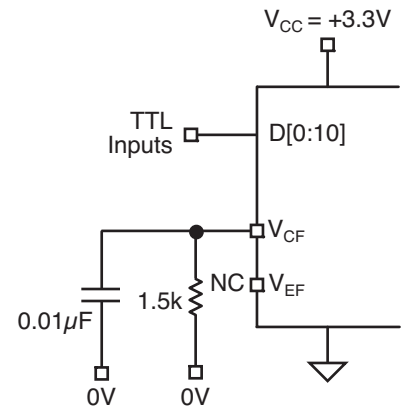
**Figure 11. V<sub>CF</sub>/V<sub>EF</sub> Biasing for LVPECL Control (D) Input**



**Figure 12. V<sub>CF</sub>/V<sub>EF</sub> Biasing for CMOS Control (D) Input**



**Figure 13. Re-Biasing an AC-Coupled Signal**

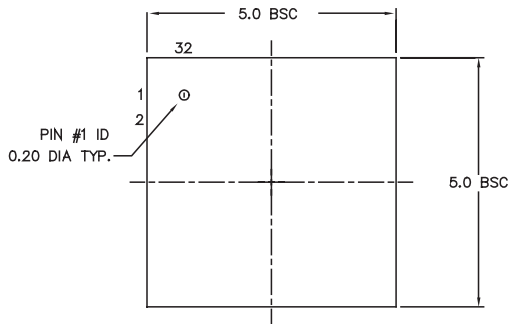


**Figure 14. V<sub>CF</sub>/V<sub>EF</sub> Biasing for LVTTTL Control (D) Input**

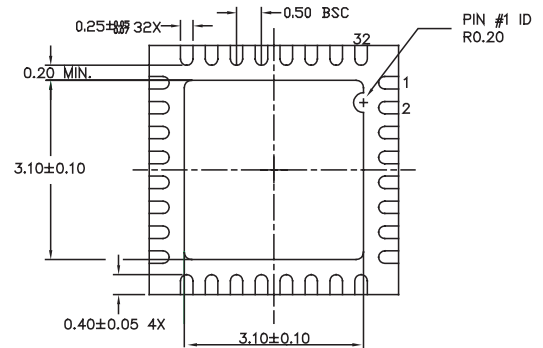
**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
SY89295U	2.5/3.3V 1.5GHz Precision LVPECL Programmable Delay	<a href="http://www.micrel.com/product-info/products/sy89295u.shtml">www.micrel.com/product-info/products/sy89295u.shtml</a>
SY89296U	2.5/3.3V 1.5GHz Precision LVPECL Programmable Delay with Fine Tune Control	<a href="http://www.micrel.com/product-info/products/sy89296u.shtml">www.micrel.com/product-info/products/sy89296u.shtml</a>
	16-MLF Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_appnote_0902.pdf">www.amkor.com/products/notes_papers/MLF_appnote_0902.pdf</a>
	HBW Solutions	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>

**32-PIN MicroLeadFrame® (MLF-32)**



TOP VIEW



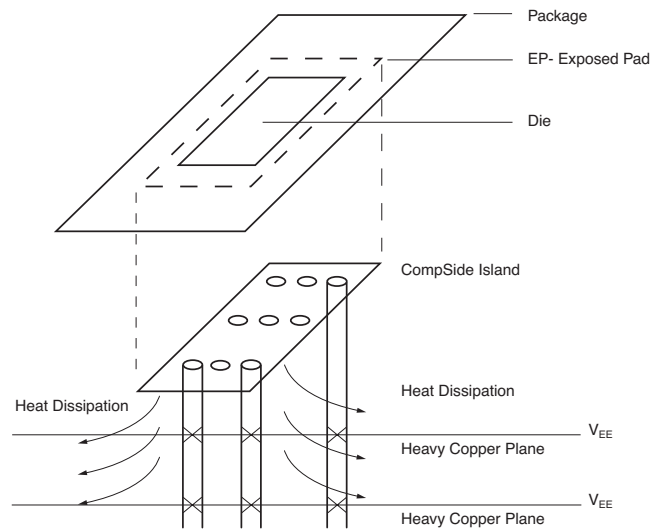
BOTTOM VIEW



SIDE VIEW

**NOTE:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

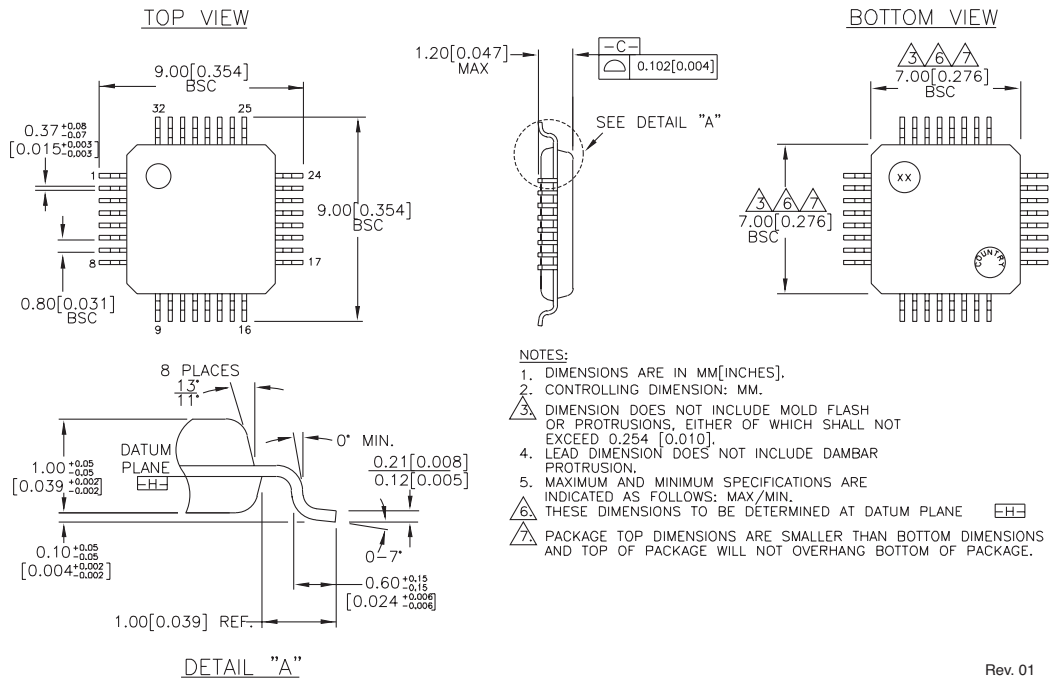


**PCB Thermal Consideration for 32-Pin MLF® Package  
(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

**32-PIN TQFP (T32-1)**



Rev. 01

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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