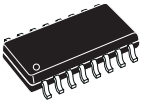
L6668

SMART PRIMARY CONTROLLER

1 General Features

- MULTIPOWER BCD TECHNOLOGY
- LOAD-DEPENDENT CURRENT-MODE CONTROL: FIXED-FREQUENCY (HEAVY LOAD), FREQUENCY FOLDBACK (LIGHT LOAD), BURST-MODE (NO-LOAD)
- ON-BOARD HIGH-VOLTAGE START-UP
- IMPROVED STANDBY FUNCTION
- LOW QUIESCENT CURRENT (< 2 mA)
- SLOPE COMPENSATION
- PULSE-BY-PULSE & HICCUP-MODE OCP
- INTERFACE WITH PFC CONTROLLER
- DISABLE FUNCTION (ON/OFF CONTROL)
- LATCHED DISABLE FOR OVP/OTP FUNCTION
- PROGRAMMABLE SOFT-START
- 2% PRECISION REFERENCE VOLTAGE EXTERNALLY AVAILABLE
- ±800 mA TOTEM POLE GATE DRIVER WITH INTERNAL CLAMP AND UVLO PULL-DOWN
- BLUE ANGEL, ENERGY STAR, EU CODE OF CONDUCT COMPLIANT

Figure 1. Package



SO-16 (Narrow)

Table 1. Order Codes

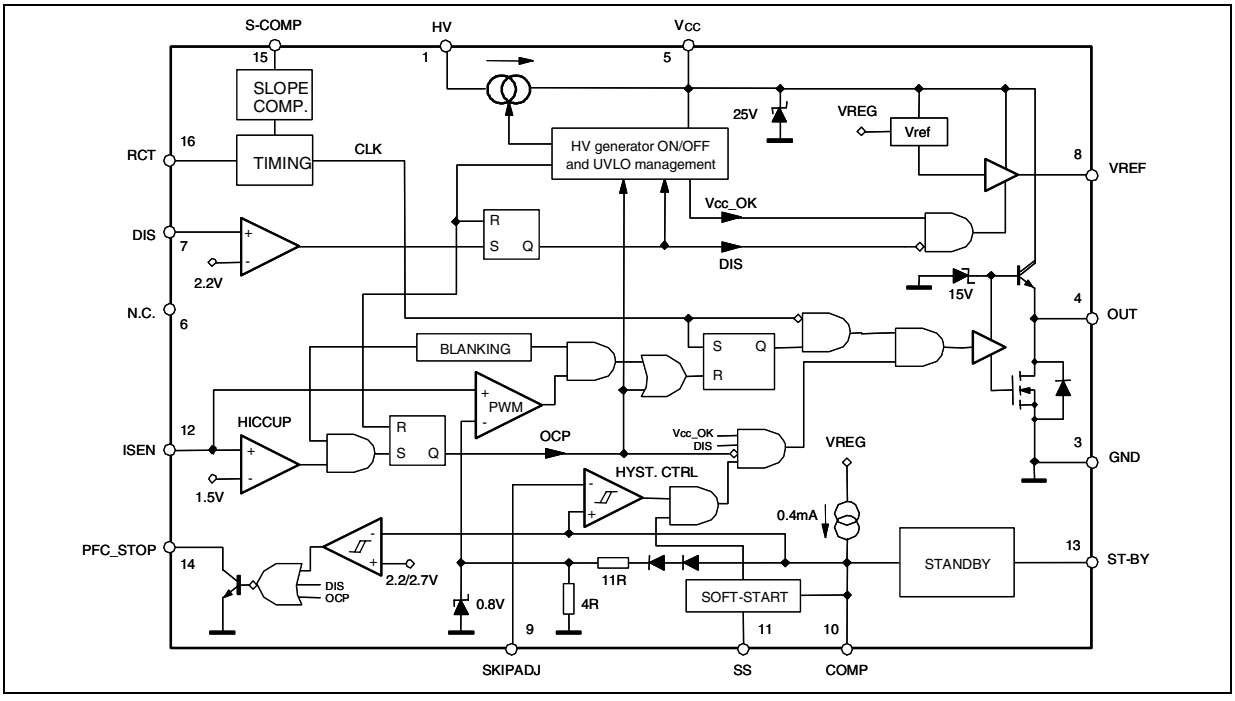
Part Number	Package
L6668	SO-16
L6668TR	SO-16 in Tape & Reel

- SO16 PACKAGE ECOPACK®

1.1 APPLICATIONS

- HI-END AC-DC ADAPTERS/CHARGERS FOR NOTEBOOKS.
- LCD/CRT MONITORS, LCD/CRT TV
- DIGITAL CONSUMER

Figure 2. Block Diagram



2 Description

L6668 is a current-mode primary controller IC, designed to build single-ended converters.

The IC drives the system at fixed frequency at heavy load and an improved Standby function causes a smooth frequency reduction as the load is progressively reduced. At very light load the device enters a special operating mode (burst-mode with fixed, externally programmed peak current) that, in addition to the on-board high-voltage start-up and the very low quiescent current, helps keep low the consumption from the mains and be compliant with energy saving regulations. To allow meeting compliance with these standards in power-factor-corrected systems too, an interface with the PFC controller is provided that enables to turn off the pre-regulator when the load level falls below a threshold.

The IC includes also a programmable soft-start, slope compensation for stable operation at duty cycles greater then 50%, a disable function, a leading edge blanking on current sense to improve noise immunity, latched disable for OVP or OTP shutdown and an effective two-level OCP able to protect the system even in case the secondary diode fails short.

Table 2. Absolute Maximum Ratings [1]

Symbol	Pin	Parameter	Value	Unit
V_{cc}	5	IC Supply voltage (Icc = 20 mA)	Self-limited	V
V_{HV}	1	High-voltage start-up generator voltage range	-0.3 to 700	V
I_{HV}	1	High-voltage start-up generator current	Self-limited	A
---		Analog Inputs & Outputs, except pin 14	-0.3 to 8	V
I_{PFC_STOP}	14	Max. sink current (low state)	2	mA
V_{PFC_STOP}	14	Max. voltage (open state)	16	V
P_{tot}		Power Dissipation @Tamb = 50°C	0.75	W
T_j		Junction Temperature Operating range	-25 to 150	°C
T_{stg}		Storage Temperature	-55 to 150	°C

Note: 1. ESD immunity for pin 1 is guaranteed up to 900V (Human Body Model).

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to AmbientMax	120	°C/W

Figure 3. Pin Connection (Top view)

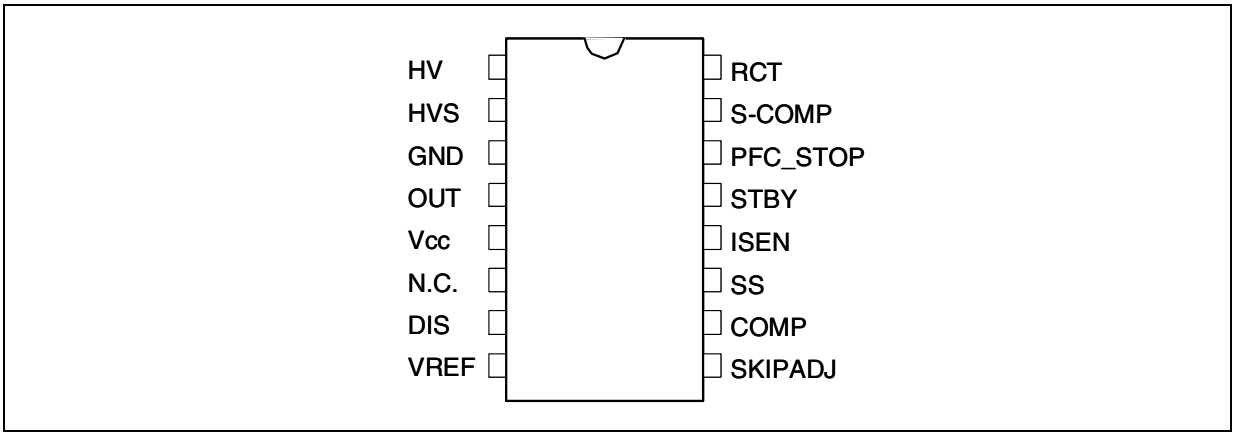


Table 4. Pin Description

Pin Number	Pin Name	Function
1	HV	High-voltage start-up. The pin is to be connected directly to the rectified mains voltage. A 0.8 mA internal current source charges the capacitor connected between pin Vcc and GND to start up the IC. When the voltage on the Vcc pin reaches the start-up threshold the generator is shut down. Normally it is re-enabled when the voltage on the Vcc pin falls below 5V, except under latched shutdown conditions, when it is re-enabled as the Vcc voltage falls 0.5V below the start-up threshold.
2	HVS	High-voltage spacer. The pin is not connected internally to isolate the high-voltage pin and comply with safety regulations (creepage distance) on the PCB.
3	GND	Chip ground. Current return for both the gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
4	OUT	Gate-drive output. The driver is capable of 0.8A min. source/sink peak current to drive MOSFET's. The voltage delivered to the gate is clamped at about 15V so as to prevent too high values when the IC is supplied with a voltage close to or exceeding 20V.
5	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The internal high voltage generator charges an electrolytic capacitor connected between this pin and GND as long as the voltage on the pin is below the start-up threshold of the IC, after that it is disabled. Sometimes a small bypass capacitor (0.1µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
6	N.C.	Connect the pin to GND.
7	DIS	Latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 2.2V, shuts the IC down and brings its consumption to a value barely higher than before start-up. The information is latched and it is necessary to recycle the input power to restart the IC: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Connect the pin to GND if the function is not used.
8	VREF	Voltage reference. An internal generator furnishes an accurate voltage reference (5V±4%, all inclusive) that can be used to supply up to 5 mA to an external circuit. A small film capacitor (0.1µF typ.), connected between this pin and GND is recommended to ensure the stability of the generator and to prevent noise from affecting the reference.
9	SKIPADJ	Burst-mode control threshold. A voltage is applied to this pin, derived from the reference voltage VREF via a resistor divider. When the control voltage at pin COMP falls 50 mV below the voltage on this pin the IC is shutdown and the consumption is reduced. The chip is re-enabled as the voltage on pin COMP exceeds the voltage on the pin. The high-voltage start-up generator is not invoked. The function is disabled during the soft-start ramp. The pin must always be biased between 0.8 and 2.5V. A voltage between 0.8 and 1.4V disables the function, if the pin is pulled below 0.8V the IC is shut down.
10	COMP	Control input for PWM regulation. The pin is to be driven by the phototransistor (emitter-grounded) of an optocoupler to modulate the voltage by modulating the current sunk from (sourced by) the pin (0.4 mA typ.). It is recommended to place a small filter capacitor between the pin and GND, as close to the IC as possible to reduce switching noise pick up, to set a pole in the output-to-control transfer function. A voltage 50 mV lower than that on pin SKIPADJ shuts down the IC and reduces its current consumption.
11	SS	Soft start. An internal 20µA generator charges an external capacitor connected between the pin and GND generating a voltage ramp across it. This ramp clamps the voltage at pin COMP during start-up, thus the duty cycle of the power switch starts from zero. During the ramp all functions monitoring the voltage at pin COMP are disabled. The SS capacitor is quickly discharged as the chip goes into UVLO.
12	ISEN	Current sense (PWM comparator) input. The voltage on this pin is internally compared with an internal reference derived from the voltage on pin COMP and when they are equal the gate drive output (previously asserted high by the clock signal generated by the oscillator) is driven low to turn off the power MOSFET. The pin is equipped with 200 ns. min. blanking time for improved noise immunity. A second comparison level located at 1.5V shuts the device down and brings its consumption almost to a "before start-up" level.

Table 4. Pin Description (continued)

Pin Number	Pin Name	Function
13	STBY	Standby function. This pin is a high-impedance one as long as the voltage on pin COMP is higher than 3V. When the voltage on pin COMP falls below 3V, the voltage on the pin tracks that on pin COMP and is capable of sinking current. A resistor connected from the pin to the oscillator allows programming frequency foldback at light load.
14	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin is intended for driving the base of a PNP transistor in systems comprising a PFC pre-regulator, to stop the PFC controller at light load by cutting its supply. The pin, normally low, opens if the voltage on COMP is lower than 2.2V and goes back low when the voltage on pin COMP exceeds 2.7V. Whenever the IC is shutdown, either latched (DIS >2.2V, ISEN >1.5V) or not (UVLO, SKIPADJ<0.8), the pin is open as well.
15	S-COMP	Voltage ramp for slope compensation. When the gate-drive output is high the pin delivers a voltage tracking the oscillator ramp (shifted down by one V_{BE}); when the gate-drive output is low the voltage delivered is zero. The pin is to be connected to pin ISEN via a resistor to make slope compensation and allow stable operation at duty cycles close to and greater than 50%.
16	RCT	Oscillator pin. A resistor to VREF and a capacitor to GND define the oscillator frequency (at full load). A resistor connect to STBY modifies the oscillator frequency when the voltage on pin COMP is lower than 3V.

Table 5. Electrical Characteristcs

(T_j = 0 to 105°C, Vcc=15V, Co=1nF; R_T =13.3k , C_T =1nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
Vcc	Operating range	After turn-on	9.4		22	V
V_{CCOn}	Turn-on threshold	(1)	12.5	13.5	14.5	V
V_{CCOff}	Turn-off threshold	(1) After turn-on	8.0	8.7	9.4	V
Hys	Hysteresis		4.0			V
V_Z	Zener Voltage	Icc = 20 mA	22	24	28	V
SUPPLY CURRENT						
$I_{start-up}$	Start-up Current	Before turn-on, Vcc=Vcc_{ON}-0.5		150		µA
I_q	Quiescent Current	After turn-on		2	2.5	mA
I_{CC}	Operating Supply Current				4	mA
I_{qdis}	Shutdown quiescent current	V_{DIS} > 2.2, or V_{ISEN} > 1.5		180		µA
		$V_{SKIPADJ}$<0.8		1	1.8	mA
		0.8 <V_{COMP} < $V_{SKIPADJ}$		1.3		mA
HIGH-VOLTAGE START-UP GENERATOR						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700			V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	60	80	105	V
I_{charge}	Vcc charge current	V_{HV} > $V_{Hvstart}$, Vcc > 3V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	V_{HV} > $V_{Hvstart}$, Vcc > 3V			1.6	mA
		V_{HV} > $V_{Hvstart}$, Vcc = 0			0.8	
$I_{HV, OFF}$	Leakage current (OFF state)	V_{HV} = 400 V			40	µA
$V_{CCrestart}$	HV generator restart voltage		4.4	5	5.6	V
		(1) After DIS tripping	12	13	14	V

Table 5. Electrical Characteristcs (continued)
(T_j = 0 to 105°C, Vcc=15V, Co=1nF; R_T =13.3k , C_T =1nF; unless otherwise specified)

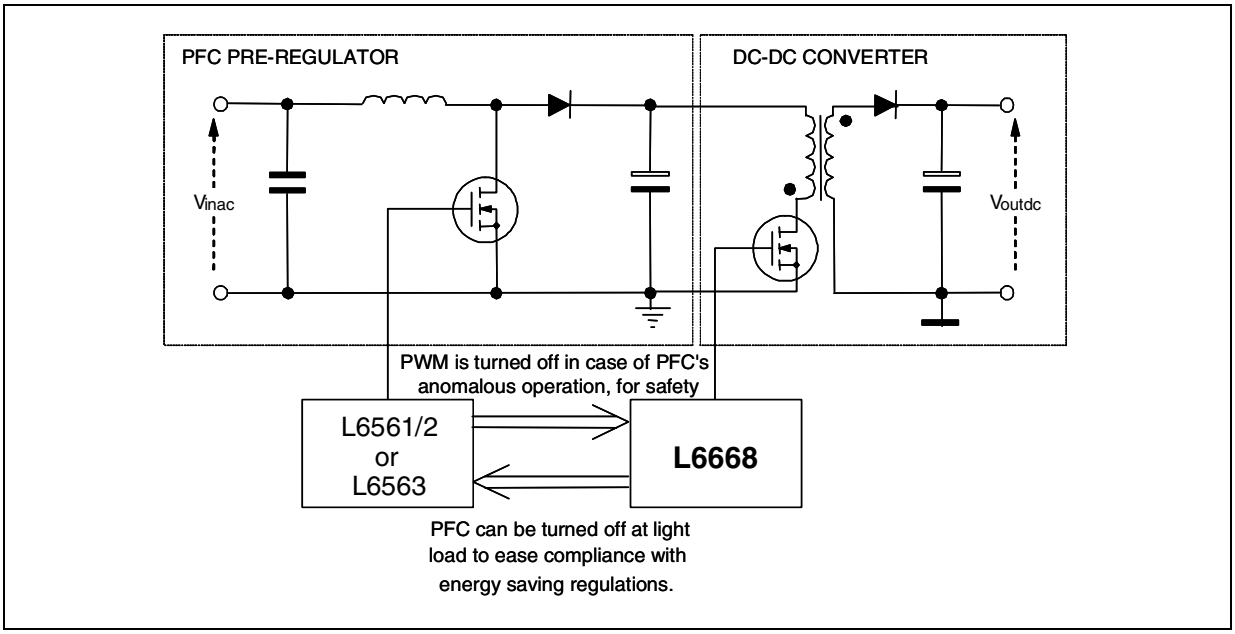
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE VOLTAGE						
V_{REF}	Output voltage	(2) Tj = 25 °C; I_{REF} = 1 mA	4.925	5	5.075	V
V_{REF}	Total variation	Vcc= 9.4 to 22 V, I_{REF} = 1 to 5 mA	4.8		5.13	V
I_{REF}	Short circuit current	V_{REF} = 0	10		30	mA
	Sink capability in UVLO	Vcc = 6V; Isink = 0.5 mA		0.2	0.5	V
PWM CONTROL						
V_{COMPH}	Maximum level	I_{COMP} =0	5.5			V
I_{COMP}	Max. source current	V_{COMP} = 1 V	320	400	480	µA
R_{COMP}	Dynamic resistance	V_{COMP} = 2 to 4 V		22		kΩ
D_{max}	Maximum duty cycle	V_{COMP} = 5 V	70		75	%
D_{min}	Minimum duty cycle	V_{COMP} = 1 V			0	%
CURRENT SENSE COMPARATOR						
I_{ISEN}	Input Bias Current	V_{ISEN} = 0			-1	µA
t_{LEB}	Leading Edge Blanking	After gate drive low-to-high transition	160	225	290	ns
$t_{d(H-L)}$	Delay to Output				100	ns
	Gain		3.56	3.75	3.94	V/V
V_{ISENx}	Maximum signal	V_{COMP} = 5 V	0.725	0.8	0.875	V
$V_{ISENdis}$	Hiccup-mode OCP level	(2)	1.35	1.5	1.65	V
STANDBY FUNCTION						
V_{drop}	V_{COMP} - V_{STBY}	I_{STBY} = 0.8 mA, V_{COMP}<3V		35		mV
V_{th}	Threshold on V_{COMP}	(2) Voltage falling		3		V
	Hysteresis		50			mV
LATCHED DISABLE FUNCTION						
I_{DIS}	Input Bias Current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold	(2) voltage rising	2.1	2.2	2.3	V
OSCILLATOR						
fsw	Oscillation Frequency	Tj = 25°C, V_{COMP} = 5 V	95	100	105	kHz
		Vcc = 9.4 to 22V, V_{COMP} = 5 V	93	100	107	kHz
Vpk	Oscillator peak voltage	(2)	2.85	3	3.15	V
Vvy	Oscillator valley voltage	(2)	0.8	0.95	1.1	V
SLOPE COMPENSATION						
$S\text{-}COMP_{pk}$	Ramp peak	$R_{S\text{-}COMP}$ = 3 kΩ to GND, OUT pin high, V_{COMP} = 5V	1.6	1.75	1.9	V
$S\text{-}COMP_{vy}$	Ramp starting value	$R_{S\text{-}COMP}$ = 3 kΩ to GND, OUT pin high	0.15	0.35	0.55	V
	Ramp voltage	OUT pin low		0		
	Source capability	$V_{S\text{-}COMP}$ = $V_{S\text{-}COMPpk}$	0.8			mA
SOFT-START						
I_{SSC}	Charge current	Tj = 25 °C	14	20	26	µA

Table 5. Electrical Characteristcs (continued)
(T_j = 0 to 105°C, Vcc=15V, Co=1nF; R_T =13.3k , C_T =1nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SSsat}	Low saturation voltage	Duty cycle = 0			0.6	V
$V_{SSclamp}$	High saturation voltage			7		V
SKIPADJ FUNCTION						
I_{bias}	Input Bias Current	V_{SKIP} = 0 to 4.5 V			-1	µA
V_{SKIP}	Operating range		1.4		2.5	V
Hys	Hysteresis	Below V_{SKIP}	25		85	mV
V_{OFF}	Shutdown threshold	Voltage falling			0.8	V
PFC_STOP FUNCTION						
I_{leak}	High level leakage current	V_{PFC_STOP} < 16V, V_{COMP} = 2V			1	µA
V_L	Low saturation level	I_{PFC_STOP} = 1mA, V_{COMP} = 4V			0.1	V
Vth	Threshold for high level	V_{COMP} falling (2)	2.1	2.2	2.3	V
Vth	Threshold for high level	V_{COMP} rising (2)	2.55	2.7	2.85	V
GATE DRIVER						
V_{OL}	Output Low Voltage	I_{sink} = 200 mA			1.0	V
V_{OH}	Output High voltage	I_{source} = 5 mA, Vcc = 12V	9.8	10.3		V
$I_{sourcepk}$	Peak source current		-0.8			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Current Fall Time			30		ns
t_r	Current Rise Time			55		ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5mA; Vcc = 20V	10	12	15	V
	UVLO saturation	Vcc= 0 to Vccon, I_{sink}= 2mA			1.1	V

(1), (2) Parameters in tracking each other

Figure 4. Typical System Block Diagram



3 Typical Electrical Performance

Figure 5. High-voltage generator ON-state sink current vs. Tj

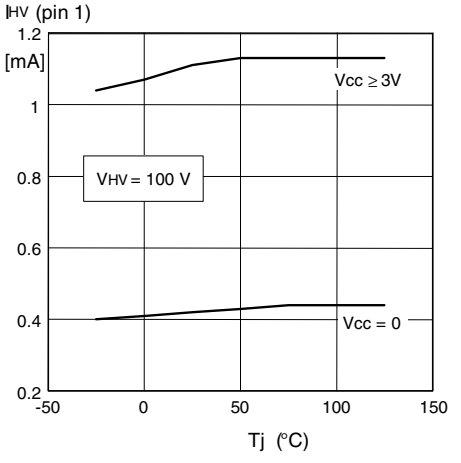


Figure 6. High-voltage generator output (Vcc charge current) vs. Tj

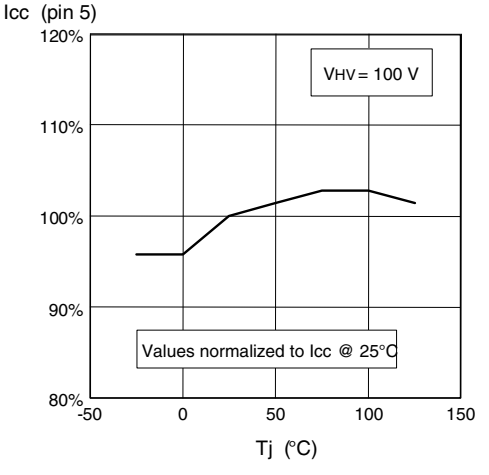


Figure 7. High-voltage pin leakage vs. Tj

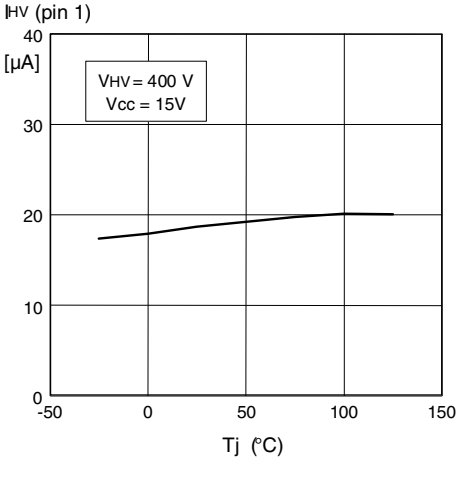


Figure 8. High-voltage generator start voltage vs. Tj

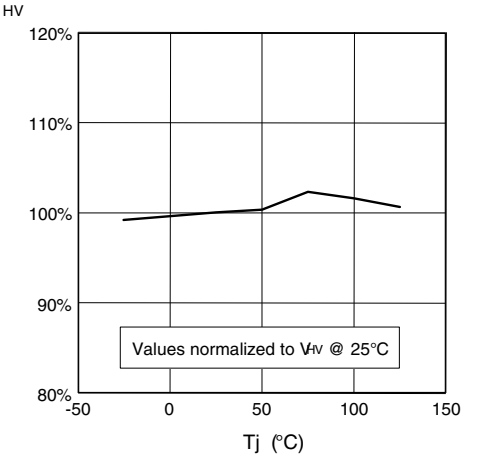


Figure 9. High-voltage generator Vcc restart voltage vs. Tj

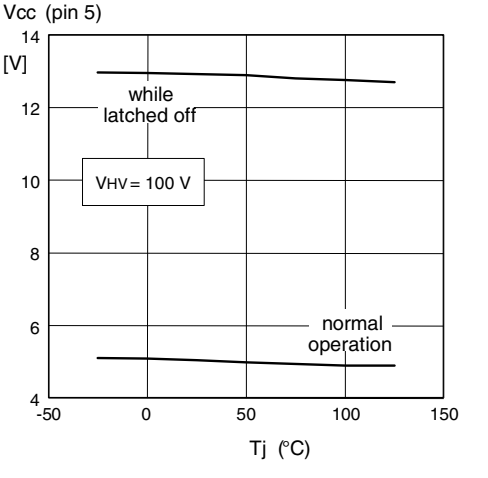


Figure 10. IC consumption vs. Tj

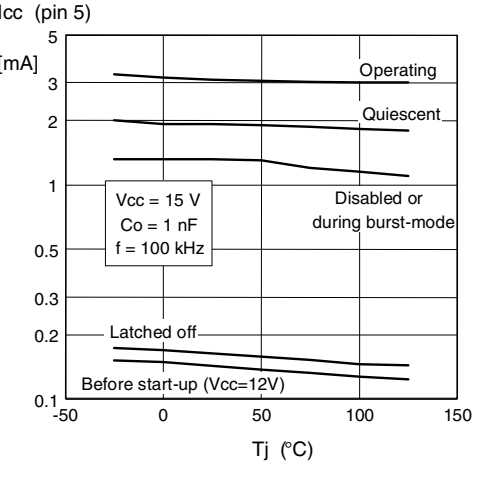


Figure 11. Start-up & UVLO vs. Tj

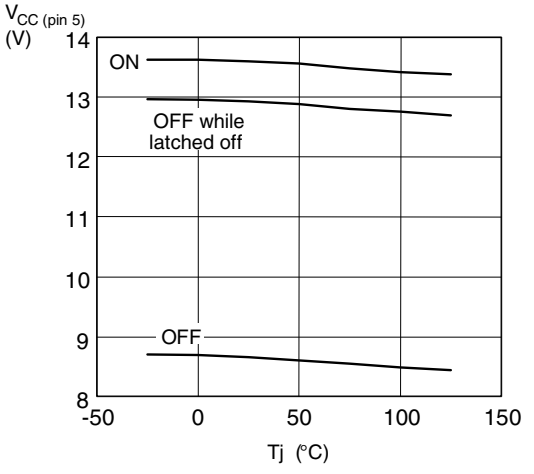


Figure 12. Vcc Zener voltage vs. Tj

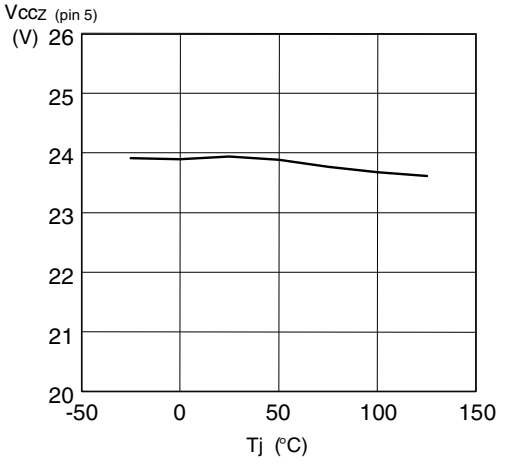


Figure 13. COMP voltage upper clamp level vs. Tj

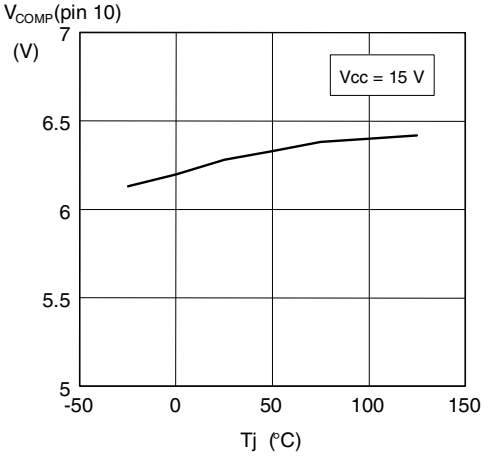


Figure 14. COMP source current vs. Tj

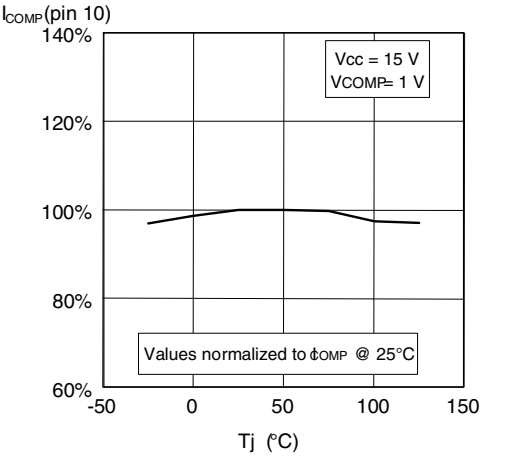


Figure 15. COMP dynamic resistance vs. Tj

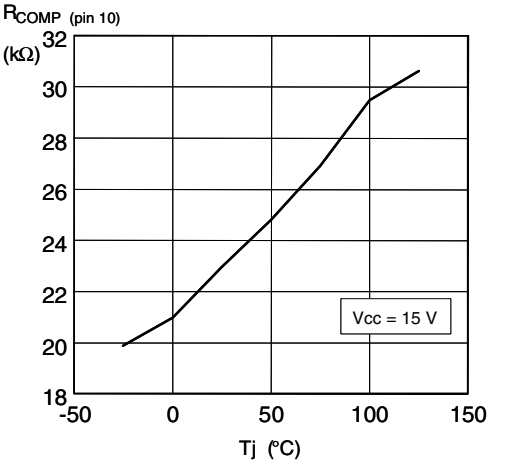


Figure 16. Max. duty-cycle vs. Tj

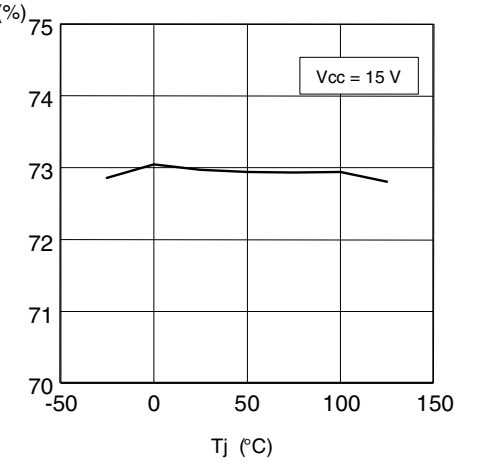


Figure 17. Oscillator frequency vs. Tj

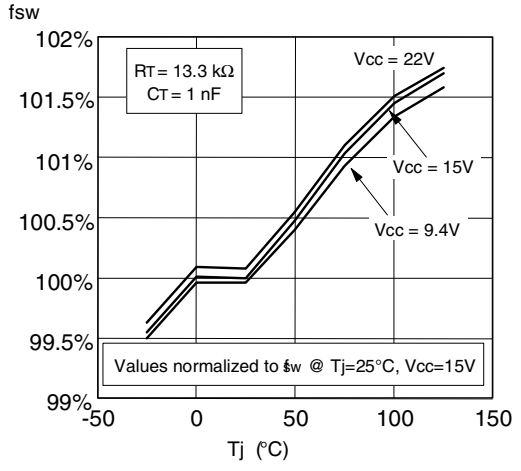


Figure 18. Oscillator ramp vs. Tj

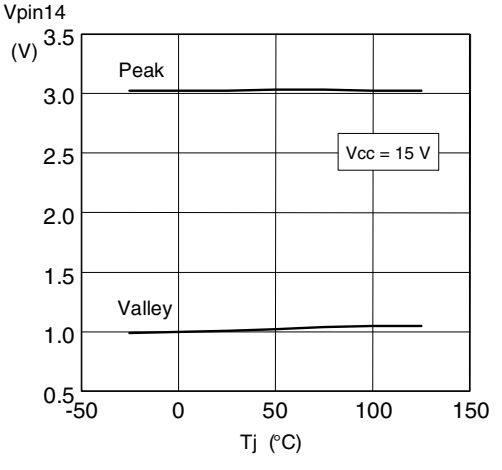


Figure 19. Current sense clamp vs. Tj

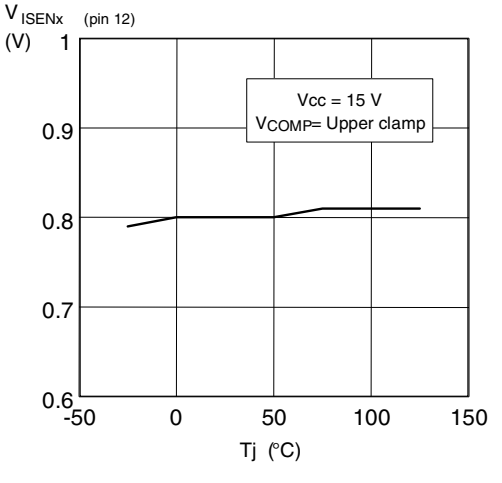


Figure 20. Disable level on current sense vs. Tj

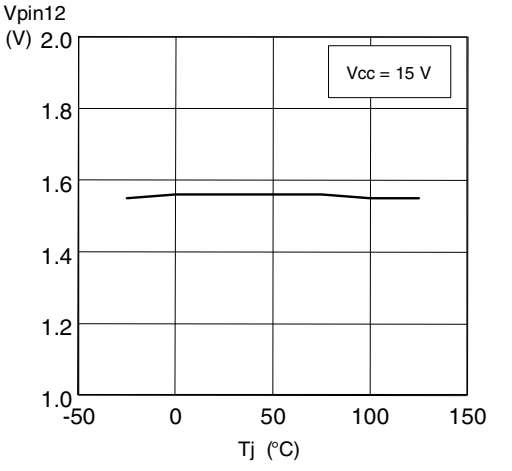


Figure 21. Reference voltage vs. Tj

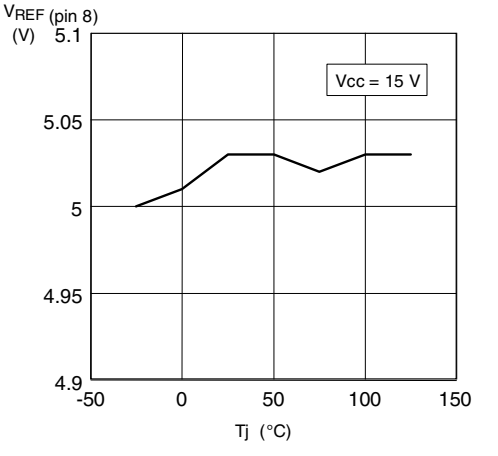


Figure 22. PFC_STOP open/low thresholds on V_{COMP} vs. Tj

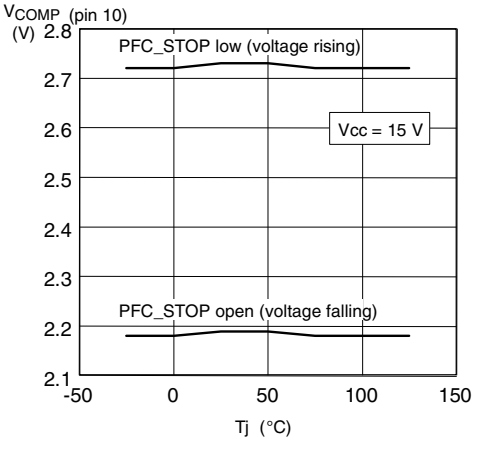


Figure 23. Standby thresholds vs. Tj

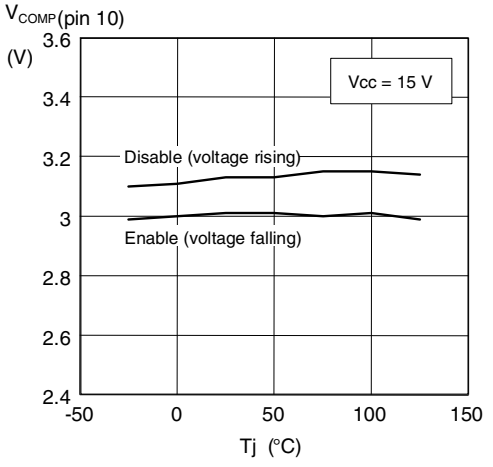


Figure 24. Standby pin dropout vs. Tj

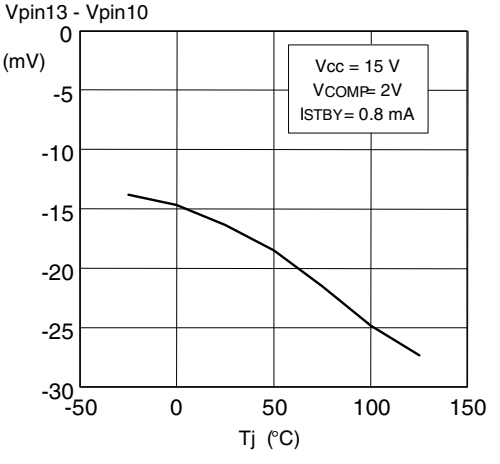


Figure 25. DIS threshold vs. Tj

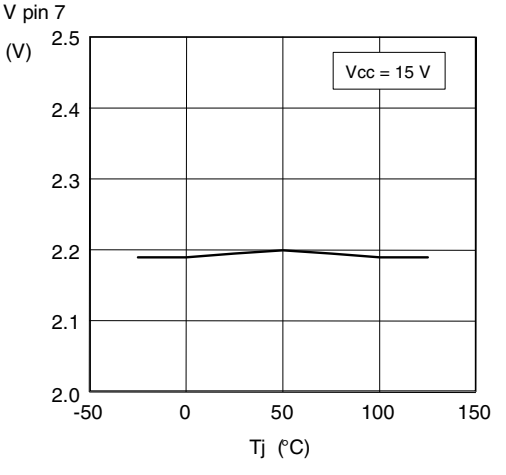


Figure 26. SKIPADJ hysteresis vs. Tj

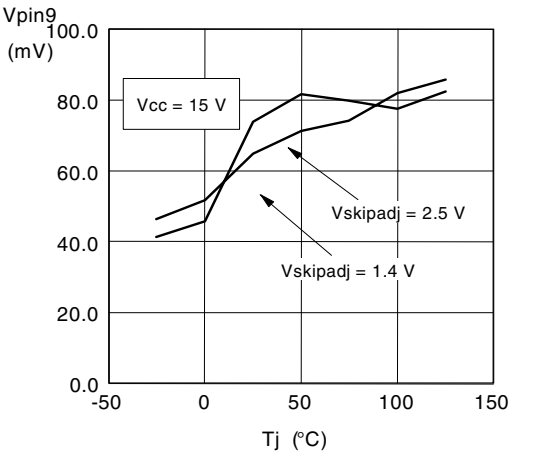


Figure 27. SKIPADJ disable threshold vs. Tj

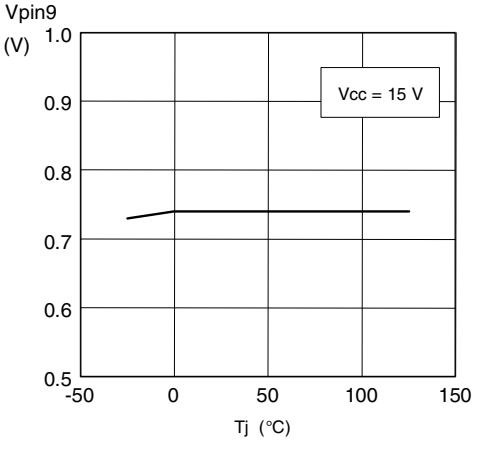


Figure 28. Soft-start charge current vs. Tj

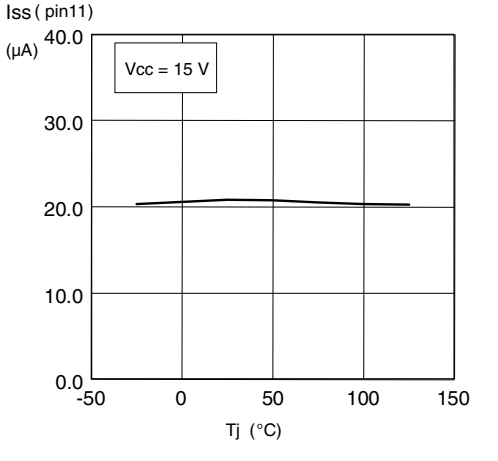


Figure 29. S-COMP ramp vs. Tj

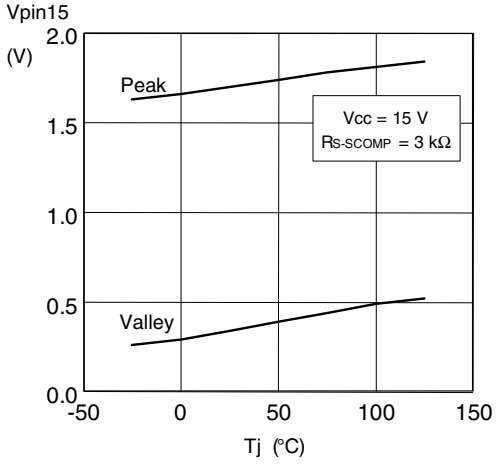


Figure 30. UVLO saturation vs. Tj

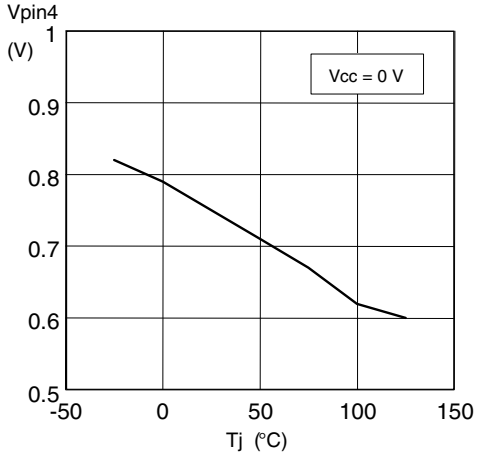


Figure 31. Gate-drive clamp vs. Tj

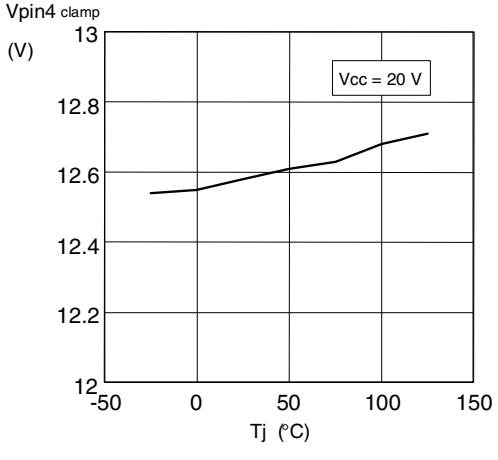


Figure 32. Gate-drive output low saturation

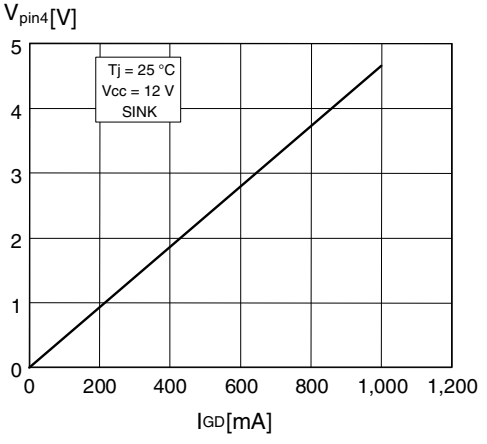
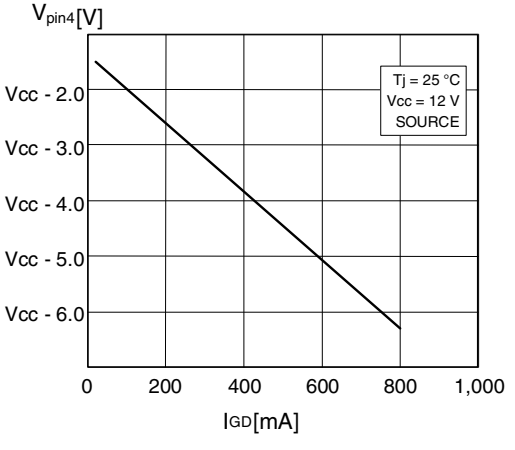


Figure 33. Gate-drive output high saturation



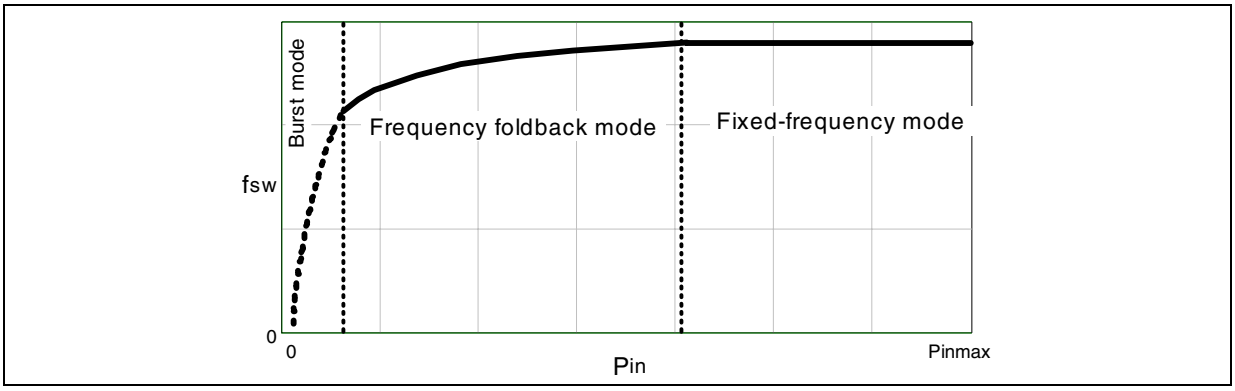
4 Application Information

The L6668 is a versatile current-mode PWM controller specific for offline fixed-frequency, peak-current-mode-controlled flyback converters.

The device is able to operate in different modes (fig. 34), depending on the converter's load conditions:

1) Fixed frequency at heavy load. In this region the IC operates exactly like a standard current mode control chip: a relaxation oscillator, externally programmable with a capacitor and a resistor, generates a sawtooth and releases a clock pulse during the falling edge of the sawtooth; the power switch is turned on by the clock pulses and is turned off by the control loop.
2) Frequency-foldback mode at medium and light load. As the load is reduced the oscillator frequency is reduced as well by slowing down the charge of the timing capacitor proportionally to the load itself.
3) Burst-mode control with no or very light load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with constant peak current. A load decrease will be then translated into a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. Being the peak current very low, no issue of audible noise arises.

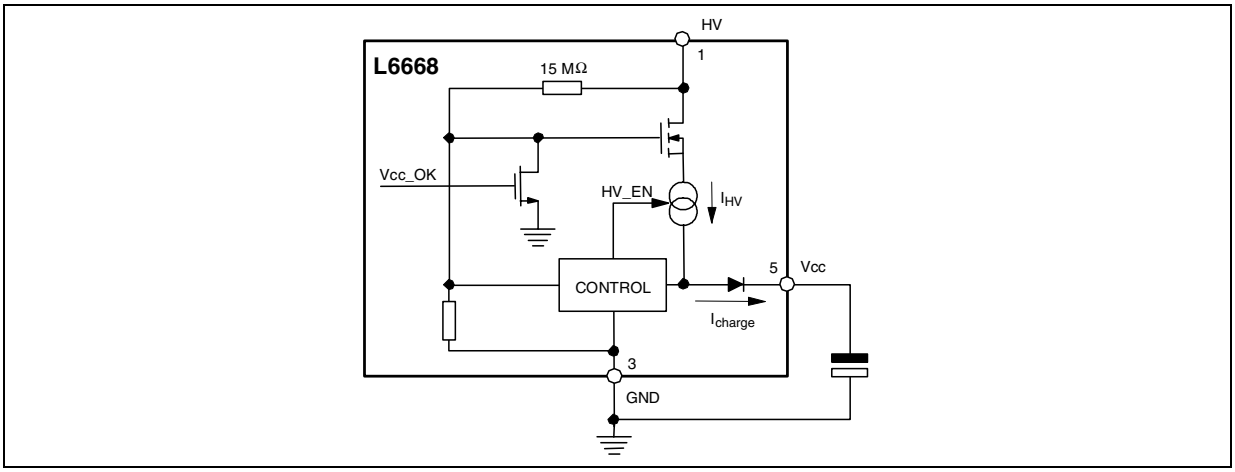
Figure 34. Multi-mode operation of the L6668



4.1 High-voltage start-up generator

Figure 35 shows the internal schematic of the high-voltage start-up generator (HV generator). It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

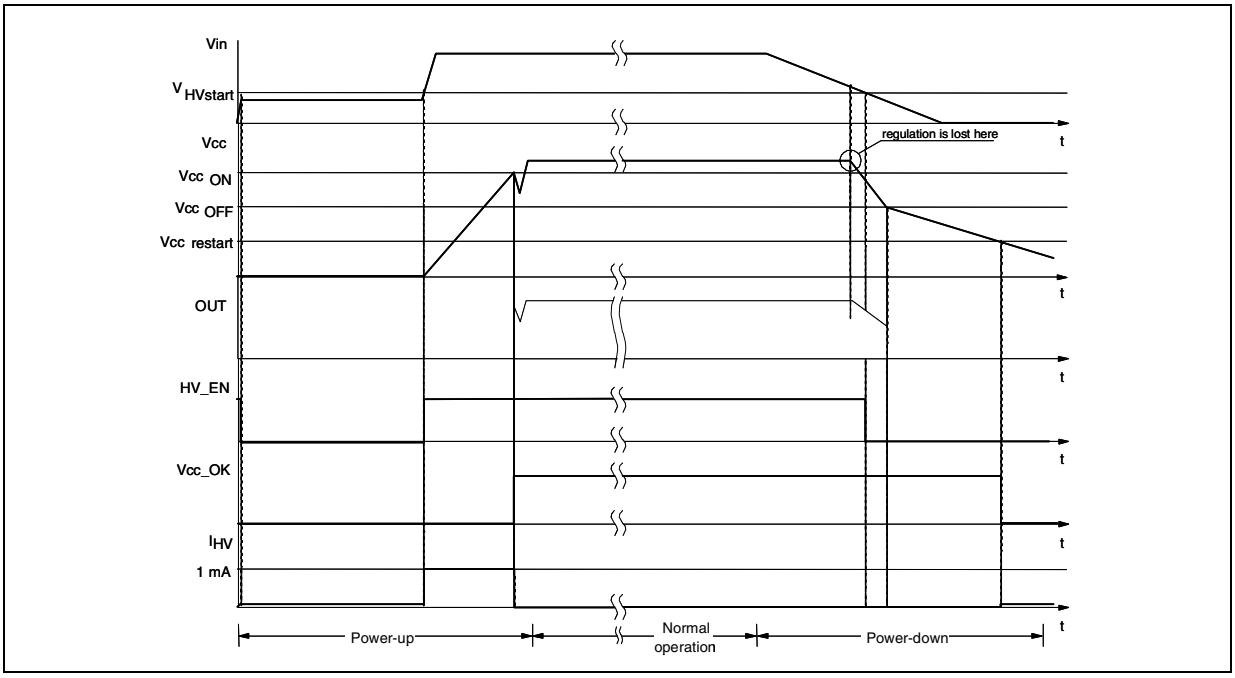
Figure 35. High-voltage start-up generator: internal schematic



The HV generator is physically located on a separate chip, made with BCD off-line technology able to withstand 700V, controlled by a low-voltage chip, where all of the control functions reside.

With reference to the timing diagram of figure 36, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, as it reaches about 80V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, diminished by the IC consumption, charges the bypass capacitor connected between pin Vcc (5) and ground and makes its voltage rise almost linearly.

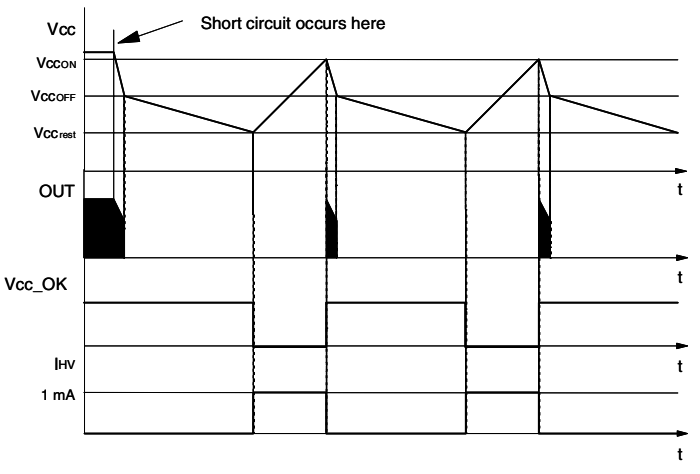
Figure 36. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the start-up threshold (13.5V typ.) the low-voltage chip starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The IC is powered by the energy stored in the Vcc capacitor until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

The residual consumption of this circuit is just the one on the 15MΩ resistor (≈10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard start-up circuit made with an external dropping resistor.

Figure 37. Timing diagram showing short-circuit behavior



At converter power-down the system will lose regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc will then drop and stop IC activity as it falls below the UVLO threshold (8.7V typ.).

The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold $Vcc_{restart}$ located at about 5V. The HV generator can now restart but, if Vin < $V_{instart}$, as shown in figure 36, HV_EN is de-asserted too and the HV generator is disabled.

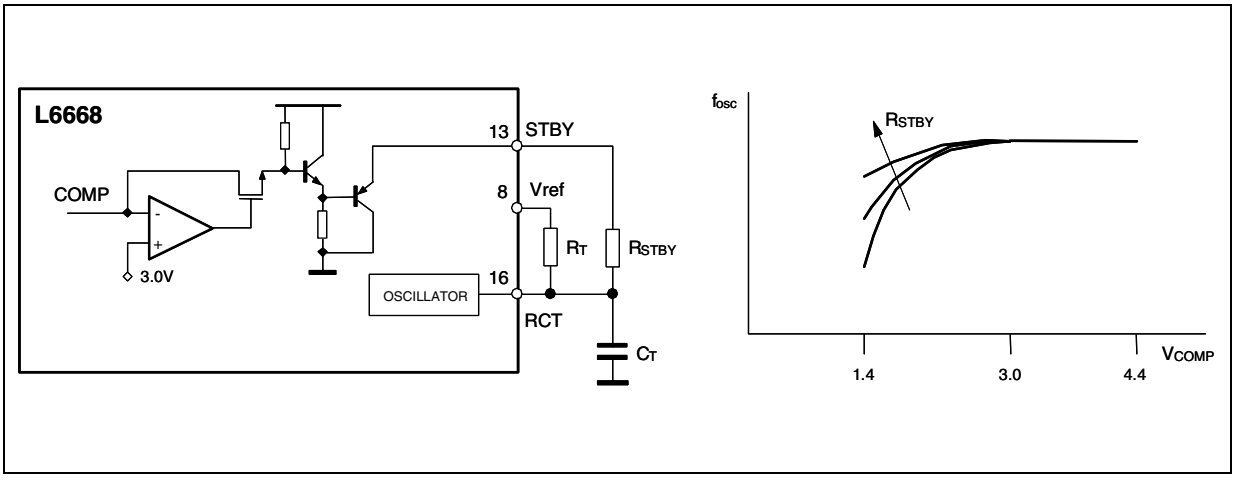
This prevents converter's re-start attempts and ensures monotonic output voltage decay at power-down. The low restart threshold $Vcc_{restart}$ ensures that, during short circuits, the restart attempts of the L6668 will have a very low repetition rate, as shown in the timing diagram of figure 37, and that the converter will work safely with extremely low power throughput.

4.2 Frequency Foldback Block and operation at medium/light load

At heavy load, namely as the voltage on pin COMP (V_{COMP}) is higher than 3V, the device works at a fixed frequency like a standard current mode PWM controller.

As the load is reduced, and the V_{COMP} voltage falls below 3V (approximately corresponding to 50% of the maximum load in a fully DCM system), the oscillator frequency can be made dependent on converter's load conditions - the lower the load, the lower the frequency and vice versa.

Figure 38. Frequency foldback function: oscillator frequency is a function of COMP voltage



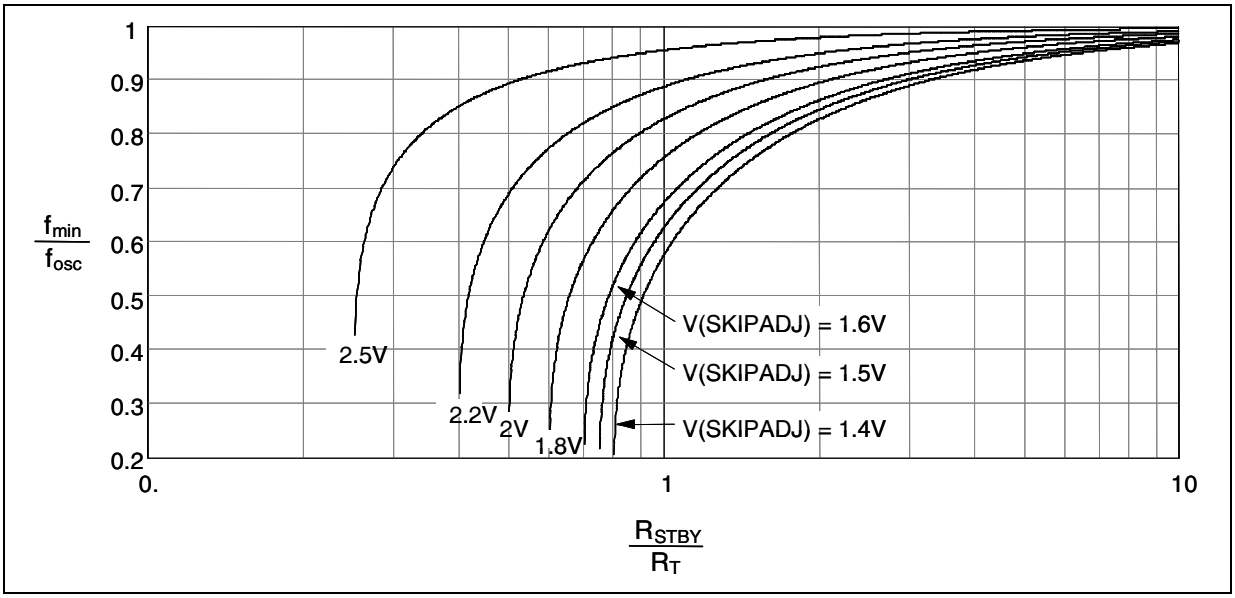
This is done by adding an external resistor R_{STBY} between pins RCT (#16) and STBY (#13), which activates the circuit shown in figure 38.

When V_{COMP} is below 3 V (oscillator's peak voltage) the voltage on the STBY pin, which is internally connected to a current sink, tracks V_{COMP} and then some of the current that charges C_T is diverted to ground through the STBY pin.

In this way the rate of rise of the voltage across C_T is slowed down and the oscillator frequency decreased, the lower V_{COMP} the lower the frequency. Instead, when V_{COMP} is greater than 3 V the STBY pin features high impedance and the oscillator frequency f_{osc} will be determined by R_T and C_T. These components can be then calculated as it is usually done with this type of oscillator:

$$R_T C_T = \frac{1.4}{f_{osc}}$$

Figure 39. Standby function: frequency shift vs. timing resistors (normalized quantities)



The determination of R_{STBY} can be done assuming that the minimum switching frequency before burst-mode operation takes place (f_{min}) is specified. This value will be above the audible range to ensure a noise-free operation. With the aid of the diagrams in figure 39, which show the relationship between the frequency shift obtained and the ratio of R_{STBY} to R_T for different values of the burst-mode threshold, it is possible to determine R_{STBY}. Draw an horizontal line corresponding to the desired f_{min}/f_{osc} ratio as long as it intercepts the characteristic corresponding to the voltage set at the pin SKIPADJ (#9). From there, draw a vertical line: on the horizontal axis it is possible to read the required R_{STBY}/R_T ratio.

Note that the characteristic for V(SKIPADJ)=1.4V corresponds to the burst-mode operation not used (see next section). Note also that, for a given V(SKIPADJ), there is both a lower limit to the R_{STBY}/R_T ratio and a maximum frequency shift allowed. Not observing these limits will result in erratic behavior.

In applications where the switching frequency needs not be tightly fixed for some specific reason there is no major drawback to this technique. In case this function is not desired, the STBY pin shall be left open.

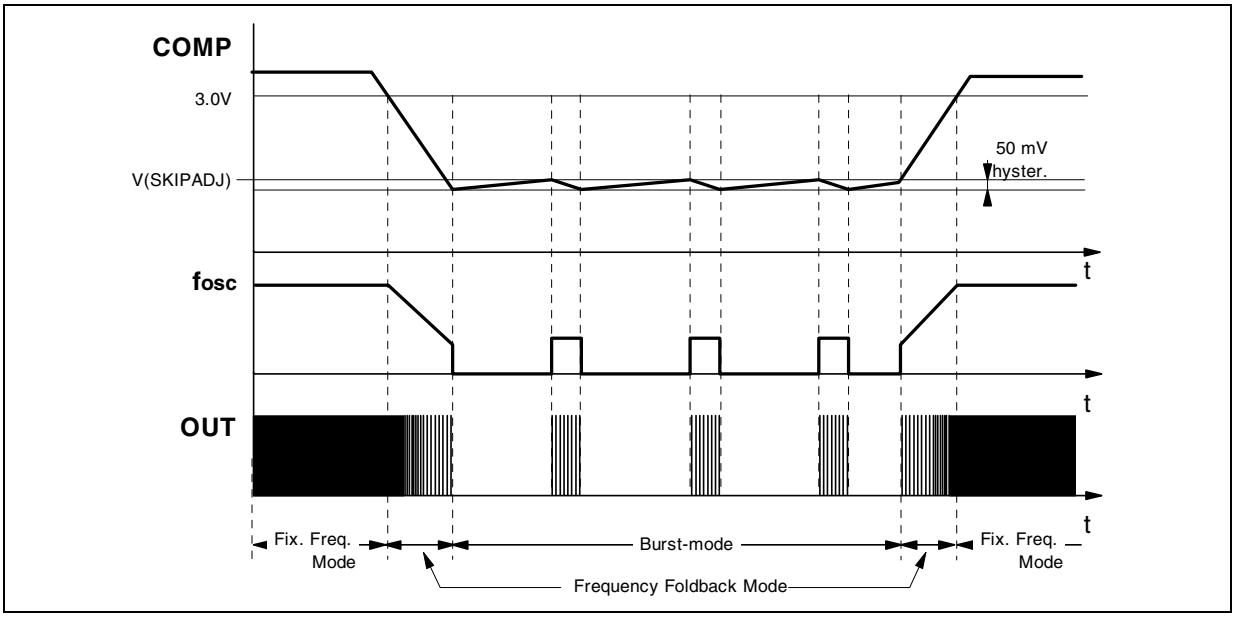
4.3 Operation at no load or very light load

When the PWM control voltage at pin COMP falls about 50 mV below a threshold externally programmable via pin 9 (SKIPADJ), the IC is disabled with the MOSFET kept in OFF state and its consumption reduced at a very low value to minimize Vcc capacitor discharge. The soft-start capacitor is not discharged.

The control voltage now will increase as a result of the feedback reaction to the energy delivery stop, the threshold will be exceeded and the IC will restart switching again. In this way the converter will work in burst-mode with a constant peak current defined by the disable level applied at pin 9. A load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and maximizing efficiency. This kind of operation is noise-free provided the peak current, which is user-defined by the bias voltage at pin 9, is very low.

The timing diagram of figure 40 illustrates this kind of operation along with the other ones, showing the most significant signals.

Figure 40. Load-dependent operating modes: timing diagram



The operating range of the voltage V(SKIPADJ) is practically limited upwards by the onset of audible noise: typically, with a voltage above 2-2.1V some noise can be heard under some line/load conditions. If, instead, V(SKIPADJ) is set below the low saturation value of the PWM control voltage (1.4V typ.) burst-mode operation will never take place. Always bias the pin at some voltage, a floating pin will result in anomalous behavior. The SKIPADJ pin doubles its function: if the voltage is pulled below 0.8V the IC is disabled completely, except for the externally available reference voltage VREF, and its quiescent consumption reduced. The soft-start capacitor is discharged so that, when the voltage on the SKIPADJ pin is pulled above 0.8V, the chip is soft-started just like exiting from UVLO. This function is useful for some kind of remote ON/OFF control. The comparator referenced to 0.8V does not have hysteresis; hence make sure that the voltage on the pin does not linger on the threshold to prevent uncertain behavior.

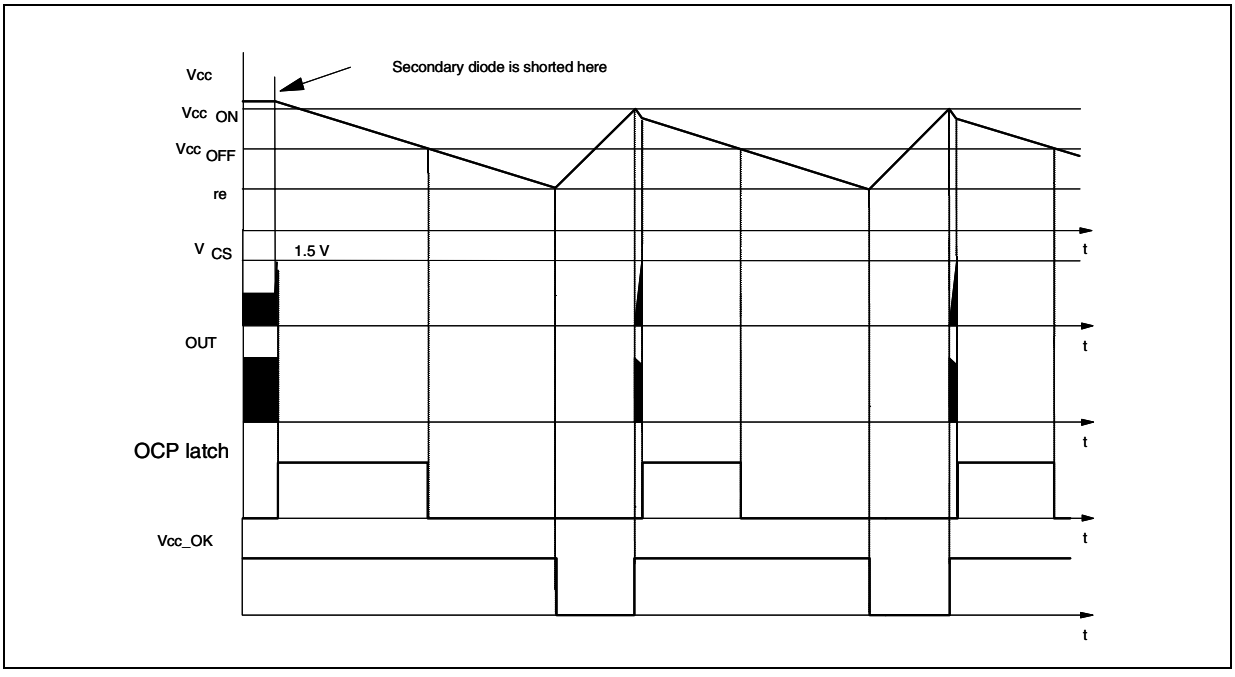
4.4 PWM control Block

The device is specific for secondary feedback. Typically, there is a TL431 at the secondary side and an optocoupler that transfers output voltage information to the PWM control at the primary side, crossing the isolation barrier. The PWM control input (pin #10, COMP) is driven directly by the phototransistor's collector (the emitter is grounded to GND) to modulate the duty cycle.

4.5 Current Comparator, PWM Latch and Hiccup-mode OCP

The current comparator senses the voltage across the current sense resistor (Rs) on pin 12 (ISEN) and, by comparing it with the programming signal derived form the control voltage on pin 10 (COMP), determines the exact time when the external MOSFET is to be switched off. The PWM latch avoids spurious switching of the MOSFET, which might result from the noise generated ("double-pulse suppression").

Figure 41. Hiccup-mode OCP: timing diagram



A second comparator senses the voltage on the current sense input and shuts the IC down if the voltage at the pin exceeds 1.5 V. Such an anomalous condition is typically generated by either a short circuit of the secondary rectifier or a shorted secondary winding or a saturated flyback transformer.

This condition is latched as long as the IC is supplied. When the IC is disabled, however, no energy is coming from the self-supply circuit, then the voltage on the Vcc capacitor will decay and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the Vcc voltage still needs to go below its restart voltage before the Vcc capacitor is charged again and the IC re-started.

Ultimately, either of the above mentioned failures will result in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. The timing diagram of figure 41 illustrates this operation.

4.6 Power Management

The L6668 is specifically designed to minimize converter's losses under light or no-load conditions, and a special function has been provided to help the designer meet energy saving requirements even in power-factor-corrected systems where a PFC pre-regulator precedes the DC-DC converter.

Actually EMC regulations require compliance with low-frequency harmonic emission limits at nominal load, no limit is envisaged when the converter operates with a light load. Then the PFC pre-regulator can be turned off, thus saving the no-load consumption of this stage (0.5 to 1W).

To do so, the device provides the PFC_STOP (#14) pin: it is an open collector output, normally low, that becomes open when the voltage V_{COMP} falls below 2.2V.

This signal will be externally used for switching off the PFC controller and the pre-regulator as shown in figure 42. To prevent intermittent operation of the PFC stage, 0.5V hysteresis is provided: the PFC_STOP pin is re-asserted low (which will re-enable the PFC pre-regulator) when V_{COMP} exceeds 2.7 V.

A capacitor (and a limiting resistor in the hundred ohms), shown in dotted lines, may be used if one wants to delay PFC turn-off

When the L6668 is in UVLO (Vcc<8.7V) the pin is kept high so as to ensure that the PFC pre-regulator will start up only after the DC-DC converter governed by the L6668 is activated.

Figure 43 shows a timing diagram where the PFC_STOP function operation is illustrated under different operating conditions.

Figure 42. How the L6668 can switch off a PFC controller at light load

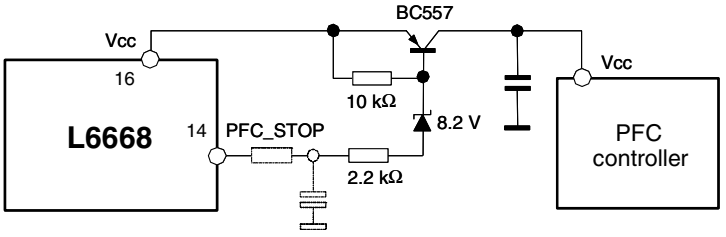


Figure 43. Operation of PFC_STOP function

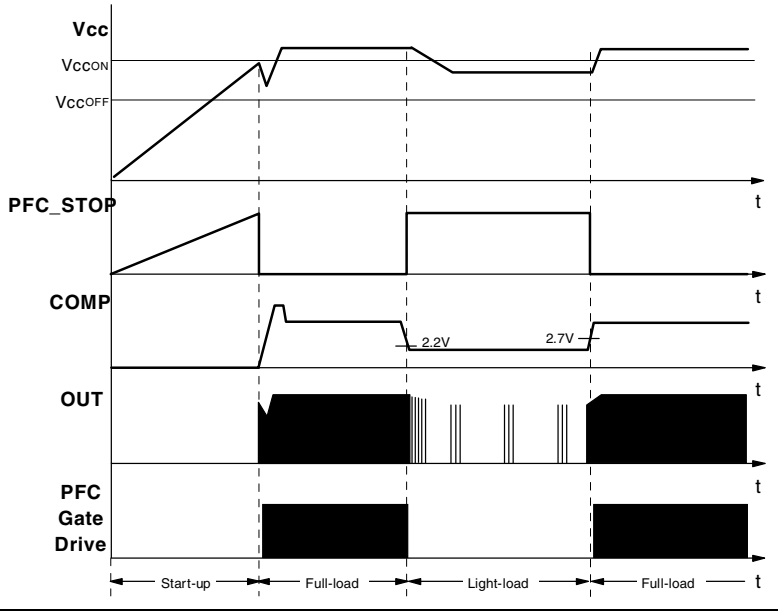
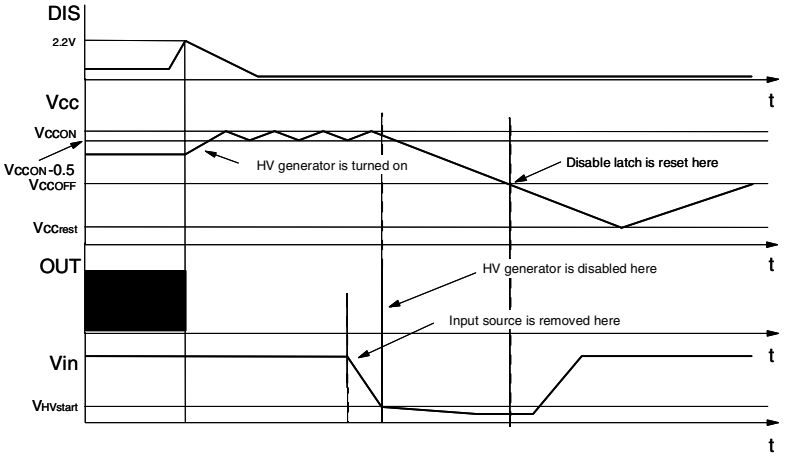


Figure 44. Operation after DIS pin activation: timing diagram



4.7 Disable function

Latched OTP or OVP functions can be easily realized with the L6668: the IC is equipped with a comparator whose non-inverting input is externally available on pin #7 (DIS), and whose inverting input is internally referenced to 2.2V.

As the voltage on the pin exceeds the threshold the IC is immediately shut down and its consumption reduced at a low value. The information is latched and it is necessary to let the voltage on the Vcc pin go below the UVLO threshold to reset the latch and restart the IC.

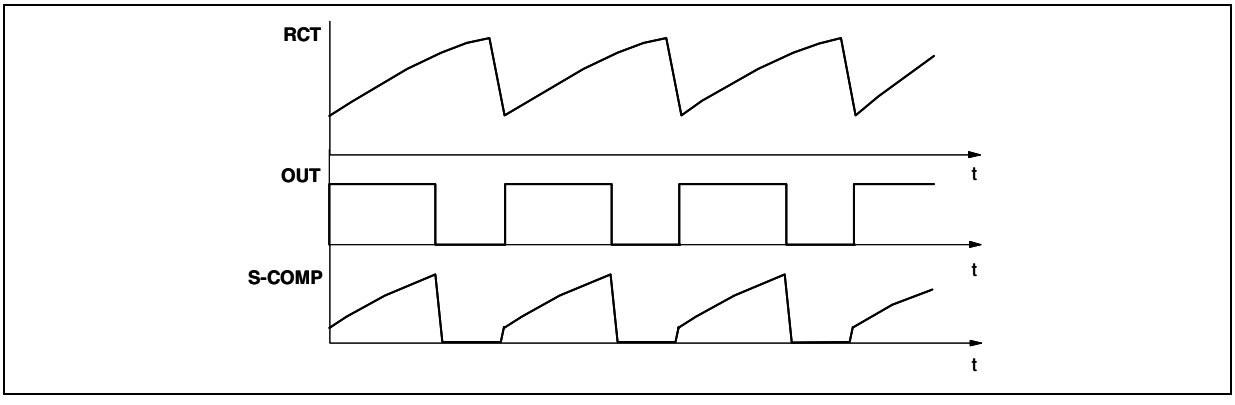
To keep the latch supplied as long as the converter is connected to the input source, the HV generator is activated periodically so that Vcc oscillates between the start-up threshold V_{ccON} and V_{ccON} - 0.5V. It is then necessary to disconnect the converter from the input source to restart the IC. This operation is shown in the timing diagram of figure 44. Activating the HV generator in this way cuts its power dissipation approximately by three and keeps peak silicon temperature close to the average value.

4.8 Slope compensation

A pin of the device (#15, S-COMP) provides a voltage ramp during MOSFET's ON-time which is a repetition of the oscillator sawtooth, buffered (0.8 mA min. capability) and level shifted down by one Vbe.

This ramp is intended for implementing additive slope compensation on current sense. This is needed to avoid the sub-harmonic oscillation that arises in all peak-current-mode-controlled converters working in continuous conduction mode with a duty cycle close to or exceeding 50%.

Figure 45. Slope compensation waveforms



The compensation will be realized by connecting a programming resistor between this pin and the current sense input (pin 12, ISEN). The pin has to be connected to the sense resistor with another resistor to make a summing node on the pin.

Since no ramp is delivered during MOSFET OFF-time (see figure 45), no external component other than the programming resistor is needed to ensure a clean operation at light loads. If slope compensation is not required the pin shall be left floating.

Figure 46. Typical Application: 80W, WRM flyback; Electrical Schematic

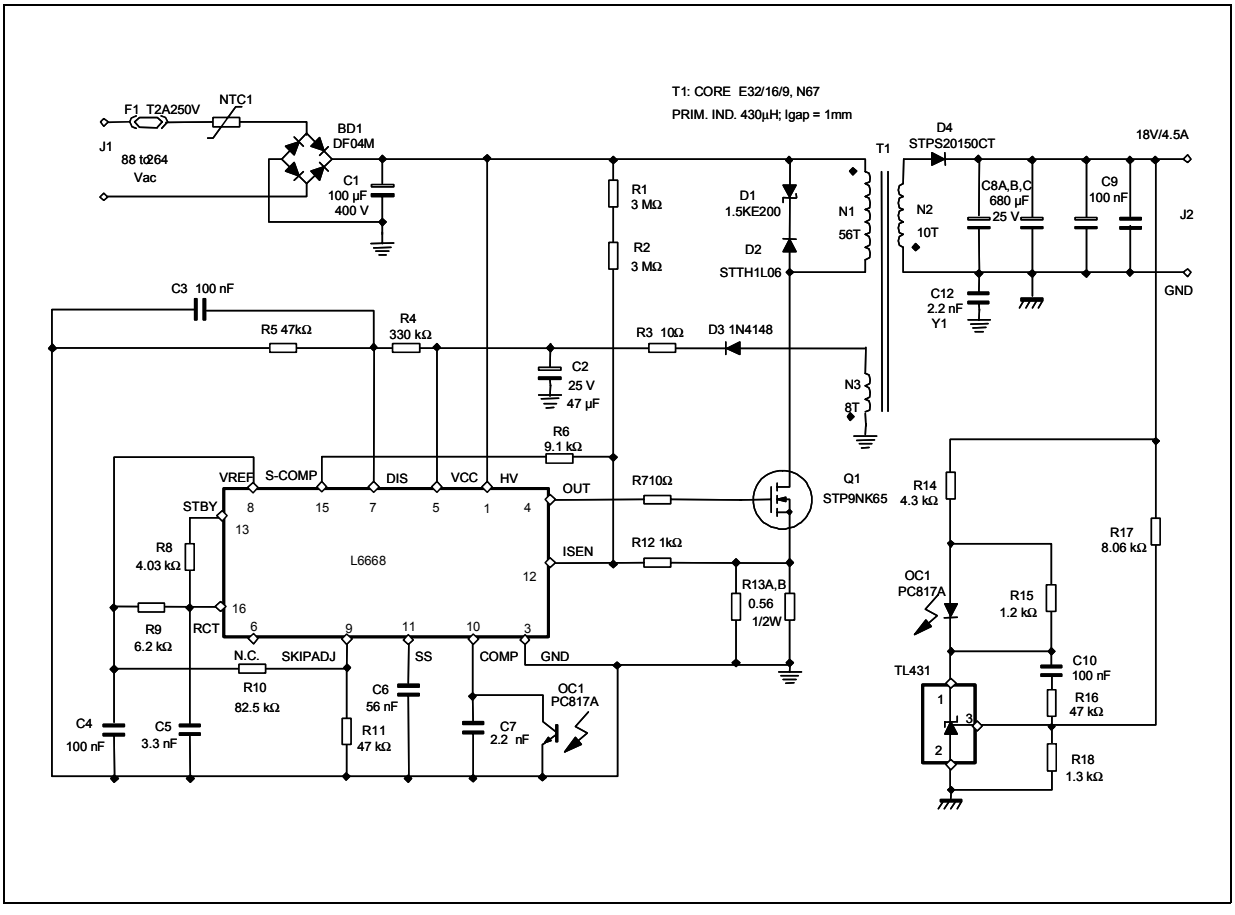


Table 6. Light load measurements on the circuit of figure 46

Output power	Test condition	Input power
Pout = 0.5 W	Vin= 110 Vac	0.71 W
	Vin= 230 Vac	0.86 W
Pout = 0 W	Vin= 110 Vac	0.09 W
	Vin= 230 Vac	0.17 W

5 Package information

In order to meet environmental requirements, STMicroelectronics offers this device in ECOPACK® package. This package has a Lead-free second level interconnect. The category of second level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark.

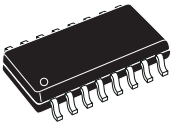
ECOPACK specifications are available at: www.st.com.

Figure 47. SO16 (Narrow) Mechanical Data & Package Dimensions

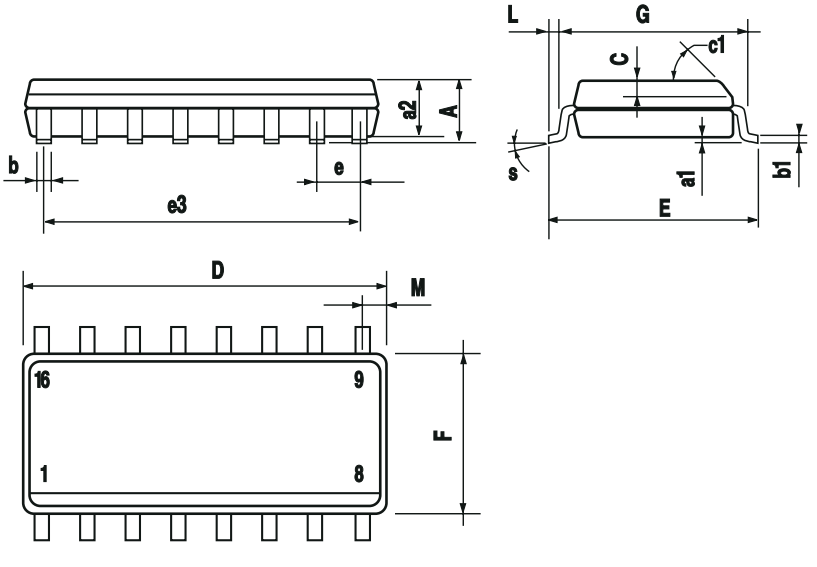
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA



SO16 (Narrow)



6 Revision History

Table 7. Revision History

Date	Revision	Description of Changes
20-May-2005	1	First Issue.
15-July-2005	2	Modify values in Electrical Characteristics
28-July-2005	3	Changed the maturity from “Preliminary Data” to “Datasheet”.
13-Jan-2006	4	Absolute Maximum Rating Update (added ESD note for pin 1). Modified value “DIS >2.2V” in the table 4 pin 14.

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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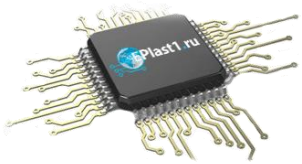
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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