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June 2014



# FSA641 — 2:1 MIPI Switch, Featuring 2-Data and 1-Data Lane Configuration

## Features

- Switch Type: 2:1
- Signal Types MIPI, DPHY
- $V_{CC}$ : 2.65 to 4.3 V
- Input Signals 0 to  $V_{CC}$
- $R_{ON}$ :
  - 7  $\Omega$  Typical HS MIPI
  - 10  $\Omega$  Typical LS MIPI
- $\Delta R_{ON}$ : 0.75  $\Omega$  Typical HS & LS MIPI
- $I_{CC}$ : 1  $\mu A$  Maximum
- $O_{IRR}$ : -50 dB Typical
- $X_{TALK}$ : -40 dB Typical
- Bandwidth: 1 GHz Typical
- Channel-to-Channel Skew: 15 ps Typical
- $C_{ON}$ : 8 pF Typical
- Package 20-Lead UMLP

## Applications

- Cellular Phones, Smartphones
- Displays

## Description

The FSA641 is a 2:1 MIPI switch made for 2-data lane and 1-data lane modules. This part is configured as a single-pole, double-throw switch (SPDT) and is optimized for switching between two high-speed or low-power MIPI sources. The FSA641 has specially been designed for the MIPI specification and allows connection to either a CSI or DSI module. The FSA641 features an extremely low on capacitance ( $C_{ON}$ ) of 8 pF. The wide bandwidth (1 GHz) results in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference.

## Related Resources

- For samples and questions, please contact: [Analog.Switch@fairchildsemi.com](mailto:Analog.Switch@fairchildsemi.com).
- FSA641 Demonstration Board

## Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA641UMX	F641	-40 to +85°C	20-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 3.0 x 3.0 mm

### Typical Application

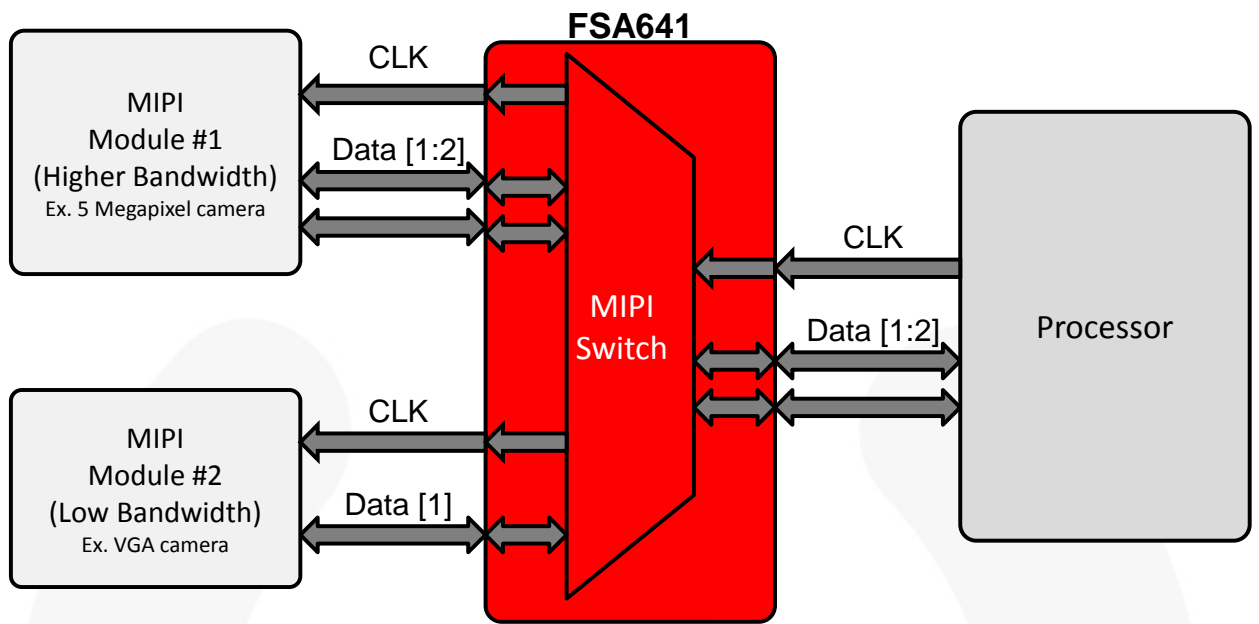


Figure 1. Mobile Phone Example

## Pin Configuration

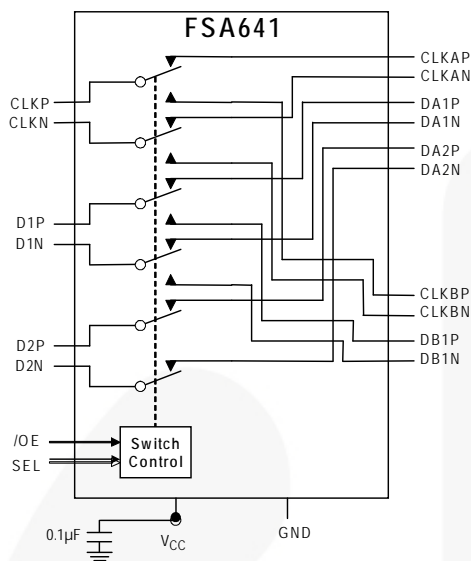


Figure 2. Functional Block Diagram

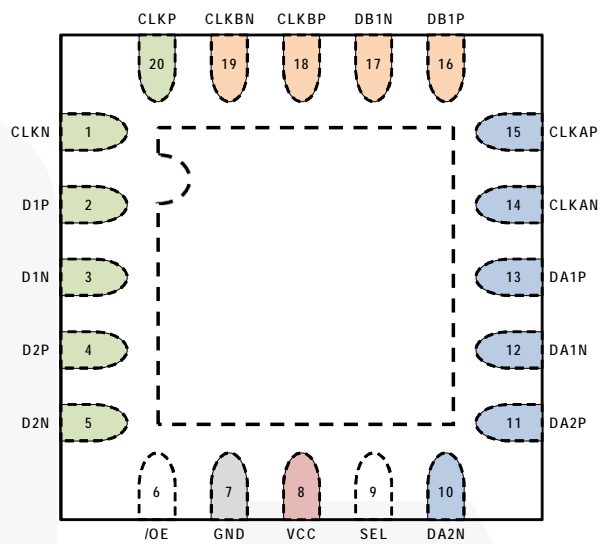


Figure 3. Pin Assignments (Top Through View)

## Pin Descriptions

Pin #	Pin Name	Type	Description	
20	CLKP	I/O	Common positive clock path	
1	CLKN	I/O	Common negative clock path	
2	D1P	I/O	Common positive data 1 path	
3	D1N	I/O	Common negative data 1 path	
4	D2P	I/O	Common positive data 2 path	
5	D2N	I/O	Common negative data 2 path	
15	CLKAP	I/O	A-port positive clock path	
14	CLKAN	I/O	A-port negative clock path	
13	DA1P	I/O	A-port positive data 1 path	
12	DA1N	I/O	A-port negative data 1 path	
11	DA2P	I/O	A-port positive data 2 path	
10	DA2N	I/O	A-port negative data 2 path	
18	CLKBP	I/O	B-port positive clock path	
19	CLKBN	I/O	B-port negative clock path	
16	DB1P	I/O	B-port positive data 1 path	
17	DB1N	I/O	B-port negative data 1 path	
6	/OE	Input	Output Enable (Active Low)	
7	GND	Ground	Ground	
8	VCC	Supply	Power; 0.1 µF decoupling capacitor to ground recommended	
9	SEL	Input	A-port or B-port Select pin	0=A-port, 1= B-port
Paddle	n/a	NC	Not Connected	

## Truth Table

SEL	/OE	Function
Don't Care	HIGH	Disconnect
LOW	LOW	D1, D2, CLK=DA1, DA2, CLKA
HIGH	LOW	D1, CLK=DB1, CLKB; D2 OPEN

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-0.50	+5.25	V
V <sub>CNTRL</sub>	DC Input Voltage (SEL, /OE) <sup>(1)</sup>	-0.5	V <sub>CC</sub>	V
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(1)</sup>	-0.5	V <sub>CC</sub> + 0.3	V
I <sub>IK</sub>	DC Input Diode Current	-50		mA
I <sub>OUT</sub>	DC Output Current		50	mA
T <sub>STG</sub>	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	6.5	kV
		I/O to GND	8.0	
		Power to GND	16.0	
	Charged Device Model, JEDEC: JESD22-C101		2.0	

**Note:**

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.65	4.30	V
V <sub>CNTRL</sub>	Control Input Voltage (SEL, /OE) <sup>(2)</sup>	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	-0.5	V <sub>CC</sub> -1 V	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

**Note:**

- The control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

All typical values are  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40$ to $+85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN}=-18$ mA	2.775			-1.2	V
$I_{IN}$	Control Input Leakage	$V_{SW}=0$ to 4.3 V	4.3	-1		1	$\mu\text{A}$
$V_{IH}$	Input Voltage High	$V_{IN}=0$ to $V_{CC}$	2.650 to 2.775	1.3			V
			4.3	1.7			
$V_{IL}$	Input Voltage Low	$V_{IN}=0$ to $V_{CC}$	2.650 to 2.775			0.5	V
$I_{OZ}$	Off-State Leakage	A, B= $0+0.3$ V to $V_{CC}-0.3$	4.3	-2		2	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$V_{CNTRL}=0$ or $V_{CC}$ , $I_{OUT}=0$	4.3			1.0	$\mu\text{A}$
$I_{CCT}$	Increase in $I_{CC}$ Current Per Control Voltage and $V_{CC}$	$V_{CNTRL}=1.8$ V	2.775			1.5	$\mu\text{A}$

## DC Electrical Characteristics, Low-Speed Mode

All typical values are  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40$ to $+85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$R_{ON}$	LS Switch On Resistance <sup>(3)</sup>	$V_{SW}=1.2$ V, $I_{ON}=-10$ mA, Figure 4	2.65		10	14	$\Omega$
$\Delta R_{ON}$	LS Delta $R_{ON}$ <sup>(4)</sup>	$V_{SW}=1.2$ V, $I_{ON}=-10$ mA (Intra-pair)	2.65		0.75		$\Omega$

### Notes:

- Measured by the voltage drop between A/B and CLK/Dn pins at the indicated current through the switch.
- Guaranteed by characterization.

## DC Electrical Characteristics, High-Speed Mode

All typical values are  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40$ to $+85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$R_{ON}$	HS Switch On Resistance <sup>(5)</sup>	$V_{SW}=0.4$ V, $I_{ON}=-10$ mA, Figure 4	2.65		7.0	9.5	$\Omega$
$\Delta R_{ON}$	HS Delta $R_{ON}$ <sup>(6)</sup>	$V_{SW}=0.4$ V, $I_{ON}=-10$ mA (Intra-pair)	2.65		0.75		$\Omega$

### Notes:

- Measured by the voltage drop between A, B, and Dn pins at the indicated current through the switch.
- Guaranteed by characterization.

## AC Electrical Characteristics

All values are at  $R_L=50\ \Omega$  and  $R_S=50\ \Omega$  and all typical values are  $V_{CC}=2.775\ \text{V}$  at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$O_{IRR}$	Off Isolation <sup>(7)</sup>	$f=100\ \text{MHz}$ , $R_T=50\ \Omega$ Figure 14	2.775		-50		dB
Xtalk	Non-Adjacent Channel Crosstalk <sup>(7)</sup>	$f=100\ \text{MHz}$ , $R_T=50\ \Omega$ Figure 15	2.775		-40		dB
BW	-3db Bandwidth <sup>(7)</sup>	$C_L=0\ \text{pF}$ , $R_T=50\ \Omega$ Figure 13	2.775		1.0		GHz
$t_{ON}$	Turn-On Time SEL, /OE to Output	$C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$ Figure 6, Figure 7	2.650 to 2.775		20	37	ns
$t_{OFF}$	Turn-Off Time SEL, /OE to Output	$C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$ Figure 6, Figure 7	2.650 to 2.775		15	27	ns
$t_{PD}$	Propagation Delay <sup>(7)</sup>	$C_L=5\ \text{pF}$ Figure 6, Figure 8	2.775		0.25		ns
$t_{BBM}$	Break-Before-Make Time	$C_L=5\ \text{pF}$ , $V_{SW1}=V_{SW2}=1.2\ \text{V}$ Figure 12	2.650 to 2.775	7	9	12	ns

### Note:

7. Guaranteed by characterization.

## AC Electrical Characteristics, High-Speed

All typical values are  $V_{CC}=2.775\ \text{V}$  at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
$t_{SK(\text{Part\_Part})}$	Channel-to-Channel Skew Across Multiple Parts <sup>(8,9)</sup>	TDR-Based Method ( $V_{SW}=0.2V_{PP}$ , $C_L=C_{ON}$ )		40	80	ps
$t_{SK(\text{Chl\_Chl})}$	Channel-to-Channel Skew Within a Single Part <sup>(8)</sup>	TDR-Based Method ( $V_{SW}=0.2V_{PP}$ , $C_L=C_{ON}$ )		15	30	ps
$t_{SK(\text{Pulse})}$	Skew of Opposite Transitions in the Same Differential Channel <sup>(8)</sup>	TDR-Based Method ( $V_{SW}=0.2V_{PP}$ , $C_L=C_{ON}$ )		10	20	ps

### Notes:

8. Guaranteed by characterization.

9. Assumes the same  $V_{CC}$  and temperature for all devices.

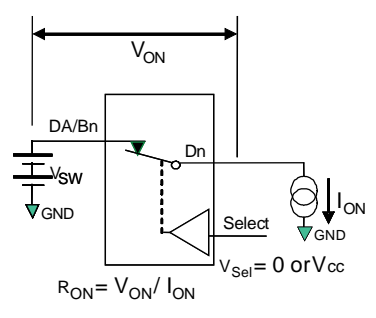
## Capacitance

Symbol	Parameter	Conditions	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
$C_{IN}$	Control Pin Input Capacitance <sup>(10)</sup>	$V_{CC}=0\ \text{V}$		1.5		pF
$C_{ON}$	Dn/CLK- On Capacitance <sup>(10)</sup>	$V_{CC}=2.775\ \text{V}$ , /OE=0V, $f=1\ \text{MHz}$ Figure 11		8.0		
$C_{OFF}$	Dn/CLK Off Capacitance <sup>(9)</sup>	$V_{CC}=2.775\ \text{V}$ , /OE=2.775 V, $f=1\ \text{MHz}$ Figure 10		2.5		

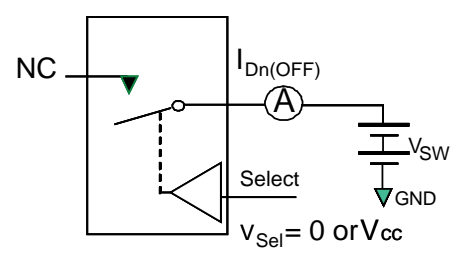
### Note:

10. Guaranteed by characterization.

### Test Diagrams

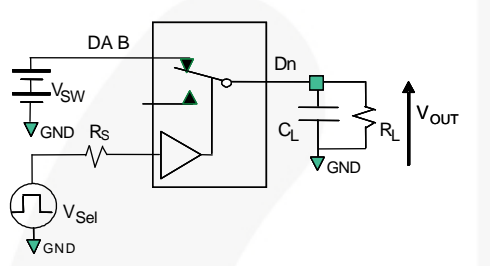


**Figure 4. On Resistance**



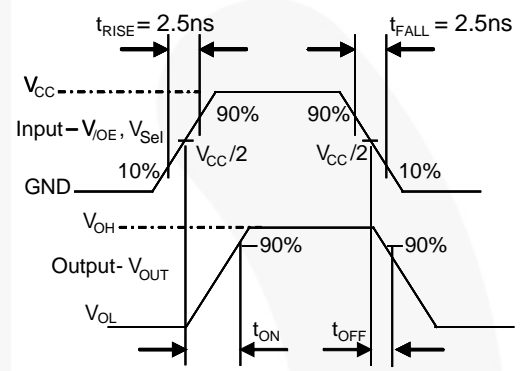
\*\*Each switch port is tested separately

**Figure 5. Off Leakage**

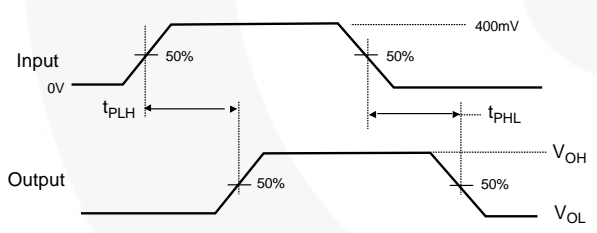


$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values).  $C_L$  includes test fixture and stray capacitance.

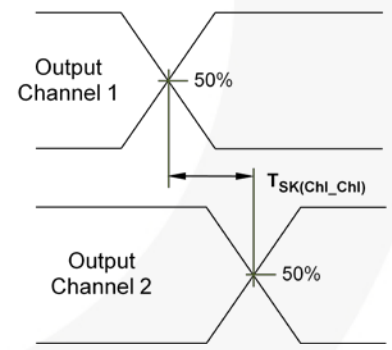
**Figure 6. AC Test Circuit Load**



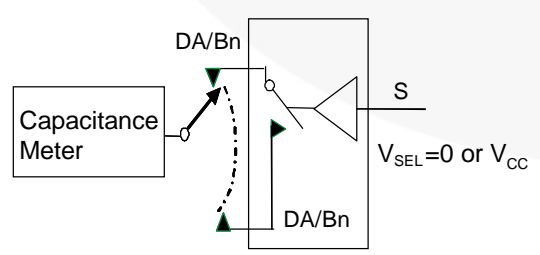
**Figure 7. Turn-On / Turn-Off Waveforms**



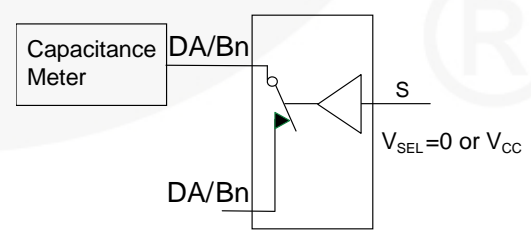
**Figure 8. Propagation Delay ( $t_{rF}$  – 500 ps)**



**Figure 9. Channel-to-Channel Skew**



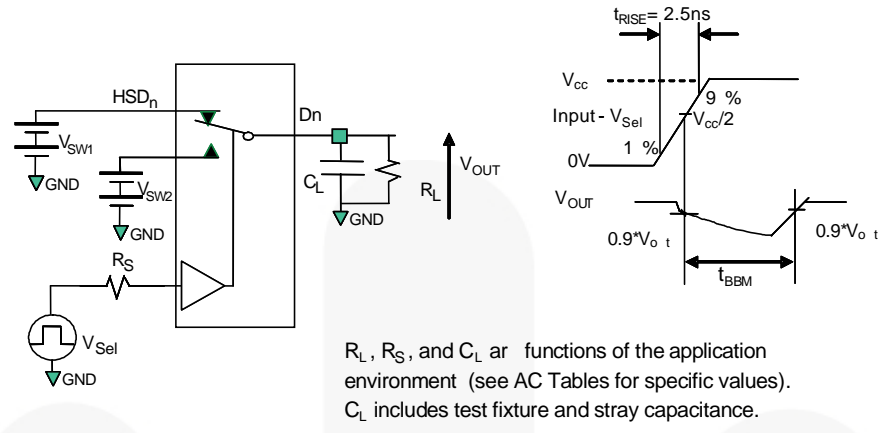
**Figure 10. Channel Off Capacitance**



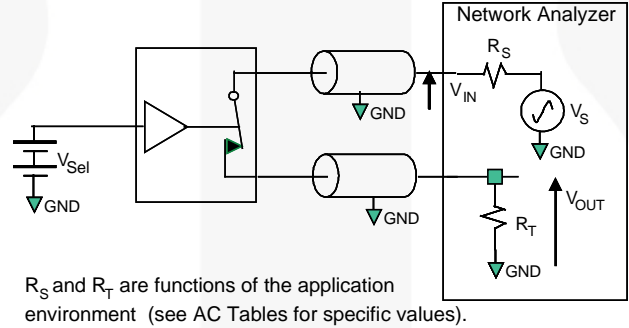
**Figure 11. Channel On Capacitance**



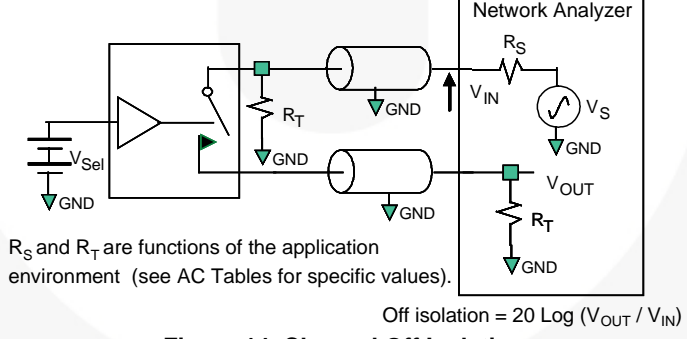
**Test Diagrams (Continued)**



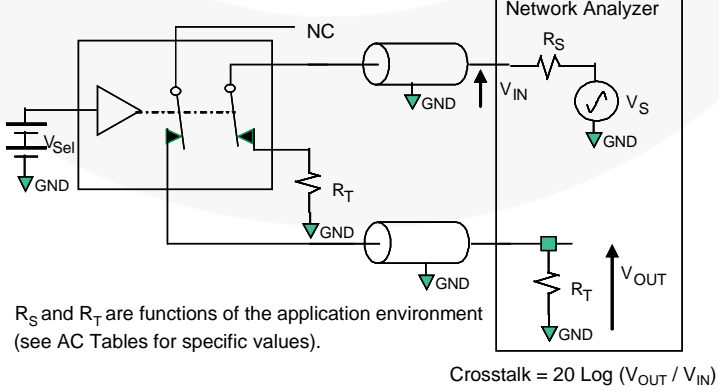
**Figure 12. Break-Before-Make Interval Timing**



**Figure 13. Bandwidth**

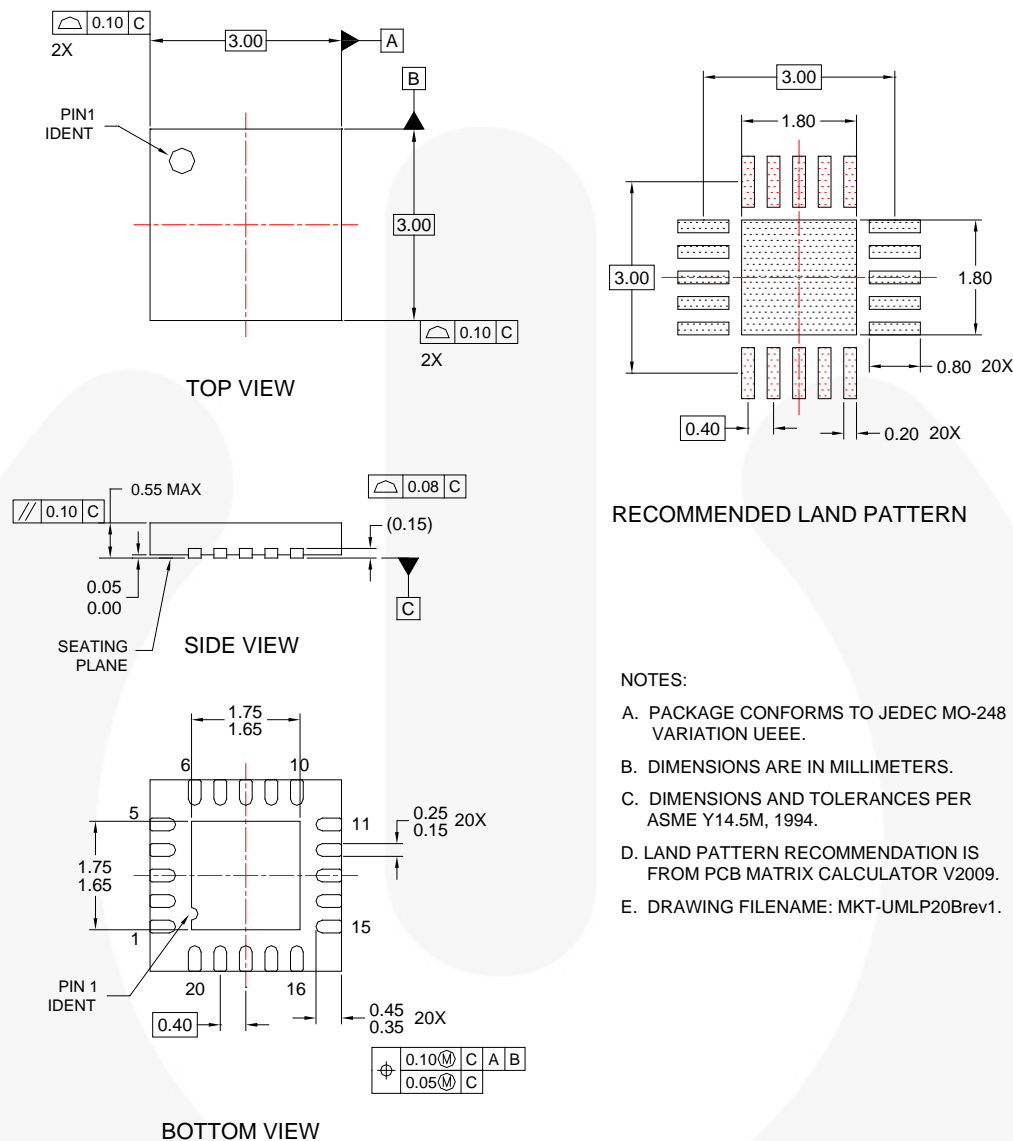


**Figure 14. Channel Off Isolation**



**Figure 15. Non-Adjacent Channel-to-Channel Crosstalk**

## Physical Dimensions



**Figure 16. 20-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 3.0 x 3.0 mm**

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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