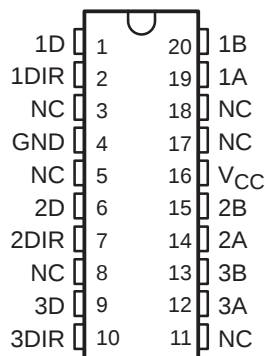


# SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS055D – AUGUST 1987 – REVISED SEPTEMBER 1995

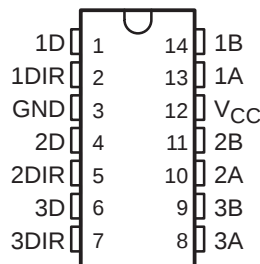
- Three Bidirectional Transceivers
- Driver Meets or Exceeds ANSI Standard EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . .  $\pm 60$  mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . .  $12\text{ k}\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 300$  mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operate From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Feature Independent Direction Controls for Each Channel

DW PACKAGE  
(TOP VIEW)



NC – No internal connection

J PACKAGE  
(TOP VIEW)



## description

The SN75ALS170 and SN75ALS170A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the driver and receiver meet ITU Recommendation V.11. The SN75ALS170A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS170 and SN75ALS170A operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 and the SN75ALS170A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

| SKEW LIMIT | PART NUMBER   |             |
|------------|---------------|-------------|
| 10 ns      | SN75ALS170DW  | SN75ALS170J |
| 5 ns       | SN75ALS170ADW |             |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN75ALS170, SN75ALS170A

## TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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### Function Tables

EACH DRIVER

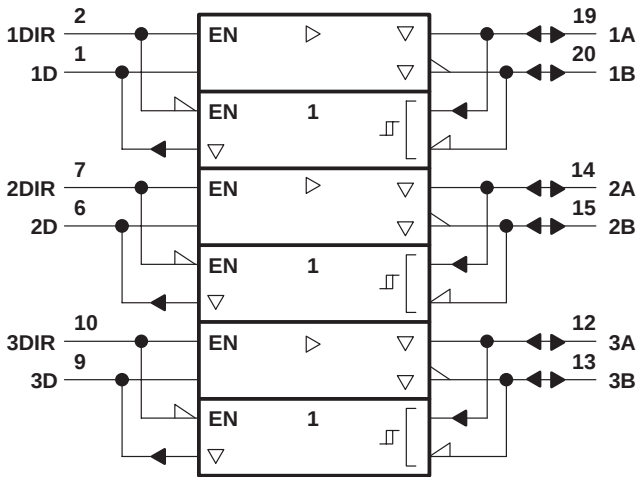
| INPUT<br>D | DIR | OUTPUTS |   |
|------------|-----|---------|---|
|            |     | A       | B |
| H          | H   | H       | L |
| L          | H   | L       | H |
| X          | L   | Z       | Z |

EACH RECEIVER

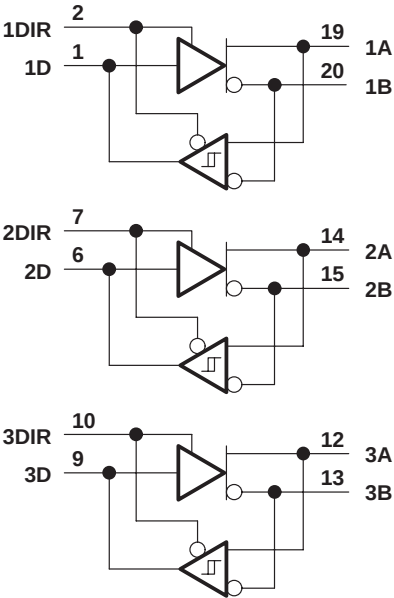
| DIFFERENTIAL INPUTS<br>A – B            | DIR | OUTPUT<br>R |
|-----------------------------------------|-----|-------------|
| $V_{ID} \geq 0.3\text{ V}$              | L   | H           |
| $-0.3\text{ V} < V_{ID} < 0.3\text{ V}$ | L   | ?           |
| $V_{ID} \leq -0.3\text{ V}$             | L   | L           |
| X                                       | H   | Z           |
| Open                                    | L   | H           |

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

### logic symbol†



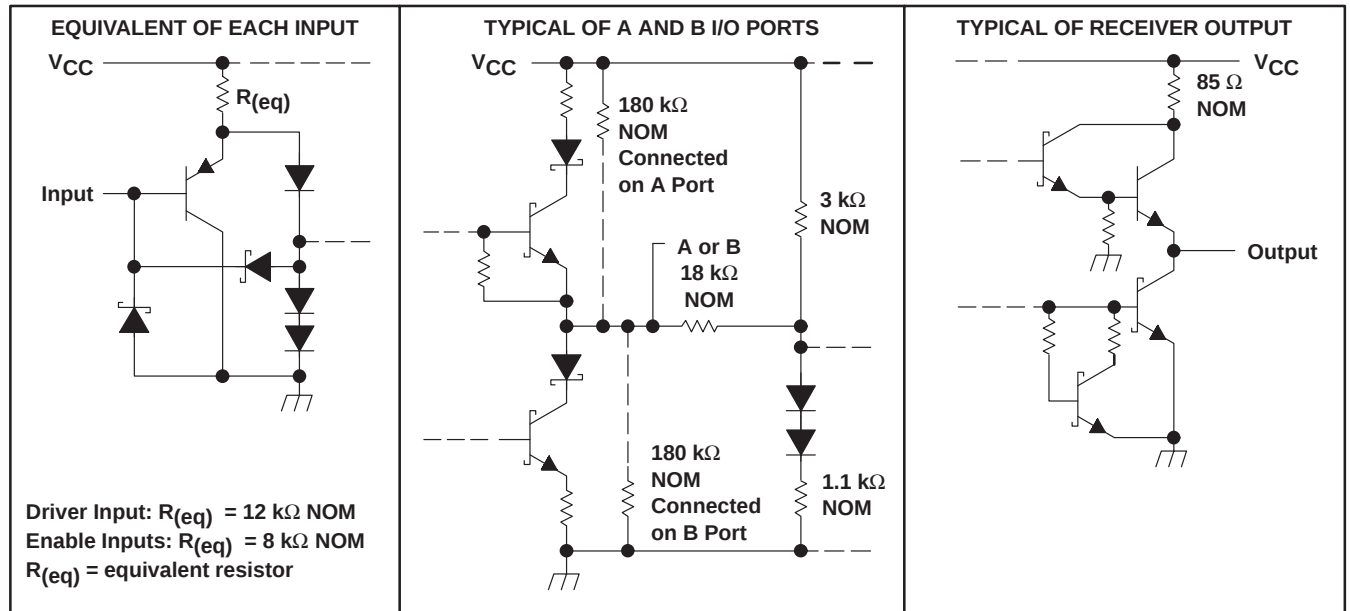
### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW package.

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                          |                              |
|--------------------------------------------------------------------------|------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                                    | 7 V                          |
| Voltage range at any bus terminal                                        | –7 V to 12 V                 |
| Enable input voltage, $V_I$                                              | 5.5 V                        |
| Continuous total power dissipation                                       | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$                              | 0°C to 70°C                  |
| Storage temperature range, $T_{stg}$                                     | –65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package | 260°C                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package  | 300°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING |
|---------|---------------------------------------------|---------------------------------------------------|------------------------------------------|
| DW      | 1125 mW                                     | 9.0 mW/°C                                         | 720 mW                                   |
| J       | 1025 mW                                     | 8.2 mW/°C                                         | 656 mW                                   |

# SN75ALS170, SN75ALS170A

## TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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### recommended operating conditions

|                                                                                            |          | MIN  | TYP | MAX  | UNIT |
|--------------------------------------------------------------------------------------------|----------|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>                                                            |          | 4.75 | 5   | 5.25 | V    |
| Voltage at any bus terminal (separately or common mode), V <sub>I</sub> or V <sub>IC</sub> |          | 12   |     |      | V    |
|                                                                                            |          | −7   |     |      |      |
| High-level input voltage, V <sub>IH</sub>                                                  | D, DIR   | 2    |     |      | V    |
| Low-level input voltage, V <sub>IL</sub>                                                   | D, DIR   | 0.8  |     |      | V    |
| Differential input voltage, V <sub>ID</sub> (see Note 2)                                   |          | ±12  |     |      | V    |
| High-level output current, I <sub>OH</sub>                                                 | Driver   | −60  |     |      | mA   |
|                                                                                            | Receiver | −400 |     |      | μA   |
| Low-level output current, I <sub>OL</sub>                                                  | Driver   | 60   |     |      | mA   |
|                                                                                            | Receiver | 8    |     |      |      |
| Operating free-air temperature, T <sub>A</sub>                                             |          | 0    |     | 70   | °C   |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

# SN75ALS170, SN75ALS170A

## TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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### DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         |                                                     | TEST CONDITIONS†                                      |                                                    | MIN                                      | TYP‡ | MAX  | UNIT |
|-------------------|-----------------------------------------------------|-------------------------------------------------------|----------------------------------------------------|------------------------------------------|------|------|------|
| V <sub>IK</sub>   | Input clamp voltage                                 | I <sub>I</sub> = −19 mA                               |                                                    |                                          |      | −1.5 | V    |
| V <sub>O</sub>    | Output voltage                                      | I <sub>O</sub> = 0                                    |                                                    | 0                                        |      | 6    | V    |
| V <sub>OH</sub>   | High-level output voltage                           | V <sub>CC</sub> = 4.75 V,<br>V <sub>IL</sub> = 0.8 V, | V <sub>IH</sub> = 2 V,<br>I <sub>OH</sub> = −55 mA | 2.7                                      |      |      | V    |
| V <sub>OL</sub>   | Low-level output voltage                            | V <sub>CC</sub> = 4.75 V,<br>V <sub>IL</sub> = 0.8 V, | V <sub>IH</sub> = 2 V,<br>I <sub>OL</sub> = 55 mA  |                                          |      | 1.7  | V    |
| V <sub>OD1</sub>  | Differential output voltage                         | I <sub>O</sub> = 0                                    |                                                    | 1.5                                      |      | 6    | V    |
| V <sub>OD2</sub>  | Differential output voltage                         | R <sub>L</sub> = 100 Ω,                               | See Figure 1                                       | 1/2V <sub>OD1</sub><br>or 2 <sup>S</sup> |      |      | V    |
|                   |                                                     | R <sub>L</sub> = 54 Ω,                                | See Figure 1                                       | 1.5                                      | 2.5  | 5    | V    |
| V <sub>OD3</sub>  | Differential output voltage                         | V <sub>test</sub> = −7 V to 12 V, See Figure 2        |                                                    | 1.5                                      |      | 5    | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage¶ | R <sub>L</sub> = 540 Ω or 100 Ω, See Figure 1         |                                                    |                                          |      | ±0.2 | V    |
| V <sub>OC</sub>   | Common-mode output voltage                          |                                                       |                                                    |                                          |      | 3    | V    |
|                   |                                                     |                                                       |                                                    |                                          |      | −1   |      |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage¶  |                                                       |                                                    |                                          |      |      |      |
| I <sub>O</sub>    | Output current                                      | Output disabled,<br>See Note 3                        | V <sub>O</sub> = 12 V                              |                                          |      | 1    | mA   |
|                   |                                                     |                                                       | V <sub>O</sub> = −7 V                              |                                          |      | −0.8 |      |
| I <sub>IH</sub>   | High-level input current                            | V <sub>I</sub> = 2.4 V                                |                                                    |                                          |      | 20   | μA   |
| I <sub>IL</sub>   | Low-level input current                             | V <sub>I</sub> = 0.4 V                                |                                                    |                                          |      | −400 | μA   |
| I <sub>OS</sub>   | Short-circuit output current                        | V <sub>O</sub> = −6 V                                 |                                                    |                                          |      | −250 | mA   |
|                   |                                                     | V <sub>O</sub> = 0                                    |                                                    |                                          |      | −150 |      |
|                   |                                                     | V <sub>O</sub> = V <sub>CC</sub>                      |                                                    |                                          |      | 250  |      |
|                   |                                                     | V <sub>O</sub> = 8 V                                  |                                                    |                                          |      | 250  |      |
| I <sub>CC</sub>   | Supply current                                      | No load                                               | Outputs enabled                                    |                                          | 69   | 90   | mA   |
|                   |                                                     |                                                       | Outputs disabled                                   |                                          | 57   | 78   |      |

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

§ The minimum  $V_{OD2}$  with a 100- $\Omega$  load is either  $1/2 V_{OD1}$  or 2 V, whichever is greater.

¶  $\Delta |V_{OD}|$  and  $\Delta |V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$  respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

# SN75ALS170, SN75ALS170A

## TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                     | TEST CONDITIONS                                                                       |                                                                                            | MIN                                     | TYP <sup>†</sup> | MAX | UNIT |    |
|-----------------------|-------------------------------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----------------------------------------|------------------|-----|------|----|
| t <sub>d</sub> (OD)   | Differential output delay time      | ALS170                                                                                | R <sub>L</sub> = 54 Ω,<br>T <sub>A</sub> =25°C,<br>C <sub>L</sub> = 50 pF,<br>See Figure 3 | 3                                       | 8                | 13  | ns   |    |
|                       | ALS170A                             | 5.5                                                                                   |                                                                                            | 8                                       | 10.5             |     |      |    |
|                       | ALS170                              | R <sub>L1</sub> = R <sub>L3</sub> = 165 Ω,<br>C <sub>L</sub> = 60 pF,<br>See Figure 4 | 3                                                                                          | 8                                       | 13               |     |      |    |
|                       | ALS170A                             |                                                                                       | 5.5                                                                                        | 8                                       | 10.5             |     |      |    |
| t <sub>sk</sub> (p)   | Pulse skew <sup>‡</sup>             | R <sub>L</sub> = 54 Ω,<br>See Figure 3                                                |                                                                                            | C <sub>L</sub> = 50 pF,                 | 1                | 5   | ns   |    |
|                       |                                     | R <sub>L1</sub> = R <sub>L3</sub> = 165 Ω,<br>C <sub>L</sub> = 60 pF,                 |                                                                                            | R <sub>L2</sub> = 75 Ω,<br>See Figure 4 | 1                | 5   | ns   |    |
| t <sub>sk</sub> (lim) | Skew limit <sup>§</sup>             | ALS170                                                                                | R <sub>L</sub> = 54 Ω,<br>See Figure 3                                                     | C <sub>L</sub> = 50 pF,                 | 10               |     | ns   |    |
|                       |                                     | ALS170A                                                                               |                                                                                            |                                         | 5                |     |      |    |
|                       |                                     | ALS170                                                                                | R <sub>L1</sub> = R <sub>L3</sub> = 165 Ω,<br>C <sub>L</sub> = 60 pF,<br>See Figure 4      | R <sub>L2</sub> = 75 Ω,<br>See Figure 4 | 10               |     |      |    |
|                       |                                     | ALS170A                                                                               |                                                                                            |                                         | 5                |     |      |    |
| t <sub>t</sub> (OD)   | Differential-output transition time | R <sub>L</sub> = 54 Ω,<br>See Figure 3                                                |                                                                                            | C <sub>L</sub> = 50 pF,                 | 3                | 8   | 13   | ns |
|                       |                                     | R <sub>L1</sub> = R <sub>L3</sub> = 165 Ω,<br>C <sub>L</sub> = 60 pF,                 |                                                                                            | R <sub>L2</sub> = 75 Ω,<br>See Figure 4 | 3                | 8   | 13   |    |

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Pulse skew is defined as the  $|t_{d(ODH)} - t_{d(ODL)}|$  of each channel.

<sup>§</sup> Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions.

### SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | EIA/TIA-422-B             | RS-485                                 |
|----------------------|---------------------------|----------------------------------------|
| $V_O$                | $V_{0a}, V_{0b}$          | $V_{0a}, V_{0b}$                       |
| $ V_{OD1} $          | $V_O$                     | $V_O$                                  |
| $ V_{OD2} $          | $V_t (R_L = 100 \Omega)$  | $V_t (R_L = 54 \Omega)$                |
| $ V_{OD3} $          |                           | $V_t$ (Test Termination Measurement 2) |
| $V_{test}$           |                           | $V_{tst}$                              |
| $\Delta  V_{OD} $    | $  V_t  -  \bar{V}_t  $   | $  V_t  -  \bar{V}_t  $                |
| $V_{OC}$             | $ V_{os} $                | $ V_{os} $                             |
| $\Delta  V_{OC} $    | $ V_{os} - \bar{V}_{os} $ | $ V_{os} - \bar{V}_{os} $              |
| $I_{OS}$             | $ I_{sa} ,  I_{sb} $      |                                        |
| $I_O$                | $ I_{xa} ,  I_{xb} $      | $I_{ia}, I_{ib}$                       |

## RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

| PARAMETER |                                            | TEST CONDITIONS                             |                                      | MIN               | TYP <sup>†</sup> | MAX    | UNIT |
|-----------|--------------------------------------------|---------------------------------------------|--------------------------------------|-------------------|------------------|--------|------|
| $V_{IT+}$ | Positive-going input threshold voltage     | $V_O = 2.7\text{ V}$ ,                      | $I_O = -0.4\text{ mA}$               |                   |                  | 0.3    | V    |
| $V_{IT-}$ | Negative-going input threshold voltage     | $V_O = 0.5\text{ V}$ ,                      | $I_O = 8\text{ mA}$                  | $-0.3^{\ddagger}$ |                  |        | V    |
| $V_{hys}$ | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                                             |                                      |                   | 60               |        | mV   |
| $V_{IK}$  | Enable-input clamp voltage                 | $I_I = -18\text{ mA}$                       |                                      |                   |                  | $-1.5$ | V    |
| $V_{OH}$  | High-level output voltage                  | $V_{ID} = 300\text{ mV}$ ,<br>See Figure 5  | $I_{OH} = -400\text{ }\mu\text{A}$ , | 2.7               |                  |        | V    |
| $V_{OL}$  | Low-level output voltage                   | $V_{ID} = -300\text{ mV}$ ,<br>See Figure 5 | $I_{OL} = 8\text{ mA}$ ,             |                   |                  | 0.45   | V    |
| $I_{OZ}$  | High-impedance-state output current        | $V_O = 2.4\text{ V}$                        |                                      |                   |                  | 20     | μA   |
|           |                                            | $V_O = 0.4\text{ V}$                        |                                      |                   |                  | $-400$ |      |
| $I_I$     | Line input current                         | Other input = 0,<br>See Note 4              | $V_I = 12\text{ V}$                  |                   |                  | 1      | mA   |
|           |                                            |                                             | $V_I = -7\text{ V}$                  |                   |                  | $-0.8$ |      |
| $I_{IH}$  | High-level enable-input current            | $V_{IH} = 2.7\text{ V}$                     |                                      |                   |                  | 20     | μA   |
| $I_{IL}$  | Low-level enable-input current             | $V_{IL} = 0.4\text{ V}$                     |                                      |                   |                  | $-100$ | μA   |
| $r_I$     | Input resistance                           |                                             |                                      | 12                |                  |        | kΩ   |
| $I_{OS}$  | Short-circuit output current               | $V_{ID} = 300\text{ mV}$ ,                  | $V_O = 0$                            | $-15$             |                  | $-85$  | mA   |
| $I_{CC}$  | Supply current                             | No load                                     | Outputs enabled                      |                   | 69               | 90     | mA   |
|           |                                            |                                             | Outputs disabled                     |                   | 57               | 78     |      |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature range**

| PARAMETER     |                                                  | TEST CONDITIONS |                                                                                                                    | MIN  | TYP <sup>†</sup> | MAX  | UNIT |
|---------------|--------------------------------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------|------|------------------|------|------|
| $t_{PLH}$     | Propagation delay time, low-to-high-level output | ALS170          | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>$C_L = 15\text{ pF}$ ,<br>$T_A = 25^\circ\text{C}$ ,<br>See Figure 6 | 9    |                  | 19   | ns   |
|               |                                                  | ALS170A         |                                                                                                                    | 11.5 |                  | 16.5 |      |
| $t_{PHL}$     | Propagation delay time, high-to-low-level output | ALS170          |                                                                                                                    | 9    |                  | 19   | ns   |
|               |                                                  | ALS170A         |                                                                                                                    | 11.5 |                  | 16.5 |      |
| $t_{sk(p)}$   | Pulse skew <sup>§</sup>                          | ALS170          | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>$C_L = 15\text{ pF}$ ,<br>See Figure 6                               |      | 2                | 6    | ns   |
|               |                                                  | ALS170A         |                                                                                                                    |      |                  | 5    |      |
| $t_{sk(lim)}$ | Skew limit <sup>¶</sup>                          | ALS170          |                                                                                                                    |      |                  | 10   | ns   |
|               |                                                  | ALS170A         |                                                                                                                    |      |                  | 5    |      |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel.

<sup>¶</sup> Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions.

# SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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## PARAMETER MEASUREMENT INFORMATION

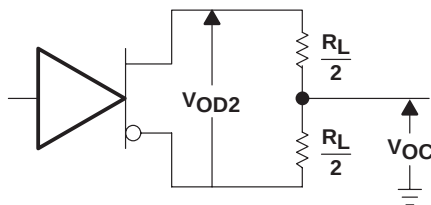


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

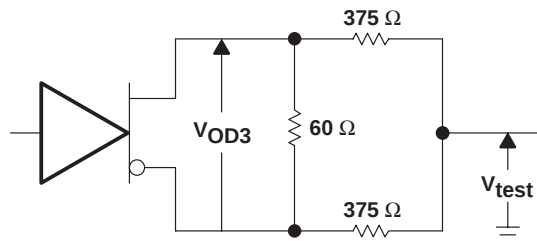
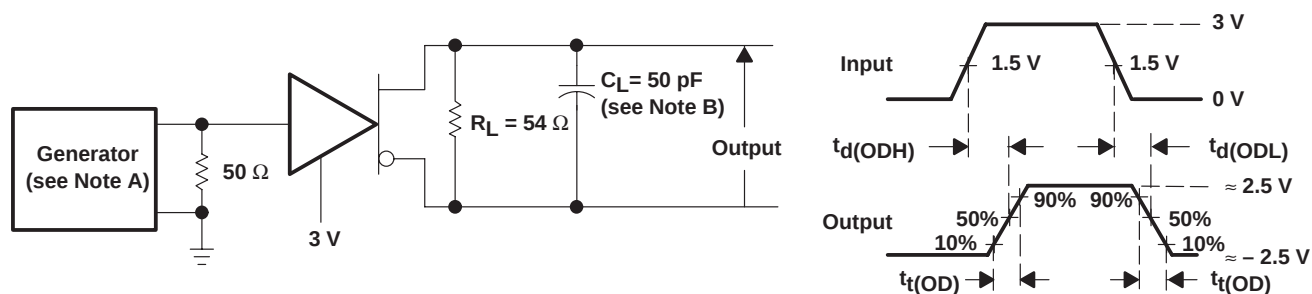


Figure 2. Driver  $V_{OD3}$



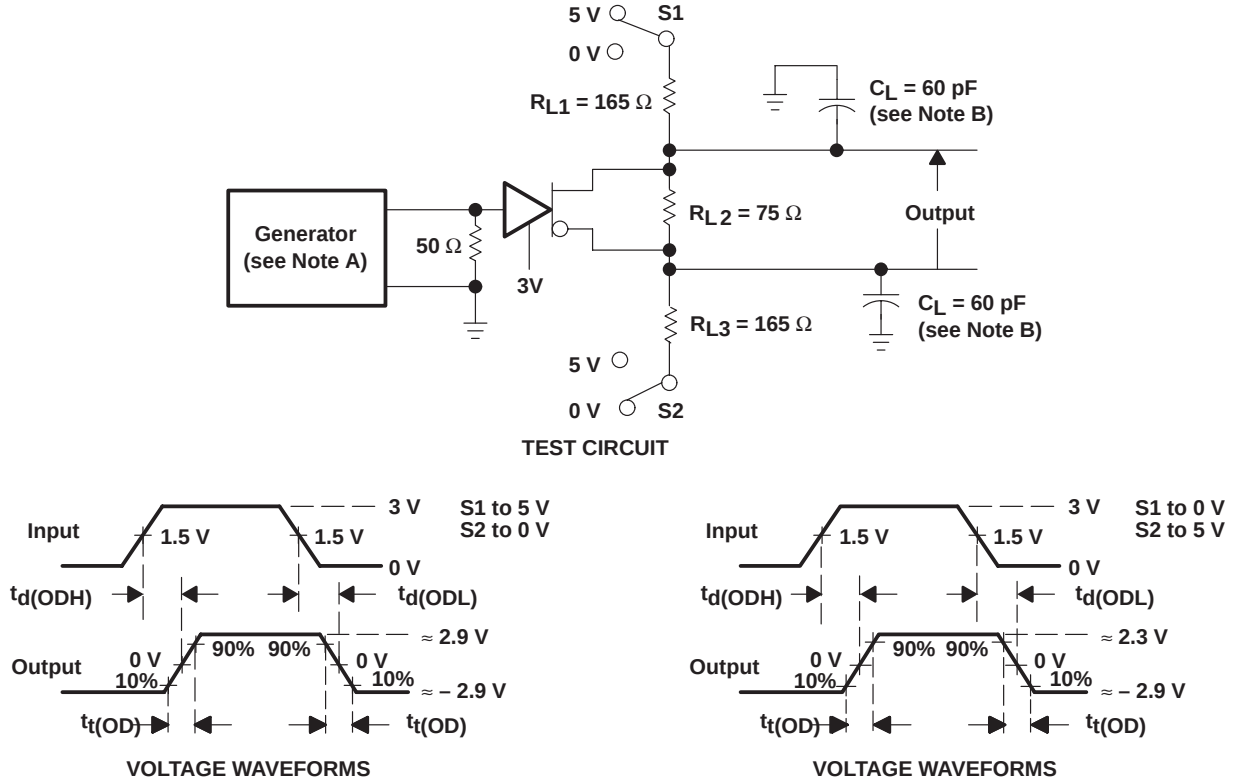
### TEST CIRCUIT

### VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\ \text{MHz}$ , 50% duty cycle,  $t_r \leq 6\ \text{ns}$ ,  $t_f \leq 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

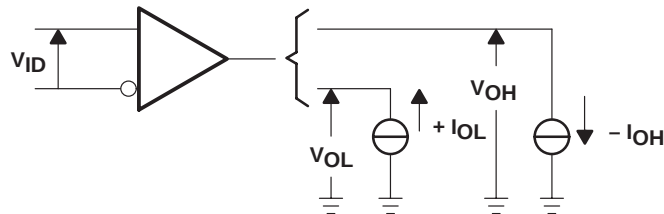
Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

**Figure 4. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load**

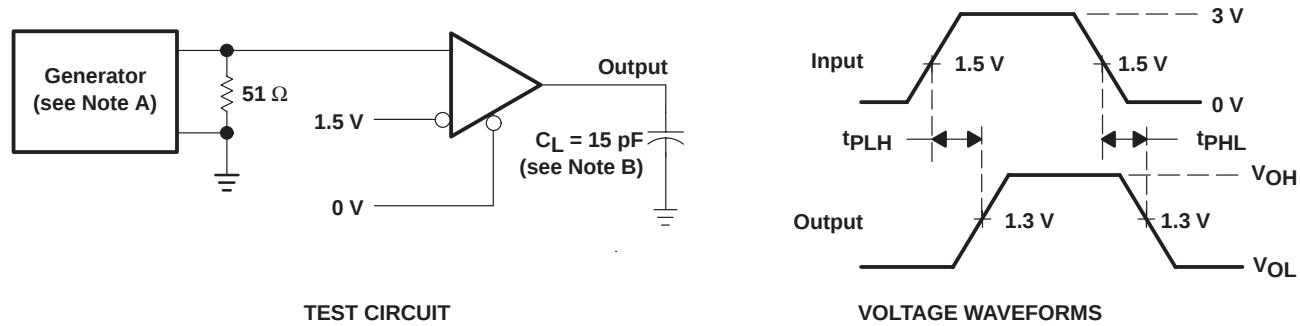


**Figure 5. Receiver  $V_{OH}$  and  $V_{OL}$**

# SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

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## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

## TYPICAL CHARACTERISTICS

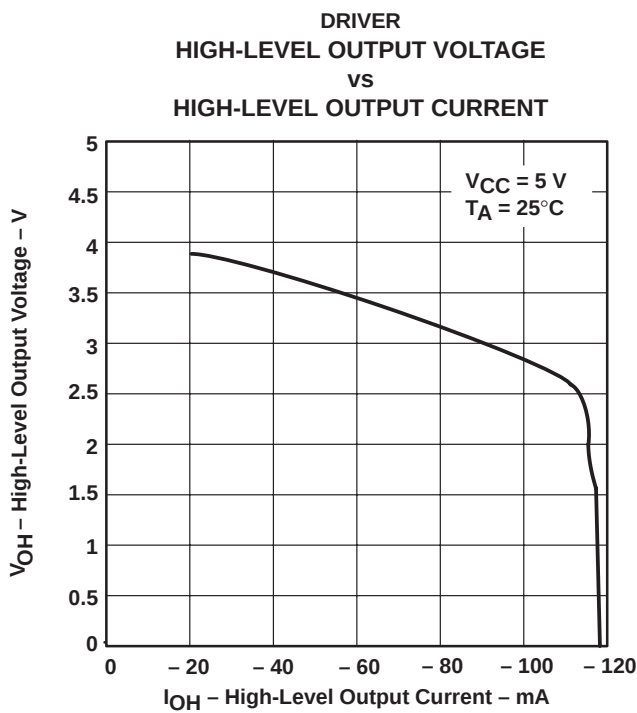


Figure 7

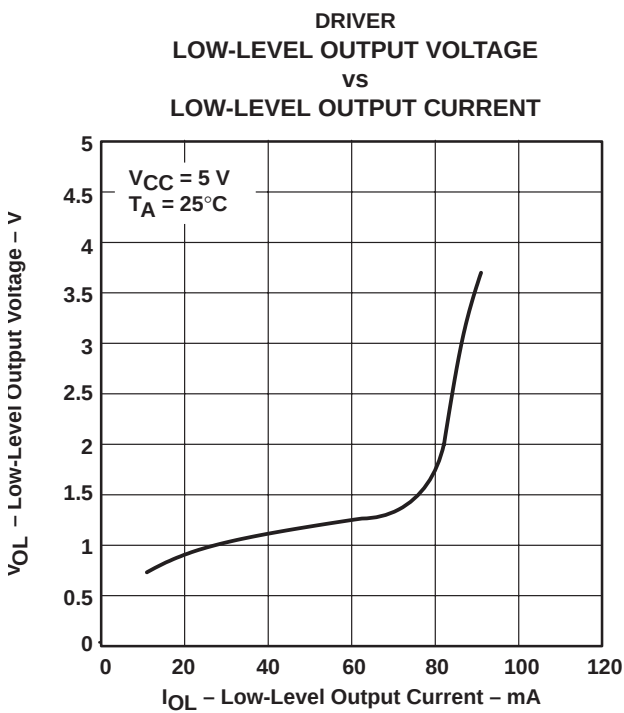


Figure 8

TYPICAL CHARACTERISTICS

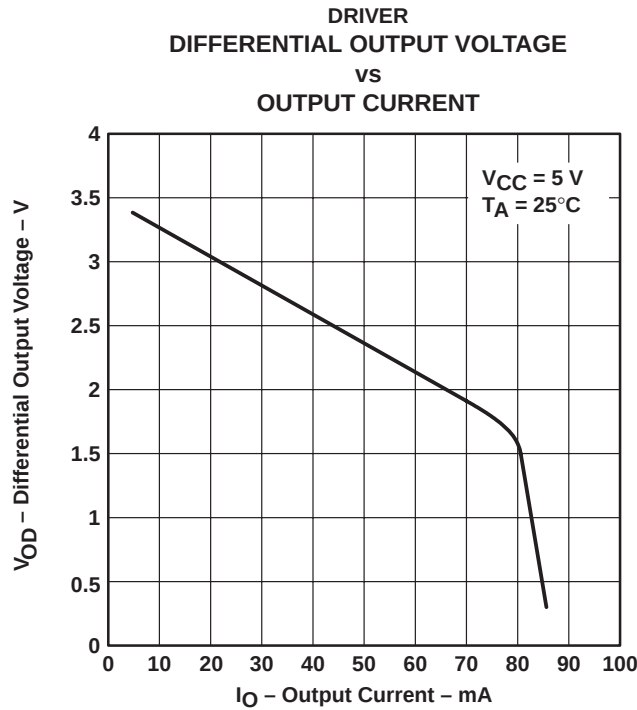


Figure 9

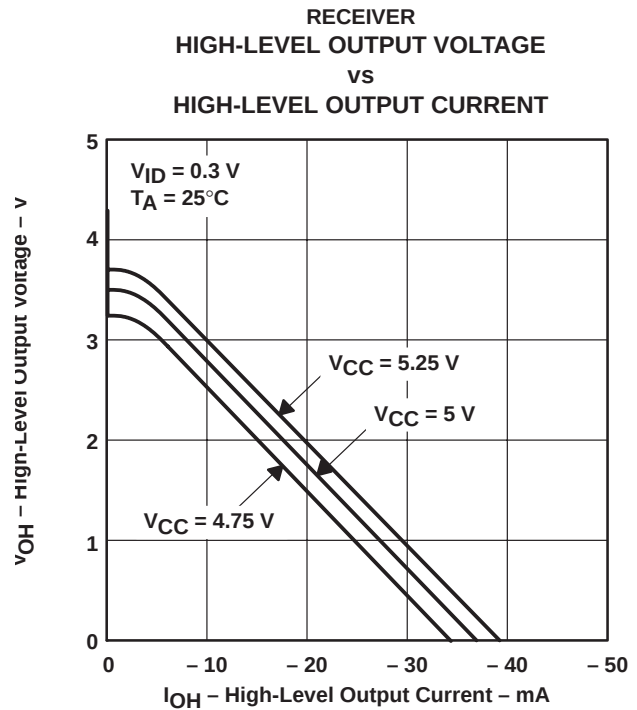


Figure 10

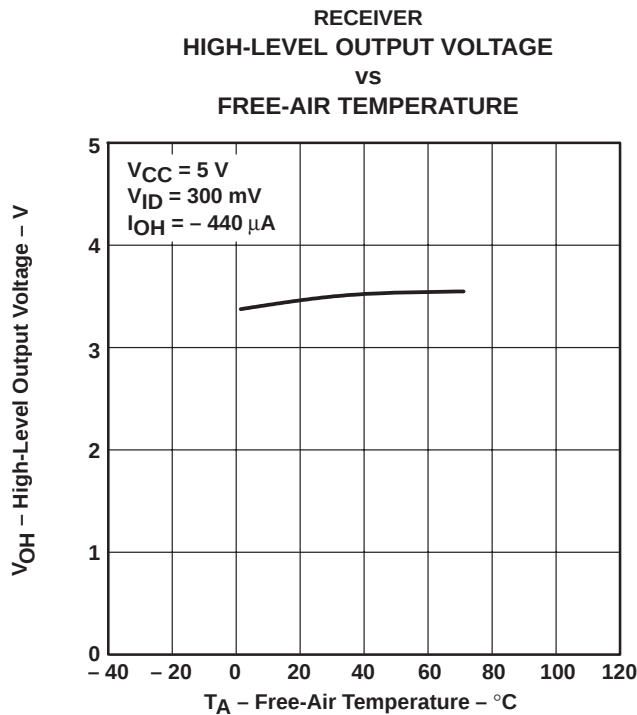


Figure 11

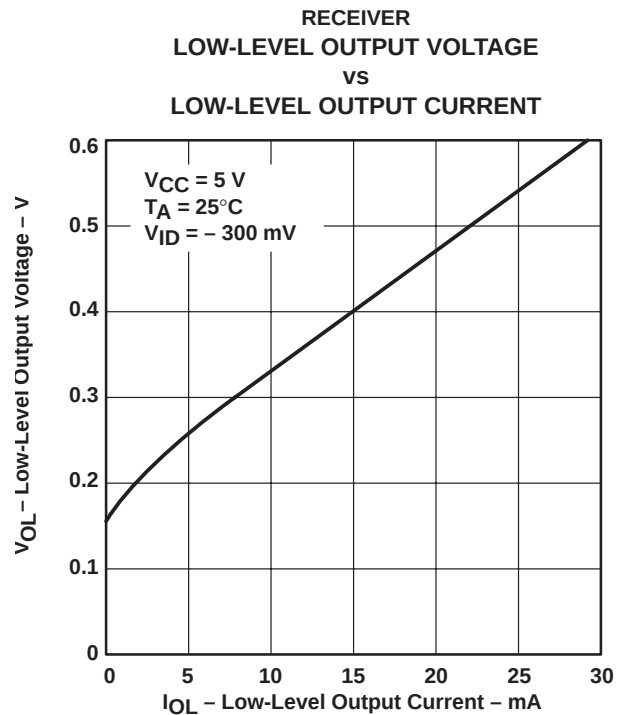


Figure 12

SN75ALS170, SN75ALS170A  
TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS055D – AUGUST 1987 – REVISED SEPTEMBER 1995

TYPICAL CHARACTERISTICS

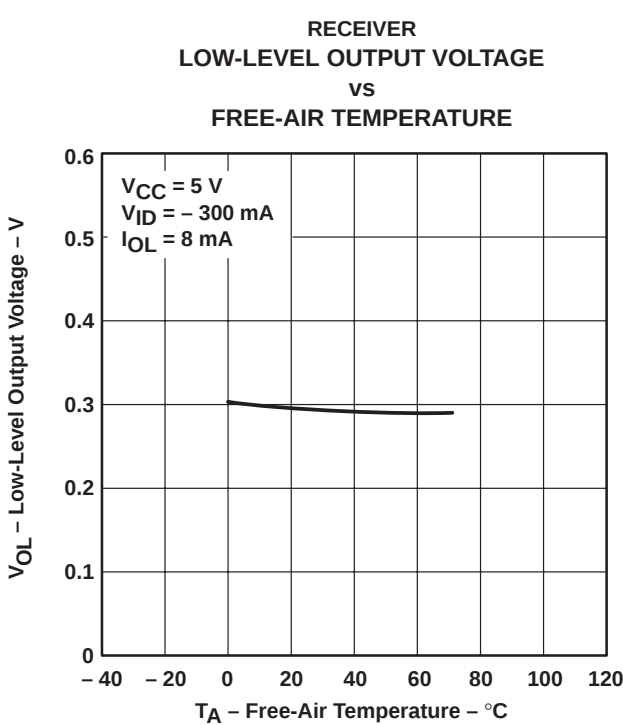


Figure 13

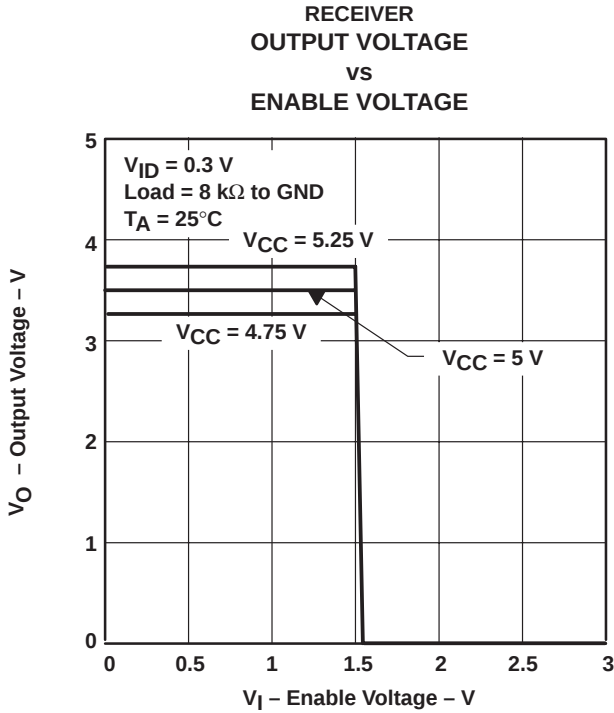


Figure 14

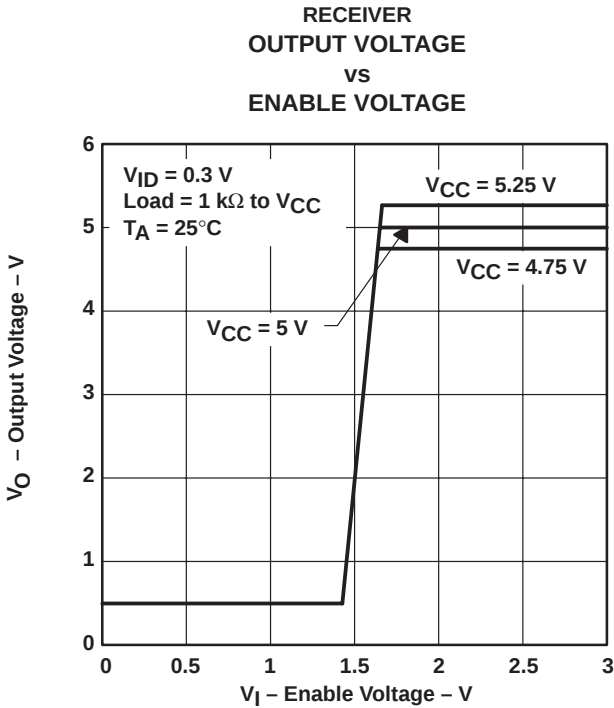
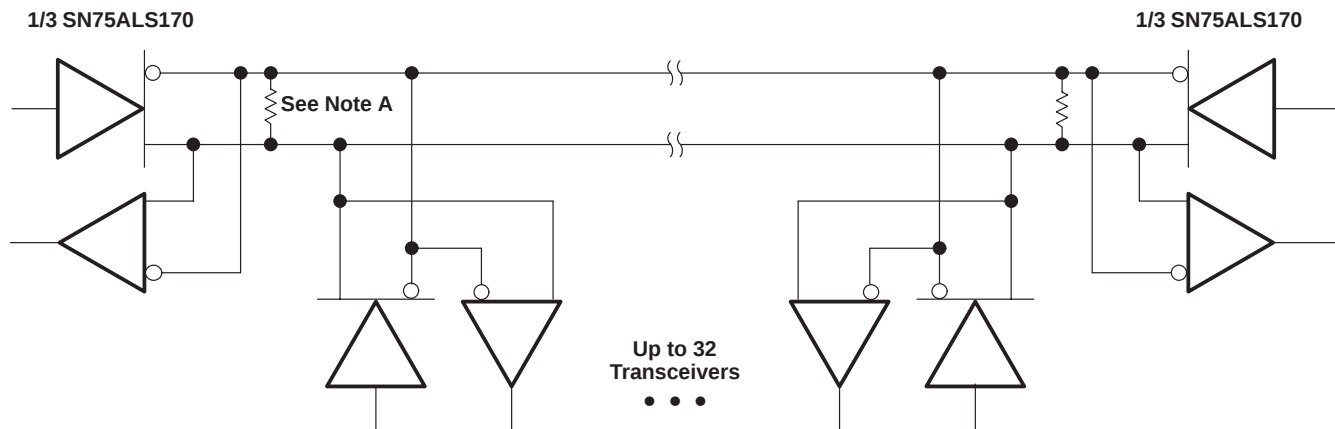


Figure 15

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

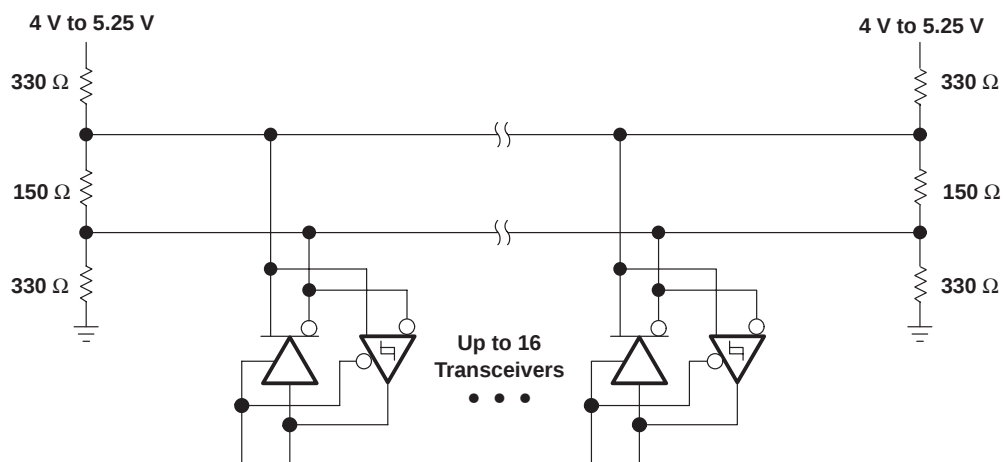


Figure 17. Typical Differential SCSI Application Circuit

# SN75ALS170, SN75ALS170A TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS055D – AUGUST 1987 – REVISED SEPTEMBER 1995

## APPLICATION INFORMATION

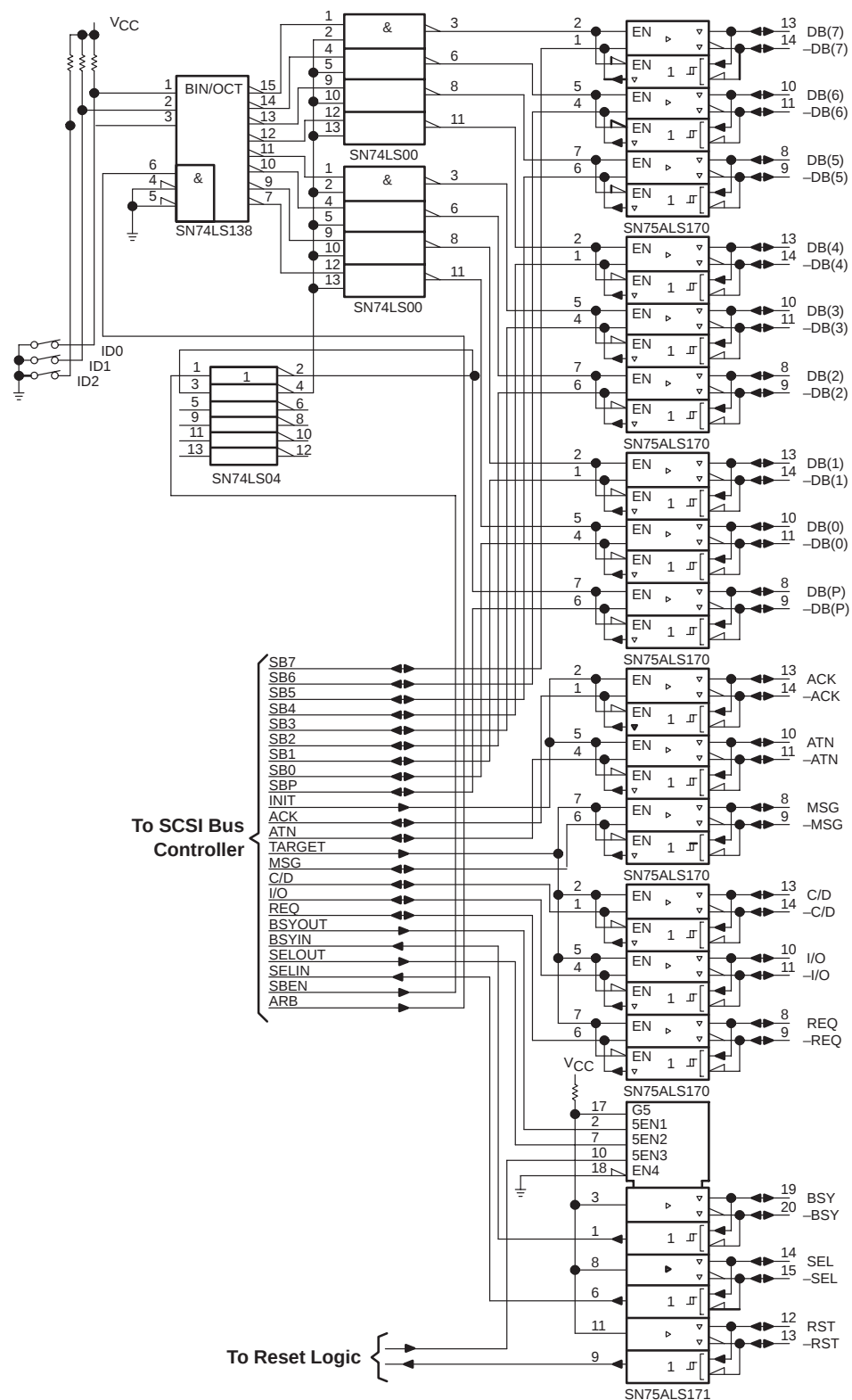


Figure 18. Typical Differential SCSI Bus Interface Implementation

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75ALS170ADW    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170ADWE4  | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170ADWG4  | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170ADWR   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170ADWRE4 | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170ADWRG4 | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DW     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DWE4   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DWG4   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DWR    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DWRE4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170DWRG4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS170J      | OBSOLETE              | CDIP         | J               | 14   |             | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS170ADWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN75ALS170DWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS170ADWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN75ALS170DWR  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

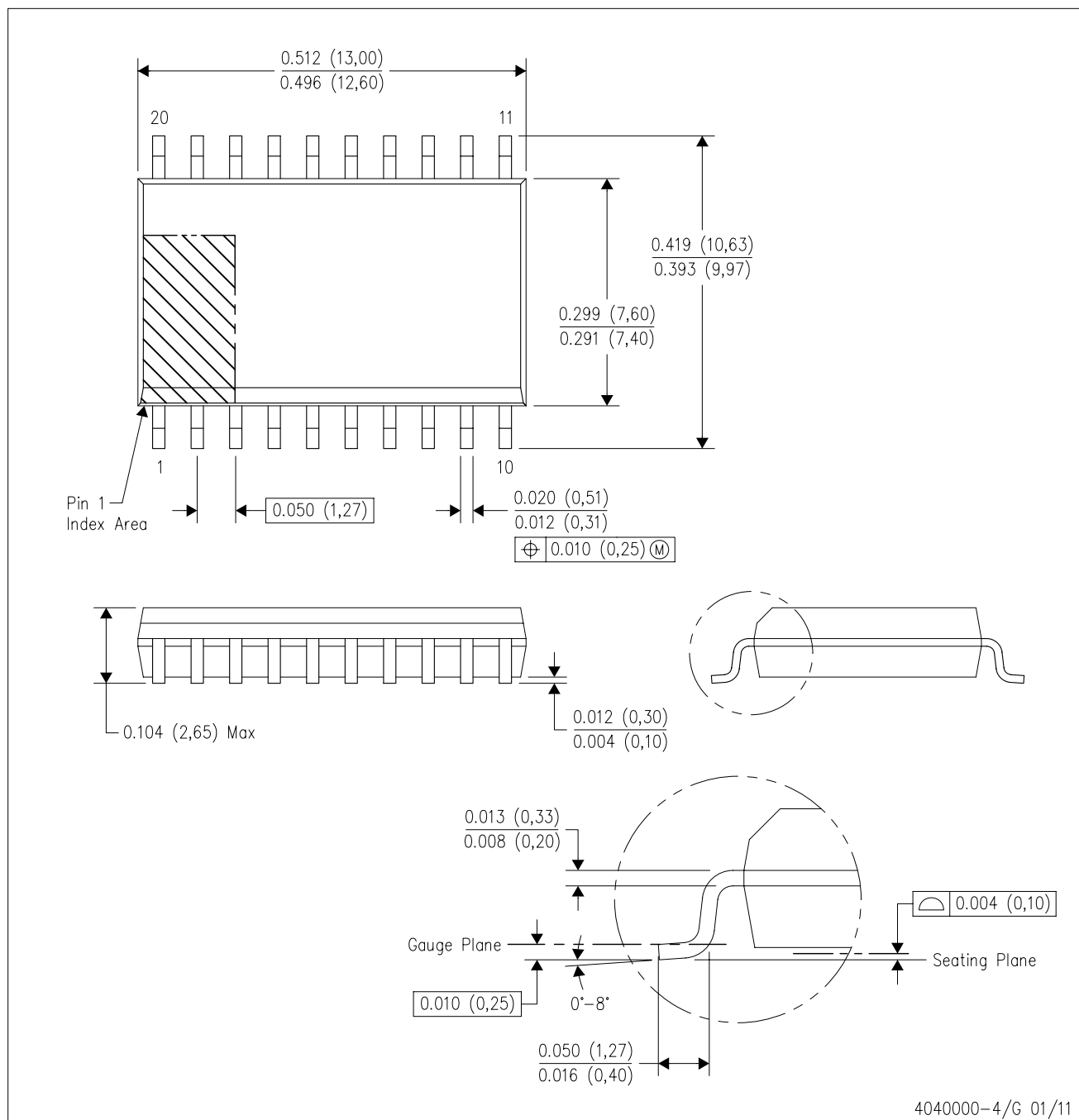


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

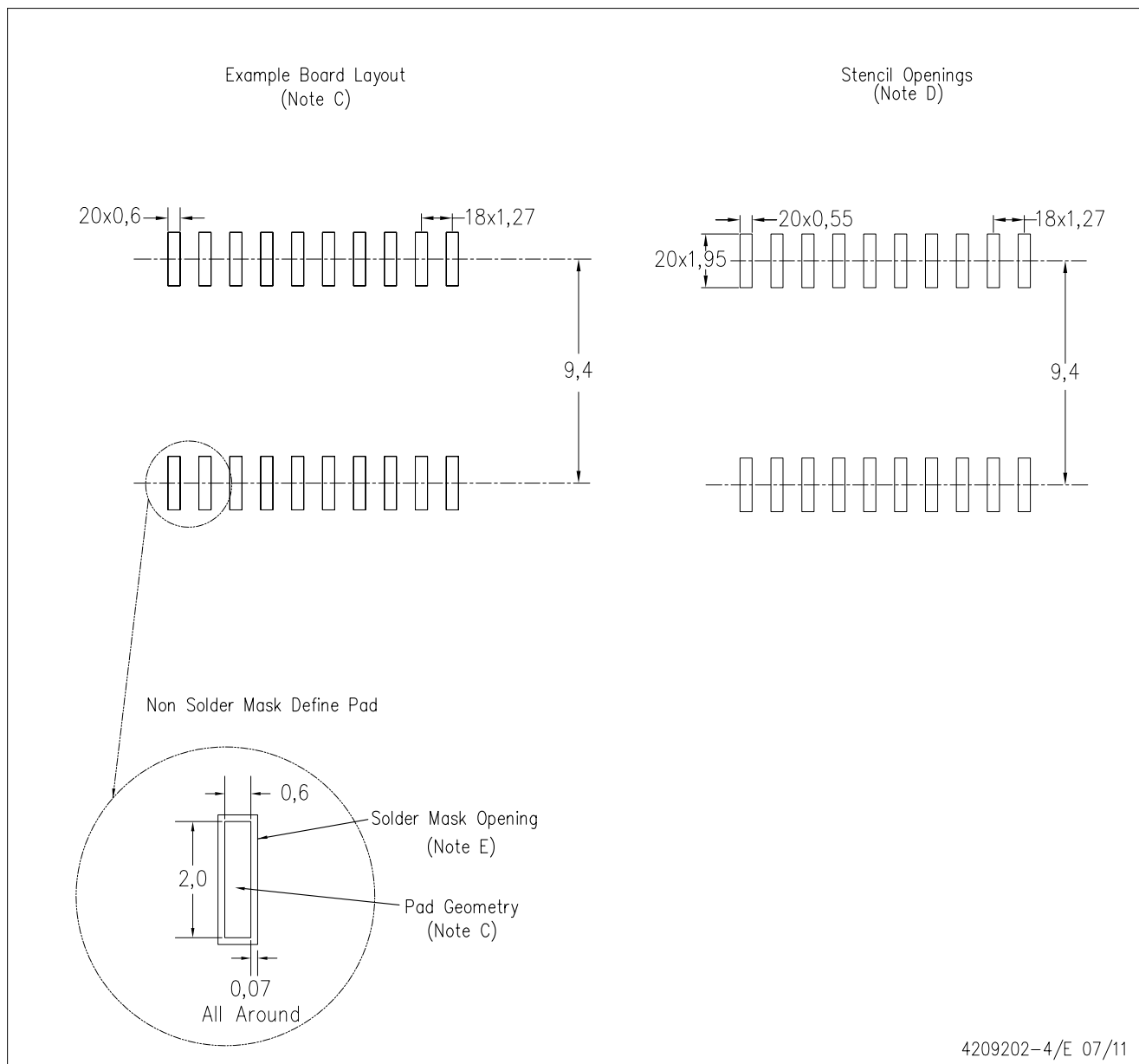
## PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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