Low-Power, Digital Temperature Sensor with Two-Wire Interface in WCSP

Check for Samples: TMP103

FEATURES

- **Multiple Device Access (MDA):**
  - **Global Read/Write Operations**
- **I²C™-/ SMBus™-Compatible Interface**
- **Resolution: 8 Bits**
- **Accuracy: ±1°C Typ (–10°C to +100°C)**
- **Low Quiescent Current:**
  - **3µA Active I_Q at 0.25Hz**
  - **1µA Shutdown**
- **Supply Range: 1.4V to 3.6V**
- **Digital Output**
- **Package: 4-Ball WCSP (DSBGA)**

APPLICATIONS

- **Handsets**
- **Notebooks**

DESCRIPTION

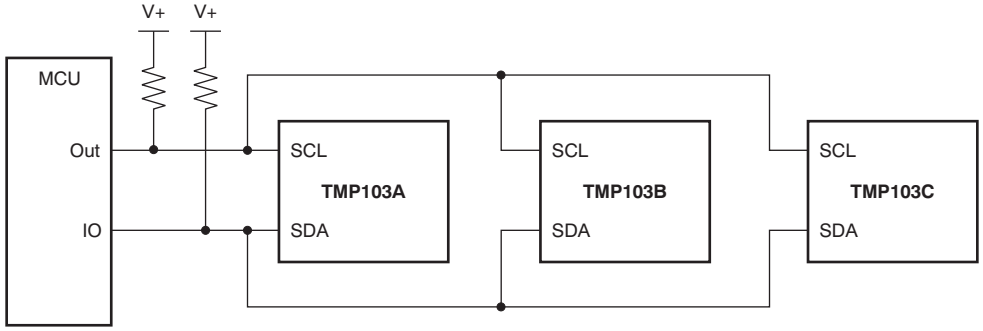
The TMP103 is a digital output temperature sensor in a four-ball wafer chip-scale package (WCSP). The TMP103 is capable of reading temperatures to a resolution of 1°C.

The TMP103 features a two-wire interface that is compatible with both I²C and SMBus interfaces. In addition, the interface supports multiple device access (MDA) commands that allow the master to communicate with multiple devices on the bus simultaneously, eliminating the need to send individual commands to each TMP103 on the bus.

Up to eight TMP103s can be tied together in parallel and easily read by the host. The TMP103 is especially ideal for space-constrained, power-sensitive applications with multiple temperature measurement zones that must be monitored.

The TMP103 is specified for operation over a temperature range of –40°C to +125°C.

TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ADDRESS	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
TMP103A	1110000	DSBGA-4	YFF	TA	TMP103AYFFR
					TMP103AYFFT
TMP103B	1110001	DSBGA-4	YFF	TB	TMP103BYFFR
					TMP103BYFFT
TMP103C	1110010	DSBGA-4	YFF	TC	TMP103CYFFR
					TMP103CYFFT
TMP103D	1110011	DSBGA-4	YFF	TD	TMP103DYFFR
					TMP103DYFFT
TMP103E	1110100	DSBGA-4	YFF	TE	TMP103EYFFR
					TMP103EYFFT
TMP103F	1110101	DSBGA-4	YFF	TF	TMP103FYFFR
					TMP103FYFFT
TMP103G	1110110	DSBGA-4	YFF	TG	TMP103GYFFR
					TMP103GYFFT
TMP103H	1110111	DSBGA-4	YFF	TH	TMP103HYFFR
					TMP103HYFFT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device prodict folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		TMP103	UNIT
Supply Voltage		3.6	V
Input Voltage (2)		–0.3 to (V+) + 0.3	V
Operating Temperature		–55 to +150	°C
Storage Temperature		–60 to +150	°C
Junction Temperature		+150	°C
ESD Rating	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input voltage rating applies to all TMP103 input voltages.

THERMAL INFORMATION

THERMAL METRIC(1)		TMP103 YFF 4	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	160	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	75	
θ_{JB}	Junction-to-board thermal resistance	76	
ψ_{JT}	Junction-to-top characterization parameter	3	
ψ_{JB}	Junction-to-board characterization parameter	74	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

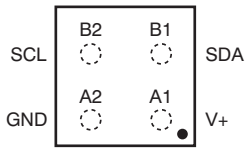
ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V+ = +1.4V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TMP103 MIN	TMP103 TYP	TMP103 MAX	UNIT
TEMPERATURE INPUT						
Range			–40		+125	°C
Accuracy (Temperature Error)		–10°C to +100°C, V+ = 1.8V		0	±2	°C
		–40°C to +125°C, V+ = 1.8V		±1	±3	°C
vs Supply				±0.2	±0.5	°C/V
Resolution				1.0		°C
DIGITAL INPUT/OUTPUT						
Input Logic Levels	V_{IH}		0.7 (V+)		V+	V
	V_{IL}		–0.5		0.3 (V+)	V
Input Current	I_{IN}	0 < V_{IN} < (V+) + 0.3V			1	µA
Output Logic Levels	V_{OL} SDA	V+ > 2V, I_{OL} = 2mA	0		0.4	V
		V+ < 2V, I_{OL} = 2mA	0		0.2 (V+)	V
Resolution				8		Bit
Conversion Time				26	35	ms
Conversion Modes		CR1 = 0, CR0 = 0 (default)		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		8		Conv/s
Timeout Time				30	40	ms
POWER SUPPLY						
Operating Supply Range			+1.4		+3.6	V
Quiescent Current	I_Q	Serial Bus Inactive, CR1 = 0, CR0 = 0 (default), V+ = 1.8V		1.5	3	µA
		Serial Bus Active, SCL Frequency = 400kHz		15		µA
		Serial Bus Active, SCL Frequency = 3.4MHz		85		µA
Shutdown Current	I_{SD}	Serial Bus Inactive, V+ = 1.8V		0.5	1	µA
		Serial Bus Active, SCL Frequency = 400kHz		10		µA
		Serial Bus Active, SCL Frequency = 3.4MHz		80		µA
TEMPERATURE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C

PIN CONFIGURATION

YFF PACKAGE
WCSP-4 (DSBGA-4)
(TOP VIEW)



PIN DESCRIPTIONS

PIN		
NO.	**NAME**	**DESCRIPTION**
A1	V+	Supply voltage
A2	GND	Ground
B1	SDA	Input/output data pin
B2	SCL	Input clock pin

TYPICAL CHARACTERISTICS

At T_A = +25°C and V+ = 1.8V, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE (0.25 Conversions per Second)

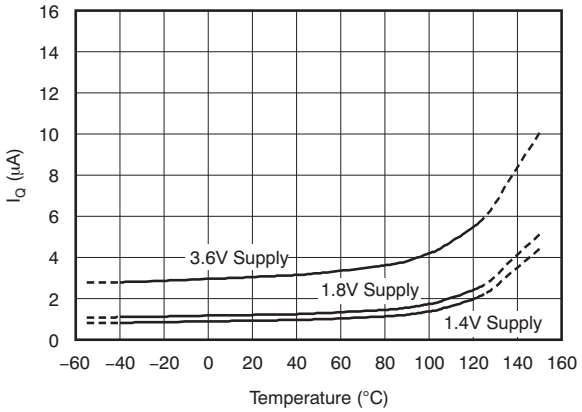


Figure 1.

SHUTDOWN CURRENT vs TEMPERATURE

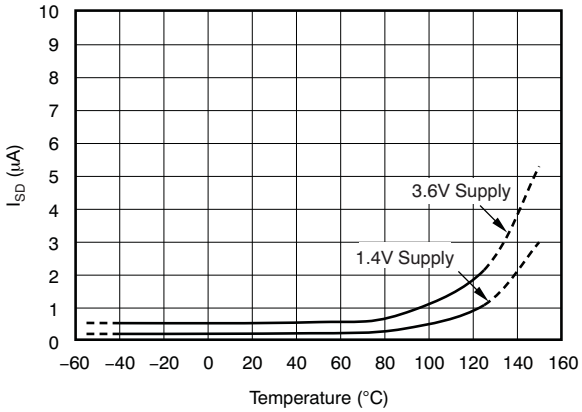


Figure 2.

CONVERSION TIME vs TEMPERATURE

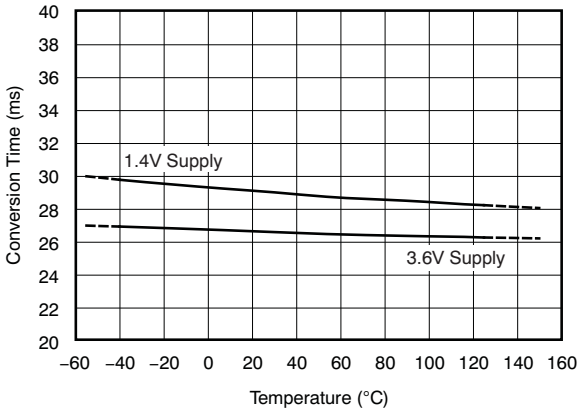


Figure 3.

QUIESCENT CURRENT vs BUS FREQUENCY (Temperature at 3.3V Supply)

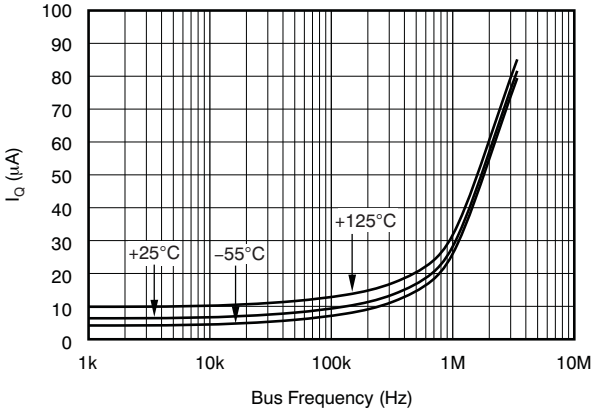


Figure 4.

TEMPERATURE ERROR vs TEMPERATURE

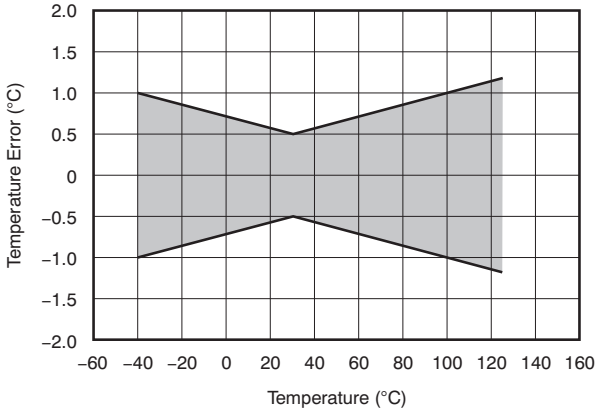


Figure 5.

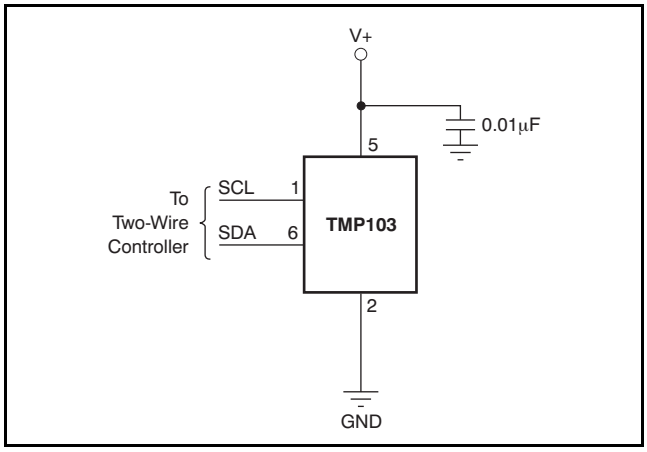
APPLICATION INFORMATION

GENERAL DESCRIPTION

The TMP103 is a digital output temperature sensor in a wafer chip-scale package (WCSP) that is optimal for thermal management and thermal profiling. The TMP103 includes a two-wire interface that is compatible with both I^2C and SMBus interfaces. In addition, the TMP103 has the capability of executing multiple device access (MDA) commands that allow multiple TMP103s to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP103 devices. The TMP103 is specified over a temperature range of –40°C to +125 °C.

The TMP103 serial interface is designed to support up to eight TMP103 devices on a single bus. The TMP103 is offered with eight internal interface addresses. Each unique address option can be used as a location or temperature zone designator. The TMP103 responds to standard I^2C/SMBus slave protocols that allow the internal registers to be written to or read from on an individual basis. The TMP103 also responds to MDA commands that allow all the devices on the bus to be written to or read from, without having to send the individual address and commands to each device.

Pull-up resistors are required on SCL and SDA. A 0.01µF bypass capacitor is also recommended, as shown in Figure 6.



NOTE: SCL and SDA pins require pull-up resistors.

Figure 6. Typical Connections

The temperature sensor in the TMP103 is the chip itself. Thermal paths run through the package bumps as well as the package. The lower thermal resistance of metal causes the bumps to provide the primary thermal path.

To maintain accuracy in applications that require air or surface temperature measurement, care should be taken to isolate the package from ambient air temperature.

POINTER REGISTER

Figure 7 shows the internal register structure of the TMP103. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. During a write command, P2 through P7 must always be '0'. Table 2 describes the pointer address of the registers available in the TMP103. Power-up reset value of P1/P0 is '00'. By default, the TMP103 reads the temperature on power-up.

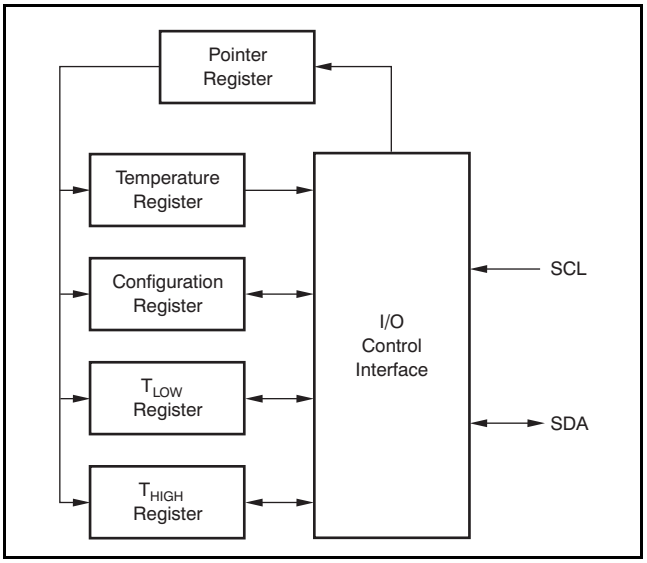


Figure 7. Internal Register Structure

Table 1. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 2. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

TEMPERATURE REGISTER

The Temperature Register of the TMP103 is configured as an eight-bit, read-only register that stores the output of the most recent conversion. A single byte must be read to obtain data, and is described in Table 3. The data format for temperature is summarized in Table 4. One LSB equals 1°C.

Table 3. Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0

Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature Register reads 0°C until the first conversion is complete.

Table 4. 8-Bit Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111	7F
127	0111 1111	7F
100	0110 0100	64
80	0101 0000	50
75	0100 1011	4B
50	0011 0010	32
25	0001 1001	19
0	0000 0000	00
–1	1111 1111	FF
–25	1110 0111	E7
–55	1100 1001	C9

(1) The resolution for the ADC is 1°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with MSB = '0'.

Example: (+50°C)/(1°C/count) = 50 = 32h = 0011 0010

For negative temperatures (for example, –25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = '1'.

Example: (|–25°C|)/(1°C/count) = 25 = 19h = 0001 1001

Twos complement format: 1110 0110 + 1 = 1110 0111

CONFIGURATION REGISTER

The Configuration Register is an eight-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format and power-up/reset value of the Configuration Register is shown in Table 5. All registers are updated at the end of the data byte.

Table 5. Configuration and Power-Up/Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
ID	CR1	CR0	FH	FL	LC	M1	M0
0	0	0	0	0	0	1	0

TEMPERATURE WATCHDOG FUNCTION

The TMP103 contains a watchdog function that monitors device temperature and compares the result to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}) in order to determine if the device temperature is within these set limits. If the temperature of the TMP103 becomes greater than the value in the T_{HIGH} register, then the flag-high bit (FH) in the configuration register is set to '1'. If the temperature falls below value in the T_{LOW} register, then the flag-low bit (FL) is set to '1'. If both flag bits remain '0', then the temperature is within the temperature *window* set by the temperature limit registers, as shown in Figure 8.

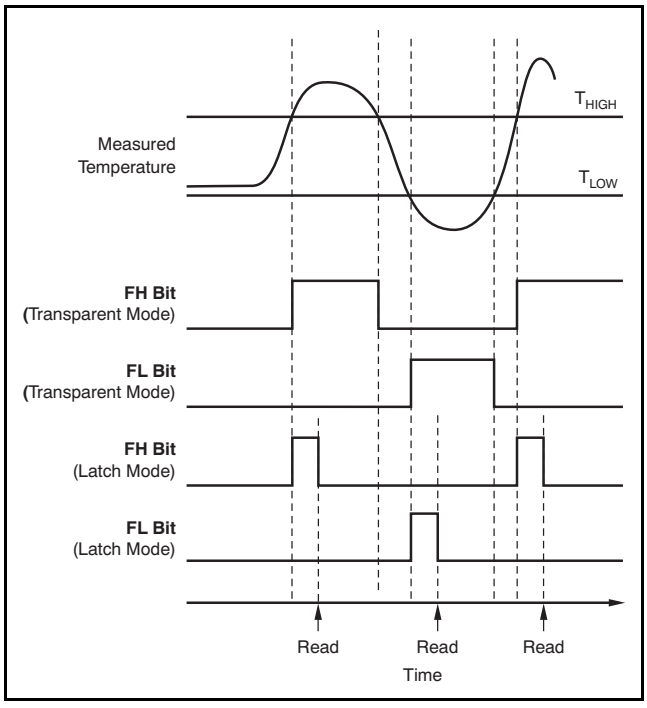


Figure 8. Temperature Flag Functional Diagram

The latch bit (LC) in the configuration register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the configuration register. The flag bits are set to '0' if a read command is received by the TMP103, or if LC = '0' and the temperature is within the temperature limits. The power-on default values for these bits are FH = '0', FL = '0', and LC = '0'.

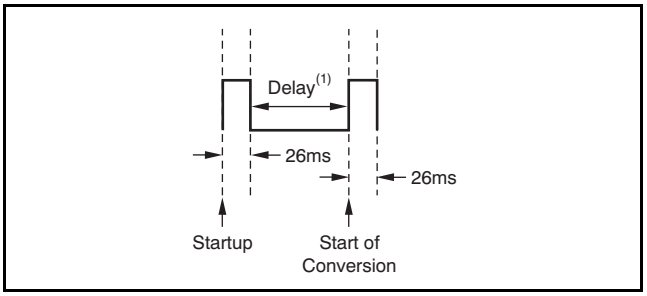
CONVERSION RATE

The conversion rate bits, CR1 and CR0 located in the Configuration Register, configure the TMP103 for conversion rates of 8Hz, 4Hz, 1Hz, or 0.25Hz (default). The TMP103 has a typical conversion time of 26ms. To achieve different conversion rates, the TMP103 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 6 shows the settings for CR1 and CR0.

Table 6. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25Hz (default)
0	1	1Hz
1	0	4Hz
1	1	8Hz

After power-up or general-call reset, the TMP103 immediately starts a conversion, as shown in Figure 9. The first result is available after 26ms (typical). The active quiescent current during conversion is 40µA (typical at +27°C, V+ = 1.8V). The quiescent current during delay is 1.0µA (typical at +27°C, V+ = 1.8V).



(1) Delay is set by CR1 and CR0.

Figure 9. Conversion Start

SHUTDOWN MODE (M1 = '0', M0 = '0')

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5µA. Shutdown mode is enabled when bits M1 and M0 (in the Configuration Register) = '00'. The device shuts down when the current conversion is completed.

ONE-SHOT (M1 = '0', M0 = '1')

The TMP103 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing a '01' to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read '01'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read '00'. This feature is useful for reducing power consumption in the TMP103 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP103 can achieve a higher conversion rate. A single conversion typically takes 26ms and a read can take place in less than 20µs. When using One-Shot mode, 30 or more conversions per second are possible.

CONTINUOUS CONVERSION MODE (M1 = '1')

When the TMP103 is in Continuous Conversion mode (M1 = '1'), a single conversion is performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the Configuration Register). The TMP103 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. See Table 6 for CR1 and CR0 settings.

TEMPERATURE LIMIT REGISTERS

The T_{HIGH} and T_{LOW} registers are used to store the temperature limit thresholds for the TMP103 watchdog function. At the end of each temperature measurement, the TMP103 compares the temperature results to each of these limits. If the temperature result is greater than the T_{HIGH} limit, then the FH bit in the configuration register is set to '1'. If the temperature result is less than the T_{LOW} limit, then the FL bit in the configuration register is set to '1'; see Figure 8.

Table 7 and Table 8 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = +60°C and T_{LOW} = –10°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 7. T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0

Table 8. T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high to low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a START or STOP signal.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SDA from low to high, while SCL is high.

SERIAL INTERFACE

The TMP103 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP103 supports the transmission protocol for both fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP103, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates the intent of executing a read or write operation.

The TMP103 is available in eight versions, each with a different slave address, as shown in Table 9. These addresses can be used as either a location or a temperature zone designator.

Table 9. Device Slave Addresses

PRODUCT	TWO-WIRE ADDRESS	TEMPERATURE ZONE
TMP103A	1110000	Zone1
TMP103B	1110001	Zone2
TMP103C	1110010	Zone3
TMP103D	1110011	Zone4
TMP103E	1110100	Zone5
TMP103F	1110101	Zone6
TMP103G	1110110	Zone7
TMP103H	1110111	Zone8

WRITING/READING OPERATION

Accessing a particular register on the TMP103 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP103 requires a value for the Pointer Register (see Figure 12).

When reading from the TMP103, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 13 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes; the TMP103 remembers the Pointer Register value until it is changed by the next write operation, or the TMP103 is reset.

SLAVE MODE OPERATIONS

The TMP103 can operate as a slave receiver or slave transmitter. As a slave device, the TMP103 never drives the SCL line.

Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP103 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP103 then acknowledges reception of the Pointer Register byte. The next byte is written to the register addressed by the Pointer Register. The TMP103 acknowledges reception of the data byte. The master can terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *Not-Acknowledge* on reception of the data byte, or generating a START or STOP condition.

GENERAL CALL

The TMP103 responds to a two-wire General Call address (0000000) if the eighth bit is '0'. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 00000110, the TMP103 internal registers are reset to power-up values. The TMP103 does not support the General Address acquire command.

HIGH-SPEED (Hs) MODE

In order for the two-wire bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP103 does not acknowledge this byte, but switches its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master transmits a START condition followed by a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP103 switches the input and output filters back to the default fast-mode operation.

TIMEOUT FUNCTION

The TMP103 resets the serial interface if SCL is held low for 30ms (typ). The TMP103 releases the bus if it is pulled low and waits for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SCL operating frequency.

MULTIPLE DEVICE ACCESS

The TMP103 supports Multiple Device Access (MDA), which allows the master to communicate with multiple TMP103 devices on the same bus interface with one interface transaction. MDA commands consist of an MDA read address (00000001) and an MDA write address (00000000). The device acknowledges the MDA address and responds to the command accordingly. In order for MDA to function correctly, different product versions of the TMP103 must be used in the system; see Table 9.

Multiple Device Access Write

The master transmits an MDA write address followed by the pointer address of the register to be accessed; see Table 2. Following the pointer, all of the TMP103 devices on the bus acknowledge and wait for the next byte of data to be written to the addressed registers. When the data byte is received by the TMP103 devices, they store and acknowledge the transmitted byte. The TMP103s store the same data on all devices on the bus in one transaction; see Figure 14.

Multiple Device Access Read

Note that before an MDA read transaction can begin, the master must first send an MDA write transaction in order to set the appropriate pointer address of the register to be accessed, as stated in the previous section. The master can then transmit an MDA read address followed by a read byte for each TMP103 used on the bus. For example, if a TMP103A and TMP103B are used on the same bus and an MDA read address is sent, the address must be followed by two bytes of data and two master acknowledges. The TMP103A sends data on the first byte and the TMP103B sends data on the second byte. The master must issue an acknowledge for each byte read in order to read all of the TMP103 devices on the bus; see Figure 15. If the master does not acknowledge each byte of data, the TMP103s stop sending subsequent data for any remaining devices.

Up to eight TMP103 devices can be on the same bus and respond to MDA commands; see Table 9.

NOTE: If the bus contains an incomplete sequence of TMP103 device addresses, the master must transmit all required dummy bytes for the missing device address to allow for normal MDA read operation. For example, if the TMP103A, TMP103B, and TMP103D devices are on the bus, the master must transmit an MDA read address followed by four bytes and four acknowledges in order to complete the MDA read transaction.

NOISE

The TMP103 is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the TMP103 can further reduce any noise the TMP103 might propagate to other components. R_F in Figure 10 should be less than 5kΩ and C_F should be greater than 10nF.

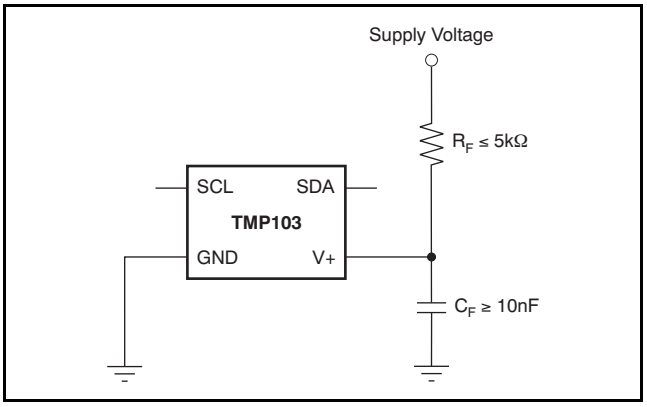


Figure 10. Noise Reduction

TIMING DIAGRAMS

The TMP103 is two-wire and SMBus compatible. Figure 11 to Figure 15 describe the various operations on the TMP103. Parameters for Figure 11 are defined in Table 10. Bus definitions are:

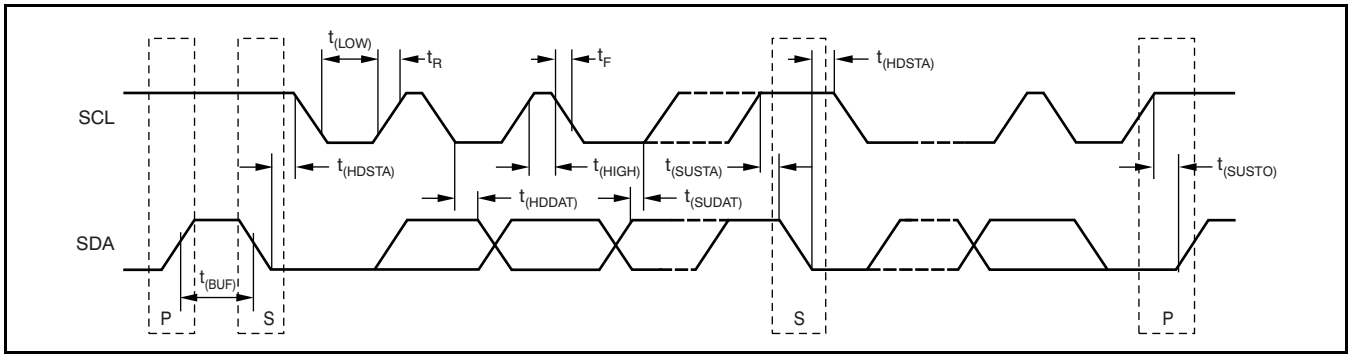
Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *Not-Acknowledge* ('1') on the last byte that has been transmitted by the slave.

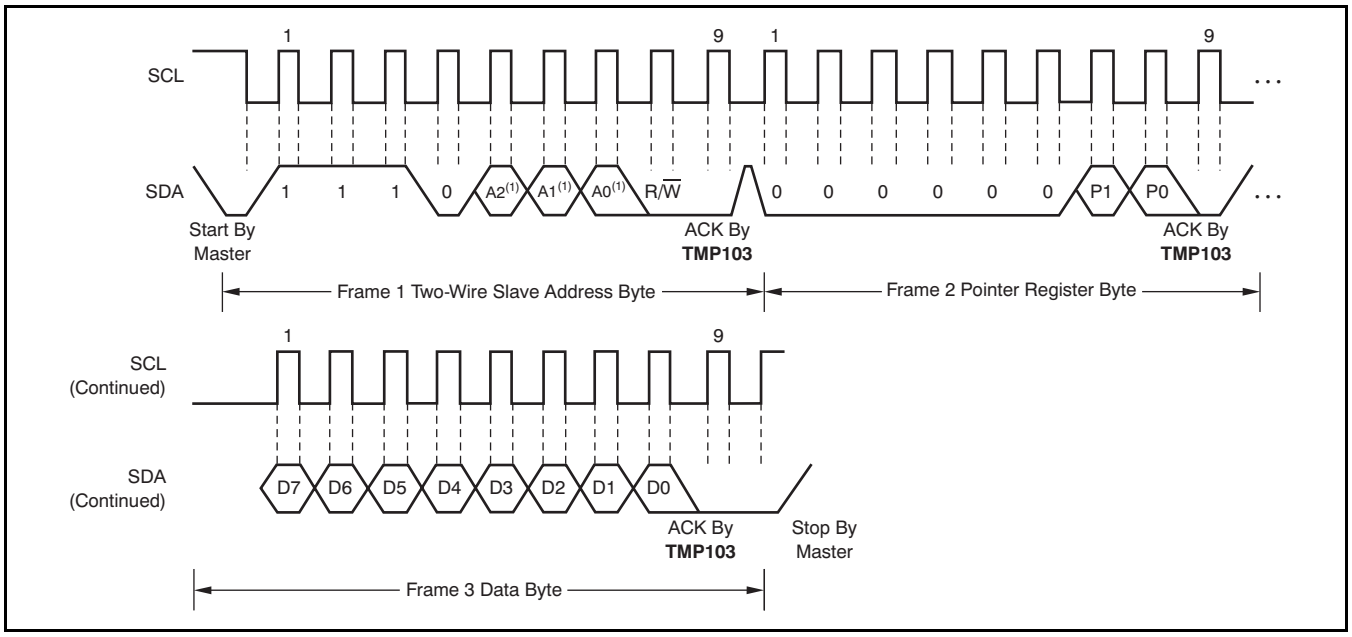


NOTE: P = STOP, S = START.

Figure 11. Two-Wire Timing Diagram

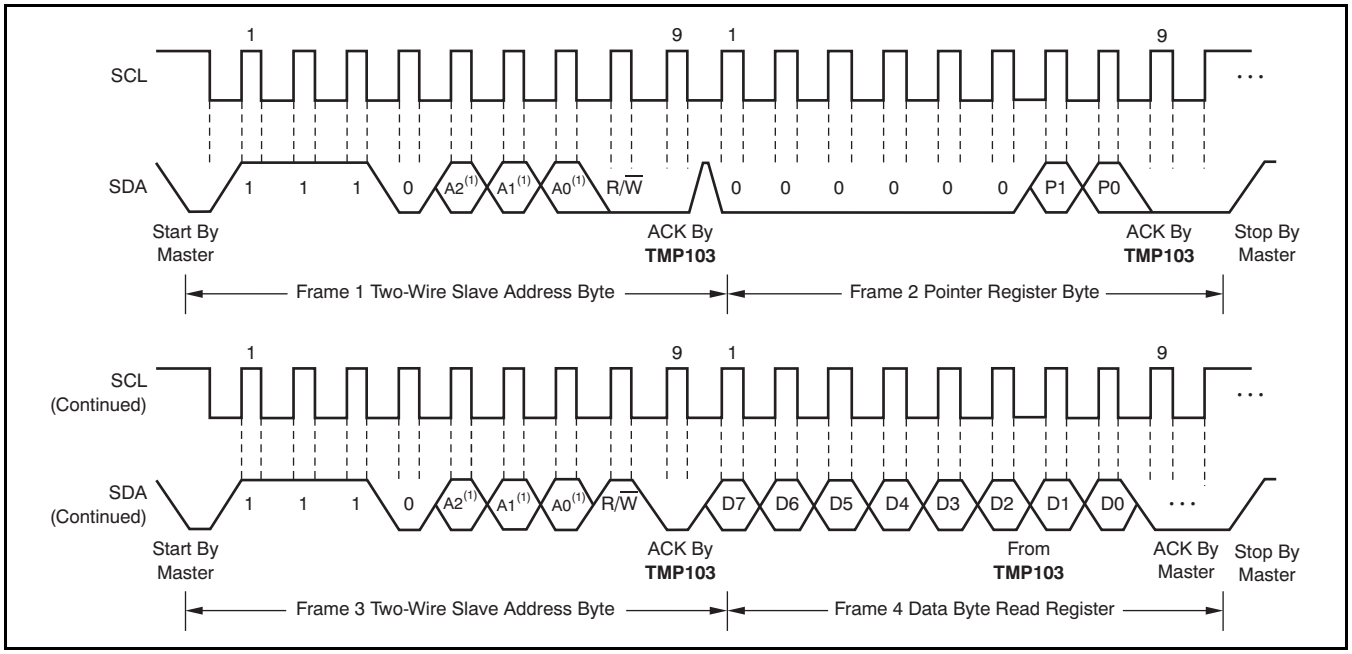
Table 10. Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL Operating Frequency, V_S > 1.7V	0.001	0.4	0.001	3.4	MHz
$f_{(SCL)}$	SCL Operating Frequency, V_S < 1.7V	0.001	0.4	0.001	2.75	MHz
$t_{(BUF)}$	Bus Free Time Between STOP and START Condition	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	100		100		ns
$t_{(SUSTA)}$	Repeated START Condition Setup Time	100		100		ns
$t_{(SUSTO)}$	STOP Condition Setup Time	100		100		ns
$t_{(HDDAT)}$	Data Hold Time	0		0		ns
$t_{(SUDAT)}$	Data Setup Time	100		10		ns
$t_{(LOW)}$	SCL Clock Low Period, V_S > 1.7V	1300		160		ns
$t_{(LOW)}$	SCL Clock Low Period, V_S < 1.7V	1300		200		ns
$t_{(HIGH)}$	SCL Clock High Period	600		60		ns
t_F	Clock/Data Fall Time		300			ns
t_R	Clock/Data Rise Time		300		160	ns
t_R	Clock/Data Rise Time for SCLK ≤ 100kHz		1000			ns



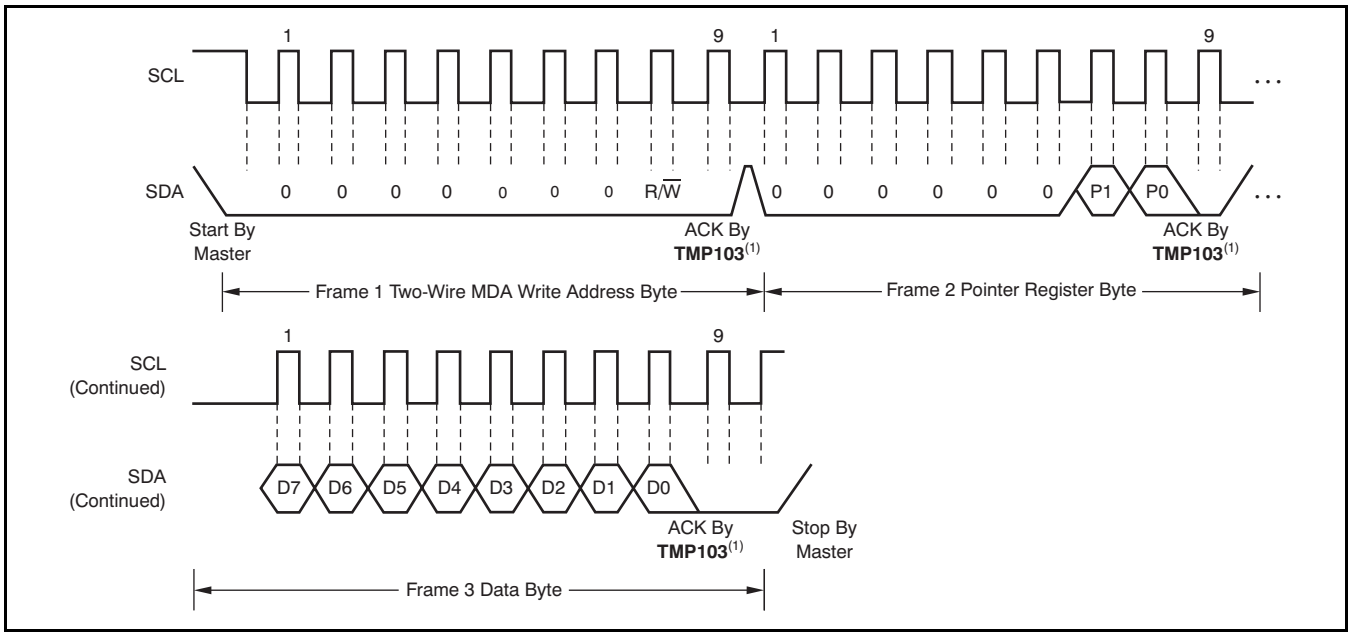
(1) The value of A0, A1, and A2 are determined by the TMP103 version; see Table 9.

Figure 12. Two-Wire Timing Diagram for Write Word Format



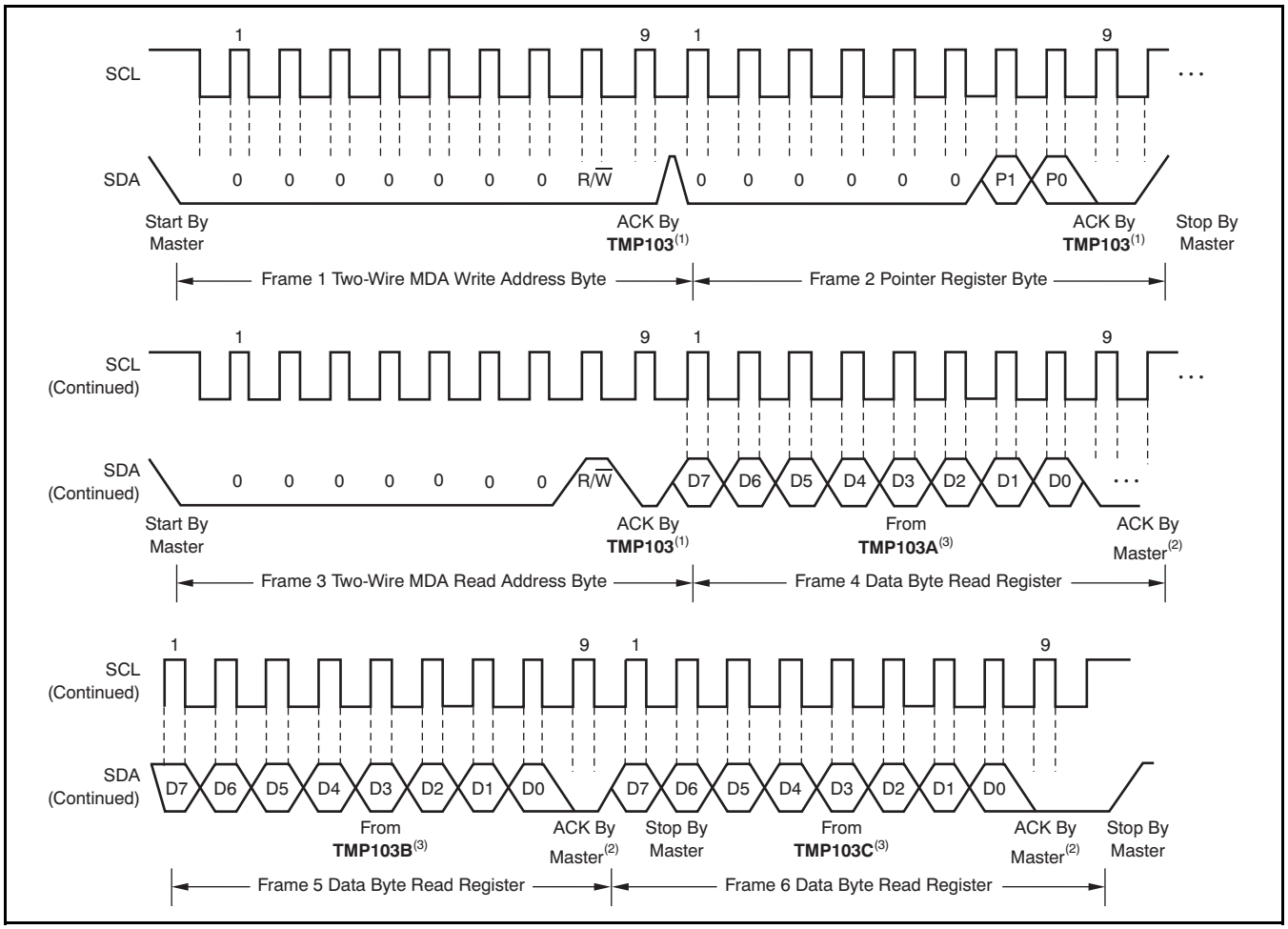
(1) The value of A0, A1, and A2 are determined by the TMP103 version; see Table 9.

Figure 13. Two-Wire Timing Diagram for Read Word Format



(1) All TMP103 devices on the bus acknowledge the byte.

Figure 14. Two-Wire Timing Diagram MDA Write Word Format



(1) All TMP103 devices on the bus acknowledge the byte.

(2) The master must issue an acknowledge for each byte read in order to read all of the TMP103 devices on the bus.

(3) Three TMP103 devices used in this case; up to eight devices can be used (see Table 9).

Figure 15. Two-Wire Timing Diagram MDA Read Word Format Using Typical Application (Front Page)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2011) to Revision A	Page
• Changed Package-Lead from WCSP-4 to DSBGA-4 in Package/Ordering Information table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMP103AYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103AYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103BYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103BYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103CYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103CYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103DYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103DYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103EYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103EYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103FYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103FYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103GYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103GYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103HYFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TMP103HYFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

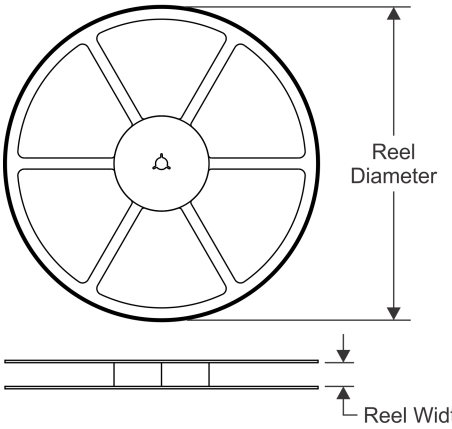
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

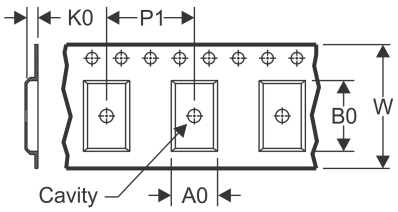
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

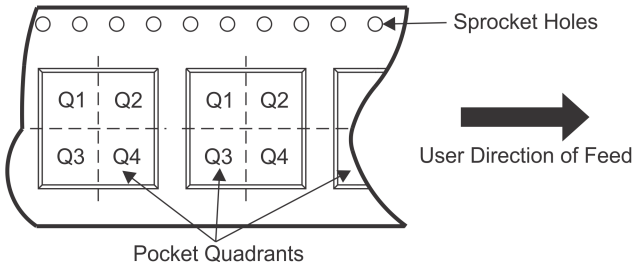


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

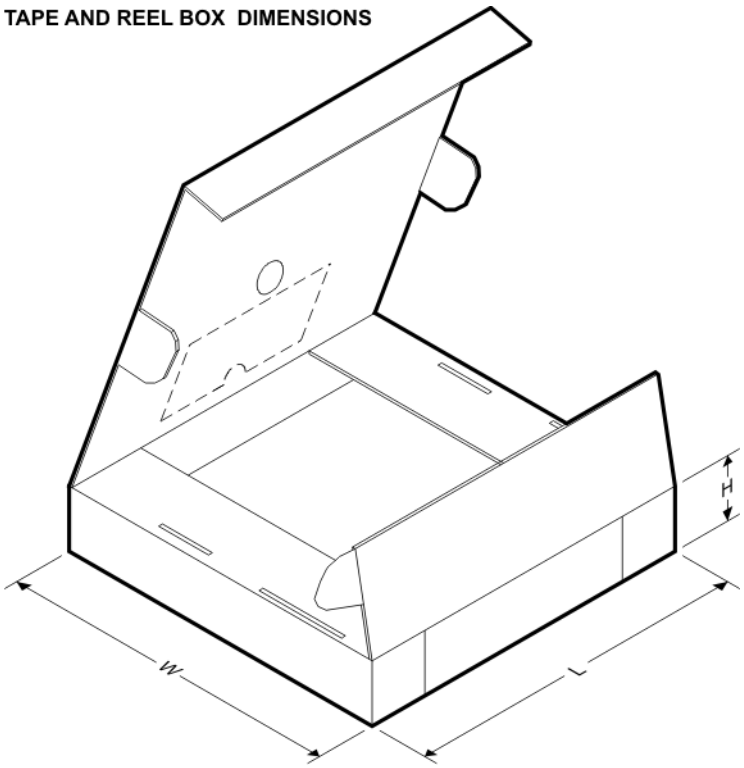
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP103AYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103AYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103BYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103BYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103CYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103CYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103DYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103DYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103EYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103EYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103FYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103FYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103GYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103GYFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TMP103HYFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1

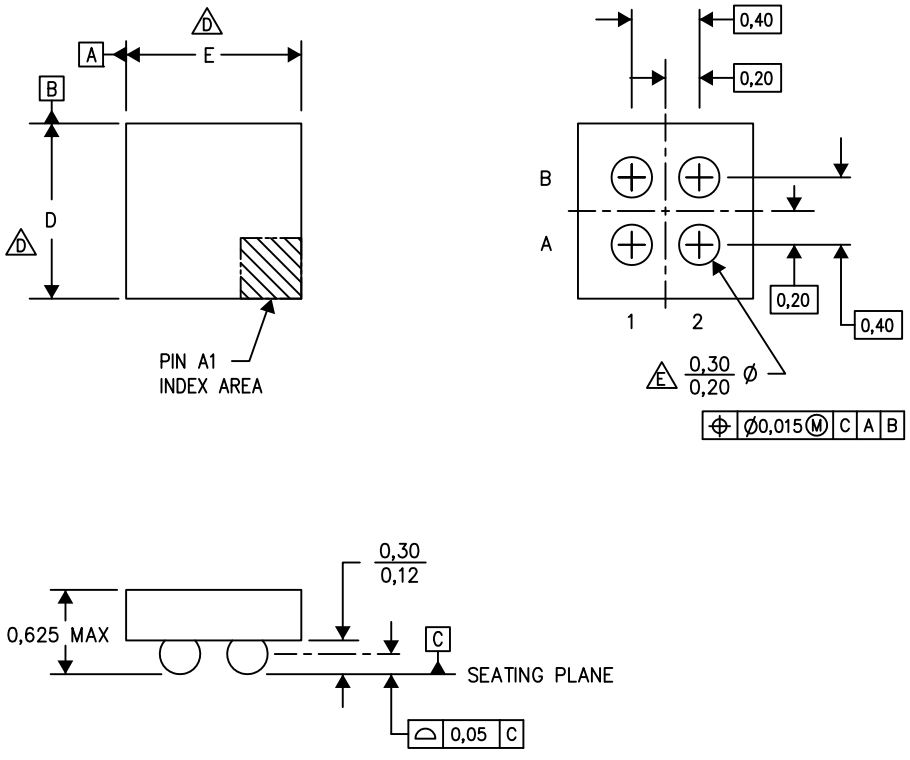
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP103AYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103AYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103BYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103BYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103CYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103CYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103DYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103DYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103EYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103EYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103FYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103FYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103GYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TMP103GYFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TMP103HYFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0

YFF (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



D: Max = 0.79 mm, Min = 0.73 mm

E: Max = 0.79 mm, Min = 0.73 mm

4207625–2/AK 11/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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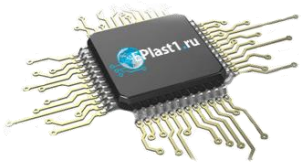
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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