IP4251/52/53/54-TTL

Integrated 4-, 6- and 8-channel passive filter network with ESD protection

Rev. 2 — 5 May 2011 Product data sheet

1. Product profile

1.1 General description

The devices are 4-, 6- and 8-channel RC low-pass filter arrays which are designed to provide filtering of undesired RF signals on the I/O ports of portable communication or computing devices. In addition, the devices incorporate diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±30 kV.

The devices are fabricated using monolithic silicon technology and integrate up to eight resistors and sixteen diodes in a 0.4 mm pitch 8-, 12- or 16-pin ultra-thin leadless Quad Flat No-leads (QFN) plastic package with a height of 0.55 mm only.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- 4-, 6- and 8-channel integrated π-type RC filter network
- ESD protection to ±30 kV contact discharge according to IEC 61000-4-2 far exceeding level 4
- QFN plastic package with 0.4 mm pitch and 0.55 mm height

1.3 Applications

General-purpose ElectroMagnetic Interference (EMI) and Radio-Frequency Interference (RFI) filtering and downstream ESD protection for:

- Cellular phone and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems
- Mobile Internet Devices (MID)
- Portable Media Players (PMP)

nexperia

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IP4251CZ8-4-TTL; IP4251CZ12-6-TTL; IP4251CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz; $V_{bias(DC)}$ = 2.5 V	[1]	-	10	-	pF
$R_{s(ch)}$	channel series resistance			80	100	120	Ω
IP4252CZ8-4-TTL; IP4252CZ12-6-TTL; IP4252CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz; $V_{bias(DC)}$ = 2.5 V	[1]	-	12	-	pF
$R_{s(ch)}$	channel series resistance			32	40	48	Ω
IP4253CZ8-4-TTL; IP4253CZ12-6-TTL; IP4253CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz; $V_{bias(DC)}$ = 2.5 V	[1]	-	30	-	pF
$R_{s(ch)}$	channel series resistance			160	200	240	Ω
IP4254CZ8-4-TTL; IP4254CZ12-6-TTL; IP4254CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz; $V_{bias(DC)}$ = 2.5 V	[1]	-	30	-	pF
$R_{s(ch)}$	channel series resistance			80	100	120	Ω

[1] For the total channel.

2. Pinning information

Table 2. Pinning

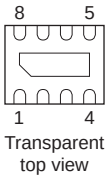
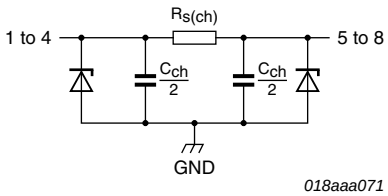
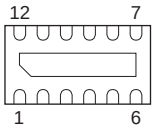
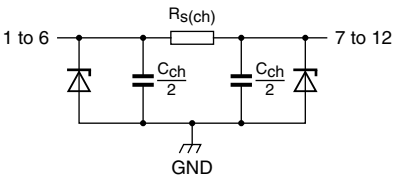
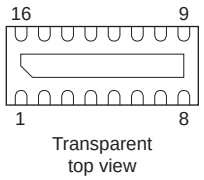
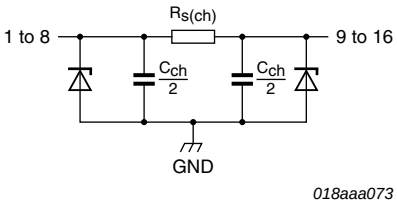
Pin	Description	Simplified outline	Graphic symbol
IP4251CZ8-4-TTL; IP4252CZ8-4-TTL; IP4253CZ8-4-TTL; IP4254CZ8-4-TTL (SOT1166-1)			
1 and 8	filter channel 1	 Transparent top view	 018aaa071
2 and 7	filter channel 2		
3 and 6	filter channel 3		
4 and 5	filter channel 4		
ground pad	ground		
IP4251CZ12-6-TTL; IP4252CZ12-6-TTL; IP4253CZ12-6-TTL; IP4254CZ12-6-TTL (SOT1167-1)			
1 and 12	filter channel 1	 Transparent top view	 018aaa072
2 and 11	filter channel 2		
3 and 10	filter channel 3		
4 and 9	filter channel 4		
5 and 8	filter channel 5		
6 and 7	filter channel 6		
ground pad	ground		

Table 2. Pinning *...continued*

Pin	Description	Simplified outline	Graphic symbol
IP4251CZ16-8-TTL; IP4252CZ16-8-TTL; IP4253CZ16-8-TTL; IP4254CZ16-8-TTL (SOT1168-1)			
1 and 16	filter channel 1		
2 and 15	filter channel 2		
3 and 14	filter channel 3		
4 and 13	filter channel 4		
5 and 12	filter channel 5		
6 and 11	filter channel 6		
7 and 10	filter channel 7		
8 and 9	filter channel 8		
ground pad	ground		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
IP4251CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP4251CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP4251CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1
IP4252CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP4252CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP4252CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1
IP4253CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP4253CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP4253CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1
IP4254CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP4254CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP4254CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
IP4251CZ8-4-TTL; IP4251CZ12-6-TTL; IP4251CZ16-8-TTL						
V_{ESD}	electrostatic discharge voltage	all pins to ground; contact discharge	[1]	-	±15	kV
IP4252CZ8-4-TTL; IP4252CZ12-6-TTL; IP4252CZ16-8-TTL						
V_{ESD}	electrostatic discharge voltage	all pins to ground; contact discharge	[1]	-	±15	kV
IP4253CZ8-4-TTL; IP4253CZ12-6-TTL; IP4253CZ16-8-TTL						
V_{ESD}	electrostatic discharge voltage	all pins to ground	[2]			
		contact discharge		-	±30	kV
		air discharge		-	±30	kV
IP4254CZ8-4-TTL; IP4254CZ12-6-TTL; IP4254CZ16-8-TTL						
V_{ESD}	electrostatic discharge voltage	all pins to ground	[2]			
		contact discharge		-	±30	kV
		air discharge		-	±30	kV
Per device						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all pins to ground				
		contact discharge		-	±8	kV
		air discharge		-	±15	kV
V_{CC}	supply voltage			−0.5	+5.6	V
P_{ch}	channel power dissipation	T_{amb} = 85 °C		-	60	mW
P_{tot}	total power dissipation	T_{amb} = 85 °C		-	200	mW
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

[1] Device tested with 1000 pulses of ±15 kV contact discharges, according to the IEC 61000-4-2 model, far exceeding IEC 61000-4-2 level 4 (8 kV contact discharge).

[2] Device tested with 1000 pulses of ±30 kV contact discharges, according to the IEC 61000-4-2 model, far exceeding IEC 61000-4-2 level 4 (8 kV contact discharge).

5. Characteristics

Table 5. Channel characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IP4251CZ8-4-TTL; IP4251CZ12-6-TTL; IP4251CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz	[1]				
		$V_{bias(DC)}$ = 2.5 V		-	10	-	pF
		$V_{bias(DC)}$ = 0 V	[2]	-	15	-	pF
$R_{s(ch)}$	channel series resistance			80	100	120	Ω
IP4252CZ8-4-TTL; IP4252CZ12-6-TTL; IP4252CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz	[1]				
		$V_{bias(DC)}$ = 2.5 V		-	12	-	pF
		$V_{bias(DC)}$ = 0 V	[2]	-	18	-	pF
$R_{s(ch)}$	channel series resistance			32	40	48	Ω
IP4253CZ8-4-TTL; IP4253CZ12-6-TTL; IP4253CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz	[1]				
		$V_{bias(DC)}$ = 2.5 V		-	30	-	pF
		$V_{bias(DC)}$ = 0 V	[2]	-	45	-	pF
$R_{s(ch)}$	channel series resistance			160	200	240	Ω
IP4254CZ8-4-TTL; IP4254CZ12-6-TTL; IP4254CZ16-8-TTL							
C_{ch}	channel capacitance	f = 100 kHz	[1]				
		$V_{bias(DC)}$ = 2.5 V		-	30	-	pF
		$V_{bias(DC)}$ = 0 V	[2]	-	45	-	pF
$R_{s(ch)}$	channel series resistance			80	100	120	Ω
Per device							
I_{LR}	reverse leakage current	per channel; V_I = 3.5 V		-	-	0.1	μA
V_{BR}	breakdown voltage	positive clamp; I_I = 1 mA		5.8	-	9	V
V_F	forward voltage	negative clamp; I_F = 1 mA		0.4	-	1.5	V

[1] For the total channel.

[2] Guaranteed by design.

Table 6. Frequency characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP4251CZ8-4-TTL; IP4251CZ12-6-TTL; IP4251CZ16-8-TTL						
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 3 GHz	-	16	-	dB
		f = 1 GHz	-	20	-	dB
α_{ct}	crosstalk attenuation	R_{source} = 50 Ω; R_L = 50 Ω; 800 MHz < f < 3 GHz	-	30	-	dB
IP4252CZ8-4-TTL; IP4252CZ12-6-TTL; IP4252CZ16-8-TTL						
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 3 GHz	-	12	-	dB
		f = 1 GHz	-	14	-	dB
α_{ct}	crosstalk attenuation	R_{source} = 50 Ω; R_L = 50 Ω; 800 MHz < f < 3 GHz	-	40	-	dB
IP4253CZ8-4-TTL; IP4253CZ12-6-TTL; IP4253CZ16-8-TTL						
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 3 GHz	-	33	-	dB
		f = 1 GHz	35	-	-	dB
α_{ct}	crosstalk attenuation	R_{source} = 50 Ω; R_L = 50 Ω; 800 MHz < f < 3 GHz	-	30	-	dB
IP4254CZ8-4-TTL; IP4254CZ12-6-TTL; IP4254CZ16-8-TTL						
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 3 GHz	-	28	-	dB
		f = 1 GHz	30	-	-	dB
α_{ct}	crosstalk attenuation	R_{source} = 50 Ω; R_L = 50 Ω; 800 MHz < f < 3 GHz	-	30	-	dB

6. Application information

6.1 Insertion loss

The devices are designed as EMI/RFI filters for multichannel interfaces.

The block schematic for measuring insertion loss in a 50 Ω system is shown in Figure 1. Typical measurements results are shown in Figure 2 to Figure 6 for the different devices.

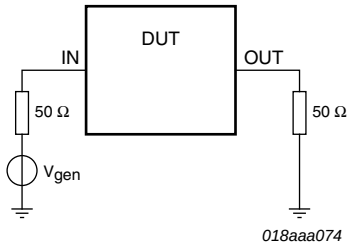
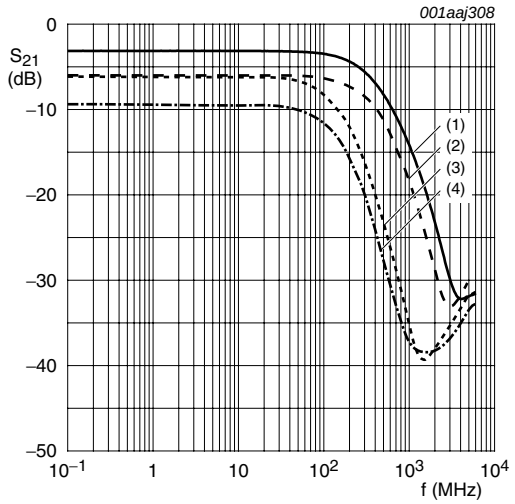
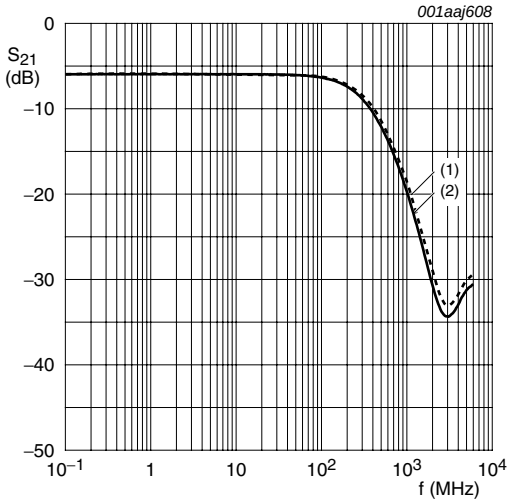


Fig 1. Frequency response setup



(1) IP4252CZ16-8-TTL - channel 1 to channel 16
(2) IP4251CZ16-8-TTL - channel 1 to channel 16
(3) IP4254CZ16-8-TTL - channel 1 to channel 16
(4) IP4253CZ16-8-TTL - channel 1 to channel 16

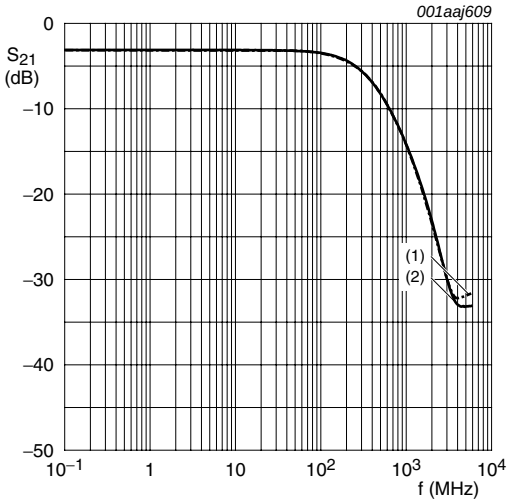
Fig 2. Frequency response curves overview



(1) Channel 1 to channel 16

(2) Channel 4 to channel 13

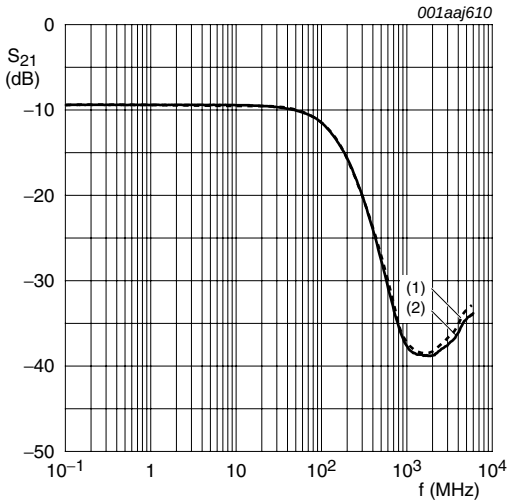
Fig 3. IP4251CZ16-8-TTL: frequency response curves



(1) Channel 1 to channel 16

(2) Channel 4 to channel 13

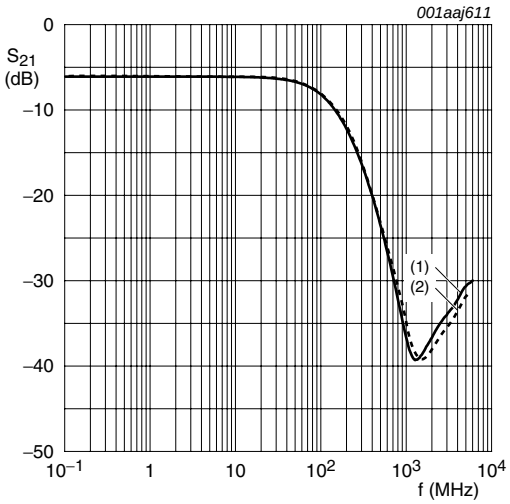
Fig 4. IP4252CZ16-8-TTL: frequency response curves



(1) Channel 1 to channel 16

(2) Channel 4 to channel 13

Fig 5. IP4253CZ16-8-TTL: frequency response curves



(1) Channel 4 to channel 13

(2) Channel 1 to channel 16

Fig 6. IP4254CZ16-8-TTL: frequency response curves

Due to the optimized silicon dice and package design, all channels in a single package show a very good matching performance as the insertion loss for a channel at the package side (e.g. channel 1 to channel 16) is nearly identical with the center channels (e.g. channel 4 to channel 13).

6.2 Selection

The selection of one of the filter devices has to be performed depending on the maximum clock frequency, driver strength, capacitive load of the sink, and also the maximum applicable rise and fall times.

6.2.1 SDHC and MMC memory interface

The Secure Digital High Capacity (SDHC) memory card interface standard specification and the Multi Media Card (MMC) (JESD 84A43) standard specification recommend a rise and fall time of 25 % to 62.5 % (62.5 % to 25 % respectively) of 3 ns or less for the input signal of the receiving interface side.

Assuming a typical capacitance of about 20 pF for the SDHC memory card itself, and approximately 4 pF to 7 pF for the Printed-Circuit Board (PCB) and the card holder, IP4252CZ12-6-TTL (6 channels, $R_{s(ch)}$ = 40 Ω, C_{ch} = 12 pF at $V_{bias(DC)}$ = 2.5 V) is a matching selection to filter and protect all relevant interface pins such as CLK, CMD, and DAT0 to DAT3/CD. Please refer to Figure 7 for a general example of the implementation of the device in an SDHC card interface.

In case additional channels such as write-protect or a mechanical card-detection switch are used, the IP4252CZ16-8-TTL (8 channels, $R_{s(ch)}$ = 40 Ω, C_{ch} = 12 pF at $V_{bias(DC)}$ = 2.5 V) offers two additional channels.

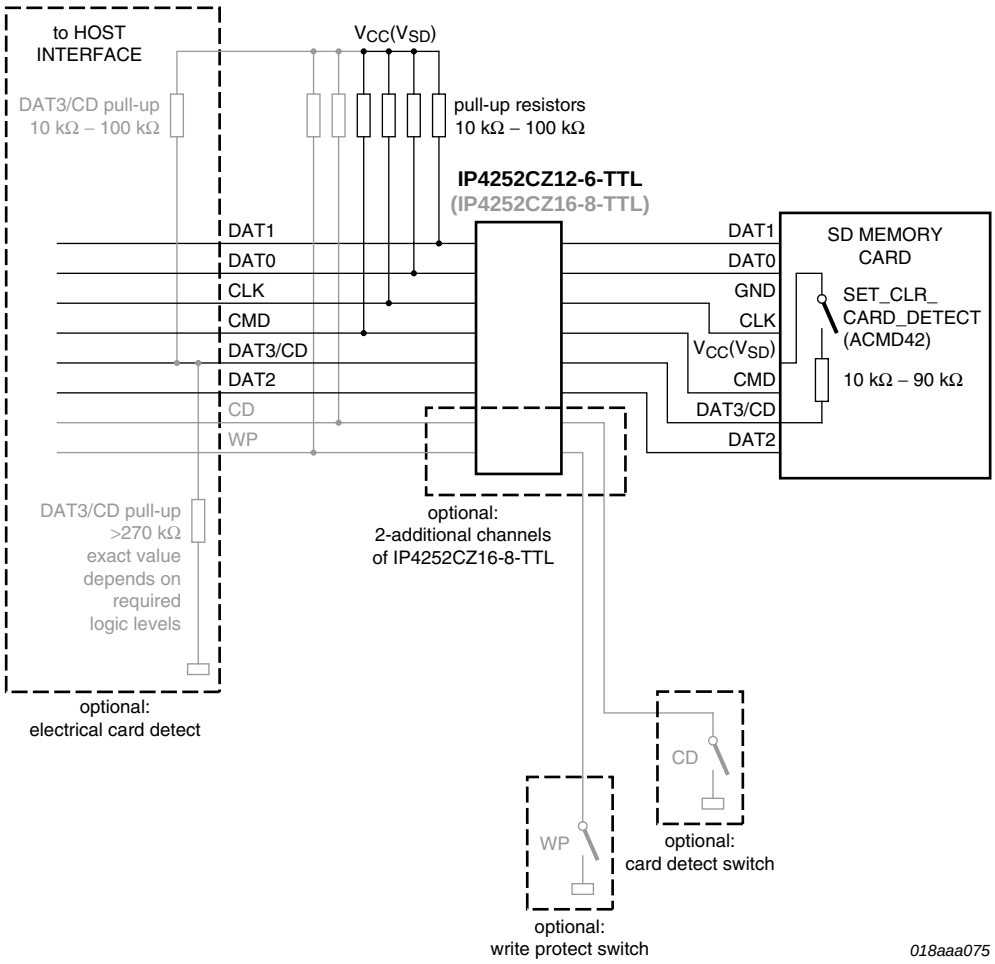


Fig 7. Example of IP4252 in an SDHC card interface

The capacitance values specified for the signal channels of the MMC interface differ from the SDHC specification. The MMC card-side interface is specified to have an intrinsic capacitance of 12 pF to 18 pF and the total channel is limited according to the specification to 30 pF only. Therefore, any filter device capacitance is limited to a maximum of up to 18 pF, including the card holder and PCB traces.

Please refer to Figure 8 for a general example of the implementation of the IP4252 in an MMC interface application.

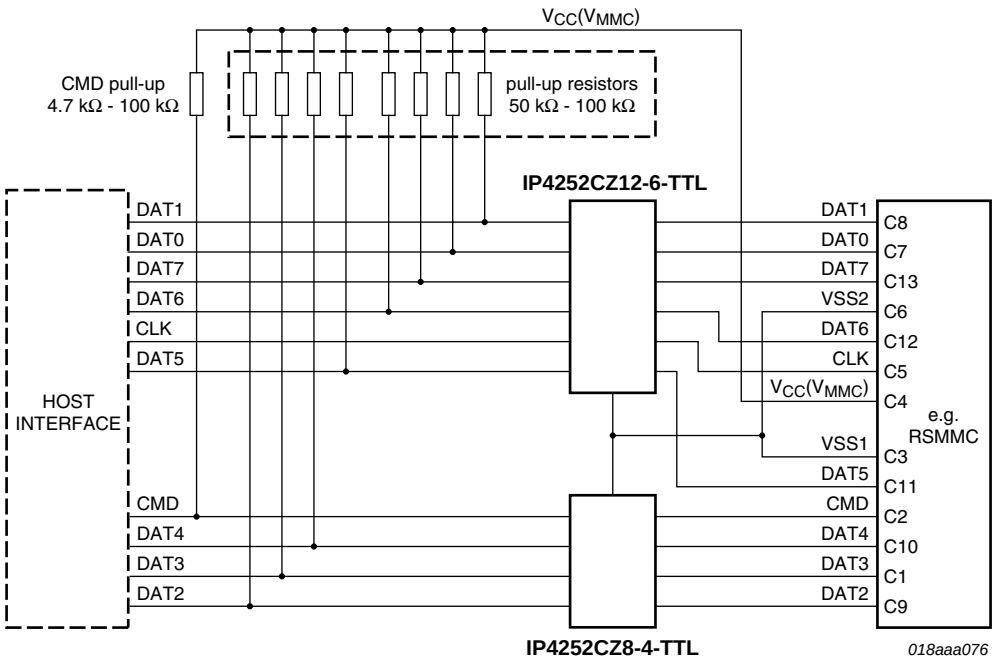


Fig 8. Example of IP4252 in an MMC interface

To generate SDHC and MMC-compliant digital signals, the driver strength should not significantly undercut 8 mA.

6.2.2 LCD interfaces, medium-speed interfaces

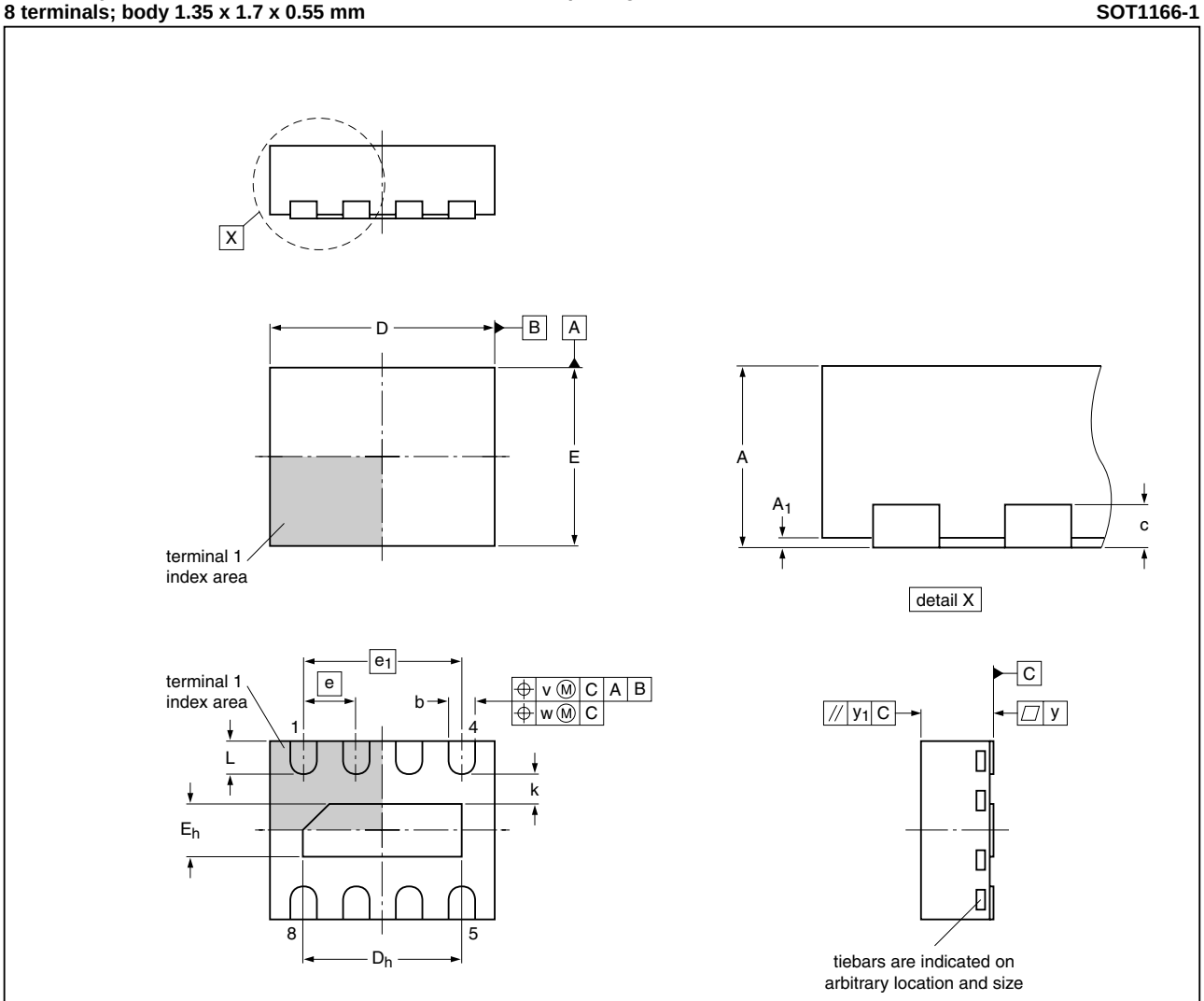
For digital interfaces such as LCD interfaces running at clock speeds between 10 MHz and 25 MHz or more, IP4251, IP4252 or IP4254 can be used depending on the sink load, clock speed, driver strength and rise and fall time requirements. Also the minimum EMI filter requirements may be a decision-making factor.

6.2.3 Keypad, low-speed interfaces

Especially for lower-speed interfaces such as keypads, low-speed serial interfaces (e.g. Recommended Standard (RS) 232) and low-speed control signals, IP4253 ($R_{s(ch)}$ = 200 Ω, C_{ch} = 30 pF at $V_{bias(DC)}$ = 2.5 V) offers a very robust ESD protection and strong suppression of unwanted frequencies (EMI filtering).

7. Package outline

HUSON8: plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 x 1.7 x 0.55 mm **SOT1166-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	0.55	0.05	0.25		1.8	1.3	1.45	0.45				0.30				
	nom			0.20	0.127	1.7	1.2	1.35	0.40	0.4	1.2		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		1.6	1.1	1.25	0.35			0.2	0.20				

Note

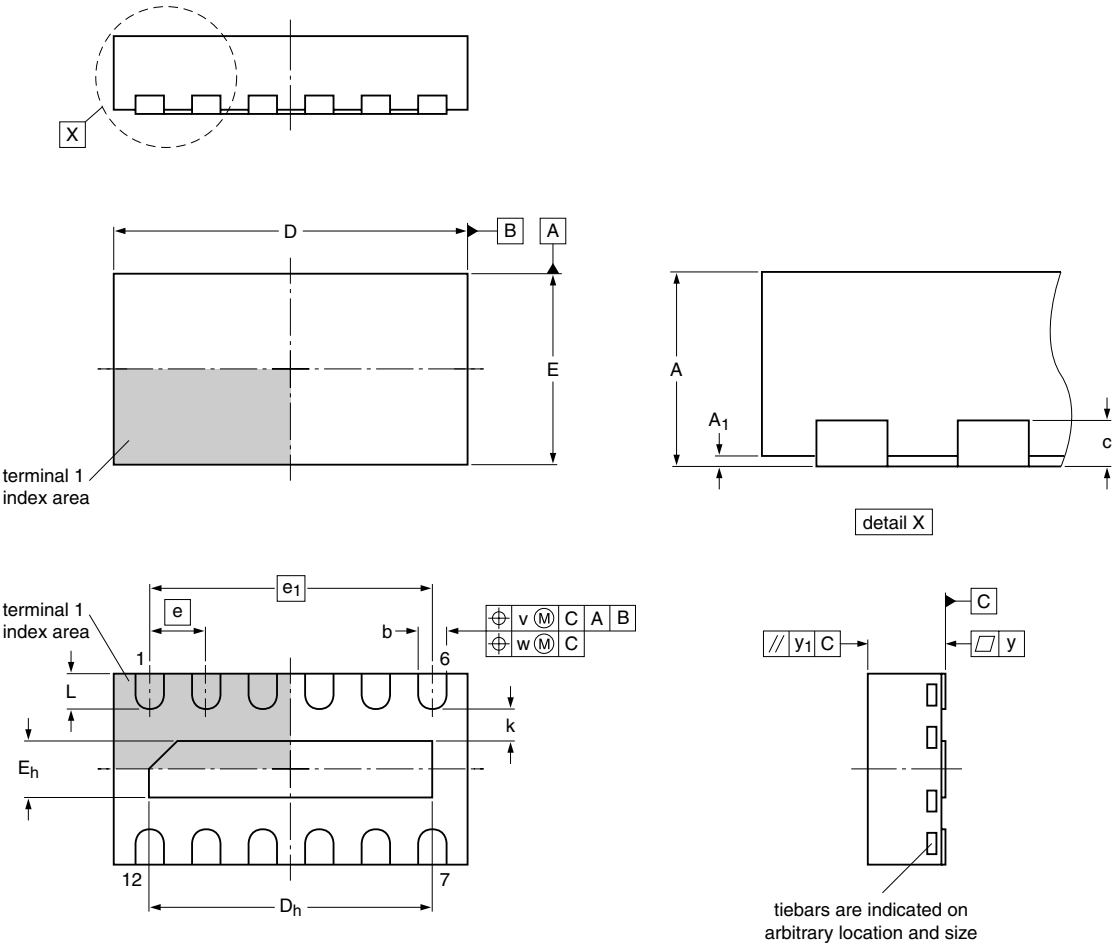
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1166-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1166-1	- - -	- - -	- - -		~~10-03-18~~ 10-03-22

Fig 9. Package outline SOT1166-1 (HUSON8)

HUSON12: plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 x 2.5 x 0.55 mm **SOT1167-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	0.55	0.05	0.25		2.6	2.1	1.45	0.45				0.30				
	nom			0.20	0.127	2.5	2.0	1.35	0.40	0.4	2.0		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		2.4	1.9	1.25	0.35			0.2	0.20				

Note

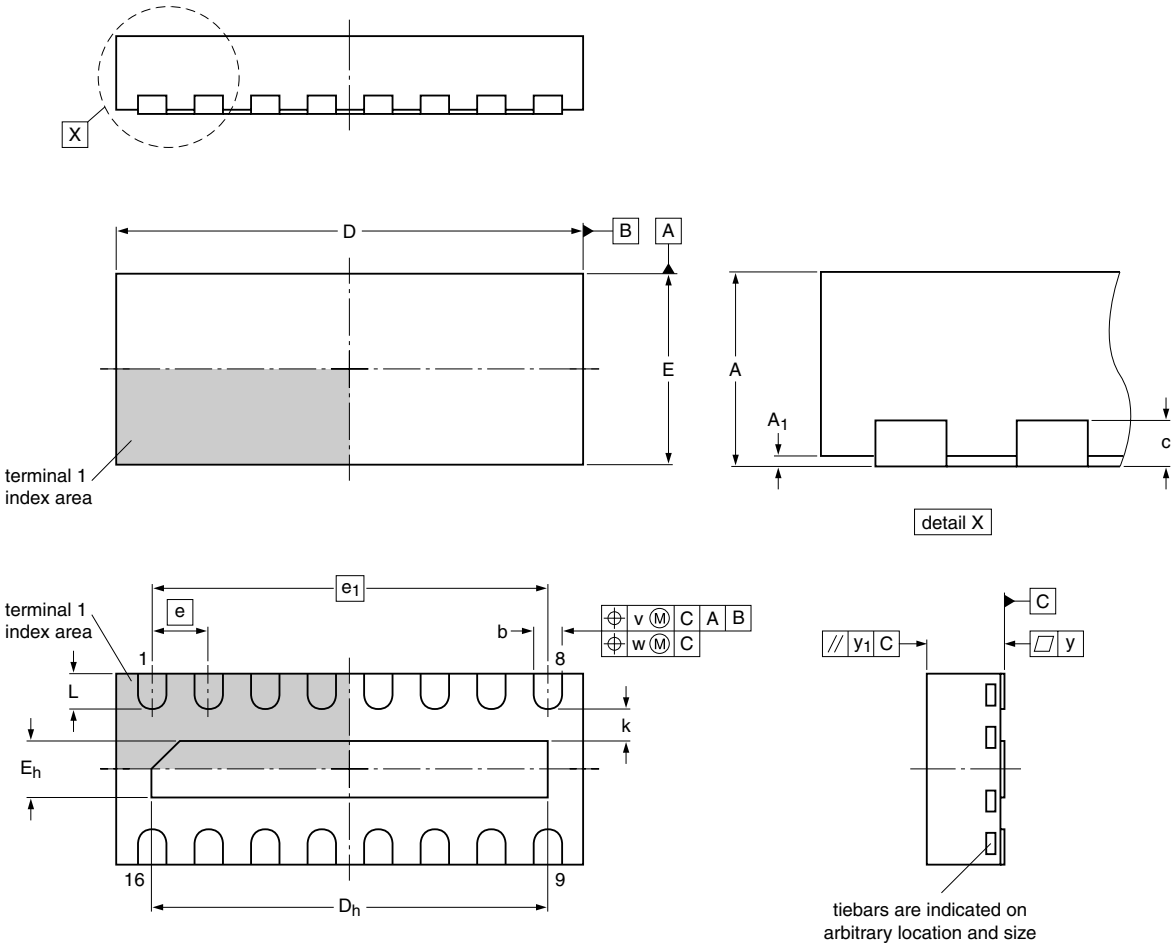
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1167-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1167-1	- - -	- - -	- - -		~~10-03-18~~ 10-03-22

Fig 10. Package outline SOT1167-1 (HUSON12)

HUSON16: plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 x 3.3 x 0.55 mm **SOT1168-1**



Dimensions

Unit[1]		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	0.55	0.05	0.25		3.4	2.9	1.45	0.45				0.30				
mm	nom			0.20	0.127	3.3	2.8	1.35	0.40	0.4	2.8		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		3.2	2.7	1.25	0.35			0.2	0.20				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1168-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1168-1	- - -	- - -	- - -			~~10-03-18~~ 10-03-22

Fig 11. Package outline SOT1168-1 (HUSON16)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4251_52_53_54-TTL v.2	20110505	Product data sheet	-	IP4251_52_53_54-TTL v.1
Modifications:	• Section 1 “Product profile”: updated. • Table 2 “Pinning”: updated. • Deleted section “Thermal characteristics”.			
IP4251_52_53_54-TTL v.1	20110131	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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Date of release: 05 May 2011

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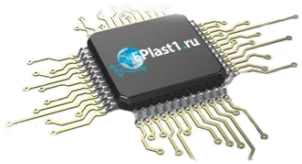

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