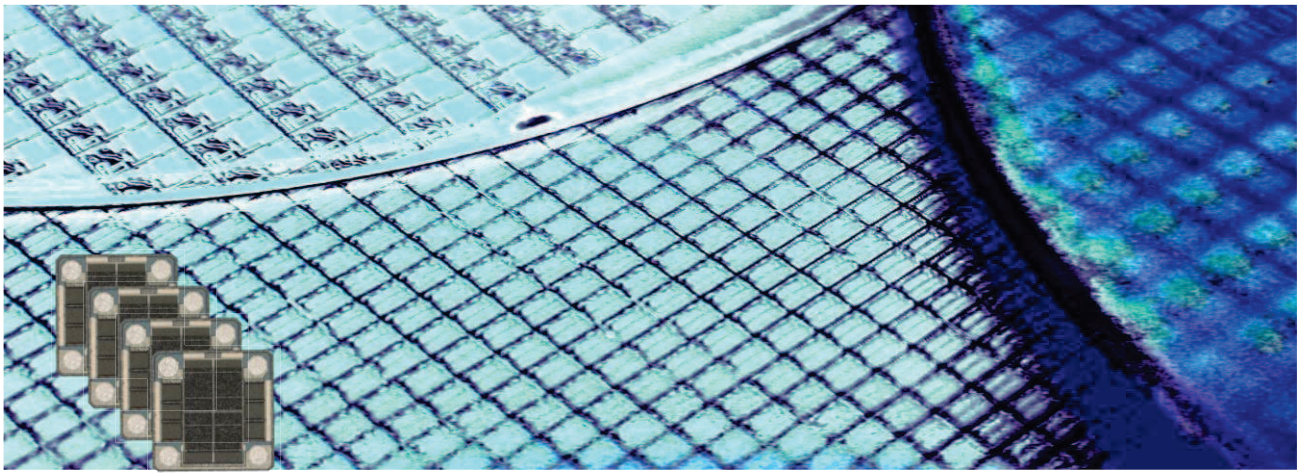
EMSC – Embedded & Wirebond Silicon Capacitor

Rev 3.5



Key features

- **Ultra low profile (100µm)**
- **Ultra high stability of capacitance value:**
  - **Temperature ±0,5% (-55°C to +150°C)**
  - **Voltage <0.1%/Volts**
  - **Negligible capacitance loss through ageing**
- **Low leakage current down to 100pA**
- **High reliability**
- **High operating temperature (up to 150°C)**

Key applications

- **Any demanding applications, such as medical, aerospace, automotive industrial…**
- **Supply decoupling / filtering of active device**
- **High reliability applications**
- **Devices with battery operations**
- **High temperature applications**
- **Volume limited applications**

Thanks to the unique IPDiA Silicon capacitor technology, most of the problems encountered in demanding applications can be solved.

EMbedded **S**ilicon **C**apacitors are available with **thicknesses down to 80µm** and are the most appropriate solution for Chip On Board, Chip On Foil, Chip On Glass, Chip On Ceramic, flip chip and embedded applications, when designers are looking at **utmost decoupling behaviours.**

EMSC are optimized for laminate substrate package, rigid/flex PCB, FR4, ceramic, glass, leadframe or foil platforms.

The Silicon capacitor technology offers a capacitor integration capability (up to 250nF/mm^2) which allows **downsizing** compared to existing solutions.

The IPDiA technology features **high reliability**, up to 10 times better than alternative capacitor technologies, such as Tantalum or MLCC, and eliminates cracking phenomena.

Silicon Capacitor technology also offers a very stable capacitor value over the full operating voltage & temperature range, with a high and stable insulation resistance.

This Silicon based technology is ROHS compliant and compatible with lead free reflow soldering process.

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Electrical Specification

Unit	Capacitance value						
	10	15	22	33	39	47	68
10pF	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	390pF/0202/30V 935 121 72C 339	470pF/0202/30V 935 121 72C 347	680pF/0202/30V 935 121 72C 368
0.1nF	1nF/0202/30V 935 121 72C 410	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
1nF	10nF/0202/30V 935 121 72C 510	*Contact IPDIA Sales*	*Contact IPDIA Sales*	33nF/0404/30V 935 121 72F 533	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
10nF	100nF/0404/11V 935 121 42F 610 100nF/0605/30V 935 121 72G 610	*Contact IPDIA Sales*	220nF/0505/11V 935 121 42H 622	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
0.1µF	1µF/1208/11V 935 121 42S 710 1µF/1616/30V 935 121 72Y 710	*Contact IPDIA Sales*	2.2µF/1612/11V 935 121 42V 722	3.3µF/1616/11V 935 121 42Y 733	*Contact IPDIA Sales*	4.7µF/2016/11V 935 121 42X 747	

(*) 80µm thickness on request

(**) For extended temperature range (up to +250°C), see Embedded Xtreme Temperature Silicon Capacitor product (EXSC).

(***) other values on request

Parameters	Value
Capacitance range	*390pF to 4.7µF*
Capacitance tolerances	*±15%(***)*
Operating temperature range	*-55 to 150 °C (**)*
Storage temperatures	*- 70 to 165 °C*
Temperature coefficient	*±0.5%, from -55 to +150°C*
Breakdown Voltage (BV)	*30V, 11V*
Capacitance variation versus RVDC	*0.1 % /V (from 0 V to RVDC)*
Equivalent Serial Inductor (ESL)	*Max 100 pH*
Equivalent Serial Resistor (ESR)	*Max 0.1Ω*
Insulation resistance	*100GΩ min @ 3V,25°C*
Aging	*Negligible, < 0.001% / 10000h*
Reliability	*FIT<0.017 parts / billions hours*
Capacitor height	*Max 100µm (*)*

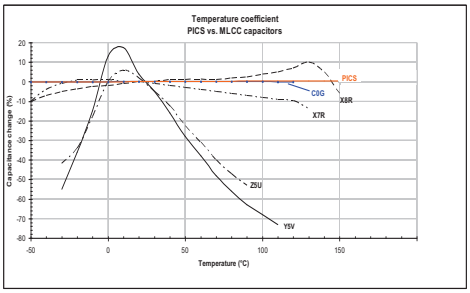


Fig.1 Capacitance change versus temperature variation compared to alternative technologies

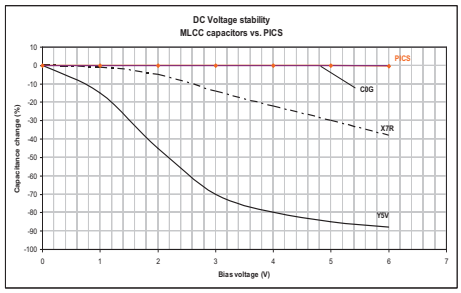


Fig.2 Capacitance change versus voltage variation compared to alternative

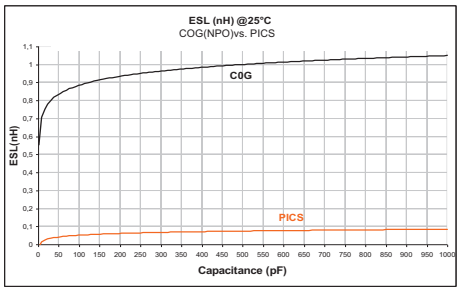


Fig.3 ESL versus capacitance value compared to alternative technologies

Part Number

935.121. **B.** **2.** **S.** **U** **xx** → **Value**

i.e: 100nF/0404 → 935 121 42F 610

Breakdown Voltage
4 = 11V
1= 20V
7= 30V
6= 50V

Size
F = 0404
H = 0505
I = 0302
S =1208
V =1216
G = 0605
C = 0202
V = 1612
Y = 1616
X =2016

Unit
0 = 10 f
1 = 0.1 p
2 = 1 p
3 = 10 p
4 = 0.1 n
5 = 1 n
6 = 10 n
7 = 0.1 µ
8 = 1 µ
9 = 10 µ

Value
10
15
22
33
39
47
68

Termination

Pad finishing in Aluminum (3µm thickness +/-10%), other finishing available such as copper, nickel or gold. Applicable for almost all embedded applications.
Parts should be glued with non conductive paste. If conductive glue is used on the backside of the silicon cap, it is strongly recommended to connect the backside and pads 3&4 to the same level (GND preferred).

Pinning definition & Outline

pin #	Symbol	Description
1, 2	Signal	Signal
3, 4	GND	Ground

Typ.		0202	0203	0303	0404	0505	0605	1208	1612	1616	2016
Comp. size	A	0.58 ±0.05	0.64 ±0.05	0.80 ±0.05	1.00 ±0.05	1.25 ±0.05	1.50 ±0.05	3.00 ±0.05	4.00 ±0.05	4.00 ±0.05	5.00 ±0.05
	B	0.58 ±0.05	0.80 ±0.05	0.80 ±0.05	1.00 ±0.05	1.25 ±0.05	1.25 ±0.05	2.00 ±0.05	3.00 ±0.05	4.00 ±0.05	4.00 ±0.05
	c	0,15	0,15	0,15	0,15	0,15	0,15	0,15	0,15	0,15	0,15
	d	0,3			0,72	0,97	1,22	2,72	3,72	3,72	4,72
	e	0,3			0,72	0,97	1,22	1,72	2,72	3,72	3,72

Packaging

Tape and reel, tray, waffle pack or wafer delivery.

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IPD Capacitor Assembly Set Up

Rev 1.0

Application Note

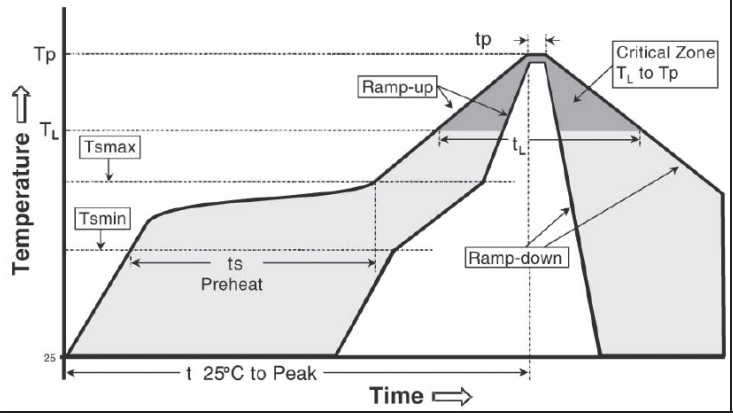
Outline

Silicon Capacitor for surface mounting device (SMD) assembly is a Wafer Level Chip Scale Packaging with the following features:

- Package dedicated to solve tombstoning effect of small SMD package;
- Package compatible with SMD assembly;
- Package without underfilling step;
- Interconnect available with various optional finishing for specific assembly.

Assembly consideration

- Standard pick & place equipment dedicated to WLCSP down to 400µm pitch.
- Solder paste type 3 in most cases of EIA size.
- Reflow has to be done with standard lead-free profile (for SAC alloys) or according to JEDEC recommendations J-STD 020D-01.



	Lead	Leadfree
	Tp: 235 °C	Tp: 260 °C
	TL: 183 °C	TL: 217 °C
	Ts min: 100 °C	Ts min: 150 °C
	Ts max: 150 °C	Ts max: 200 °C
	tL: 60-150 s	tL: 60-150 s

Process recommendation

After soldering, no solder paste should touch the side of the capacitor die as that might results in leakage currents due to remaining flux.

In order to use IPDiA standard capacitors within the JEDEC format and recommendation, the solder flux must be cleaned after reflow soldering step.
Notes: for a proper flux cleaning process, “rosin” flux type (R) or “water soluble” flux type (WS) is recommended for the solder printing material. “No clean” flux (NC) solder paste is not recommended.

In case the flux is not cleaned after the reflow soldering, the standard JEDEC would probably not be appropriate and the solder volume must be controlled:

- using smallest aperture design for the stencil, and using finer solder paste type 4 or 5 for a proper printing process.
- Mirroring pads would be the best recommendation

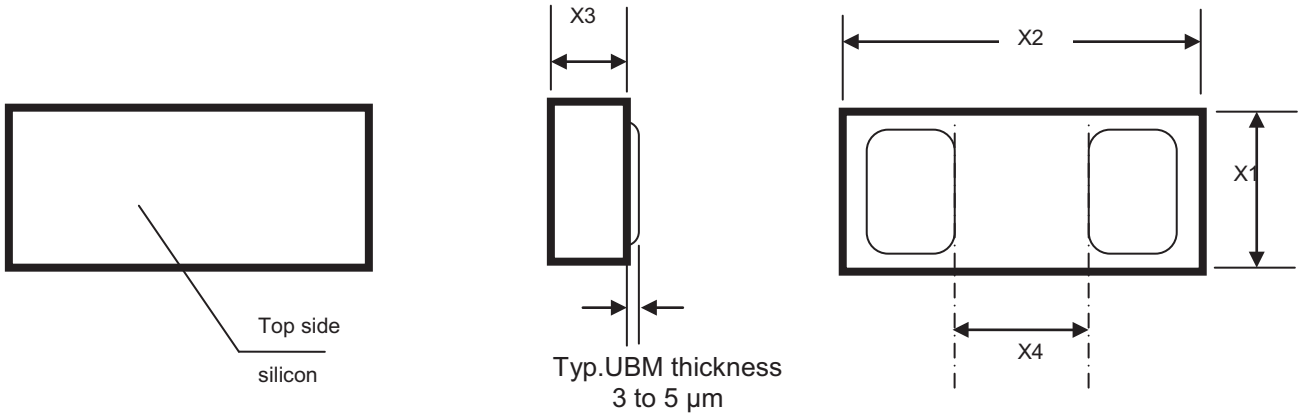
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Pad recommendation

The capacitor is compatible with generic requirements for flip chip design (IPC7094).
Standard IPDiA 3D package can be compliant with established EIA size (0201, 0402, 0603, …).

Die size and land pattern dimensions is set up according to following range :

EIA size	0201	0402	0603	0805	1206	1812
Dimension max(X1 x X2) mm	0.86x0.66	1.26x0.76	1.86x1.16	2.26x1.46	3.46x1.86	4.76x3.66
Typical . die thickness X3 (mm)	0.1 or 0.4					
Typical pad size* (mm)	0.15x0.40	0.30x0.50	0.40x0.90	0.50x1.20	0.60x1.60	0.90x3.40
Typical pad separation (X4 mm)	0.3	0.4	0.8	1	2	2.7



After soldering, no solder paste should touch the side of the capacitor die as that might result in leakage currents due to remaining flux.

Manual Handling Considerations

These capacitors are designed to be mounted with a standard SMT line, using solder printing step, pick and place machine and a final reflow soldering step. In case of manual handling and mounting conditions, please follow below recommendations:

- Minimize mechanical pressure on the capacitors (use of a vacuum nozzle is recommended).
- Use of organic tip instead of metal tip for the nozzle.
- Minimize temperature shocks (Substrate pre-heating is recommended).
- No wire bonding on 0402 47nF, 0402 100nF, 1206 1µF and 1812 3,3µF

Process steps:

- On substrate, form the solder meniscus on each land pattern targeting 100 µm height after reflow (screen printing, dispensing solder paste or by wire soldering).
- Pick the capacitor from the tape & reel or the Gel Pack keeping backside visible using a vacuum nozzle and organic tip.
- Temporary place the capacitor on land pattern assuming the solder paste (Flux) will stick and maintain the capacitor.
- Reflow the assembly module with a dedicated thermal profile (see reflow recommendation profile).

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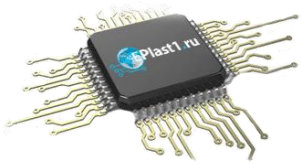
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