



N-Channel Reduced Q_g, Fast Switching MOSFET

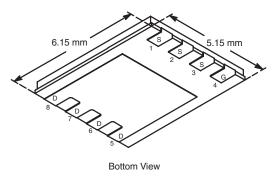
PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	
30	0.0185 at V _{GS} = 10 V	15	
	$0.030 \text{ at V}_{GS} = 4.5 \text{ V}$	12	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFETs
- High-Efficient PWM Optimized
- 100 % R_g and UIS Tested

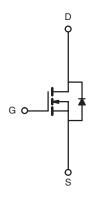






Ordering Information: Si7652DP-T1-E3 (Lead (Pb)-free)

Si7652DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise n	noted ^a		
Parameter		Symbol	Limits	Unit	
Drain-Source Voltage		V _{DS}	30		
Gate-Source Voltage		V_{GS}	± 25		
Out in the County (T. 150.00)	T _C = 25 °C	1	15		
Continuous Drain Current (T _J = 150 °C) ^a	T _C = 70 °C	- I _D	12		
Pulsed Drain Current		I _{DM}	40	А	
Continuous Source Current (Diode Conduction) ^a		I _S	3.2		
Single-Pulse Avalanche Current	L = 0.1 mH	I _{AS}	15		
Avalanche Energy	L = 0.1 IIII	E _{AS}	11.25	mJ	
	T _A = 25 °C	P _D	3.9	W	
Maximum Power Dissipation ^a	T _A = 70 °C	гD	2.5	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	ာင	
Soldering Recommendations (Peak Temperature) ^{c, d}			260		

THERMAL RESISTANCE RATINGS ^a					
Parameter		Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b}	R _{thJA}	24	32	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	7	9		

Notes

- a. Surface Mounted on 1" x 1" FR4 board, $t \le 10$ s.
- b. Maximum under steady state condition is 75 °C/W.
- c. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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MOSFET SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.8		1.8	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	1 5 μA	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	В	V _{GS} = 10 V, I _D = 9 A		0.0155	0.0158	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$		0.023	0.030		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 9 A		16		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			8.7	13		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 5.0 \text{ V}, I_D = 9 \text{ A}$		1.5		nC	
Gate-Drain Charge	Q_{gd}			3.5			
Gate Resistance	R_g		0.5	1.4	2.2	Ω	
Turn-On Delay Time	t _{d(on)}			7	15		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		32	50	ns	
Fall Time	t _f			14	25		
Source-Drain Reverse Recovery Time	t _{rr}	$I_F = 2.3 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$		30	60		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board, $t \le 10$ s Pulse test; pulse width $\le 300 \ \mu s$, duty cycle $\le 2 \ \%$.
- b. Surface Mounted on 1" x 1" FR4 board, t ≤ 10 s Guaranteed by design, not subject to production testing.

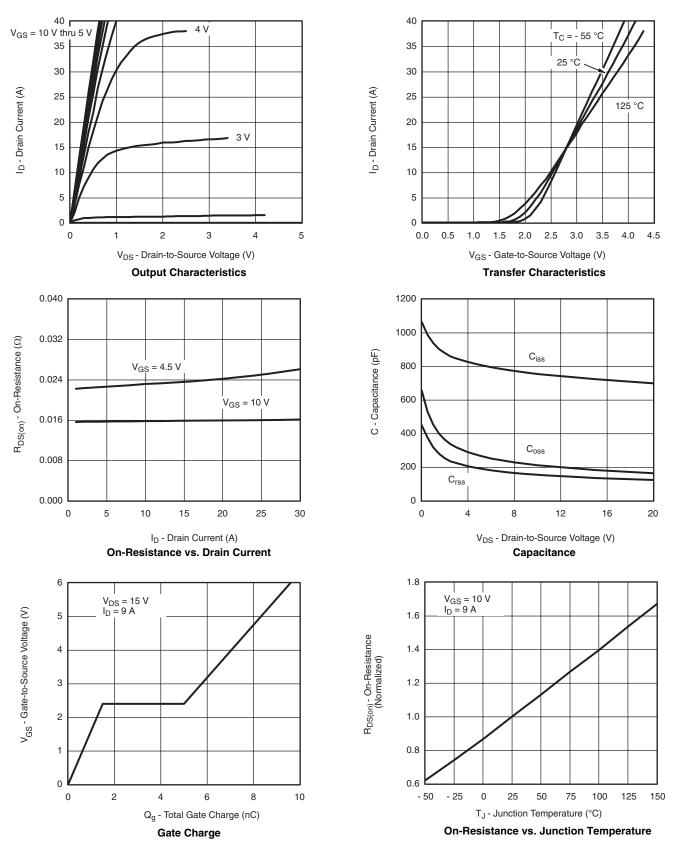
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







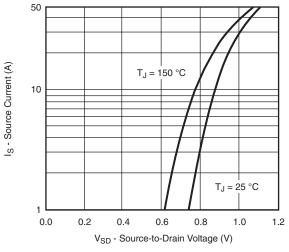
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

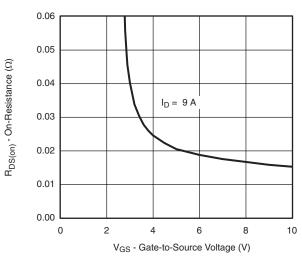


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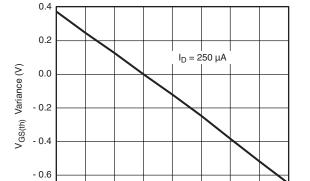
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

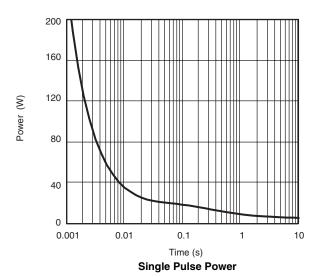




Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage





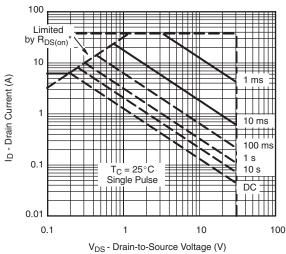
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75

100

125

150



 V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

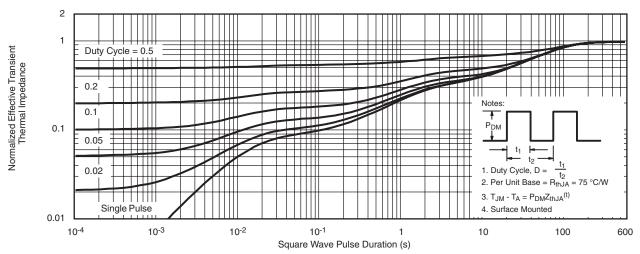
Safe Operating Area, Junction-to-Ambient

- 0.8 L - 50

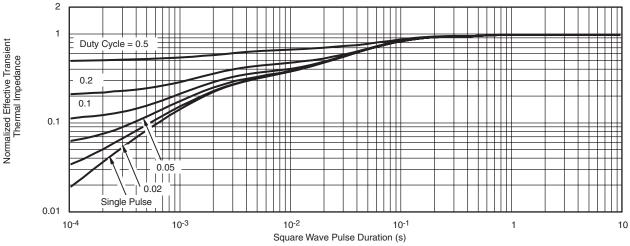
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Care

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73485.



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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