IQS231A/B Datasheet

Single Channel Capacitive Proximity/Touch Controller for SAR applications

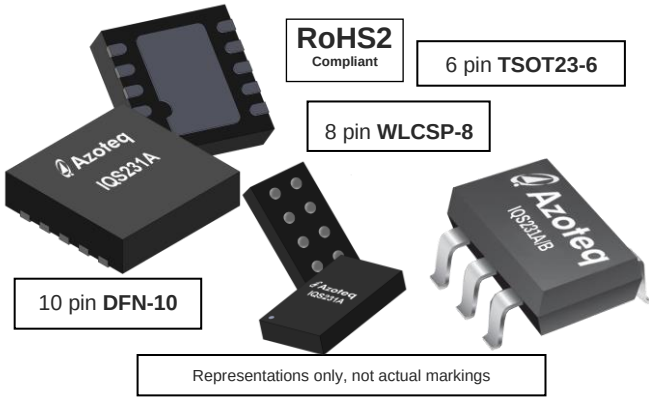
1 Device overview

The IQS231A/B ProxSense® IC is a self-capacitance controller designed for applications where an awake/activate on proximity function is required. The IQS231A/B is an ultra-low power solution that uses unique release and/or movement detection for applications that require long- term detection. The IQS231A/B operates standalone or I2C and features configuration via OTP (One Time Programmable) bits. Switching from I2C to standalone during runtime is also possible in order to access all settings while offering the simplicity of a standalone output.

IQS231B offers alternate hardware with identical firmware to the IQS231A. IQS231B hardware offers improved temperature response and low temperature range.

1.1 Main Features

- Integrated SAR user interface offering a simple GPIO output
- **Quick release detection –** effectively prevent false triggers from remaining
- Quick release **sensitivity options**
- **Wide range of control** for sensing in high power RF environments
- **Pin compatible** with devices of same package type (IQS229 DFN10, all ProxSense TSOT23-6 devices[1],IQS211A WLCSP-8 device)
- **1.8V (-2%) to 3.6V** Input voltage
- Capacitive resolution down to 0.02fF
- Capacitive load capability up to 200pF
- **External threshold adjustment** pin (minimize need for pre-empted OTP adjustments)
- **Minimal external components** (direct input strap)
- Standalone failsafe mode (backwards compatible failsafe output, short pulses on output to indicate operational device)
- **Default** OTP options focus on **safety and passing SAR lab qualification**, OTP changes offer performance advantages
- **I2C interface option** (improved compatibility)



- **Extended controls in I²C mode** (setup in I²C, runtime with standalone output)
- **Optional input for synchronized implementations** (input to instruct IC when to sense)
- **Synchronization output** – failsafe pulses may be used by the master to synchronize on. Sensing is done after each pulse
- **Synchronization input** – Sensing is only done while Sync input is low
- Low power sensing: 30Hz (default), 100Hz, 8Hz, 4Hz (sub 6uA mode)
- **Constant sampling rates during all power modes with rapidly debounced output changes**
- **Advanced temperature & interference compensation** option

[1] Input voltage level and pin functions may differ

1.2 Applications

- SAR sensor
- Integrated hybrid designs (RF and capacitive sensing combined)
- Movement sensing applications (user interaction detection, anti-theft)
- Hold detection for screen activation
- On-ear detection

T_A	DFN10	TSOT23-6	WLCSP-8 (1.5 x 0.9 x 0.4mm)
-20ºC to 85 ºC	**IQS231A**	**IQS231A**	**IQS231A** (NRFND)
-40ºC to 85 ºC		**IQS231B**	**IQS231B**

1.3 Block diagram

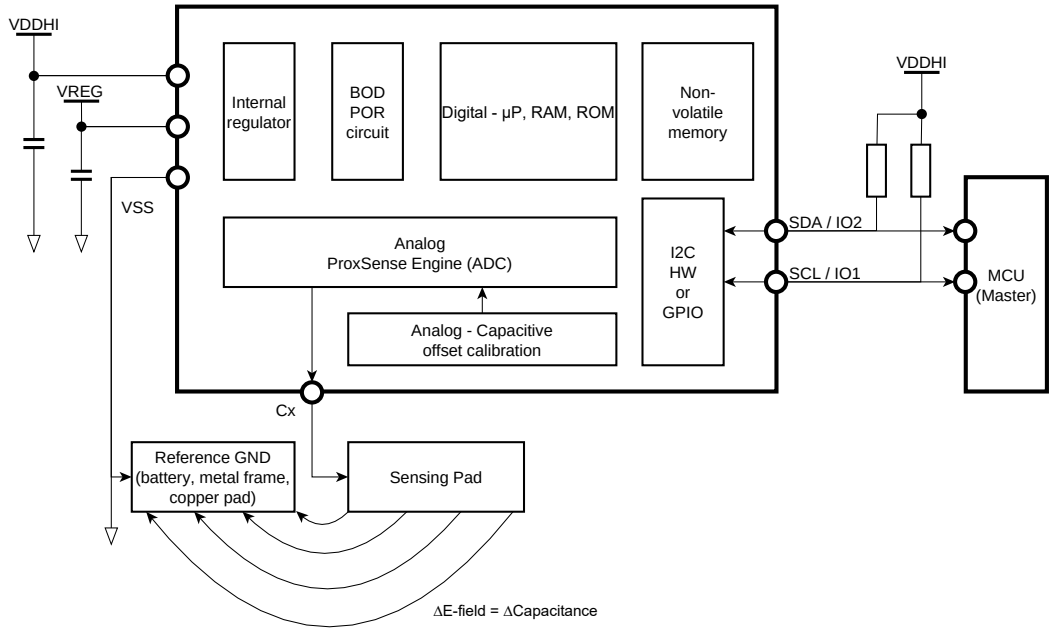


Figure 1.1 Functional block diagram for IQS231A/B

The IQS231A/B supports relative capacitance measurements for detecting capacitance changes.

Basic features of the IQS231A/B include:

- Charge-transfer capacitance measurement technology (Analog ProxSense® Engine)
- Finite state machine to automate detection and environmental compensation without MCU interaction (integrated microprocessor)
- Self-capacitance measurements
- Signal conditioning to provide signal gain (Analog – Capacitive offset calibration)
- Signal conditioning to provide offset compensation for parasitic capacitance (Analog – Capacitive offset calibration)
- Integrated calibration capacitors (Analog – Capacitive offset calibration)
- Integrated timer for timer triggered conversions
- Integrated LDO regulator for increased immunity to power supply noise
- Integrated oscillator
- Processing logic to perform measurement filtering, environmental compensation, threshold detection and movement detection

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2 Packaging and Pin-Out

2.1 TSOT23-6 & DFN10

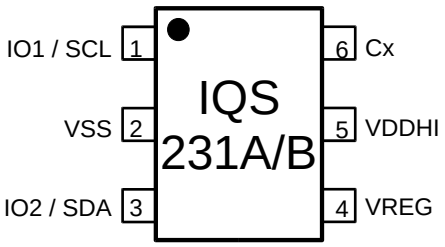


Figure 2.1 IQS231A/B TSOT23-6 pin-out

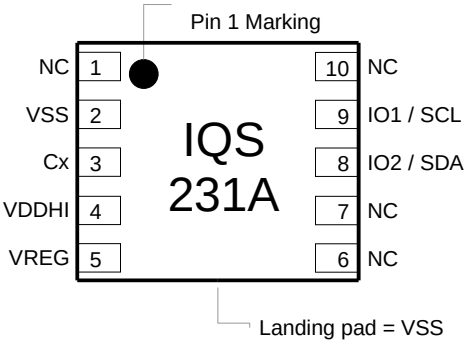


Figure 2.2 IQS231A DFN10 pin-out

Table 2.1 TSOT23-6 Pin-out description

IQS231A/B TSOT23-6			
Pin	**Name**	**Type**	**Function**
1	PRIMARY I/O	Digital Input/Output	Multifunction **IO1** / **SCL** (I^2C Clock signal)
2	VSS	Signal GND	
3	SECONDARY I/O	Digital Input/Output	Multifunction **IO2 / SDA** (I^2C Data output)
4	VREG	Regulator output	Requires external capacitor
5	VDDHI	Supply Input	Supply:1.764V – 3.6V
6	Cx	Sense electrode	Connect to conductive area intended for sensor

Table 2.2 DFN10 Pin-out description

IQS231A DFN10			
Pin	**Name**	**Type**	**Function**
1	NC		
2	VSS	Signal GND	
3	Cx	Sense electrode	Connect to conductive area intended for sensor
4	VDDHI	Supply Input	Supply:1.764V – 3.6V
5	VREG	Regulator output	Requires external capacitor
6	NC		
7	NC		
8	SECONDARY I/O	Digital Input/Output	Multifunction **IO2 / SDA** (I^2C Data output)
9	PRIMARY I/O	Digital Input/Output	Multifunction **IO1** / **SCL** (I^2C Clock signal)
10	NC		

Table 2.3 Multifunction pin descriptions

Multifunction pin name	Multifunction pin option	Output type
IO1	Proximity output / Proximity output with heartbeat	Open-drain[2]
IO2	Sensitivity input / Synchronization input / Movement output / Touch output	Open-drain[2]

2.2 WLCSP

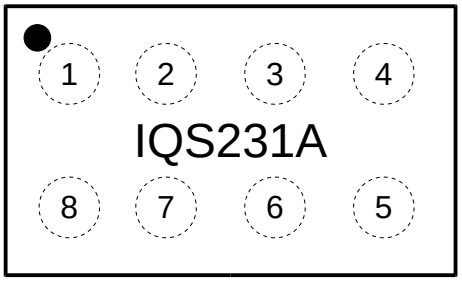


Figure 2.2 IQS231A 8-pin WLCSP (top view)

Table 2.2 8-pin WLCSP Pin-out description

IQS231A 8-pin WLCSP			
Pin	**Name**	**Type**	**Function**
1	Cx	Sense electrode	Connect to conductive area intended for sensor
2	PRIMARY I/O	Digital Input/Output	Multifunction **IO1** / **SCL** (I^2C Clock signal)
3	VREG	Regulator output	Requires external capacitor
4	VSS	Signal GND	
5	FLOATING IO	Digital Input/Output	Not used. Floating input during runtime. Recommended: Connect to GND
6	SECONDARY I/O	Digital Input/Output	Multifunction **IO2 / SDA** (I^2C Data output)
7	VDDHI	Supply Input	Supply:1.764V – 3.6V
8	PGM	Configuration pin	Connection for OTP programming. Floating input during runtime. Recommended: Connect to GND. Connect separate pad/pin for in-circuit programming (separate modules only)

[2] Requires pull-up resistor

3 Reference Schematics:

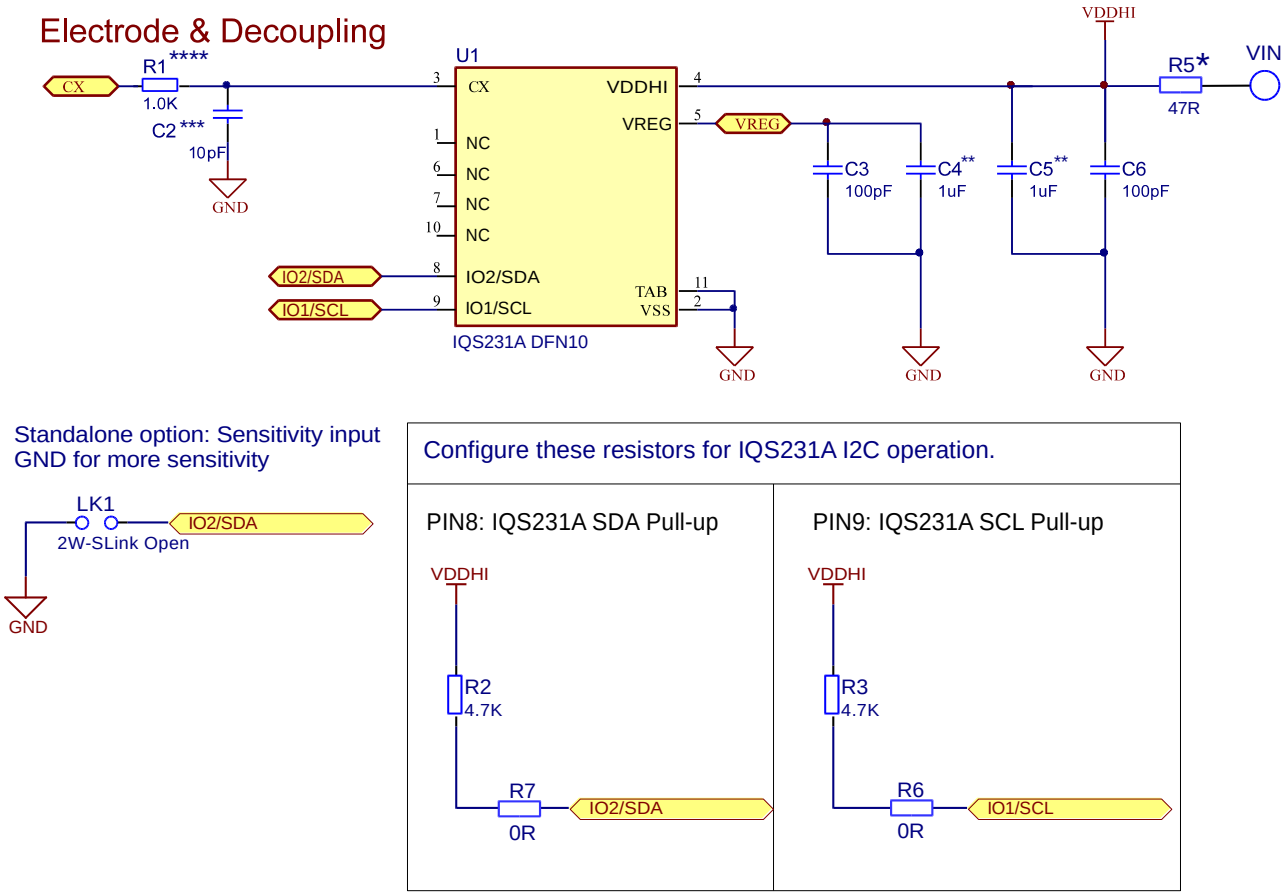


Figure 3.1 IQS231A DFN10 reference schematic

Footnotes:

* R5: Place a 47Ω resistor in the VDDHI supply line to prevent a potential ESD induced latch-up. Maximum supply current should be limited to 80mA on the IQS231A/B VDDHI pin to prevent latch-up.

** C4 & C5: Choose these capacitors based on the selected sampling rate. The target is to prevent the VREG voltage to drop more than 50mV from its regulated value during a sleep cycle (see Figure 9.1).

	30Hz	100Hz	8Hz	4Hz
C4	1uF	1uF	2.2uF	4.7uF
C5	1uF	1uF	4.7uF	10uF

***C2: Example load of 10pF. This value may vary to adjust sensitivity. 1pF for higher sensitivity and up to 60pF for proximity detection use. A total load capacitance of 200pF is allowed by the sensing system.

****R1: Vary this value to control the RC slope of the capacitance measurement signal. Use for harmonic suppression and to enable a high impedance sensing path in a low impedance system.

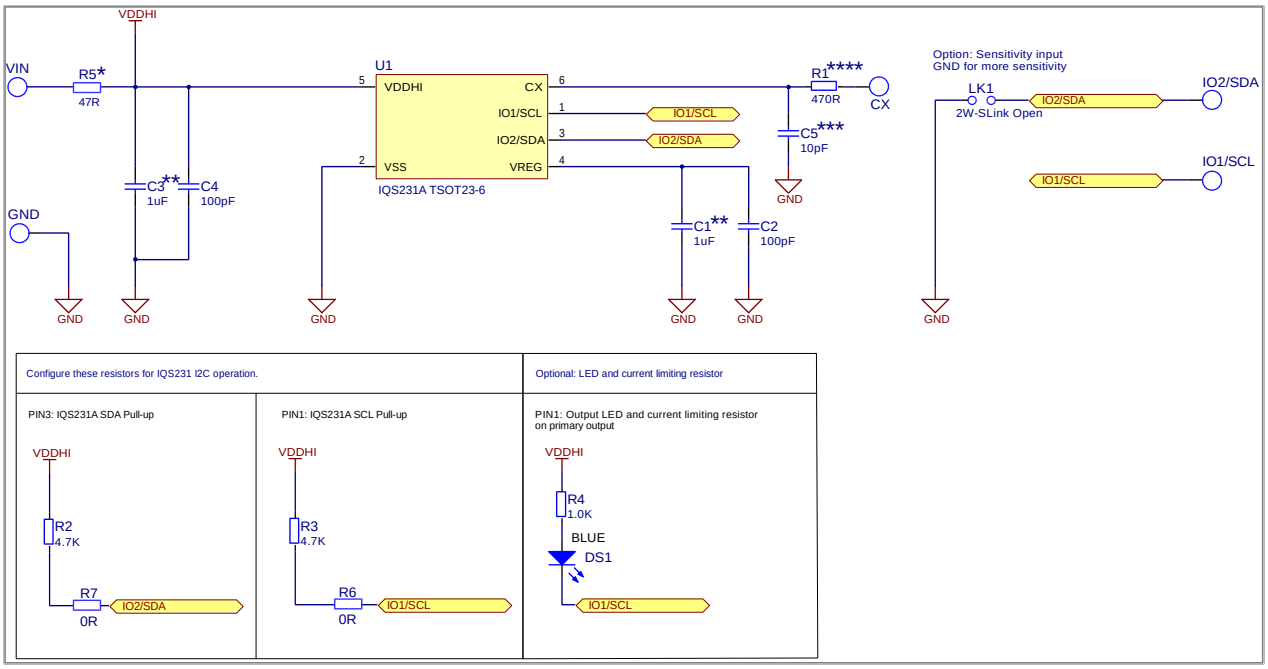


Figure 3.2 IQS231A/B TSOT23-6 reference schematic

Footnotes:

* R5: Place a 47Ω resistor in the VDDHI supply line to prevent a potential ESD induced latch-up. Maximum supply current should be limited to 80mA on the IQS231A/B VDDHI pin to prevent latch-up.

** C1 & C3: Choose these capacitors based on the selected sampling rate. The target is to prevent the VREG voltage to drop more than 50mV from its regulated value during a sleep cycle (see Figure 9.1).

	30Hz	100Hz	8Hz	4Hz
C1	1uF	1uF	2.2uF	4.7uF
C3	1uF	1uF	4.7uF	10uF

***C5: Example load of 10pF. This value may vary to adjust sensitivity. 1pF for higher sensitivity and up to 60pF for proximity detection use. A total load of 200pF is allowed by the sensing system.

****R1: Vary this value to control the RC slope of the capacitance measurement signal. Use for harmonic suppression and to enable a high impedance sensing path in a low impedance system.

4 Summary: One-Time-Programmable (OTP) options

OTP bank 0		IQS231A/B 000000**xx** TSR					
Bit7	6	5	4	3	2	1	Bit 0
Movement time-out		Reserved	Movement threshold	Quick release threshold		Quick release beta	
Prox no mov UI 00 – 2s 01 – 5s 10 – 10s 11 – Disabled (0s) Prox&Mov Uis 00 – 10s 01 – 30s 10 – 60s 11 – 10min *See time-out accuracy section		n/a	0 – 4 counts 1 – 6 counts	00 – moderate 01 – strict 10 – relaxed 11 – very strict	100 counts 150 50 250	00 – 2 (fast following) 01 – 3 10 – 4 11 – 5 (slow following)	

OTP Bank 1		IQS231A/B 0000**xx**00 TSR					
Bit7	6	5	4	3	2	1	Bit 0
I2C address		Proximity Threshold (low/high)		AC Filter		Touch threshold	
00 – standalone 01 – 44H 10 – 46H 11 – 47H *See time-out accuracy section		Sensitivity input low / Sync input active / Mov output / Touch output 00 – 4 counts ([1]Warning) 01 – 6 10 – 8 11 – 10 Sensitivity input high (internal 20kΩ pull-up) 00 – 8 counts 01 – 10 10 – 12 11 – 14		00 – 1 01 – 2 10 – 3 11 – 0		00 – 32 counts 01 – 64 10 – 256 11 – 320	

OTP Bank 2		IQS231A/B 00**xx**0000 TSR					
Bit7	6	5	4	3	2	1	Bit 0
Increase debounce	Target	Base value		Failsafe	Quick release	User interface	
0 – 6in, 4out 1 – 12in, 8out	0 = 1200 / 1096 (movement) 1 = 768	00 – 100 counts 01 – 75 10 – 150 11 – 200		0 – Disabled 1 – Enabled	0 – Enabled 1 – Disabled	00 – Prox / No movement 01 – Prox with movement 10 – Prox with movement / Touch with no movement 11 – Same as '10', touch output forced on IO2	

OTP Bank 3		IQS231A/B **xx**000000 TSR					
Bit7	6	5	4	3	2	1	Bit 0
Charge transfer frequency		Temperature & interference compensation	IO2 function		ATI events on IO1	Sample rate	
00 – 500kHz 01 – 125 kHz 10 – 64 kHz 11 – 16.5kHz		0 – Disabled 1 – Enabled	00 – Sensitivity input (proximity threshold adjust) 01 – Sync input 10 – Movement output 11 – Ignore input, no output		0 – Enabled 1 – Disabled	Sample-to-sample time (Response time) Includes 6 sample debounce burst of 24ms 00 – 30 Hz (57ms) 01 – 100 Hz (34ms) 10 – 8 Hz (154ms) 11 – 4 Hz (280ms) *See time-out accuracy section 8.8 & 8.9	

[1]Careful design is key when using a threshold of 4 combined with a base value of 100 / 75 and a target of 1200. Contact Azoteq.

5 Summary: Programming reference (I²C memory map)

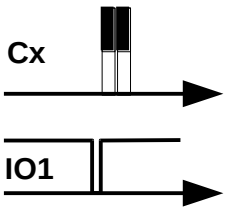
I2C Communications Layout											
Address/ Command/ Byte	**Register name/s**	**R/W**	**Default Value**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DEFAULT COMMS POINTER	MAIN_EVENTS	R	n/a		DEBUG	SENSING DISABLED	WARM BOOT	COLD BOOT	RELEASE	TOUCH	PROX
Each read instruction returns 'MAIN_EVENTS' byte as first byte, followed by the data at the specified address											
00H	PRODUCT_NUMBER	R	0x40	0x40							
01H	SOFTWARE_VERSION	R	0x06	0x06 (IQS231A), 0x07 (IQS231B – Identical to 0x06 software)							
02H	DEBUG_EVENTS	R	n/a	RESERVED	ATI_ERROR	CH0_ATI	RESERVED	QUICK RELEASE	EXIT MOV DETECT	ENTER MOV DETECT	MOVEMENT
03H	Reserved	R/W	n/a	RESERVED							
04H	COMMANDS	R/W	0x00	ATI_CH0	DISABLE SENSING	ENABLE SENSING	TOGGLE AC FILTER	RESERVED	TOGGLE ULP MODE	RESERVED	WARM BOOT
05H	OTP Bank 1	R/W	0x00	Standalone / I2C address		Proximity threshold Read only		AC Filter		Touch threshold Read only	
06H	OTP Bank 2	R/W	0x00	Increase debounce	Target	Base value		Failsafe pulses IO1	Quick release	User interface selection	
07H	OTP Bank 3	R/W	0x00	Charge transfer frequency		Temperature & interference compensation	IO2 Function		ATI events on IO1	Sample rate	
08H	QUICK RELEASE	R/W	0x00	Quick release threshold LUT 0xC = 500 0xD = 750 0xE = 850 0xF = 1000	 0x8 = 75 0x9 = 200 0xA = 300 0xB = 400	 0x4 = 10 0x5 = 20 0x6 = 25 0x7 = 30	 0x0 = 100 0x1 = 150 0x2 = 50 0x3 = 250	Quick release beta			
09H	MOVEMENT	R/W	0x34 (2s, 8)	Filter halt time 0xC = 10min 0xD = 30min 0xE = 60min 0xF = 90min	 0x8 = 30s 0x9 = 1min 0xA = 2min 0xB = 5min	 0x4 = 4s 0x5 = 5s 0x6 = 10s 0x7 = 20s	 0x0 = 0s 0x1 = 0.5s 0x2 = 1s 0x3 = 2s	Movement threshold = (Value × 2) Available range: 0 – 30 0 = always movement trigger			
0AH	TOUCH THRESHOLD	R/W	0x07 (32)	Touch threshold = (Value × 4) + 4 Available range: 4 – 1024							
0BH	PROXIMITY THRESHOLD	R/W	0x00	Reserved				Reserved		00 – 4 counts 01 – 6 10 – 8 11 – 10	
0CH	Temperature & interference threshold	R/W	0x03	Temperature tracking threshold when not in touch / prox detect							
0DH	CH0 Multipliers	R/W	n/a	Reserved	Reserved	CH0 Sensitivity Multiplier 0 – 3		CH0 Compensation multiplier 0 – 15			
0EH	CH0 Compensation	R/W	n/a	0 – 255							
0FH	CH1 Multipliers	R/W	n/a	Reserved	Reserved	CH1 Sensitivity Multiplier 0 – 3		CH1 Compensation multiplier 0 – 15			
10H	CH1 Compensation	R/W	n/a	0 – 255							
11H	System flags	R	n/a	I2C	TEMP	CH1_ACTIVE	CURRENT_CH	NO SYNC	CH0_LTA_HALTED	ATI_MODE	ZOOM MODE
12H	UI flags	R	n/a	TEMP CHANNEL ATI	TEMPERATURE RESEED	Reserved	UI AUTO ATI OFF	UI SENSING DISABLED	QUICK_RELEASE	Reserved	OUTPUT ACTIVE
13H	ATI flags	R	n/a	Reserved							
14H	Event flags	R	n/a	CH1_ATI ERROR	Reserved		CH1 MOVEMENT	CH0_ATI ERROR	CH0 UNDEBOUNCED	CH0_ TOUCH	CH0_PROX
15H	CH0 ACF_H	R	n/a	Proximity channel: Filtered count value 0 – 2000							
16H	CH0 ACF_L	R	n/a								
17H	CH0 LTA_H	R	n/a	Proximity channel: Reference count value (Long term average) 0 – 2000							
18H	CH0 LTA_L	R	n/a								
19H	CH0 QRD_H	R	n/a	Proximity channel: Quick release detect reference value 0 – 2000							
1AH	CH0 QRD_L	R	n/a								
1BH	CH1 ACF_H	R	n/a	Movement channel: Filtered count value 0 – 2000							
1CH	CH1 ACF_L	R	n/a								
1DH	CH1 UMOV_H	R	n/a	Movement channel: Upper reference count value 0 – 2000							
1EH	CH1 UMOV_L	R	n/a								
1FH	CH1 LMOV_H	R	n/a	Movement channel: Lower reference count value 0 – 2000							
20H	CH1 LMOV_L	R	n/a								
21H	CH1_RAW_H	R	n/a	Temperature channel: Unfiltered count value (if temperature feature enabled) 0 – 2000							
22H	CH1_RAW_L	R	n/a								
23H	TEMPERATURE_H	R	n/a	Movement channel temperature reference (a previous value of temperature channel) 0 – 2000							
24H	TEMPERATURE_L	R	n/a								
25H	LTA_HALT_TIMER_H	R	n/a	Countdown timer to give active feedback on the time-out. Movement events will reset this timer (0 – 255) × 100ms | Timer range: 0 – 90min							
26H	LTA_HALT_TIMER_L	R	n/a								
27H	FILTER_HALT_TIMER	R	n/a	Countdown timer to give active feedback on the fixed 5sec time-out when in filter halt mode (before entering Proximity detect) 0 – 50 x 100ms | Timer range: 0 – 5 seconds							
28H	TIMER_READ_INPUT	R	n/a	Countdown timer to signal when a read operation is done on IO2 (0 – 10) x 100ms | Timer range: 0 – 1 seconds							
29H	TIMER_REDO_ATI	R	n/a	Countdown timer to give active feedback on the time until re-calibration is attempted after ATI-error (0 – 255) × 100ms | Timer range: 0 – 25s							

6 Summary: Features

Pin compatibility	Designs using the IQS229 or IQS128 will benefit from a “drop-in” replacement on a production device for evaluation. Using the added I²C capability on the IQS231A/B will require an added connection to the master device.
 **DYCAL / Quick release**	A DYCAL-type implementation (referring to dynamic threshold calibration) is recommended as main stability feature for the latest SAR user interface. Passing the device SAR qualification with this type of interface has been proven successful. “Quick release” detection is the improved “DYCAL”-type implementation and focusses on a release characteristic within a time window. Movement features add a second level of protection against stuck conditions with the quick release detection. The quick release will be detected on the proximity channel (not the secondary movement channel) and the signal slope will be monitored to enable the quick release. A single action from a touch/proximity state will trigger the quick release event and the event will only remain as long the proximity state holds.
Control in RF environments	A number of features are offered to ensure operation in various designs where high power RF signals may influence the sensing signal: • Increased low frequency sensing options to allow for high impedance filter circuits • Increased debounce option to prevent RF noise triggers • Advanced temperature compensation for fast temperature variations caused by high power RF circuits • Interference compensation for false triggers caused by conducted/radiated noise.
Advanced temperature & interference compensation	An improved compensation feature is offered to prevent false triggers due to quickly varying temperature & high interference environments. This feature effectively tracks temperature changes & compensates for interference only when no proximity trigger is present.
UI **User interface selection**	The device offers 3 main Uis intended for SAR use. These are: • Proximity UI, no continuous movement sensing • Proximity UI, continuous movement sensing • Proximity & touch UI, continuous movement sensing during proximity, no movement sensing during touch (No time-out during long duration stationary SAR tests) In all cases the use of the quick release feature is recommended to prevent typical non-human activations from remaining. In all cases “no movement” and “movement sensing” refers to the capacitive movement sensing during normal activation. “Hand held detection” and “quick release” features will enable

	movement sensing with a no-movement time-out, irrespective of which UI is selected.

Summary: Features (Continued 1…)

 **Movement detection**	Movement detection is designed to function as human presence detection in a localized area. This device can't be used to fulfil an accelerometer function ("G-sensor" function). Human presence detection requires an exception in SAR testing because the qualification testing only uses stationary "phantom bodies". Optimized human detection is offered through an integrated separate channel, dedicated towards human detection.
Sensitivity adjustment	Default input use: internal pull-up (20kΩ) by default, tie directly to GND for more sensitive option. Apart from the simple external adjustment, an external capacitor is recommended for sensitivity adjustments. 1pF is considered a small change in sensitivity, while 10pF changes are considered large. A maximum of 60pF load is recommended for effective proximity sensing.
 **Failsafe heartbeat**	A single pulse of 500µs is integrated on IO1. This pulse is the failsafe heartbeat, sent on each sensing event. This pulse will be sent during the "stabilize time" as shown in Figure 9.1. The failsafe indicator signal will precede the conversions (sampling). The failsafe signal will be repeated during burst mode in order to offer synchronization output to the master, indicating exactly when sensitive measurements are done. Measurement times have a fixed maximum which the user can implement. The failsafe signal is disabled by default and may be enabled via OTP option or I²C initialize with standalone setup.
 High configurability	Through I²C the IQS231A/B can be used in many ways and the configuration can be updated during later stages of development than with the OTP route.
Switch I²C to standalone	Configure the device via a dedicated I²C type connection and switch to any standalone mode for runtime operation. This minimises the processor load and spurious content from communication signals. Unexpected reset conditions should be managed via the failsafe pulse OTP option or by polling the device periodically. When the heartbeat disappears or I2C responds to the polling, default state applies, and the master should reconfigure the device through I²C.

Summary: Features (Continued 2…)

Sync input	In order to ensure a stable sensing environment, sensing may be done in strategic time windows controlled by a master device.
Automatic tuning (ATI)	The Automatic tuning implementation (ATI) ensures optimal sensitivity during runtime for various sensor environments. Two channels are calibrated (proximity channel and movement channel). Both run on the same Cx pin in different time slots. An ATI-block time is defined to prevent re-ATI loops during touch release events. The ATI-block is fixed for the movement channel, and fixed for the standard touch/proximity channel
Reference signal behaviour	Long-term-average (LTA: signal reference) behavior is optimized for SAR where trigger tests are important in product qualification. The LTA will therefore be slow while still able to prevent typical temperature drift from causing activations.
 **Improved I²C interface**	Standard I²C polling for: • Debugging & normal use • Device polling optimized for guaranteed response (within $t_{CLK\_stretch}$ – clock stretching will be applied to the bus SCL line)

7 Features: Extended details

7.1 ATI (Automatic Tuning Implementation)

External sensor connections are calibrated in the following ways:

- Power On Reset (proximity channel is calibrated at each POR)
- Movement channel is only calibrated with POR when hand-held detection is enabled
- Proximity & movement channel is calibrated when the reference is out of bounds (1/8 of target counts). The reference of the proximity channel is rapidly adapted when capacitance moves away from the trigger threshold OR when an automatic “reseed” is done (Reseed: reference = actual sensor value). The reference of the movement channel is rapidly adapted in any direction of capacitive changes.
- Redo-ATI of the proximity channel can be initiated by the user in I^2C mode using an I^2C command.

During each proximity channel ATI event, the proximity output is activated to indicate the event and ensure a safe output during the event and in the case of an ATI-error.

7.2 Sensitivity adjustment

Apart from the simple external adjustment, an external capacitor is recommended for sensitivity adjustments. 1pF is considered a small change in sensitivity, while 10pF changes are considered large. A maximum of 60pF load is recommended for effective proximity sensing.

8 I²C Programming Guide (Summary)

The IQS231A/B device interfaces to a master controller via a 2-wire (SDA and SCL) serial interface bus that is I²C™ compatible, with a maximum communication speed of 400kbit/s.

The protocol acknowledges an address request independently. The I²C hardware module is awake for address recognition while the IQS231A/B is in sleep mode, giving the ability to wake the device at any time and effectively communicate via serial interface. This is different compared to other ultra-low power Azoteq solutions where the communications module also sleeps during standard IC sleep times. Repeated polling requests where required in such case.

8.1 Add I2C connection

When using I²C mode, ensure the connections as shown in Figure 2.. Internal pull-up resistors are sufficient for communication speeds up to 100kbits/s with low capacitance on the lines (<15pF). For 400kbit/s, be sure to place pull-up resistors (4.7kΩ recommended)

8.2 I2C command structure

By writing to address 0x04, commands are sent to the device. The commands are as follows:

Table 8.1 I²C command structure

Reg 0x04 Bit	Name	Description	Toggle (yes/no)
0	SWITCH TO STANDALONE (warm boot)	Switch from I2C so standalone outputs Soft reset, all registers remain as written, UI resets	No
1	AUTO ATI	Enable or disable automatic calibration when sensing signal is out of bounds	Yes
2-4	RESERVED	n/a	n/a
5	DISABLE SENSING	Disables all conversions	No
6	ENABLE SENSING	Enable capacitive sensing	No
7	ATI CH0	Perform re-calibration on proximity channel	No

8.3 Control Byte

The Control byte indicates the 7-bit device address (44H default) and the Read/Write indicator bit. The structure of the control byte is shown in Figure 8.1.

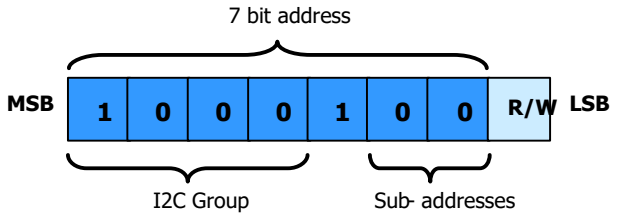


Figure 8.1 IQS231A/B control byte

The I²C device has a 7 bit Slave Address (default 0x44H) in the control byte as shown in Figure 8.1. To confirm the address, the software compares the received address with the device address. Sub-address values can be set by OTP programming options.

The IQS231A/B has alternate slave address options of 0x46 and 0x47.

8.4 Test mode (address 0x45)

During the power-on period (t_{test_mode}) the device will respond to polling requests on address **0x45** (test-mode address). Test-mode is used during IC production and OTP (programming) configuration.

With another device on the I²C bus with address 0x45, power-up sequence and communication timing should be considered.

8.5 I2C typical setup

The typical I²C setup would adjust the following registers:

- Quick release beta
- Quick release threshold
- Movement threshold
- Touch threshold
- Proximity threshold
- Filter halt time
- User interface
- IC mode

The rest of the settings will only require adjustment with specific requirement.

8.6 I2C read (Event register)

Each I2C read will always return the event register (default address pointer) as the first byte. When reading from a specific register (write address before read), 2x reads should be done. See memory map first line for detail on the event register.

When reading without writing an address, the main events register data (default address pointer) is returned. Consecutive reads will step through the memory map, starting from address 0x00 after the default address pointer.

8.7 I2C polling and sensing timing

Polling may be done at any time. Polling of the specific device will dictate the sensing rate.

Series resistance (example schematic R6 = R_{I2C_series} & R7 = R_{I2C_series}) on the I²C lines are effective in preventing interference on sensitive configurations. R_{I2C_series} is recommended for using the IQS231A/B on a bus with other devices.

8.8 Movement time-out accuracy

When I²C mode is enabled (OTP bank 1 bit7:6 is not “00”) the time out settings in register 0x09 bit7:4 will respond as shown in the graph below (typical measured values for a constant polling rate):

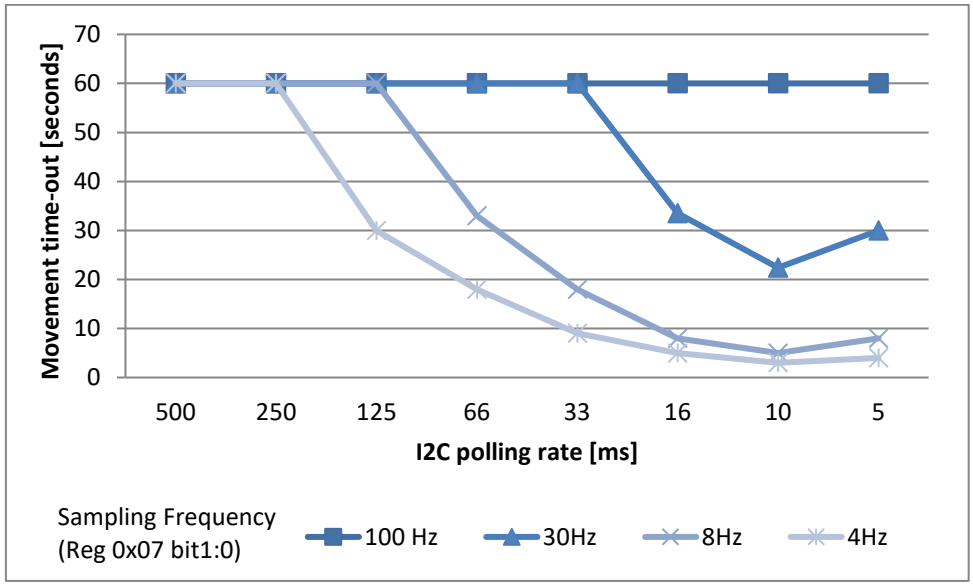


Figure 8.2 60 second movement time-out vs polling rate

While any polling rate is acceptable for 100Hz sampling, it is recommended to poll slower than the sampling frequency in order to keep an accurate time-out.

8.9 Sampling frequency vs sensing frequency

Sampling frequency (Reg 0x07 bit1:0) is the rate at which samples are taken by the sensor. The sensing frequency (Reg 0x07 bit7:6), or “charge transfer frequency” is the frequency at which the complete capacitive load is charged and discharged.

Depending on the charge transfer frequency, the sampling frequency is automatically adapted to accurately complete charge transfers for 30Hz (default) mode. For 100Hz mode, performance is prioritized and sampling time may vary during “Prox with movement” UIs or “Temperature & interference compensation” enabled. In such case, Reg 0x07 bit1:0 is not forced to a different value. The automatic adapt is done as shown in Figure 8.3

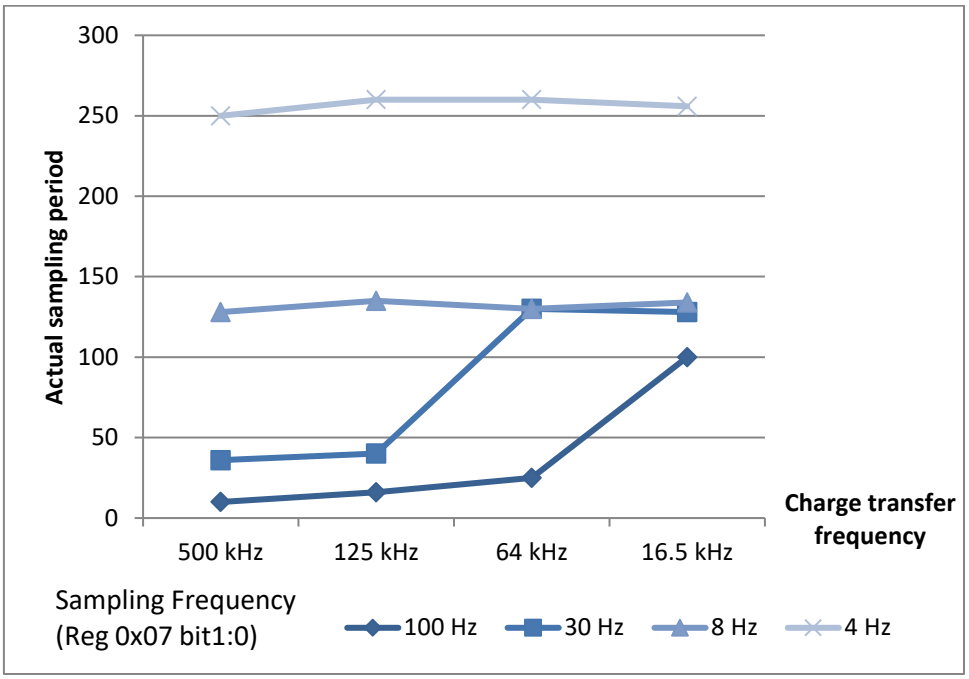


Figure 8.3 Actual sampling period vs sampling frequency selected[1]

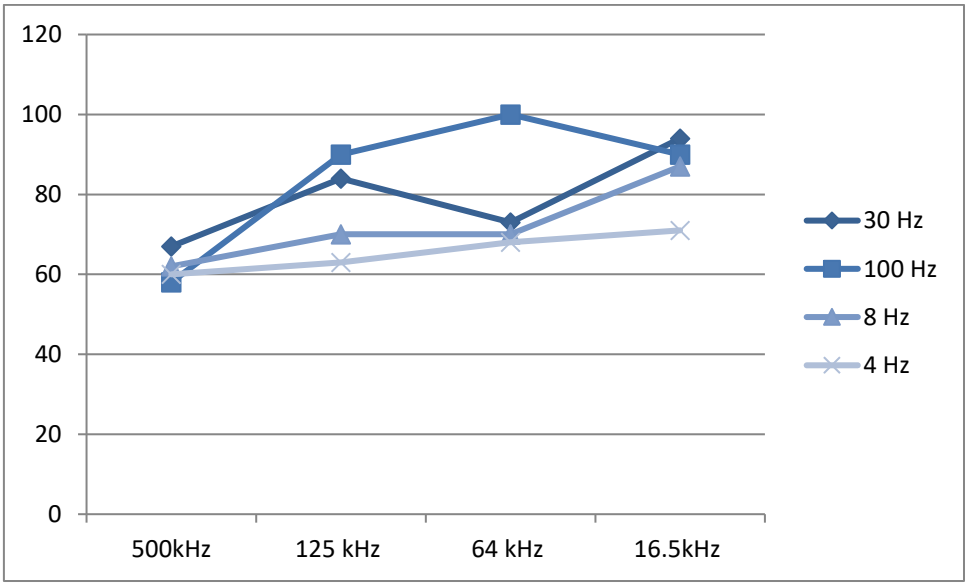


Figure 8.4 Actual 60 second time-out example[1] at various charge transfer frequencies

[1]Testing was done to obtain typical values using the recommended schematic as in Figure 3.2 (1uF capacitors for C1 & C3) at 25°C.

9 Configuration Options

The IQS231A/B offers various user selectable options. The options are defined via I²C setup or **one-time programmable (OTP)** configuration. OTP configured devices can be ordered pre-programmed for bulk orders or in-circuit programming techniques may be implemented during the product-testing phase. I²C setup allows access to all device settings while entering direct output mode when selected by the MCU.

Azoteq offers a Configuration Tool (CT210 or later) and associated software that can be used to program the OTP user options for prototyping purposes. For further information regarding this subject, please contact your local distributor or submit enquiries to Azoteq at: info@azoteq.com

9.1 OTP Details: Bank 0

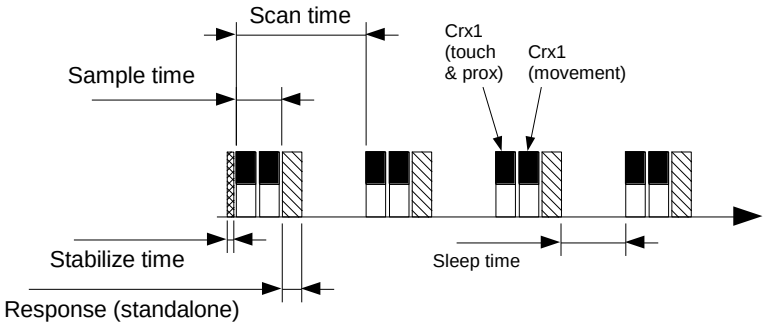
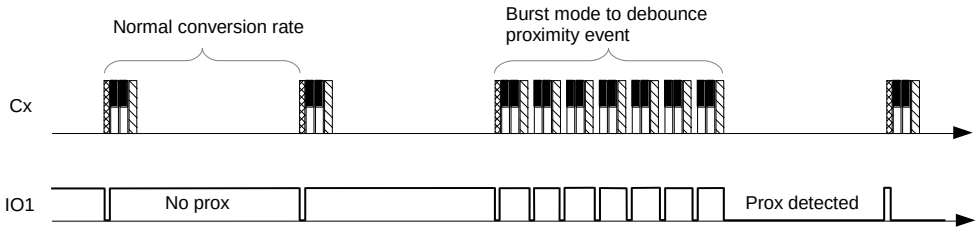
Movement time-out **(bit 7:6)**	When no movement is detected within a time period, a movement time-out occurs. The reference is halted until the timer clears. After the timer clears, the reference signal is made equal to the actual signal, nullifying any signal delta that may have caused a proximity or touch event. The timer is reloaded with every movement event detected.
Movement threshold **(bit 4)**	A low count threshold region is defined for a movement signal internally stored. Movement characteristics accumulate and triggers as soon as it reaches the threshold. The accumulated effect restarts in order to detect the next possible movement event.
Quick release threshold **(bit 3:2)**	The quick release feature will operate according to the parameters as specified in: • DYCAL / Quick release definition • Quick release beta • Quick release threshold The quick release threshold defines the trigger point for the feature where the counts deviate from a quick release moving average in a certain direction. The direction is with increasing counts
Quick release beta **(bit 1:0)**	The quick release beta forms part of the quick release feature and is the filter intensity of the reference value used to follow the actual counts. The quick release triggers according to the difference between this reference value and the actual counts. When this value is large, the quick release will trigger for a variety of release types from slow to fast releases. When this value is small, the quick release will only trigger for fast releases.

9.2 OTP Details: Bank 1

IC mode (bit 7:6)	Standalone (default), or I2C. Use I²C for runtime operation, or switch to standalone after initializing the device The advantage of this "runtime" option is explained in the Switch I²C to standalone section of the features summary. When choosing I2C, the address options of 0x44, 0x46 and 0x47 exist. Avoid the use of address 0x45 on this I²C-bus, this could activate a test mode in the IC during a power-up window.
Proximity Threshold (low/high) (bit 5:4)	By default this is the only trigger threshold in the system (touch threshold also available). The threshold is adjustable in actual counts values (count values can be seen when streaming I2C value through the IQS231A/B GUI). The threshold is the amount of counts the actual signal **falls below** the reference signal (long-term average) In the default configuration the input pin IO2 will be active. IO2 = VSS will enable the chosen option in the OTP (4-10 counts) IO2 = VDDHI (8-14 counts) The system will default to the IO2 = VSS option when sync input or movement output is enabled.
AC Filter (bit 3:2)	Incoming samples are slightly filtered by default (AC filter = 1). This option gives the ability to significantly increase the filter strength. Default is an IIR (infinite impulse response) filter of 2 (2^1). The "increased" options enables an IIR filter of 4 (2^2) or 8 (2^3). Movement detection is not affected by this setting. For movement detection the IIR filter is fixed on AC filter = 2.
Touch threshold (bit 1:0)	Threshold in counts that defines the level below the proximity threshold that cancels a quick release event and disables any active movement detection.

9.3 OTP Details: Bank 2

Increase Debounce (bit 7)	Once a threshold is crossed, a rapid debounce action ensures performance in low SNR environments and short reaction time in low power modes. An increased debounce is offered for situations where RF noise coupling into the sensor is large
Target (bit 6)	The target count is an offset value of the actual system capacitance. The actual signal (expressed in counts) will be calibrated as close as possible to this value. A larger target optimizes sensitivity at the cost of charge transfer time. A lower target offers more stability, but less sensitivity.
Base value	The base value is a lower target value for the actual signal and implies the system gain. A base value of 100 and target of 1000 implies a x10

(bit 5:4)	gain, while base value of 200 and target of 1000 implies a x5 gain.
Failsafe **(bit 3)**	This bit is only has an effect when User interface is set to Standalone. The output IO1 will have pulses superimposed on the regular output (pulse duration $t_{failsafe}$), separated by the sampling period. A pulse will be on output every time a capacitive conversion is done. Conversion rate and debounce events may be debugged through this output.  **Figure 9.1 Conversion signal on Cx timing description**  **Figure 9.2 Conversion diagram with failsafe output signal**

OTP Details: Bank 2 (...continued)

Quick release
(bit 2)

The quick release feature can be disabled via this bit (enabled by default).

The quick release feature offers improved user experience and does not influence trigger performance. The feature is directed at SAR applications, but also has significant benefits for long-term detection applications.

The touch depth and speed of release is used to detect the instance where the user interaction implies a release condition. This is required for cases where the normal threshold release is not triggered for any of the following reasons:

- Device placed on table while releasing the hand (the capacitive influence of the table remains)
- Place device inside a bag while releasing the hand (the capacitive influence of the bag remains)
- Fit a protective cover during use (the capacitive influence of the cover remains)
- Extreme temperature (cool down) shift causes a shift in capacitive environment
- Capacitance impulse recovery (drop test, transient bursts etc)

User interface
(bit 1:0)

When movement UIs are enabled, the timeout is only active in the proximity region. When in touch, only quick release can get the IC out of a stuck condition. In such case no movement time-out for quick release is fixed at 2sec and no-movement time-out for proximity is as defined in OTPs

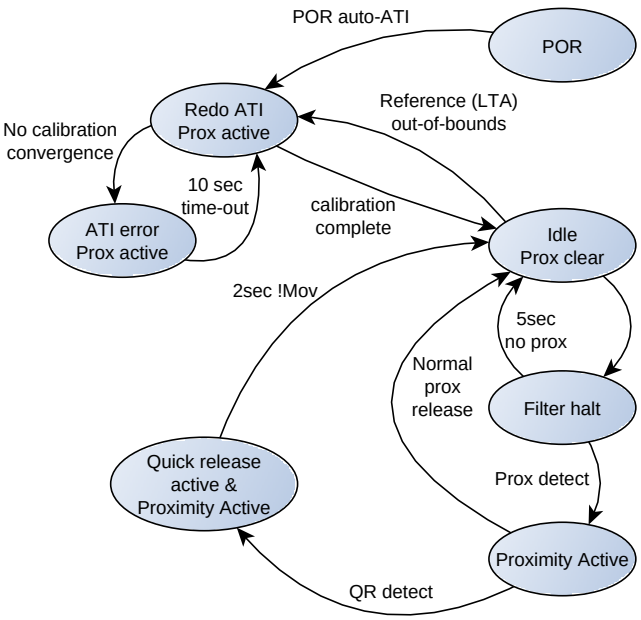


Figure 9.3 Proximity UI no movement

OTP Details: Bank 2 (...continued)

User interface (bit 1:0) (continued..)

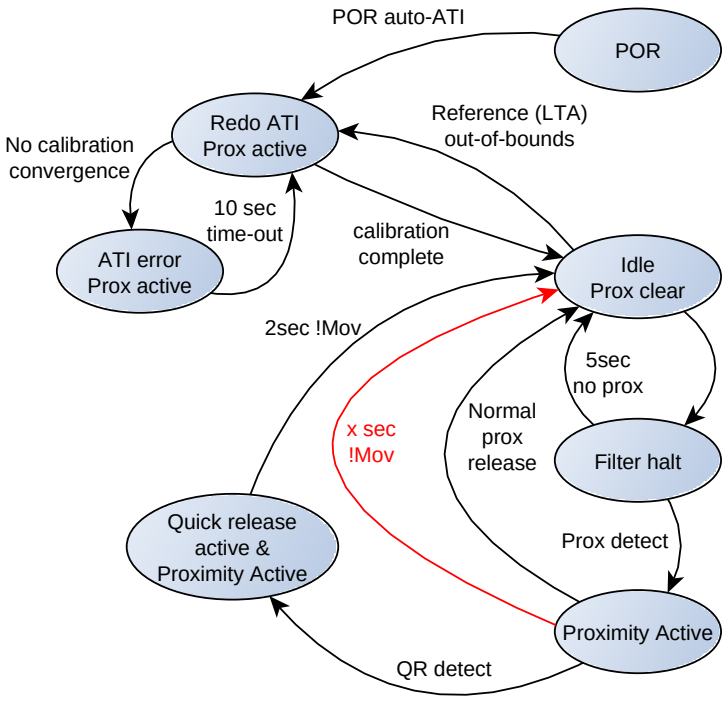


Figure 9.4 Proximity UI with movement

User interface (bit 1:0) (continued..)

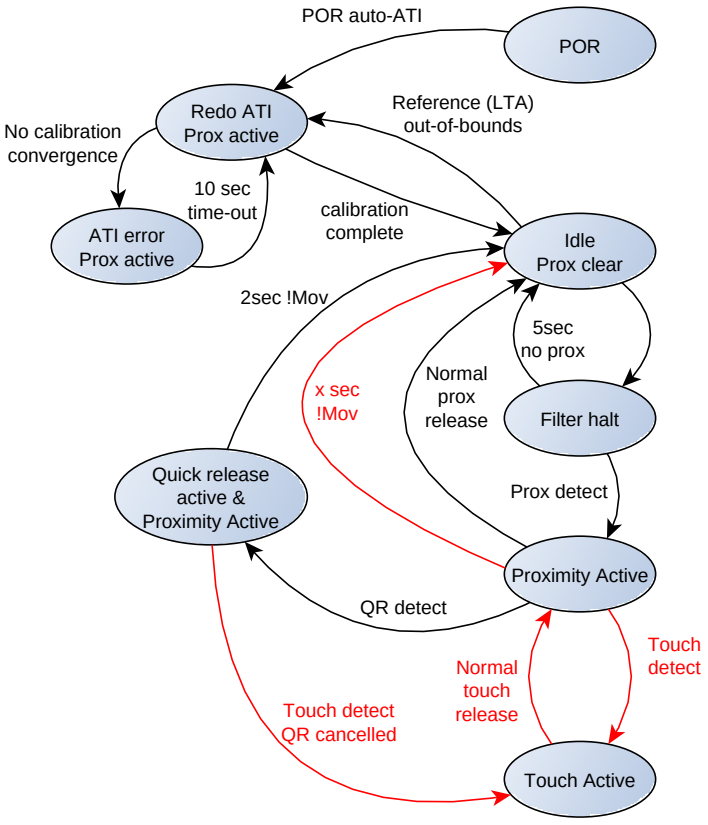
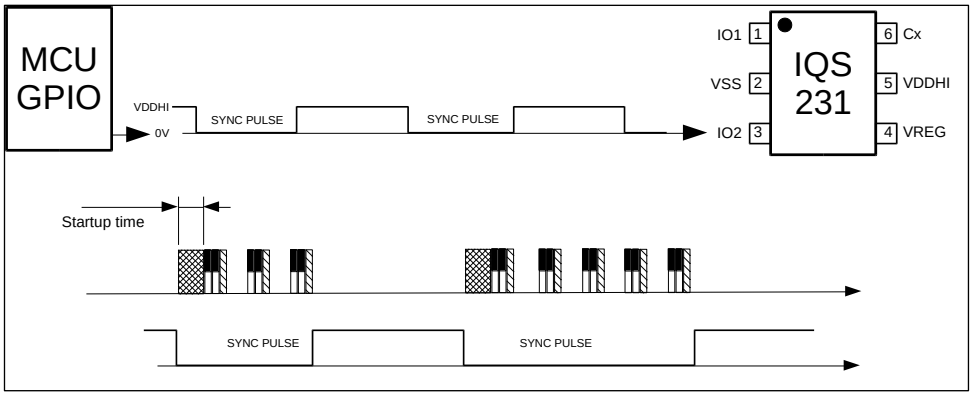


Figure 9.5 Proximity & touch UI (with movement enabled in proximity & movement disabled in touch)

9.4 OTP Details: Bank 3

Charge Transfer frequency (bit 7:6)	Various charge transfer frequencies are offered to allow for standard reference design filters to highly resistive and reactive filter elements. These options give the ability to retain signal integrity along with the isolation properties of the filter elements. These options are useful for hybrid antenna designs where the RF and sensing signal share the same conductive structure.
Temperature & Interference Compensation (bit 5)	Advanced temperature compensation is disabled by default. When enabled the IQS231A/B is able to track strong temperature changes when a proximity is not detected. This may be required when the sensor is placed on a PCB with highly varying temperature effects (example: close to an RF amplifier)
IO2 function (bit 4:3)	By default IO2 will be a sensitivity adjustment input. An internal pull-up ($R_{internal}$) will by default select a less sensitive option (IO2 = VDDHI). By strapping then pin directly to Vss, a more sensitive option is selected (IO2 = VSS). When the movement output is enabled, the input defaults to the “more sensitive option” as shown with IO2 = VSS With the output enabled the movement events are shown on IO2. The output is in an active low, open drain configuration. The output will remain low for t_{awake} when movement is detected and this will occur during the sample time after the movement trigger occurs (the movement trigger is delayed with the sample rate) Sync input: The input (pin IO2) may be used to detect when to sense and when to halt the sensing.  **Figure 9.6 Sync input of the IQS231A/B**
ATI events on IO1 (bit 2)	Calibration events (ATI) are shown on the standalone output pin (IO1). During this time, the calibration is active and proximity events during this time may influence the calibration time. The output is enabled by default and can be disabled through this bit
Sample rate (bit 1:0)	The various sample rates offered are mainly given for the user to determine an ideal balance between power consumption and response time. Overall response times of the IQS231A/B are improved with SAR trigger testing in mind.It is recommended to reduce or disable AC-filtering when using lower power modes to improve reaction time.

10 Full programming reference

A detailed list of the I²C registers follows and follows the structure of the memory map summary on page 11.

ADDR	Register name	Bit	Description
xxH	MAIN_EVENTS	7	n/a
		6	
		5	SENSING DISABLED – An indication of forced or implied times when no sensing signals are applied to the sense pin. When this bit is set and bit 2 is cleared, sensing is disabled. When this bit and bit 2 is set, sensing is enabled again.
		4	WARM BOOT – A software reset command in register 0x04 will lead to a warm boot. This will imply a reset for the user interface and re-calibration will be triggered.
		3	COLD BOOT – A hard reset (power supply cycle) will cause all registers to return to a default value. This indicator will imply the need to re-initialize the device.
		2	RELEASE – A touch, prox or sensing event may be paired with a release indication to show an exit of the flagged event.
		1	TOUCH – Disabled by default, this bit will be active when a touch and prox user interface is chosen.
		0	PROX - The main feedback bit to indicate an activation
00H	PRODUCT_ NUMBER	n/a	The product number is fixed at 0x40
01H	SOFTWARE_ VERSION	n/a	The software version is 0x06 for IQS231A The software version is 0x07 for IQS231B (firmware identical to 0x06)
02H	DEBUG_ EVENTS	7	n/a
		6	ATI_ERROR – when a recalibration cannot converge, due to external tampering or instability, this bit will indicate the error and implies that the calibration does not offer optimal sensitivity. The PROX event in the main events register will be set along with this bit in such case.
		5	CH0_ATI – An indication that a recalibration of the proximity sensing channel has occurred. With calibration, the PROX output in main events will be set and after calibration, the PROX output will release.
		4	n/a
		3	QUICK RELEASE – The quick release feature is a single event that is indicated here. This event will always imply an “ENTER MOV DETECT”, but is not the only event that causes movement detection to be activated.
		2	EXIT MOV DETECT – The user interface dictates when the movement channel is deactivated. The deactivation of movement sensing will be reported in this bit.
		1	ENTER MOV DETECT – Movement detection is user interface dependant and not continually active. Movement detection implies that a separate movement channel is activated. This activation will be reported in this bit.
		0	MOVEMENT – Each trigger detected by the movement algorithm is reported as an event that resets along with each read operation.
03H	Reserved	n/a	
04H	COMMANDS	7	ATI_CH0 – Recalibrate the proximity channel. Only after closing

ADDR	Register name	Bit	Description
			the communications window, a recalibration of the proximity sensing electrode will be started.
		6	DISABLE SENSING – Sensing can be disabled to save power or synchronize sensing in a more complex system and limit certain signals from affecting the measurement.
		5	ENABLE SENSING – Sensing can be enabled at strategic times to limit interference in the sensitive measurement environment. ENABLE / DISABLE sensing will be reflected in the MAIN_EVENTS register. ENABLE sensing will result in a "SENSING DISABLED" and "RELEASE" bit being set simultaneously.
		4	RESERVED
		3	
		2	
		1	AUTO ATI toggle on/off
		0	SWITCH TO STANDALONE – Triggers a user interface restart in standalone (GPIO) mode while keeping all register changes made. Sending the command will execute as soon as the communications window is closed.
05H	OTP Bank 1	7	Standalone / I^2C mode selection including I^2C address options (see OTP bank definition) *To switch to standalone mode directly from I^2C mode This powerful feature enables the designer to configure the device in I^2C mode and thereafter reduce the I^2C overhead and related EMI by switching to standalone for runtime. The actual mode switch occurs as soon as the communications window is closed with a stop command. It is recommended to enable the failsafe heartbeat when going from I^2C mode to standalone. The absence of the heartbeat should be used to indicate an unexpected reset event, implying the need for I^2C reconfiguration.
		6	
		5	Proximity Threshold (low/high) read only For reading OTP setting only. Note that the actual proximity threshold is defined in register 0x0B.
		4	
		3	AC Filter (see OTP bank definition)
		2	
		1	Touch threshold (read only) For reading OTP setting only. Note that the actual touch threshold is defined in register 0x0A.
		0	
06H	OTP Bank 2	7	Increase debounce (see OTP bank definition)
		6	Target (see OTP bank definition)
		5	Base value (see OTP bank definition)
		4	
		3	Failsafe (see OTP bank definition)
		2	Quick release (see OTP bank definition)
		1	User interface (see OTP bank definition)
		0	
07H	OTP Bank 3	7	Charge transfer frequency
		6	
		5	Advanced temperature compensation (see OTP bank definition)
		4	IO2 function (see OTP bank definition)
		3	
		2	ATI events on IO1 (see OTP bank definition)
		1	Sample rate (see OTP bank definition)

ADDR	Register name	Bit	Description
		0	
08H	QUICK RELEASE	7 6 5 4	The OTP options for quick release (see Quick release threshold in OTP Bank 0) is extended in I²C mode to enable a very specific release characteristic. Quick release threshold look-up table: 0x0 = 150 counts 0x1 = 100 0x2 = 50 0x3 = 250 0x4 = 10 0x5 = 20 0x6 = 25 0x7 = 30 0x8 = 75 0x9 = 200 0xA = 300 0xB = 400 0xC = 245 0xD = 230 0xE = 335 0xF = 500
		3 2 1 0	Quick release beta – This beta value is an indication of the filter strength used to track the characteristic of the release signal. The faster the tracking, the less likely the release will be detected (only very quick events will be detected). The slower the tracking, the more likely the quick release occur (quick events and slow events will be detected as a quick release) Practical values for the beta range between: 0 (fast events only) and 4 (fast and slow events) The maximum of 0xF is impractical and high values are not recommended.
09H	MOVEMENT	7 6 5 4	MOVEMENT TIME-OUT – Depending on the user interface, a movement detection channel may be started along with specific events (proximity / quick release). The timer is set and cleared as mentioned in Movement time-out (OTP Bank 0). No movement time-out value: 0x0 = 0s 0x1 = 0.5s 0x2 = 1s 0x3 = 2s 0x4 = 4s 0x5 = 5s 0x6 = 10s 0x7 = 20s 0x8 = 30s 0x9 = 1min 0xA = 2min 0xB = 5min 0xC = 10min 0xD = 30min 0xE = 60min 0xF = 90min

ADDR	Register name	Bit	Description
		3 2 1 0	MOVEMENT THRESHOLD. Movement threshold = (Value × 2) Available range: 0 – 30 For description see Movement threshold in OTP Bank 0. Note that the movement threshold in OTP Bank 1 is loaded in this register at start up and the OTP setting becomes read only. All movement threshold adjustments are performed in this register. 0 will cause movement to always trigger.
0AH	TOUCH THRESHOLD	n/a	Touch threshold = (Value × 4) + 4 Available range: 4 – 1024 For details on the touch threshold operation and uses see Touch threshold in OTP Bank 1. Note that the touch threshold in OTP Bank 1 is loaded in this register at start up and the OTP setting becomes read only. All touch threshold adjustments are performed in this register.
0BH	PROXIMITY THRESHOLD	7 6 5 4 3 2	Reserved
		1 0	Proximity threshold Available range: 4 – 10 (IO2 low / I^2C mode) Available range: 8 – 14 (IO2 high) For details on the proximity threshold operation and uses see Proximity Threshold (low/high) in OTP Bank 1. Note that the proximity threshold in OTP Bank 1 is loaded in this register at start up and the OTP setting becomes read only. All runtime proximity threshold adjustments are performed in this register.
0CH	Temperature & interference tracking threshold	n/a	0 – 255 Default 3. Low values are recommended for intended effect. Use a higher value when using the feature in a noisy environment.
0DH	CH0 Multipliers	7 6	Reserved
		5 4	CH0 Sensitivity Multiplier (Values: 0 – 3)
		3 2 1 0	CH0 Compensation multiplier (Values: 0 – 15)
0EH	CH0 Compensation	n/a	0 – 255
0FH	CH1 Multipliers	7 6	Reserved
		5 4	CH1 Sensitivity Multiplier (Values: 0 – 3)
		3 2 1 0	CH1 Compensation multiplier (Values: 0 – 15)
10H	CH1 Compensation	n/a	0 – 255

ADDR	Register name	Bit	Description
11H	System flags	7	I^2C mode active bit
		6	Advanced temperature tracking active
		5	CH1 ACTIVE – Indicates if the movement channel (CH1) is activated
		4	RESERVED
		3	NO SYNC – no sync input active bit
		2	CH0 LTA HALTED – Indicates that some proximity shift has been detected according to the threshold in register 0x05 bit 7. This event automatically clears if a proximity is not detected within t_{filter_halt}
		1	ATI MODE – Indicates that CH0 or CH1 is busy with the recalibration routine. Read the ATI in flags in register 0x13 for more information
		0	ZOOM MODE – At each threshold of the proximity channel (proximity & touch threshold), a signal “debounce” is done rapidly. During this rapid event, this bit will be set.
12H	UI flags	7	Reserved
		6	
		5	
		4	Auto-ATI off bit
		3	Sensing disabled indication bit
		2	Quick release – Indicates when a quick release action has been detected
		1	Reserved
		0	Output active – Indicates an active proximity detection
13H	ATI flags	n/a	Reserved
14H	Event flags	7	CH1_ATI ERROR – This will indicate that the movement channel is not operating under optimal sensitivity and the calibration will automatically be redone in $t_{redoATI}$. The count-down time until next attempt can be read in register 0x25 and 0x26.
		6	Reserved
		5	
		4	CH1 MOVEMENT
		3	CH0_ATI ERROR – Because of external interference, strong EMI or extreme capacitive load conditions the calibration will not be able to reach the target sensitivity (target count – as defined in register 0x06 bit 6). The proximity output will be set in such case in order to fail towards the safe side. The calibration will automatically be redone in $t_{redoATI}$. The count-down time until next attempt can be read in register 0x23 and 0x24.
		2	CH0 UNDEBOUNCED – An indication that a proximity event has been detected before a debounce operation has been done.
		1	CH0_ TOUCH – The touch event is flagged here for the duration of the touch
		0	CH0_PROX – The proximity event is flagged here for the duration of the proximity
15H	CH0 ACF_H	n/a	Proximity channel: Filtered count value 0 – 2000 This count value is related to an offset actual capacitive load. The offset is done though calibration and ensures system sensitivity.
16H	CH0 ACF_L		
17H	CH0 LTA_H	n/a	Proximity channel: Reference count value (Long term average) 0 – 2000
18H	CH0 LTA_L		

ADDR	Register name	Bit	Description
19H	CH0 QRD_H	n/a	Proximity channel: Quick release detect reference value 0 – 2000
1AH	CH0 QRD_L		
1BH	CH1 ACF_H	n/a	Movement channel: Filtered count value 0 – 2000
1CH	CH1 ACF_L		
1DH	CH1 UMOV_H	n/a	Movement channel: Upper reference count value 0 – 2000
1EH	CH1 UMOV_L		
1FH	CH1 LMOV_H	n/a	Movement channel: Lower reference count value 0 – 2000
20H	CH1 LMOV_L		

11 Specifications

11.1 Absolute maximum ratings

Absolute maximum parameters specified for the device:

Exceeding these maximum specifications may cause damage to the device.

• Operating temperature	IQS231A: -20°C to 85°C IQS231B: -40°C to 85°C
• Supply Voltage (VDDHI – VSS)	3.6V
• Maximum pin voltage	VDDHI + 0.5V (may not exceed VDDHI max)
• Maximum continuous current (for specific Pins)	10mA
• Minimum pin voltage	VSS – 0.5V
• Minimum power-on slope	100V/s
• ESD protection	±8kV (Human body model)
• Moisture Sensitivity Level (MSL)	1 (DFN-10, TSOT23-6, WLCSP-8)

Table 11.1 IQS231A/B General Operating Conditions

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		V_{DDHI}	1.764	n/a	3.6	V
Internal regulator output	1.764 ≤ V_{DDHI} ≤ 3.6	V_{REG}	1.62	1.65	1.72	V
Default Operating Current	3.3V, Scan time = 30ms	$I_{IQS231ALP30}$		33		µA
Full Power Setting	3.3V, Scan time =9ms	$I_{IQS231AFP}$		80		µA
Low Power Setting 1	3.3V, Scan time =128ms	$I_{IQS231ALP128}$		7.5		µA
Low Power Setting 2	3.3V, Scan time =256ms	$I_{IQS231ALP256}$		5		µA

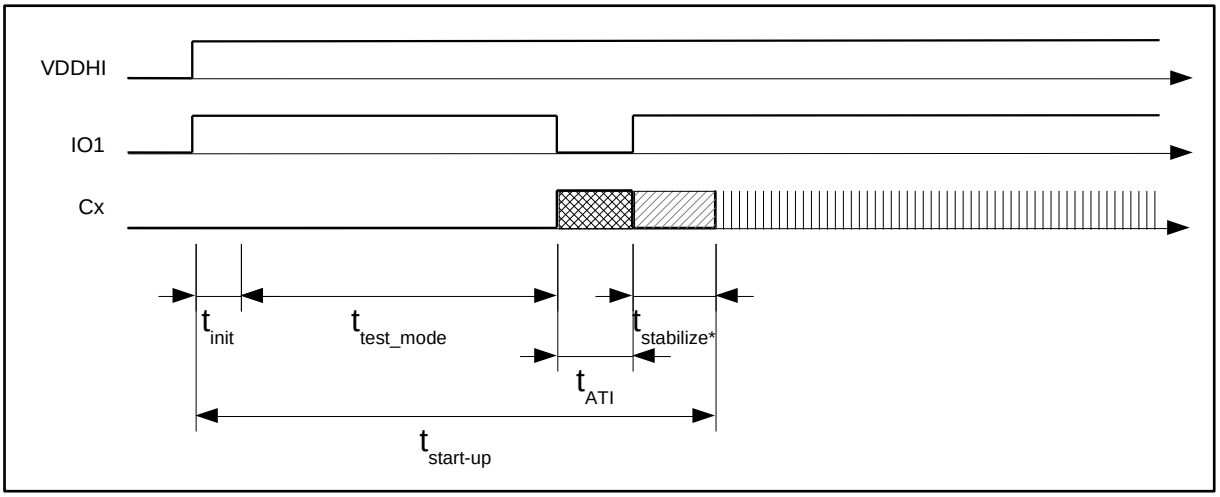
Table 11.2 Start-up and shut-down slope Characteristics

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
Power On Reset	V_{DDHI} Slope ≥ 100V/s[1]	POR_{VDDHI}	0.3[2]	1.7	V
VDDHI Brown Out Detect	V_{DDHI} Slope ≥ 100V/s[1]	BOD_{VDDHI}	N/A	1.7	V
VREG Brown Out Detect	V_{DDHI} Slope ≥ 100V/s[1]	BOD_{VREG}	N/A	1.58[3]	V

[1]Applicable to full “operating temperature” range

[2]For a power cycle, ensure lowering VDDHI below the minimum value before ramping VDDHI past the maximum POR value

[3]Figure 3.1 Capacitors C4 & C5 should be chosen to comply with this specification



*Proximity or touches made during $t_{stabilize}$ will not be recognized but rather be part of the calibration.

Figure 11.1 Timing specification during power-on

Table 11.3 Various IQS231A/B characteristics

DESCRIPTION	MIN	TYP	MAX	UNIT
t_{init}		15		ms
t_{test_mode}		340		ms
$t_{sensing\_inactive\ 30Hz\ –\ default}$	396		436	ms
t_{ATI}	41	41	81	ms
$t_{stabilize\ 30Hz\ –\ default}$		340		ms
$t_{stabilize\ 100Hz}$		128		ms
$t_{stabilize\ 8Hz}$		1192		ms
$t_{stabilize\ 4Hz}$		2344		ms
$t_{comms\_timeout}$	-	20	-	ms
$t_{failsafe}$		500		us
$t_{CLK\_stretch}$		5		ms
t_{filter_halt}		5		s
$t_{redoATI}$		10		s
t_{awake}		9		ms
$R_{internal}$		20		kΩ
R_{I2C_series}			100	Ω
$f_{sampling}$	16.5	500	500	kHz

Table 11.4 Digital input trigger levels

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
All digital inputs	Full VDDHI range	Input low level voltage	0.3 * VDDHI	n/a	V
All digital inputs	Full VDDHI range	Input high level voltage	n/a	0.7 * VDDHI	V

Table 11.5 Digital output levels

DESCRIPTION	Conditions	PARAMETER	@1mA*	@10mA*	UNIT
Output voltage low	VDDHI = 3.3V	V_{OL}	0.01	0.1	V
Output voltage high	VDDHI = 3.3V	V_{OH}	n/a**	n/a**	V

* Current sinked into output pin

** Only open drain output offered. Pull-up resistor to VDD recommended

11.2 I²C timing specifications

Table 11.6 I²C timing limits[4]

PARAMETER		Standard-mode		Fast-mode		UNIT
		Min	Max	Min	Max	
V_{IL}	SDA/SCL digital input trigger low-level	-0.5	0.3*VDDHI	-0.5	0.3*VDDHI	V
V_{IH}	SDA/SCL digital input trigger high-level	0.7*VDDHI	VDDHI +0.5	0.7*VDDHI	VDDHI +0.5	V
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{LOW}	LOW period of the SCL clock	4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL clock	4		0.6		µs
$t_{HD,STA}$	Hold time (repeated) START	4		0.6		µs
$t_{SU,STA}$	Setup time for a repeated START	4.7		0.6		µs
$t_{HD,DAT}$	Data hold time	0		0		µs
$t_{SU,DAT}$	Data setup time	100		100		ns
$t_{VD,DAT}$	Data valid time	0	3.45	0	0.9	µs
$t_{VD,ACK}$	Data valid acknowledge time	0	3.45	0	0.9	µs
$t_{SU,STO}$	Setup time for STOP	4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		µs
t_r	Rise time for SDA and SCL		1000		300	ns
t_f	Fall time for SDA and SCL		300		300	ns
C_b	Capacitive load for each bus line		400		400	
t_{SP}	Pulse duration of spikes suppressed by input filter	No noise pulse suppression filter implemented				ns
t_{WDT}	Clock low time-out (watchdog)	130	140	130	140	ms

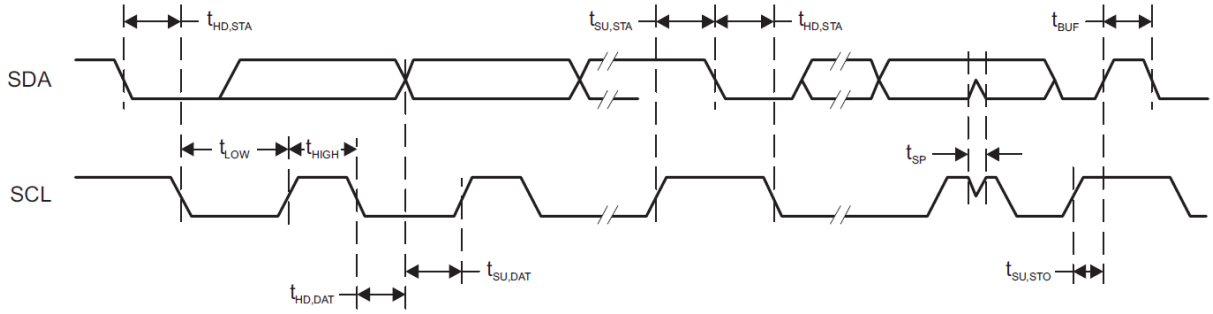


Figure 11.2 I²C mode timing

[4] Applicable over the full temperature range at VDDHI = 3.3V

12 Package information

The device is available in three packages: TSOT23-6, DFN-10 & WLCSP-8.

12.1 TSOT23-6

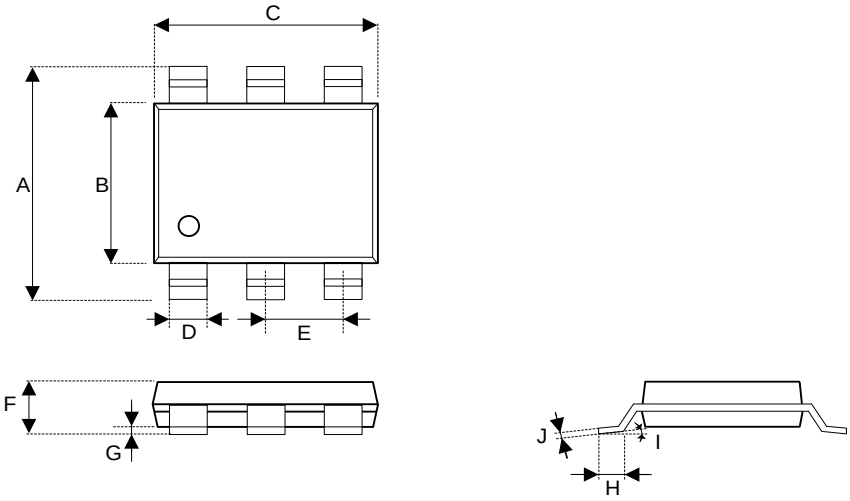


Figure 12.1 TSOT23-6 Packaging[5]

Table 12.1 TSOT23-6 Dimensions

Dimension	Min (mm)	Max (mm)
A	2.60	3.00
B	1.50	1.70
C	2.80	3.00
D	0.30	0.50
E	0.95 Basic	
F	0.84	1.00
G	0.00	0.10
H	0.30	0.50
I	0°	8°
J	0.03	0.20

[5] Drawing not on Scale

12.2 DFN-10

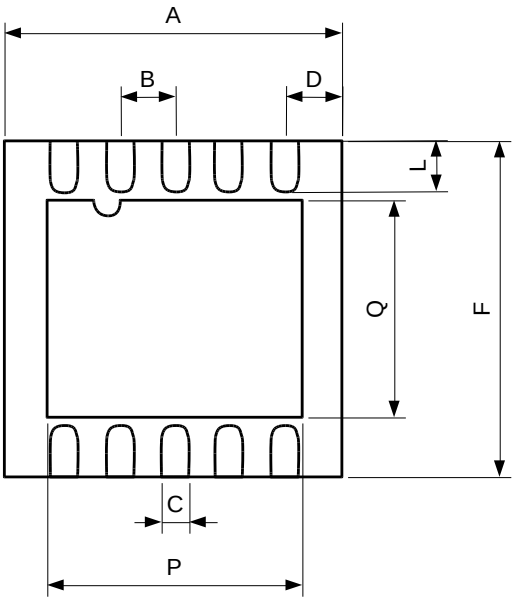


Figure 12.2 DFN-10 Package dimensions (bottom view)

Table 12.2 DFN-10 Package dimensions (bottom)

Dimension	[mm]
A	3 ±0.1
B	0.5
C	0.25
D	n/a
F	3 ±0.1
L	0.4
P	2.4
Q	1.65

Table 12.3 DFN-10 Package dimensions (side)

Dimension	[mm]
G	0.05
H	0.65
I	0.7-0.8

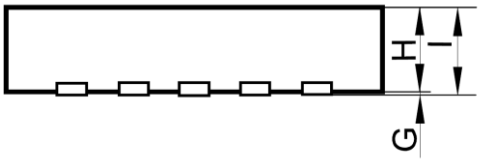


Figure 12.3 DFN-10 Package dimensions (side)

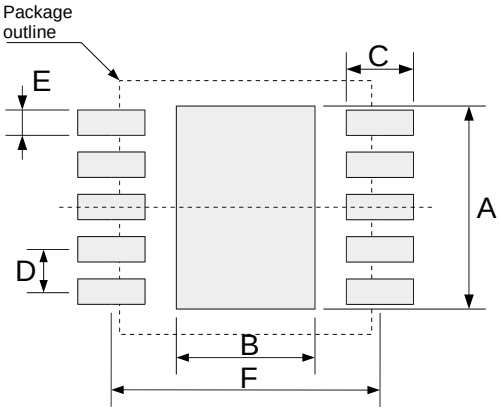
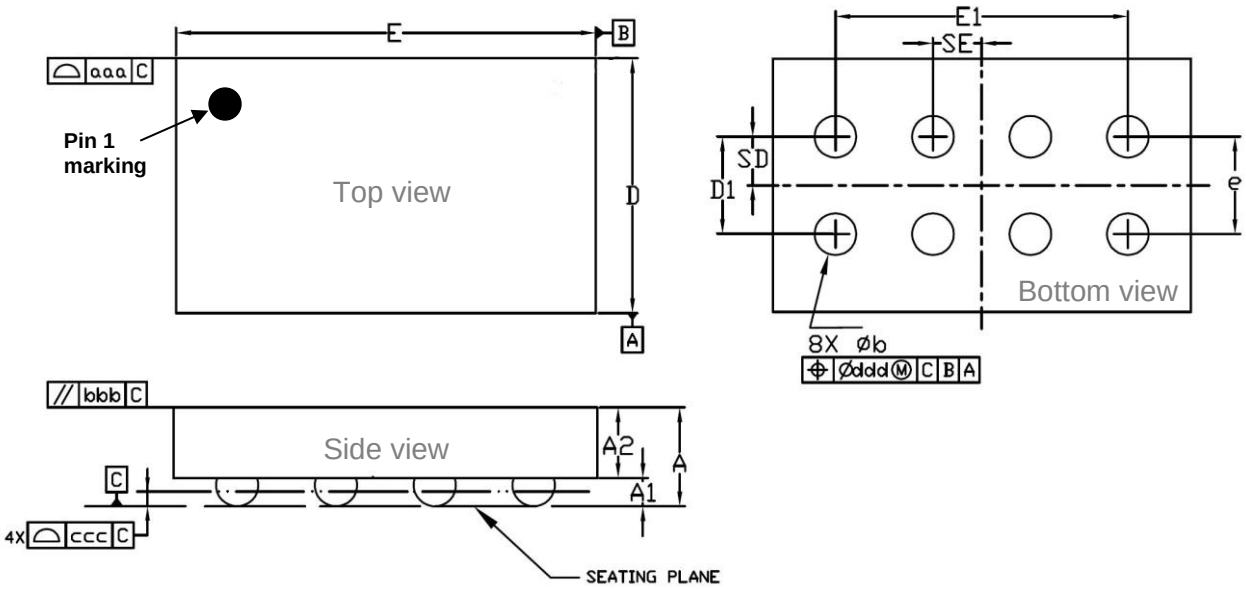


Figure 12.4 Recommended DFN-10 Landing dimensions

Table 12.4 DFN-10 Landing dimensions

Dimension	[mm]
A	2.4
B	1.65
C	0.8
D	0.5
E	0.3
F	3.2

12.3 WLCSP-8



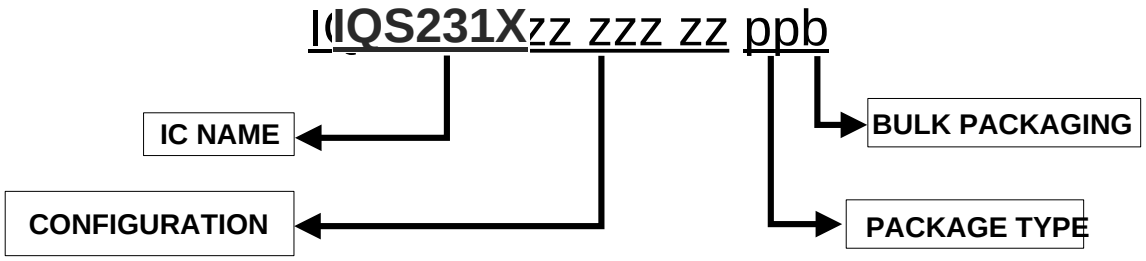
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.310	0.350	0.390
A1	0.085	0.100	0.115
A2	0.225	0.250	0.275
D	0.865	0.880	0.895
E	1.455	1.470	1.485
D1	0.300	0.350	0.400
E1	1.000	1.050	1.100
b	0.125	0.150	0.175
e	0.350 BSC		
SD	0.175 BSC		
SE	0.175 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Figure 12.5 IQS231A WLCSP-8 dimensions (in mm)

13 Ordering and Part-number Information

13.1 Ordering Information

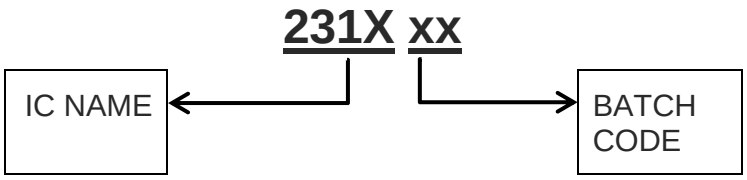
Please check stock availability with your local distributor.



IC NAME	231A	=	IQS231A
	231B	=	IQS231B
CONFIGURATION	zzz zzz zz	=	IC configuration (hexadecimal)
			Default 000 000 00 (other configurations
			available on special request)
PACKAGE TYPE	DN	=	DFN(3x3)-10 (IQS231A only)
	TS	=	TSOT23-6 package
	CS	=	WLCSP-8 package
BULK PACKAGING	R	=	Reel (3000pcs/reel) – MOQ = 3000pcs
			MOQ = 1 reel (orders shipped as full reels)

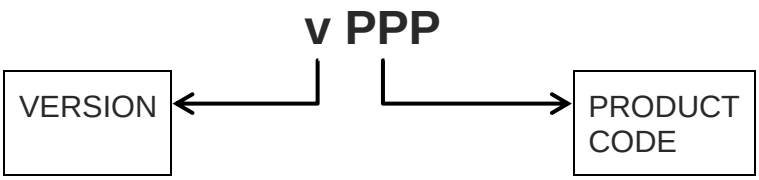
13.2 Device Numbering Convention – TSOT23-6

Top



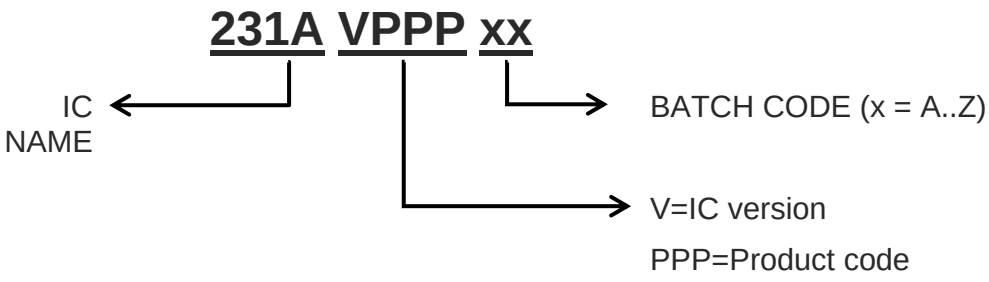
IC NAME	231A	=	IQS231A
	231B	=	IQS231B
Batch Code	xx	=	AA to ZZ

Bottom



13.3 Device numbering convention: 8-pin WLCSP

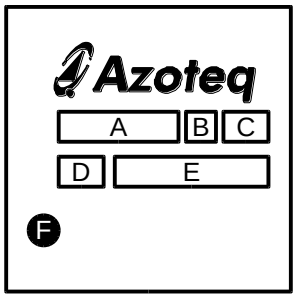
Top



Bottom

No marking present

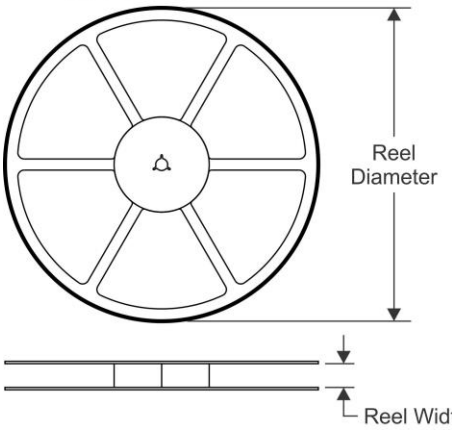
13.4 Device Numbering Convention – DFN10



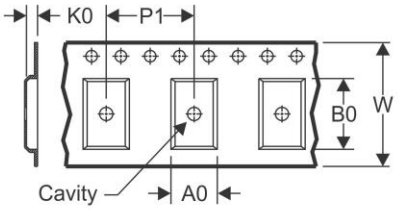
DEVICE NAME	**A**	=	IQS231A
REVISION	**B**	=	v (IC Version Number)
TEMPERATURE RANGE	**C**	=	t (-20°C to 85°C)
DATE CODE	**D**	=	p (Internal use)
	E	=	wwyy (Batch number)
PIN 1 MARKING	**F**	=	Dot to indicate pin 1

14 Tape and reel information

REEL DIMENSIONS

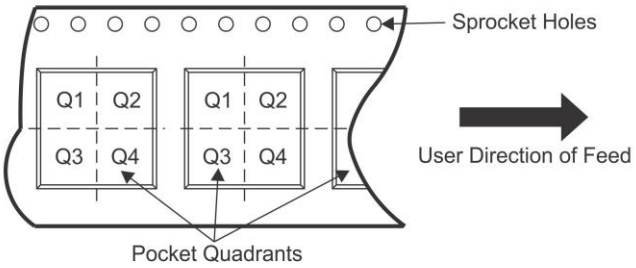


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	QTY per reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
IQS231AzzzzzzzzTSR	TSOT23/6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3
IQS231BzzzzzzzzTSR	TSOT23/6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3
IQS231AzzzzzzzzDNR	DFN10	DFN-10	10	3000	330	12.4	3.3	3.3	1.1	8	12	Q1
IQS231AzzzzzzzzCSR	WLCSP8	WLCSP-8	8	3000	179	8.4	1	1.55	0.48	4	8	Q3
IQS231BzzzzzzzzCSR	WLCSP8	WLCSP-8	8	3000	179	8.4	1	1.55	0.48	4	8	Q3

15 Revision History

Revision Number	Description	Date of issue
v1.0	IC release version	16 March 2016
V1.1	TSOT23-6 package added BOD and POR values updated	18 July 2016
V1.2	Reference schematic updated. Component selection guide also included	8 September 2016
V1.3	Introduction added to first page Start-up and ATI time description added	13 December 2016
V1.4	Switch from I2C to standalone mode information updated	10 February 2017
V1.5	WLCSP package information added	13 March 2017
V1.6	Proximity threshold options in I²C mode corrected Commands updated to include “Auto ATI on/off” Temperature compensation feature renamed to include the detection of radiated and conducted interference “I2C and sensing timing” section added. Schematics updated with recommended components.	18 July 2017
V1.7	Movement threshold option in I²C mode errata Capacitive resolution and load capability added to introduction page WLCSP package pin 5 recommendation	4 September 2017
V1.8	Added functional block diagram with basic function descriptions Added warning to section 4 OTP table when using the most sensitive settings. Updated and added AC filter information to section 9.2 Added section 8.8 & 8.9 with timing accuracy information Bottom marking changes for new device versions: see product change notices IQS231A minimum temperature has changed from -40°C to -20°C	10 November 2017
V2.0	IQS231B TSOT23-6 option added	28 May 2019
V2.2	Tape and reel information added	9 January 2020
V2.3	IQS231B WLCSP details added	22 January 2020

Appendix A Contact Information

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Fax	+1 512 672 8442		+27 21 863 1512
Email	info@azoteq.com	linayu@azoteq.com.cn	info@azoteq.com

Please visit www.azoteq.com for a list of distributors and worldwide representation.

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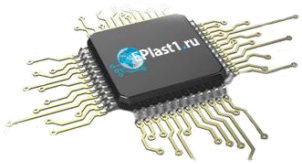
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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