

FEATURES

- 16-bit resolution with no missing codes**
- 8-channel multiplexer with choice of inputs**
- Unipolar single-ended**
- Differential (GND sense)**
- Pseudobipolar**
- Throughput: 250 kSPS**
- INL: -2.5 LSB minimum, ± 0.4 LSB typical, +2.5 LSB maximum**
- Dynamic range: 93.8 dB**
- SINAD: 91 dB typical at 20 kHz, $V_{REF} = 5$ V**
- THD: -100 dB at 20 kHz**
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD**
- Multiple reference types**
 - Internal selectable 2.5 V or 4.096 V
 - External buffered (up to 4.096 V)
 - External (up to VDD)
- Internal temperature sensor (TEMP)**
- Channel sequencer, selectable 1-pole filter, busy indicator**
- No pipeline delay, SAR architecture**
- Single-supply 2.3 V to 5.5 V operation with 1.8 V to 5.5 V logic interface**
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP**
- Power dissipation**
 - 3.5 mW typical at 2.5 V, 200 kSPS
 - 12.5 mW typical at 5 V, 250 kSPS
- Standby current: 50 nA**
- Low cost grade available**
- Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.**

APPLICATIONS

- Multichannel system monitoring**
- Battery-powered equipment**
- Medical instruments: ECG/EKG**
- Mobile communications: GPS**
- Power line monitoring**
- Data acquisition**
- Seismic data acquisition systems**
- Instrumentation**
- Process control**

FUNCTIONAL BLOCK DIAGRAM

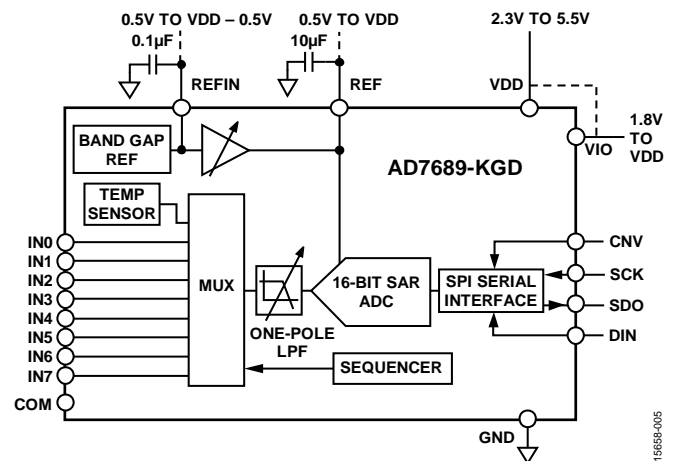


Figure 1. Composite View

GENERAL DESCRIPTION

The AD7689-KGD is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7689-KGD contains all components for use in a multi-channel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; an 8-channel low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7689-KGD uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7689-KGD is specified from -40°C to $+125^{\circ}\text{C}$.

Additional application and technical information can be found in the [AD7689](#) data sheet.

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REVISION HISTORY

7/2019—Rev. C to Rev. D

| | |
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| Changes to Features Section and General Description Section ... | 1 |
| Changes to Integral Linearity Error Parameter, Offset Error Parameter, Signal-to-Noise Ratio (SNR) Parameter, and Signal-to-Noise-and-Distortion Ratio (SINAD) Parameter, Table 1 | 3 |
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1/2019—Rev. B to Rev. C

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2/2018—Rev. A to Rev. B

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10/2017—Rev. 0 to Rev. A

| | |
|--|---|
| Changed Metal Mask Die Image Section to Functional Block Diagram Section | 1 |
| Changes to Figure 1..... | 1 |

7/2017—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, REF voltage (V_{REF}) = VDD, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|-------------------|-------------|-------------------|------------------|
| RESOLUTION | | 16 | | | Bits |
| ANALOG INPUT | | | | | |
| Voltage Range | Unipolar mode | 0 | | $+V_{REF}$ | V |
| | Bipolar mode | $-V_{REF}/2$ | | $+V_{REF}/2$ | V |
| Absolute Input Voltage | Positive input, unipolar and bipolar modes | -0.1 | | $V_{REF} + 0.1$ | V |
| | Negative or COM input, unipolar mode | -0.1 | | +0.1 | V |
| | Negative or COM input, bipolar mode | $V_{REF}/2 - 0.1$ | $V_{REF}/2$ | $V_{REF}/2 + 0.1$ | V |
| Analog Input Common-Mode Rejection Ratio (CMRR) | Input frequency (f_{IN}) = 250 kHz | | 68 | | dB |
| Leakage Current at 25°C | Acquisition phase | | 1 | | nA |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | | |
| Full Bandwidth ¹ | VDD = 4.5 V to 5.5 V | 0 | | 250 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 200 | kSPS |
| ¼ Bandwidth ¹ | VDD = 4.5 V to 5.5 V | 0 | | 62.5 | kSPS |
| | VDD = 2.3 V to 4.5 V | 0 | | 50 | kSPS |
| Transient Response | Full-scale step, full bandwidth | | | 1.8 | µs |
| | Full-scale step, ¼ bandwidth | | | 14.5 | µs |
| ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Integral Linearity Error | $T_A \leq 85^\circ\text{C}$ | -2.5 | ±0.4 | +2.5 | LSB ² |
| | $T_A > 85^\circ\text{C}$ | -3.0 | ±0.4 | +3.0 | LSB ² |
| Differential Linearity Error | | -1 | ±0.25 | +2 | LSB ² |
| Transition Noise | REF = VDD = 5 V | | 0.5 | | LSB ² |
| Gain Error | | -24 | ±1 | +24 | LSB ² |
| Gain Error Match | | -6 | ±0.5 | +6 | LSB ² |
| Gain Error Temperature Drift | | | ±1 | | ppm/°C |
| Offset Error | VDD = 4.5 V to 5.5 V, $T_A \leq 85^\circ\text{C}$ | -8 | ±1 | +8 | LSB ² |
| | VDD = 4.5 V to 5.5 V, $T_A > 85^\circ\text{C}$ | -11 | | +11 | LSB ² |
| | VDD = 2.3 V to 4.5 V | | ±5 | | LSB ² |
| Offset Error Match | | -6 | ±0.5 | +6 | LSB ² |
| Offset Error Temperature Drift | | | ±1 | | ppm/°C |
| Power Supply Sensitivity | VDD = 5 V ± 5% | | ±1.5 | | LSB ² |
| AC ACCURACY ³ | | | | | |
| Dynamic Range | | | 93.8 | | dB ⁴ |
| Signal-to-Noise Ratio (SNR) | | | | | |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 5\text{ V}$ | 88.5 | 91 | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 4.096\text{ V}$, internal REF, $T_A \leq 85^\circ\text{C}$ | 87 | 90.5 | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 4.096\text{ V}$, internal REF, $T_A > 85^\circ\text{C}$ | 86 | | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 2.5\text{ V}$, internal REF | 83.5 | 86 | | dB ⁴ |
| Signal-to-Noise-and-Distortion Ratio (SINAD) | | | | | |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 5\text{ V}$, $T_A \leq 85^\circ\text{C}$ | 88.5 | 91 | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 5\text{ V}$, $T_A > 85^\circ\text{C}$ | 87.5 | | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 5\text{ V}$, -60 dB input | | 33.5 | | dB ⁴ |
| | $f_{IN} = 20\text{ kHz}$, $V_{REF} = 4.096\text{ V}$ internal REF, $T_A \leq 85^\circ\text{C}$ | 87.5 | 90 | | dB ⁴ |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|------|-------|-----|---------------|
| Total Harmonic Distortion (THD) Spurious-Free Dynamic Range (SFDR) Channel to Channel Crosstalk | $f_{IN} = 20 \text{ kHz}$, $V_{REF} = 4.096 \text{ V}$ internal REF, $T_A > 85^\circ\text{C}$ | 85.5 | | | dB^4 |
| | $f_{IN} = 20 \text{ kHz}$, $V_{REF} = 2.5 \text{ V}$ internal REF | 84.5 | 86 | | dB^4 |
| | $f_{IN} = 20 \text{ kHz}$ | | -100 | | dB^4 |
| | $f_{IN} = 20 \text{ kHz}$ | | 110 | | dB^4 |
| | $f_{IN} = 100 \text{ kHz}$ on adjacent channel(s) | | -125 | | dB^4 |
| SAMPLING DYNAMICS | | | | | |
| -3 dB Input Bandwidth | Full bandwidth | | 1.7 | | MHz |
| | $\frac{1}{4}$ bandwidth | | 0.425 | | MHz |
| Aperture Delay | $VDD = 5 \text{ V}$ | | 2.5 | | ns |

¹ The bandwidth is set in the configuration register.

² LSB means least significant bit. With the 5 V input range, one LSB is 76.3 μV .

³ With $VDD = 5 \text{ V}$, unless otherwise noted.

⁴ All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|---|-----------|-------|------------|--------|
| INTERNAL REFERENCE | | | | | |
| REF Output Voltage | 2.5 V at 25°C | 2.490 | 2.500 | 2.510 | V |
| | 4.096 V at 25°C | 4.086 | 4.096 | 4.106 | V |
| REFIN Output Voltage ¹ | 2.5 V at 25°C | | 1.2 | | V |
| | 4.096 V at 25°C | | 2.3 | | V |
| REF Output Current | | | ±300 | | µA |
| Temperature Drift | | | ±10 | | ppm/°C |
| Line Regulation | VDD = 5 V ± 5% | | ±15 | | ppm/V |
| Long-Term Drift | 1000 hours | | 50 | | ppm |
| Turn-On Settling Time | Reference capacitance (C _{REF}) = 10 µF | | 5 | | ms |
| EXTERNAL REFERENCE | | | | | |
| Voltage Range | REF input | 0.5 | | VDD + 0.3 | V |
| | REFIN input (buffered) | 0.5 | | VDD – 0.5 | V |
| Current Drain ² | 250 kSPS, REF = 5 V | | 50 | | µA |
| TEMPERATURE SENSOR | | | | | |
| Output Voltage ³ | 25°C | | 283 | | mV |
| Temperature Sensitivity | | | 1 | | mV/°C |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| Input Voltage | | | | | |
| Low, V _{IL} | | -0.3 | | +0.3 × VIO | V |
| High, V _{IH} | | 0.7 × VIO | | VIO + 0.3 | V |
| Input Current | | | | | |
| Low, I _{IL} | | -1 | | +1 | µA |
| High, I _{IH} | | -1 | | +1 | µA |
| DIGITAL OUTPUTS | | | | | |
| Data Format ⁴ | | | | | |
| Pipeline Delay ⁵ | | | | | |
| Output Voltage | | | | | |
| Low, V _{OL} | Sink current (I _{SINK}) = 500 µA | | | 0.4 | V |
| High, V _{OH} | Source current (I _{SOURCE}) = -500 µA | VIO – 0.3 | | | V |
| POWER SUPPLIES | | | | | |
| VDD ⁶ | Specified performance | 2.3 | | 5.5 | V |
| VIO | Specified performance | 1.8 | | VDD + 0.3 | V |
| Standby Current ^{7, 8} | VDD and VIO = 5 V at 25°C | | 50 | | nA |
| Power Dissipation | VDD = 2.5 V, 100 SPS throughput | | 1.7 | | µW |
| | VDD = 2.5 V, 200 kSPS throughput | | 3.5 | | mW |
| | VDD = 5 V, 250 kSPS throughput, T _A ≤ 85°C | | 12.5 | 18 | mW |
| | VDD = 5 V, 250 kSPS throughput, T _A > 85°C | | | 19 | mW |
| | VDD = 5 V, 250 kSPS throughput with internal reference, T _A ≤ 85°C | | 15.5 | 21 | mW |
| Energy per Conversion | VDD = 5 V, 250 kSPS throughput with internal reference, T _A > 85°C | | | 22 | mW |
| | VDD = 5 V | | 60 | | nJ |
| TEMPERATURE RANGE | | | | | |
| Specified Performance | T _{MIN} to T _{MAX} | -40 | | +125 | °C |

¹ This is the output from the internal band gap.

² This is an average current and scales with throughput.

³ The output voltage is internal and present on a dedicated multiplexer input.

⁴ Unipolar mode is serial 16-bit straight binary. Bipolar mode is serial 16-bit twos complement.

⁵ Conversion results available immediately after completed conversion.

⁶ The minimum VDD supply must be 3 V when the 2.5 V internal reference is enabled, and 4.5 V when the 4.096 V internal reference is enabled.

⁷ With all digital inputs forced to VIO or GND as required.

⁸ During acquisition phase.

TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

| Parameter ¹ | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-----------------------|-----|-----|------|
| CONVERSION TIME CNV Rising Edge to Data Available | t _{CONV} | | | 2.6 | μs |
| ACQUISITION TIME | t _{ACQ} | 1.8 | | | μs |
| TIME BETWEEN CONVERSIONS | t _{CYC} | 4.0 | | | μs |
| DATA WRITE/READ DURING CONVERSION | t _{DATA} | | | 1.2 | μs |
| SCK | | | | | |
| Period | t _{SCK} | t _{DSDO} + 2 | | | ns |
| Low Time | t _{SCKL} | 11 | | | ns |
| High Time | t _{SCKH} | 11 | | | ns |
| Falling Edge to Data Remains Valid | t _{HSDO} | 4 | | | ns |
| Falling Edge to Data Valid Delay | t _{DSDO} | | | 18 | ns |
| VIO Above 2.7 V, | | | | 23 | ns |
| VIO Above 2.3 V | | | | 28 | ns |
| VIO Above 1.8 V | | | | | ns |
| CNV | | | | | |
| Pulse Width | t _{CNVH} | 10 | | | ns |
| Low to SDO D15 MSB Valid | t _{EN} | | | 18 | ns |
| VIO Above 2.7 V | | | | 22 | ns |
| VIO Above 2.3 V | | | | 25 | ns |
| VIO Above 1.8 V | | | | 32 | ns |
| High or Last SCK Falling Edge to SDO High Impedance | t _{DIS} | | | | ns |
| Low to SCK Rising Edge | t _{CLSCK} | 10 | | | ns |
| DIN | | | | | |
| Valid Setup Time from SCK Rising Edge | t _{SDIN} | 5 | | | ns |
| Valid Hold Time from SCK Rising Edge | t _{HDIN} | 5 | | | ns |

¹ See Figure 2 and Figure 3 for load conditions.

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

| Parameter ¹ | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-----------------------|-----|-----|------|
| CONVERSION TIME CNV Rising Edge to Data Available | t _{CONV} | | | 3.6 | μs |
| ACQUISITION TIME | t _{ACQ} | 1.8 | | | μs |
| TIME BETWEEN CONVERSIONS | t _{CYC} | 5 | | | μs |
| DATA WRITE/READ DURING CONVERSION | t _{DATA} | | | 1.2 | μs |
| SCK | | | | | |
| Period | t _{SCK} | t _{DSDO} + 2 | | | ns |
| Low Time | t _{SCKL} | 12 | | | ns |
| High Time | t _{SCKH} | 12 | | | ns |
| Falling Edge to Data Remains Valid | t _{HSDO} | 5 | | | ns |
| Falling Edge to Data Valid Delay | t _{DSDO} | | | | |
| VIO Above 3 V | | | | 30 | ns |
| VIO Above 2.7 V | | | | 36 | ns |
| VIO Above 2.3 V | | | | 44 | ns |
| VIO Above 1.8 V | | | | 54 | ns |
| CNV | | | | | |
| Pulse Width | t _{CNVH} | 10 | | | ns |
| Low to SDO D15 MSB Valid | t _{EN} | | | | |
| VIO Above 3 V | | | | 27 | ns |
| VIO Above 2.7 V | | | | 33 | ns |
| VIO Above 2.3 V | | | | 41 | ns |
| VIO Above 1.8 V | | | | 51 | ns |
| High or Last SCK Falling Edge to SDO High Impedance | t _{DIS} | | | 50 | ns |
| Low to SCK Rising Edge | t _{CLSCK} | 10 | | | ns |
| DIN | | | | | |
| Valid Setup Time from SCK Rising Edge | t _{SDIN} | 5 | | | ns |
| Valid Hold Time from SCK Rising Edge | t _{HDIN} | 5 | | | ns |

¹ See Figure 2 and Figure 3 for load conditions.

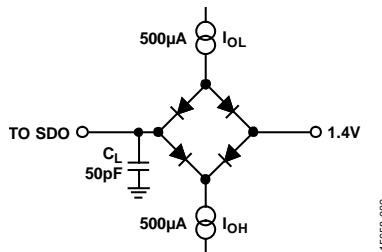
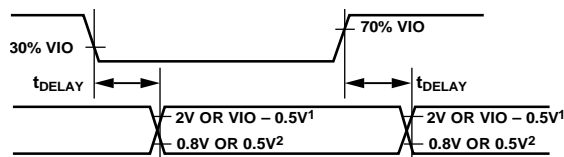


Figure 2. Load Circuit for Digital Interface Timing



¹2V IF VIO ABOVE 2.5V, VIO - 0.5V IF VIO BELOW 2.5V.
²0.8V IF VIO ABOVE 2.5V, 0.5V IF VIO BELOW 2.5V.

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|----------------------------------|---|
| Analog Inputs IN0 to IN7, COM | GND – 0.3 V to VDD + 0.3 V or VDD ± 130 mA |
| REF, REFIN | GND – 0.3 V to VDD + 0.3 V |
| Supply Voltages | |
| VDD, VIO to GND | –0.3 V to +7 V |
| VIO to VDD | –0.3 V to VDD + 0.3 V |
| DIN, CNV, SCK to GND | –0.3 V to VIO + 0.3 V |
| SDO to GND | –0.3 V to VIO + 0.3 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

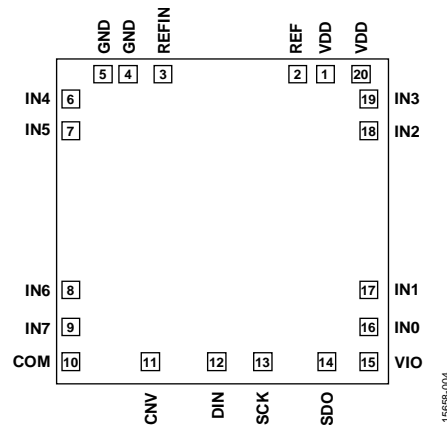


Figure 4. Pad Configuration

Table 6. Pad Function Descriptions

| Pad No. | Mnemonic | X-Axis (μm) | Y-Axis (μm) | Pad Type ¹ | Description |
|---------|----------|--------------------------|--------------------------|-----------------------|--|
| 1 | VDD | +650 | +1079 | AI | Power Supply. Nominally 2.5 V to 5.5 V. |
| 2 | REF | +475 | +1078 | AI | Reference Input/Output. |
| 3 | REFIN | -473 | +1078 | AI | Internal Reference Output/Reference Buffer Input. |
| 4 | GND | -659 | +1079 | P | Power Supply Ground. |
| 5 | GND | -838 | +1079 | P | Power Supply Ground. |
| 6 | IN4 | -1085 | +892 | AI | Analog Input Channel 4. |
| 7 | IN5 | -1085 | +653 | AI | Analog Input Channel 5. |
| 8 | IN6 | -1085 | -528 | AI | Analog Input Channel 6. |
| 9 | IN7 | -1085 | -769 | AI | Analog Input Channel 7. |
| 10 | COM | -1085 | -1015 | P | Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V. |
| 11 | CNV | -519 | -1087 | DI | Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indicator is enabled. |
| 12 | DIN | -71 | -1087 | DI | Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion. |
| 13 | SCK | +231 | -1087 | DI | Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on. |
| 14 | SDO | +667 | -1087 | DO | Serial Data Output. |
| 15 | VIO | +1079 | -1056 | P | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). |
| 16 | IN0 | +1085 | -769 | AI | Analog Input Channel 0. |
| 17 | IN1 | +1085 | -528 | AI | Analog Input Channel 1. |
| 18 | IN2 | +1085 | +653 | AI | Analog Input Channel 2. |
| 19 | IN3 | +1085 | +894 | AI | Analog Input Channel 3. |
| 20 | VDD | +997 | +1079 | P | Power Supply. Nominally 2.5 V to 5.5 V. |

¹ AI is analog input, P is power, DI is digital input, and DO is digital output.

OUTLINE DIMENSIONS

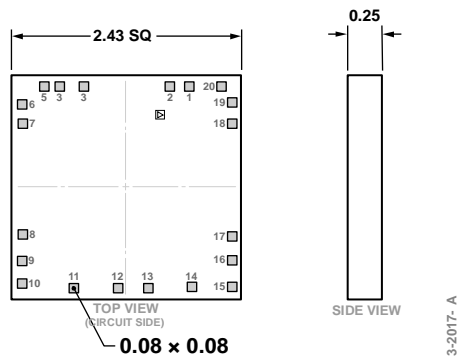


Figure 5. 20-Pad Bare Die [CHIP]
(C-20-2)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

| Parameter | Value | Unit |
|--------------------------|------------------------------|----------------|
| Scribe Line Width | 80 × 80 | μm |
| Die Size (Maximum Size) | 2430 × 2430 | μm |
| Thickness | 250 | μm |
| Bond Pads (Minimum Size) | 80 × 80 | μm |
| Bond Pad Composition | 0.5 AlCu | % |
| Backside | Standard assembly die attach | Not applicable |
| Passivation | Oxynitride | Not applicable |
| Chip Size | 2350 × 2350 | μm |

Table 8. Assembly Recommendations

| Assembly Component | Recommendation |
|--------------------|--|
| Die Attach | Epoxy adhesive |
| Bonding Method | Gold ball ¹ or aluminum wedge |
| Bonding Sequence | Bond pin five first |

¹ Evaluate the gold wire for suitability before use at elevated temperatures for extended durations.

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|-------------------|------------------------|----------------|
| AD7689-KGD-PT | −40°C to +125°C | 20-Pad Bare Die [CHIP] | C-20-2 |



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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