Micropower Single-Supply Rail-to-Rail Input/Output Op Amps

OP191/OP291/OP491

FEATURES

Single-supply operation: 2.7 V to 12 V
Wide input voltage range
Rail-to-rail output swing
Low supply current: 300 μA/amp
Wide bandwidth: 3 MHz
Slew rate: 0.5 V/μs
Low offset voltage: 700 μV
No phase reversal

APPLICATIONS

Industrial process control
Battery-powered instrumentation
Power supply control and protection
Telecommunications
Remote sensors
Low voltage strain gage amplifiers
DAC output amplifiers

PIN CONFIGURATIONS

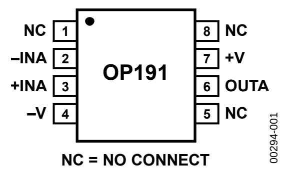

Figure 1. 8-Lead Narrow-Body SOIC

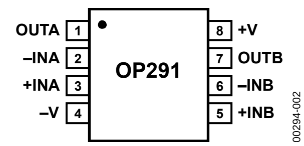

Figure 2. 8-Lead Narrow-Body SOIC

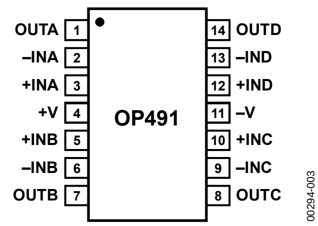

Figure 3. 14-Lead Narrow-Body SOIC

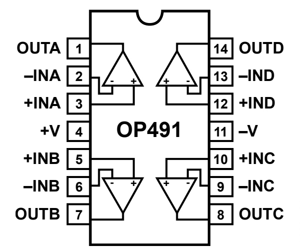

Figure 4. 14-Lead PDIP

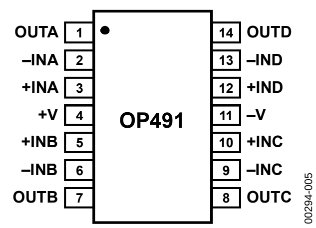

Figure 5. 14-Lead TSSOP

GENERAL DESCRIPTION

The OP191, OP291, and OP491 are single, dual, and quad micropower, single-supply, 3 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. All are guaranteed to operate from a +3 V single supply as well as ±5 V dual supplies.

Fabricated on Analog Devices CBCMOS process, the OPx91 family has a unique input stage that allows the input voltage to safely extend 10 V beyond either supply without any phase inversion or latch-up. The output voltage swings to within millivolts of the supplies and continues to sink or source current all the way to the supplies.

Applications for these amplifiers include portable tele-communications equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The OP191/OP291/OP491 are specified over the extended industrial –40°C to +125°C temperature range. The OP191 single and OP291 dual amplifiers are available in 8-lead plastic SOIC surface-mount packages. The OP491 quad is available in a 14-lead PDIP, a narrow 14-lead SOIC package, and a 14-lead TSSOP.

Rev. E

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

@ V_S = 3.0 V, V_{CM} = 0.1 V, V_O = 1.4 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP191G	V_{OS}			80	500	µV
		−40°C ≤ T_A ≤ +125°C			1	mV
OP291G/OP491G	V_{OS}			80	700	µV
		−40°C ≤ T_A ≤ +125°C			1.25	mV
Input Bias Current	I_B			30	65	nA
		−40°C ≤ T_A ≤ +125°C			95	nA
Input Offset Current	I_{OS}			0.1	11	nA
		−40°C ≤ T_A ≤ +125°C			22	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.9 V	70	90		dB
		−40°C ≤ T_A ≤ +125°C	65	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 2.7 V	25	70		V/mV
		−40°C ≤ T_A ≤ +125°C		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.95	2.99		V
		−40°C to +125°C	2.90	2.98		V
		R_L = 2 kΩ to GND	2.8	2.9		V
		−40°C to +125°C	2.70	2.80		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		−40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	75	mV
		−40°C to +125°C			130	mV
Short-Circuit Limit	I_{SC}	Sink/source	±8.75	±13.50		mA
		−40°C to +125°C	±6.0	±10.5		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		−40°C ≤ T_A ≤ +125°C	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		200	350	µA
		−40°C ≤ T_A ≤ +125°C		330	480	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	−SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		30		nV/√Hz
Current Noise Density	i_n			0.8		pA/√Hz

@ V_S = 5.0 V, V_{CM} = 0.1 V, V_O = 1.4 V, T_A = 25°C, unless otherwise noted. +5 V specifications are guaranteed by +3 V and ±5 V testing.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP191	V_{OS}			80	500	µV
		−40°C ≤ T_A ≤ +125°C			1.0	mV
OP291/OP491	V_{OS}			80	700	µV
		−40°C ≤ T_A ≤ +125°C			1.25	mV
Input Bias Current	I_B			30	65	nA
		−40°C ≤ T_A ≤ +125°C			95	nA
Input Offset Current	I_{OS}			0.1	11	nA
		−40°C ≤ T_A ≤ +125°C			22	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.9 V	70	93		dB
		−40°C ≤ T_A ≤ +125°C	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 4.7 V	25	70		V/mV
		−40°C ≤ T_A ≤ +125°C		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.95	4.99		V
		−40°C to +125°C	4.90	4.98		V
		R_L = 2 kΩ to GND	4.8	4.85		V
		−40°C to +125°C	4.65	4.75		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		−40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	75	mV
		−40°C to +125°C			155	mV
Short-Circuit Limit	I_{SC}	Sink/source	±8.75	±13.5		mA
		−40°C to +125°C	±6.0	±10.5		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		−40°C ≤ T_A ≤ +125°C	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		220	400	µA
		−40°C ≤ T_A ≤ +125°C		350	500	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	−SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
Current Noise Density	i_n			0.8		pA/√Hz

@ V_O = ±5.0 V, −4.9 V ≤ V_{CM} ≤ +4.9 V, T_A = +25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP191	V_{OS}			80	500	µV
		−40°C ≤ T_A ≤ +125°C			1	mV
OP291/OP491	V_{OS}			80	700	µV
		−40°C ≤ T_A ≤ +125°C			1.25	mV
Input Bias Current	I_B			30	65	nA
		−40°C ≤ T_A ≤ +125°C			95	nA
Input Offset Current	I_{OS}			0.1	11	nA
		−40°C ≤ T_A ≤ +125°C			22	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±5 V	75	100		dB
		−40°C ≤ T_A ≤ +125°C	67	97		dB
Large Signal Voltage Gain	A_{VO}	R_L = +10 kΩ, V_O = ±4.7 V	25	70		
		−40°C ≤ T_A ≤ +125°C		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 100 kΩ to GND	±4.93	±4.99		V
		−40°C to +125°C	±4.90	±4.98		V
		R_L = 2 kΩ to GND	±4.80	±4.95		V
		−40°C ≤ T_A ≤ +125°C	±4.65	±4.75		V
Short-Circuit Limit	I_{SC}	Sink/source	±8.75	±16.00		mA
		−40°C to +125°C	±6	±13		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V	80	110		dB
		−40°C ≤ T_A ≤ +125°C	75	100		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		260	420	µA
		−40°C ≤ T_A ≤ +125°C		390	550	µA
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L = 10 kΩ		0.5		V/µs
Full-Power Bandwidth	BW_P	1% distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
Current Noise Density	i_n			0.8		pA/√Hz

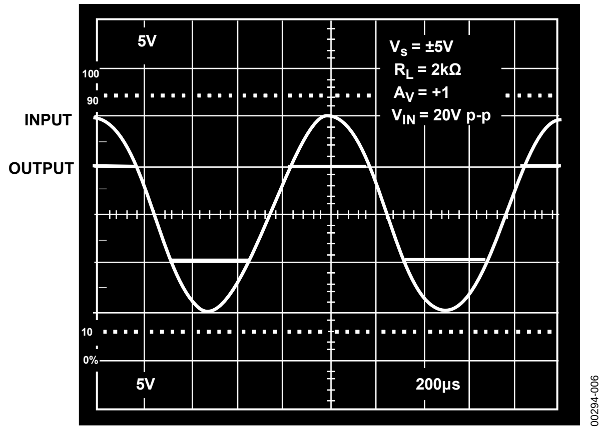


Figure 6. Input and Output with Inputs Overdriven by 5 V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	16 V
Input Voltage	GND to (V_S + 10 V)
Differential Input Voltage	7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
N, R, RU Packages	−65°C to +150°C
Operating Temperature Range	
OP191G/OP291G/OP491G	−40°C to +125°C
Junction Temperature Range	
N, R, RU Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for device in socket for PDIP packages; θ_{JA} is specified for device soldered in circuit board for TSSOP and SOIC packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R)	158	43	°C/W
14-Lead PDIP (N)	76	33	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

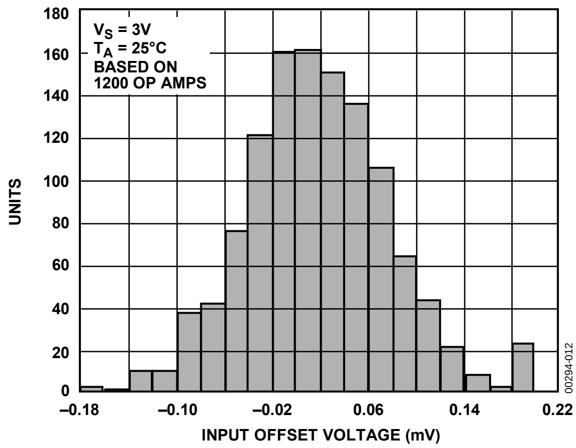


Figure 7. OP291 Input Offset Voltage Distribution, $V_S = 3$ V

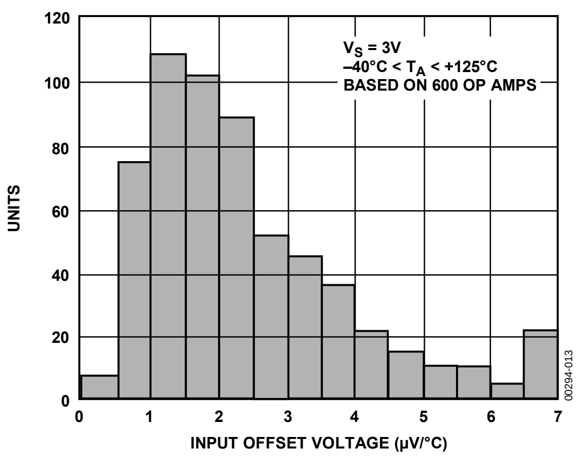


Figure 8. OP291 Input Offset Voltage Drift Distribution, $V_S = 3$ V

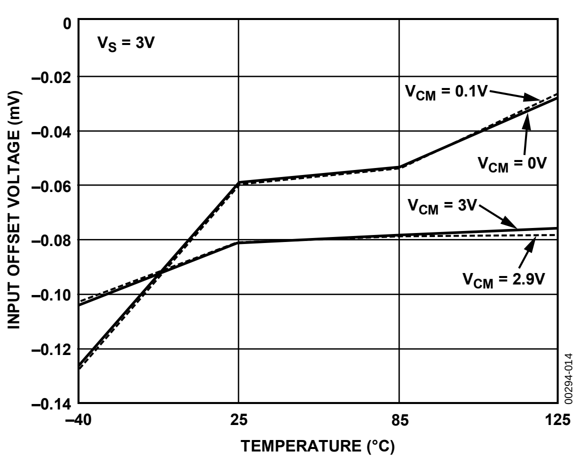


Figure 9. Input Offset Voltage vs. Temperature, $V_S = 3$ V

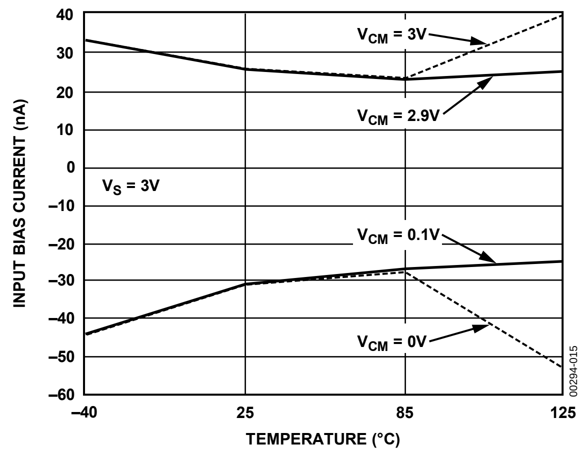


Figure 10. Input Bias Current vs. Temperature, $V_S = 3$ V

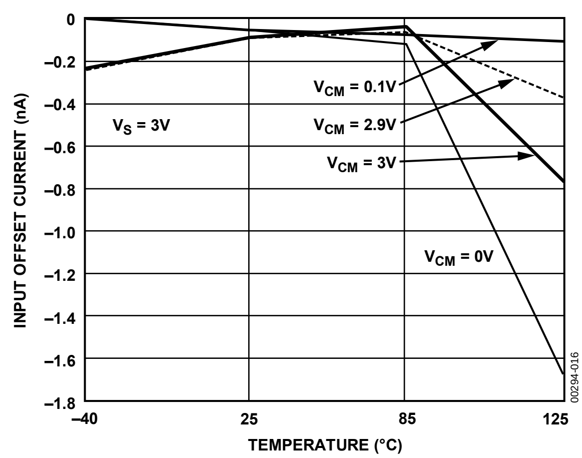


Figure 11. Input Offset Current vs. Temperature, $V_S = 3$ V

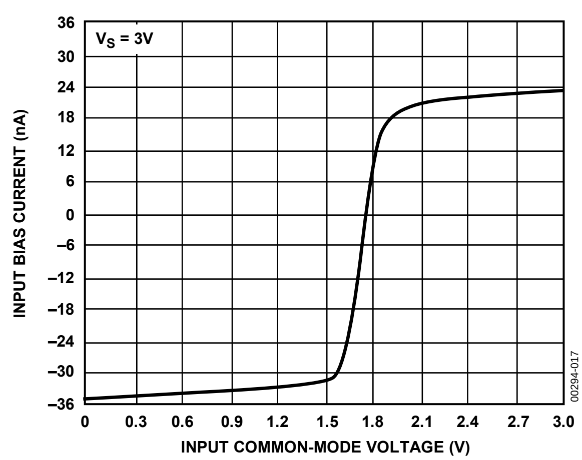


Figure 12. Input Bias Current vs. Input Common-Mode Voltage, $V_S = 3$ V

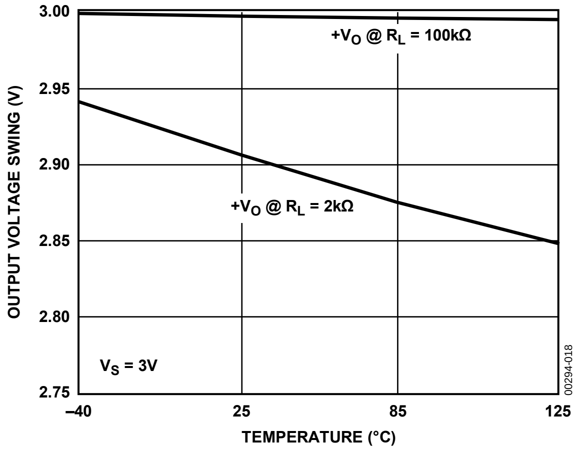


Figure 13. Output Voltage Swing vs. Temperature, $V_S = 3$ V

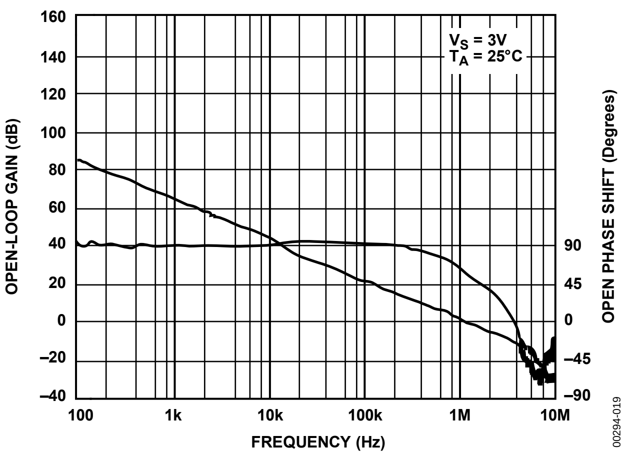


Figure 14. Open-Loop Gain and Phase vs. Frequency, $V_S = 3$ V

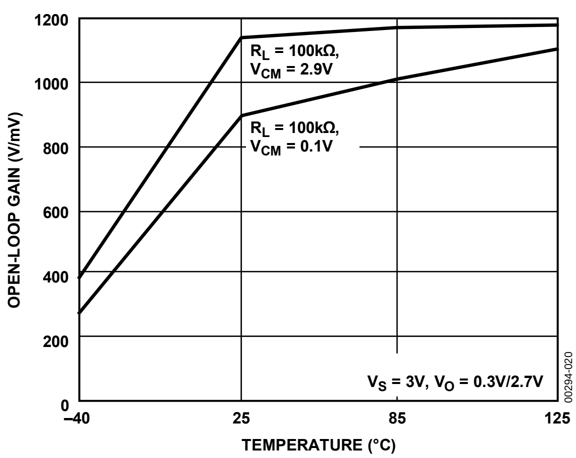


Figure 15. Open-Loop Gain vs. Temperature, $V_S = 3$ V

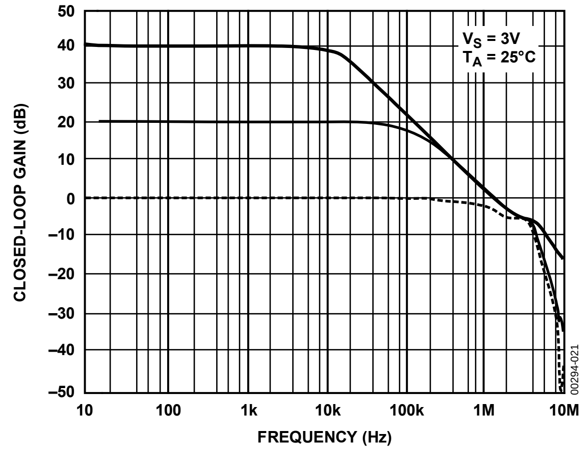


Figure 16. Closed-Loop Gain vs. Frequency, $V_S = 3$ V

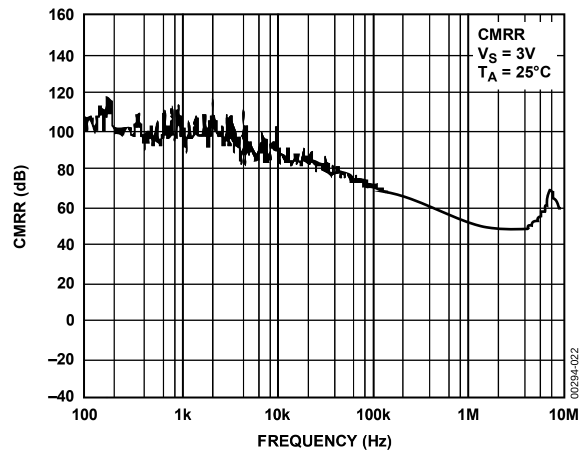


Figure 17. CMRR vs. Frequency, $V_S = 3$ V

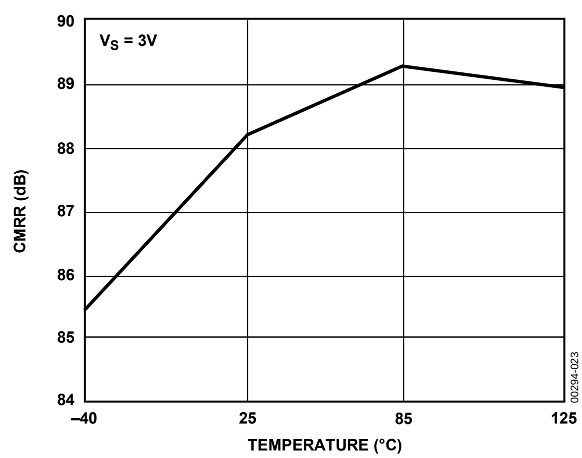


Figure 18. CMRR vs. Temperature, $V_S = 3$ V

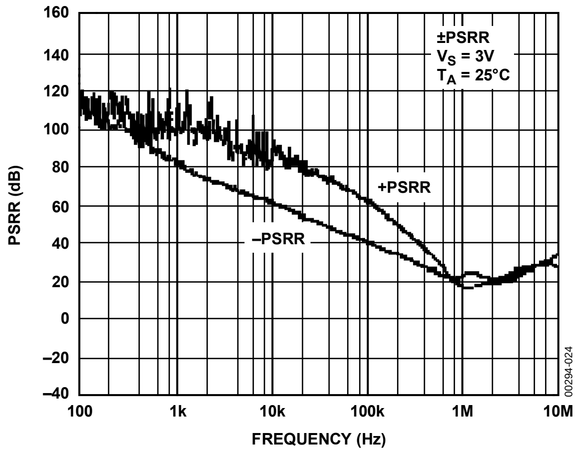


Figure 19. PSRR vs. Frequency, $V_S = 3$ V

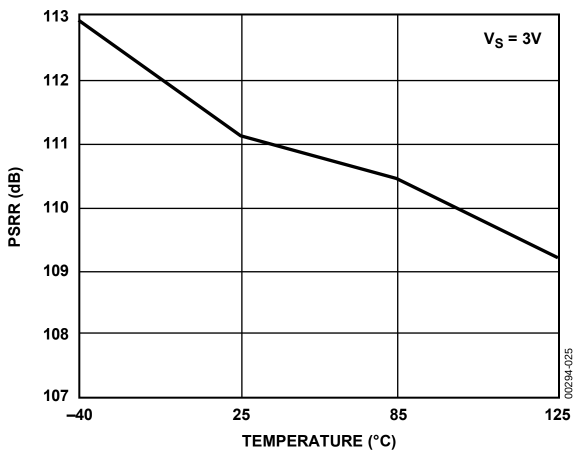


Figure 20. PSRR vs. Temperature, $V_S = 3$ V

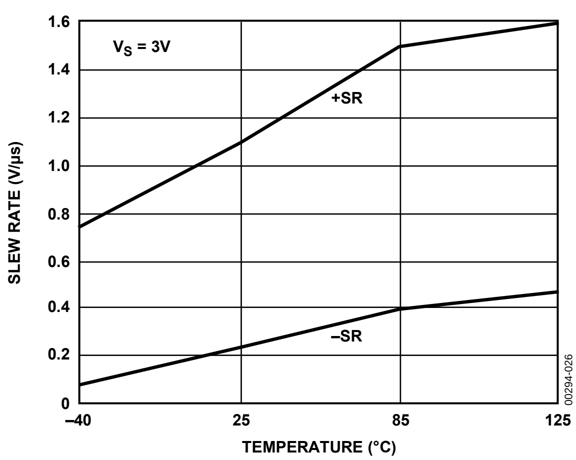


Figure 21. Slew Rate vs. Temperature, $V_S = 3$ V

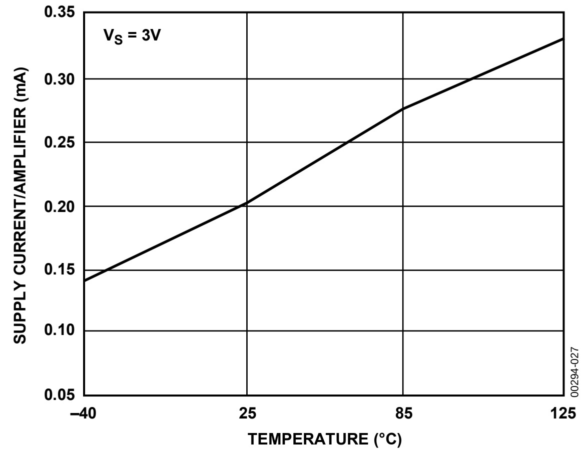


Figure 22. Supply Current vs. Temperature, $V_S = +3$ V, $+5$ V, ± 5 V

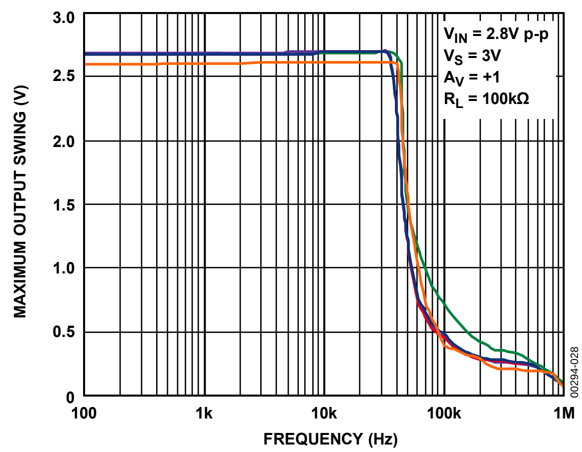


Figure 23. Maximum Output Swing vs. Frequency, $V_S = 3$ V

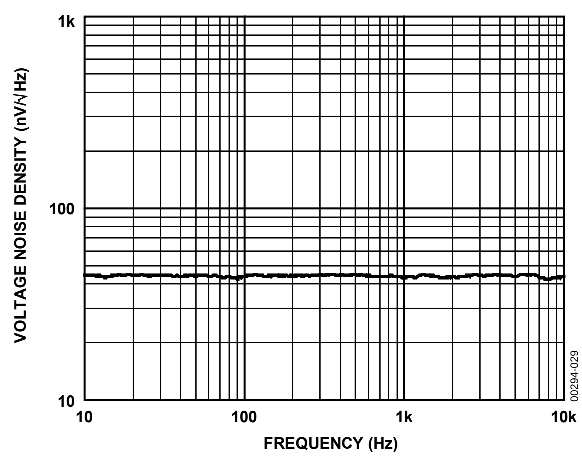


Figure 24. Voltage Noise Density, $V_S = 5$ V or ± 5 V

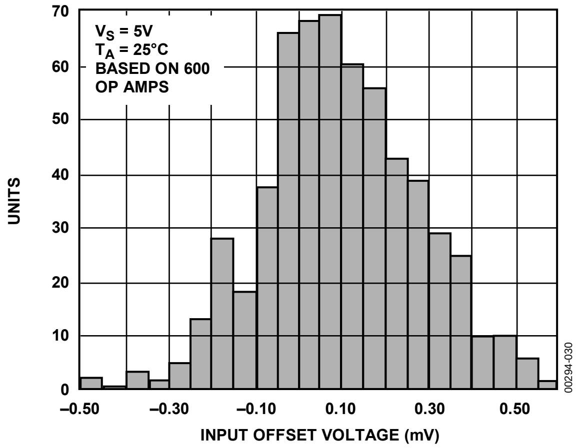


Figure 25. OP291 Input Offset Voltage Distribution, $V_S = 5$ V

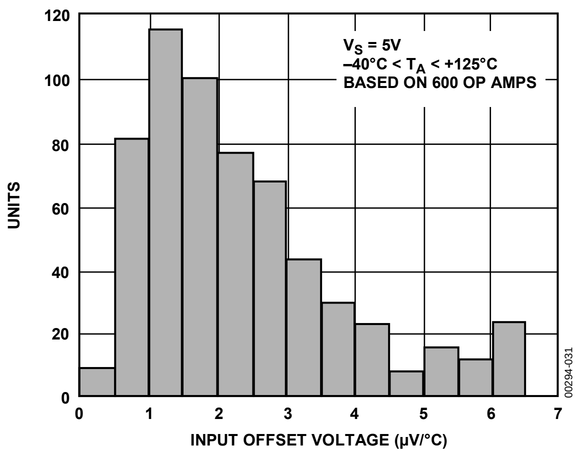


Figure 26. OP291 Input Offset Voltage Drift Distribution, $V_S = 5$ V

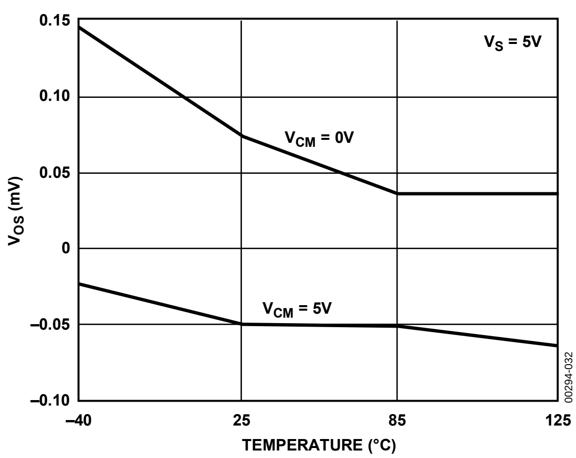


Figure 27. Input Offset Voltage vs. Temperature, $V_S = 5$ V

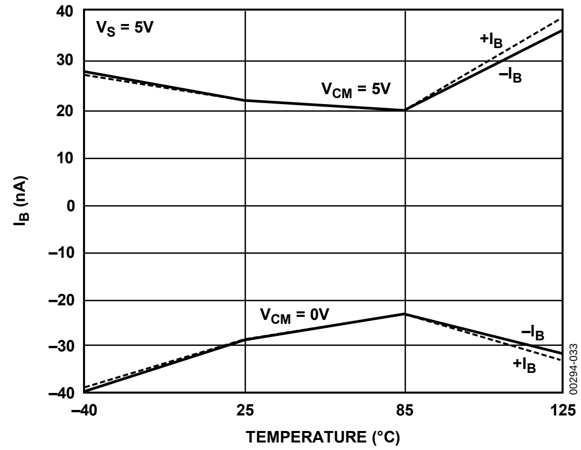


Figure 28. Input Bias Current vs. Temperature, $V_S = 5$ V

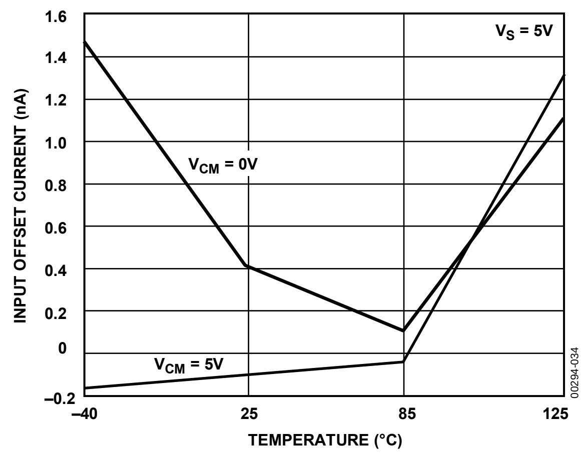


Figure 29. Input Offset Current vs. Temperature, $V_S = 5$ V

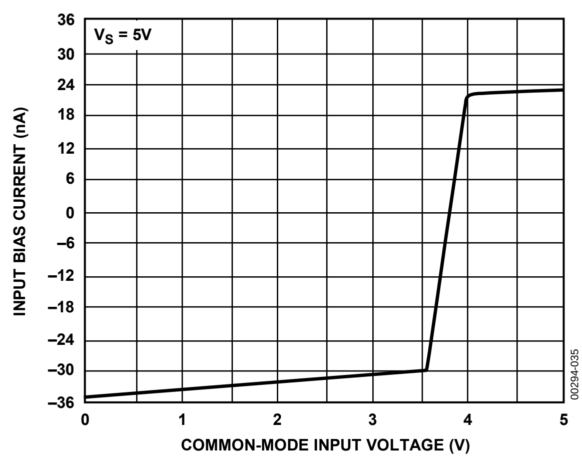


Figure 30. Input Bias Current vs. Common-Mode Input Voltage, $V_S = 5$ V

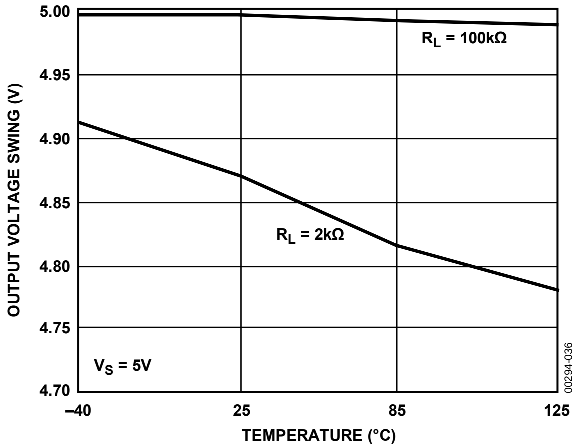


Figure 31. Output Voltage Swing vs. Temperature, $V_S = 5$ V

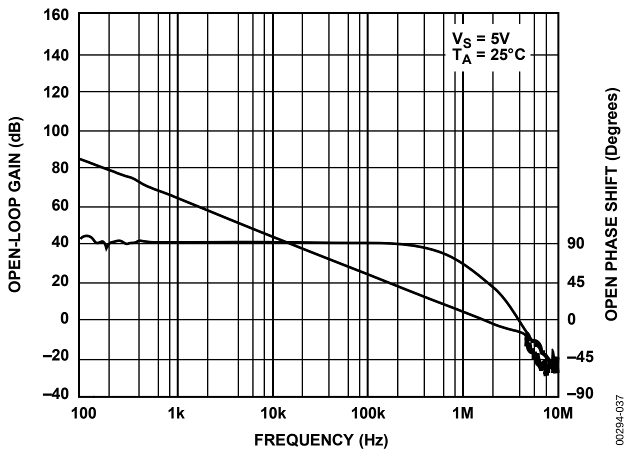


Figure 32. Open-Loop Gain and Phase vs. Frequency, $V_S = 5$ V

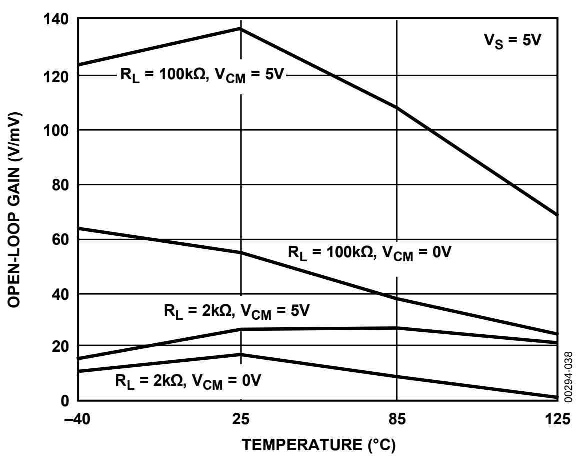


Figure 33. Open-Loop Gain vs. Temperature, $V_S = 5$ V

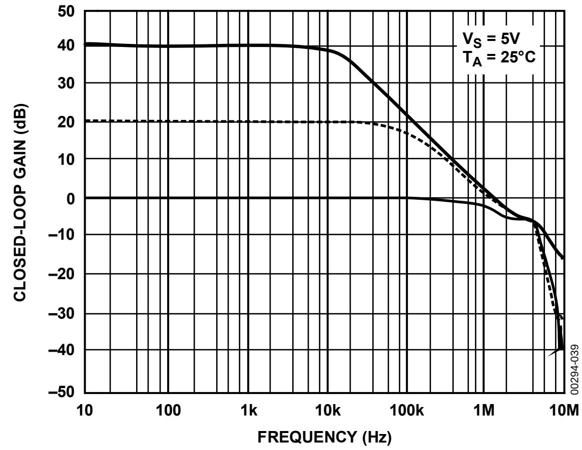


Figure 34. Closed-Loop Gain vs. Frequency, $V_S = 5$ V

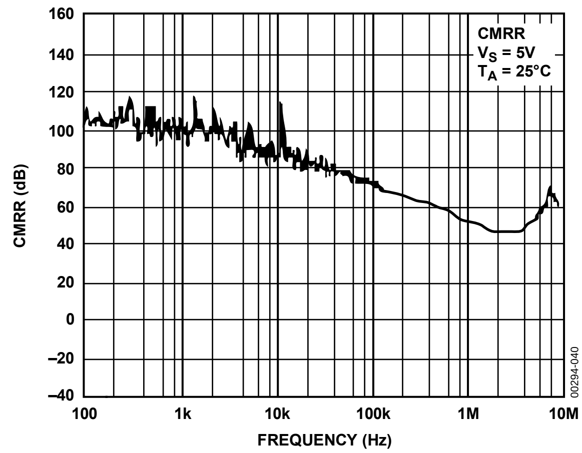


Figure 35. CMRR vs. Frequency, $V_S = 5$V

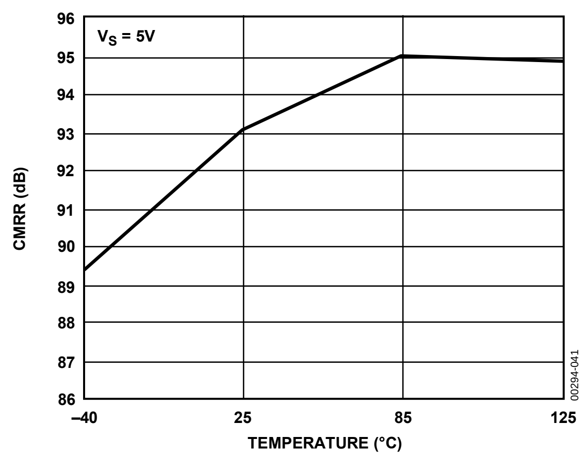


Figure 36. CMRR vs. Temperature, $V_S = 5$ V

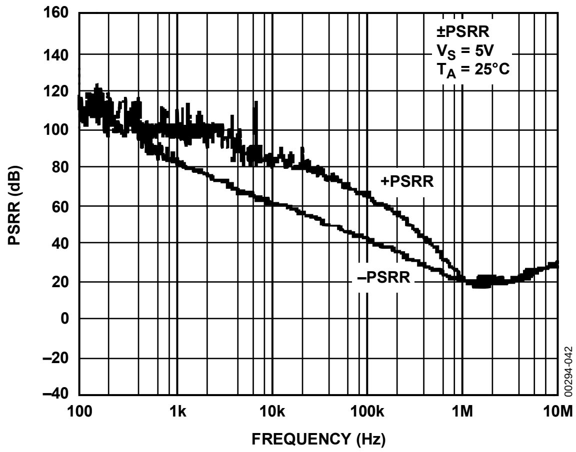


Figure 37. PSRR vs. Frequency, V_S = 5 V

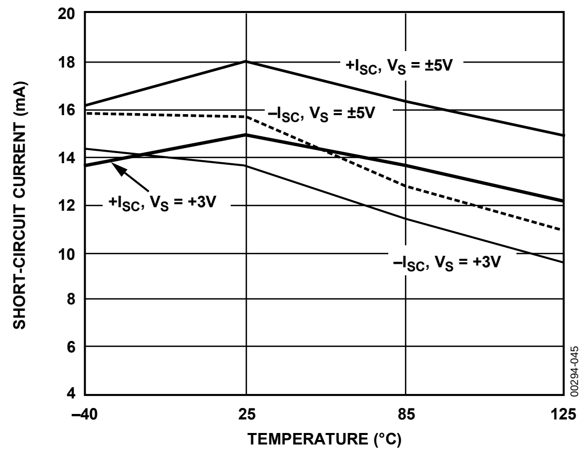


Figure 40. Short-Circuit Current vs. Temperature, V_S = +3 V, +5 V, ±5 V

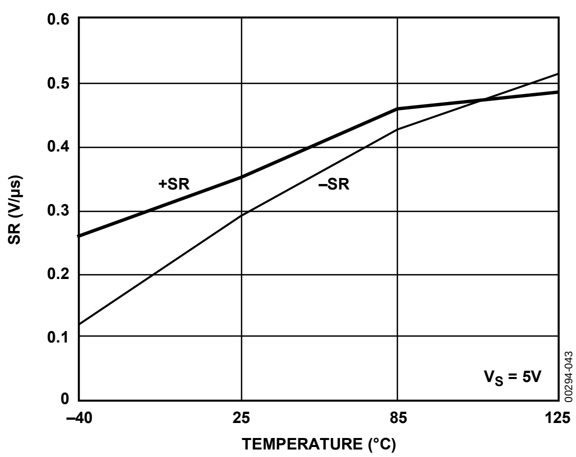


Figure 38. OP291 Slew Rate vs. Temperature, V_S = 5 V

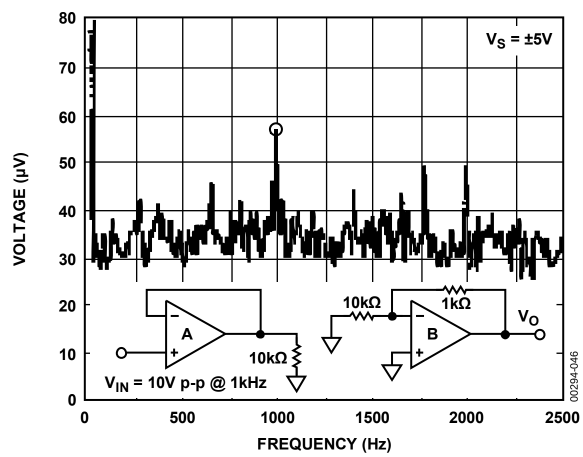


Figure 41. Channel Separation, V_S = ±5 V

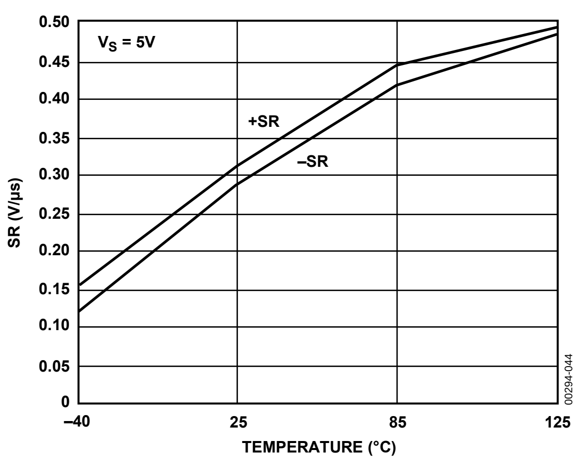


Figure 39. OP491 Slew Rate vs. Temperature, V_S = 5 V

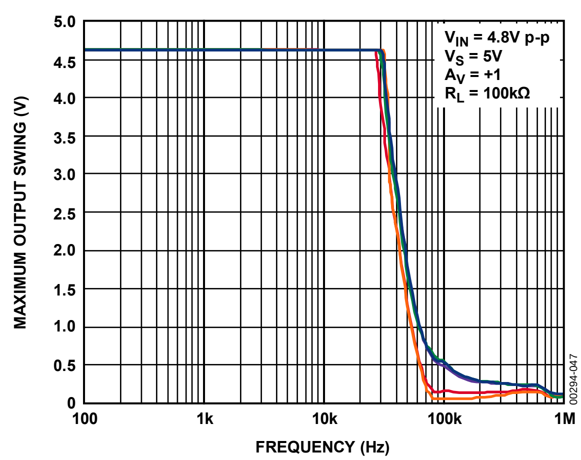


Figure 42. Maximum Output Swing vs. Frequency, V_S = 5 V

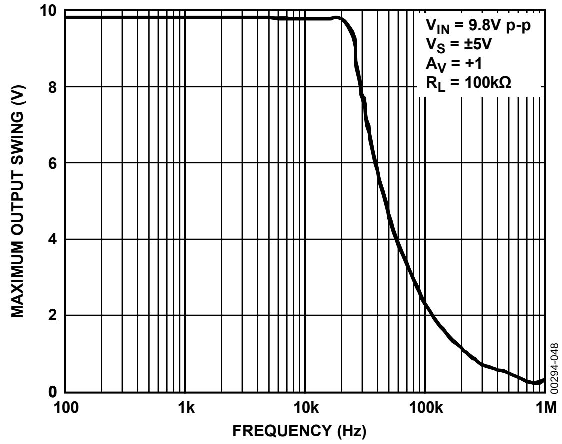


Figure 43. Maximum Output Swing vs. Frequency, $V_S = \pm5$ V

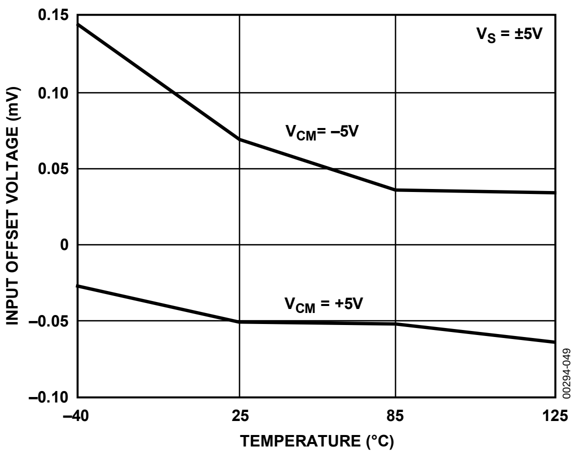


Figure 44. Input Offset Voltage vs. Temperature, $V_S = \pm5$ V

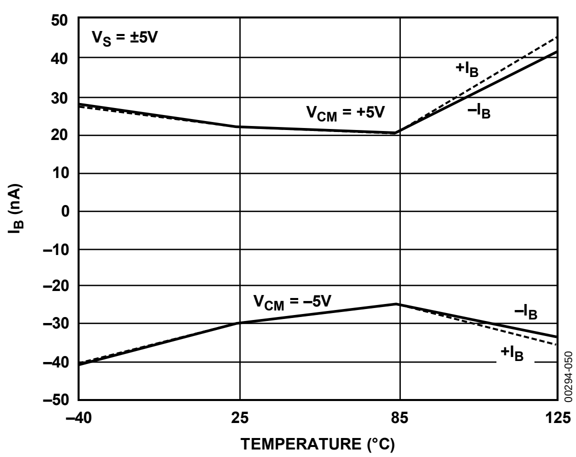


Figure 45. Input Bias Current vs. Temperature, $V_S = \pm5$ V

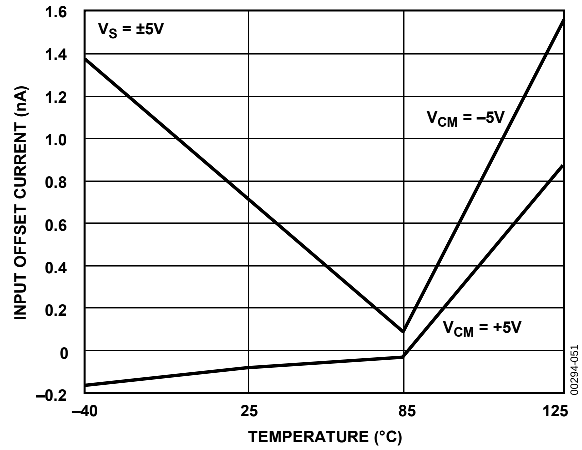


Figure 46. Input Offset Current vs. Temperature, $V_S = \pm5$ V

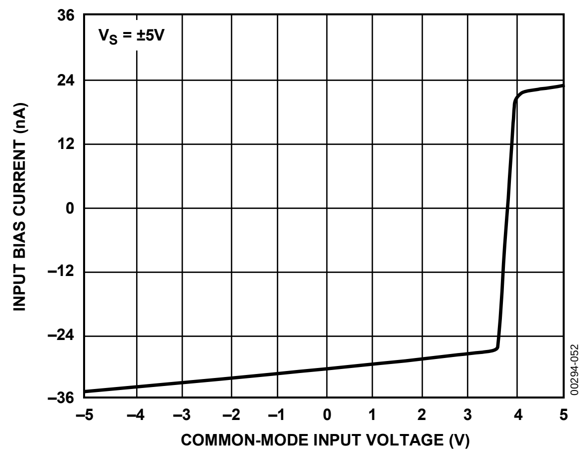


Figure 47. Input Bias Current vs. Common-Mode Voltage, $V_S = \pm5$ V

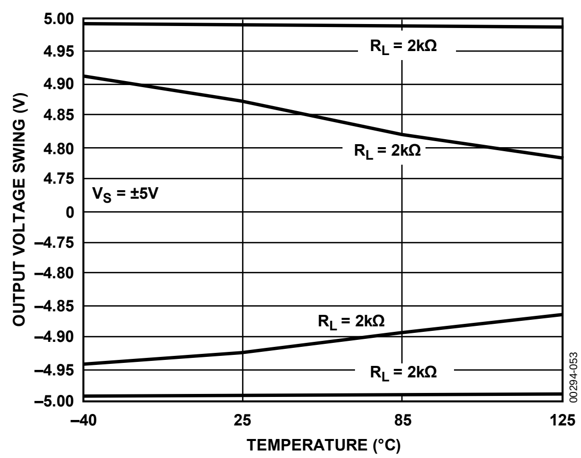


Figure 48. Output Voltage Swing vs. Temperature, $V_S = \pm5$ V

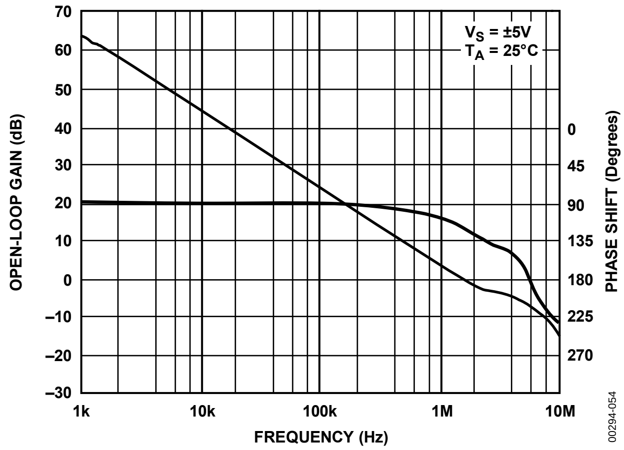


Figure 49. Open-Loop Gain and Phase vs. Frequency, $V_S = \pm 5$ V

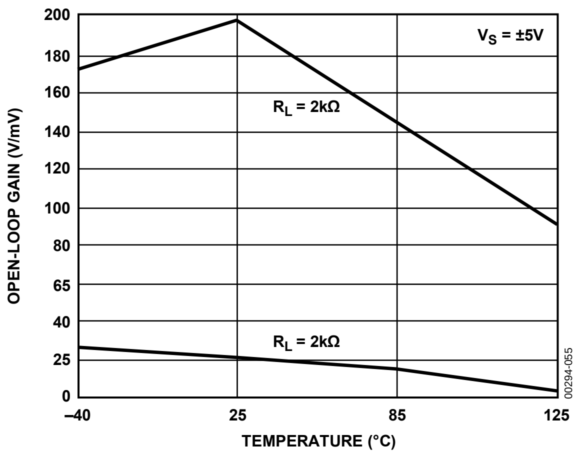


Figure 50. Open-Loop Gain vs. Temperature, $V_S = \pm 5$ V

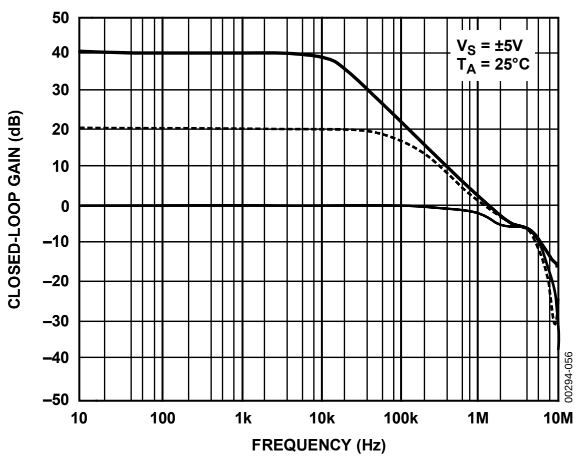


Figure 51. Closed-Loop Gain vs. Frequency, $V_S = \pm 5$ V

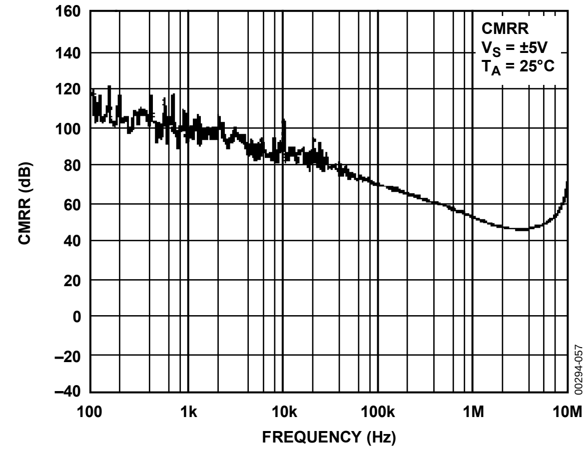


Figure 52. CMRR vs. Frequency, $V_S = \pm 5$ V

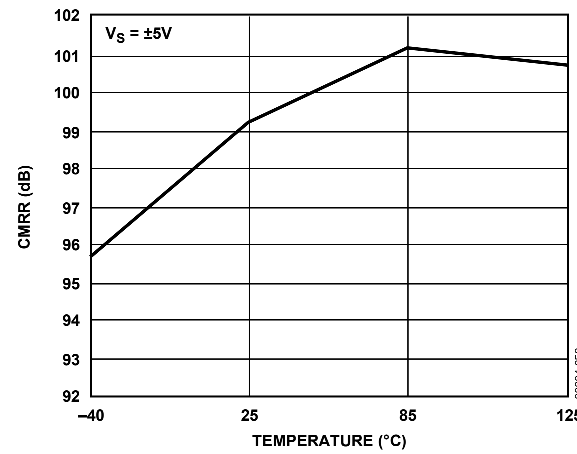


Figure 53. CMRR vs. Temperature, $V_S = \pm 5$ V

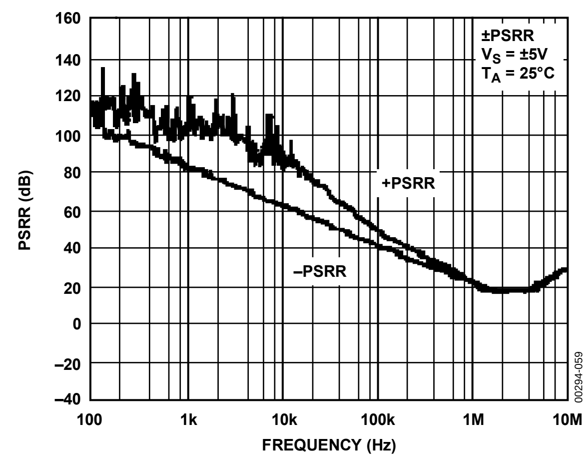


Figure 54. PSRR vs. Frequency, $V_S = \pm 5$ V

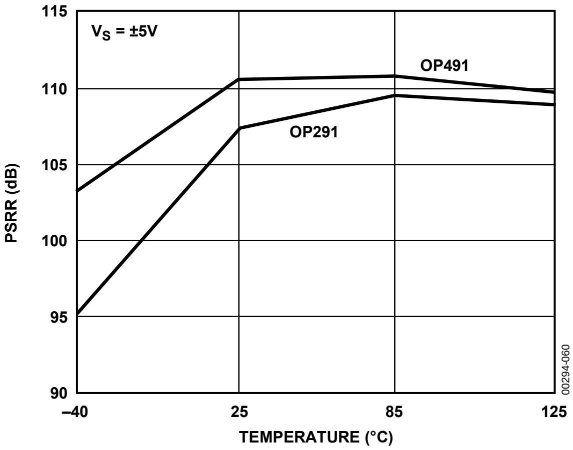


Figure 55. OP291/OP491 PSRR vs. Temperature, V_S = ±5 V

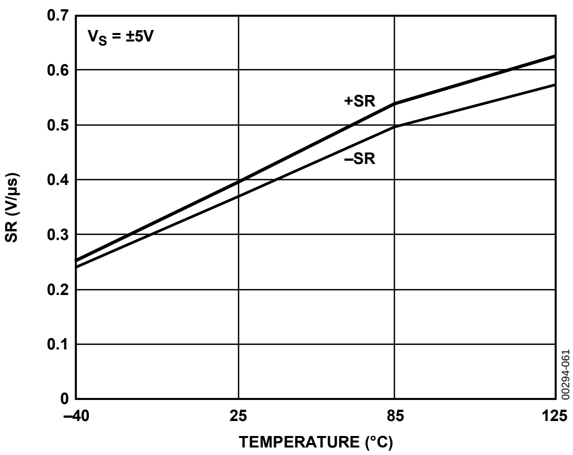


Figure 56. Slew Rate vs. Temperature, V_S = ±5 V

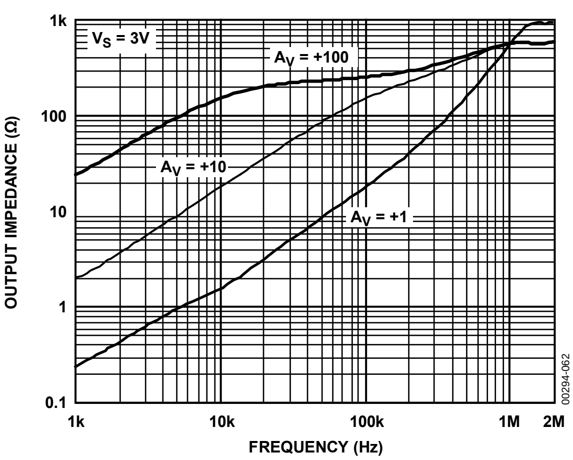


Figure 57. Output Impedance vs. Frequency

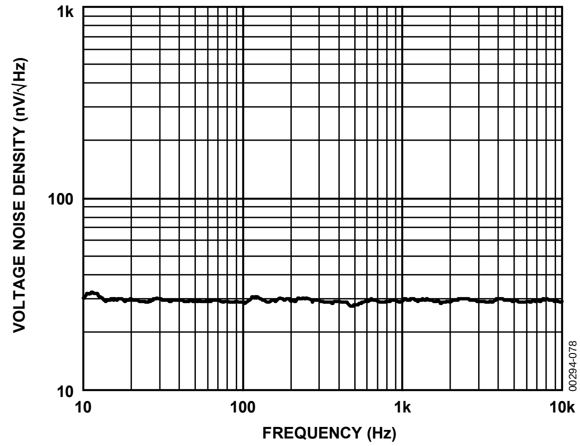


Figure 58. Voltage Noise Density, V_S = 3 V

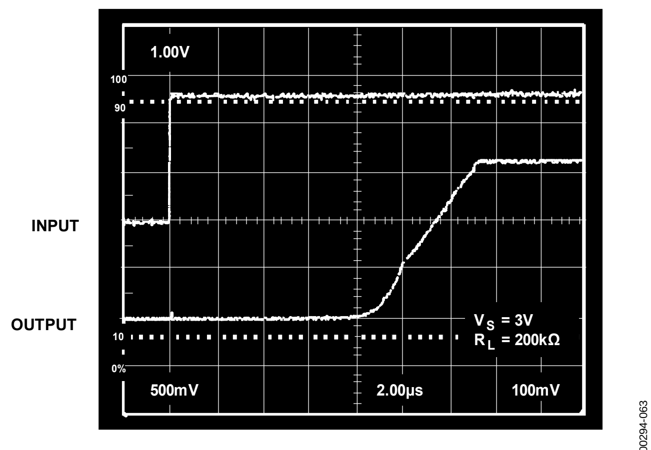


Figure 59. Large Signal Transient Response, V_S = 3 V

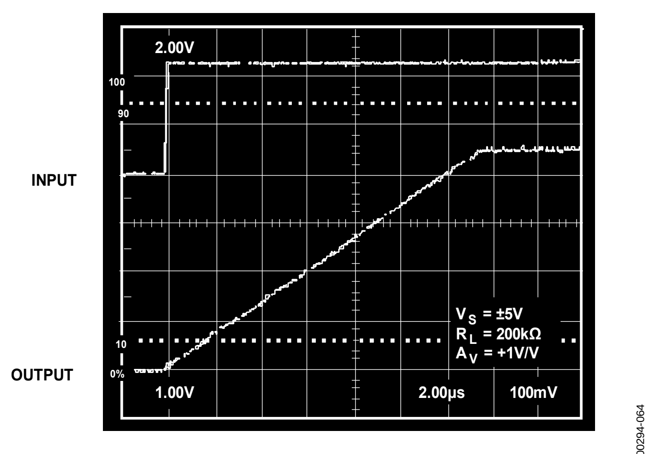


Figure 60. Large Signal Transient Response, V_S = ±5 V

THEORY OF OPERATION

The OP191/OP291/OP491 are single-supply, micropower amplifiers featuring rail-to-rail inputs and outputs. To achieve wide input and output ranges, these amplifiers employ unique input and output stages. In Figure 61 , the input stage comprises two differential pairs, a PNP pair and an NPN pair. These two stages do not work in parallel. Instead, only one stage is on for any given input signal level. The PNP stage (Transistor Q1 and Transistor Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. On the other hand, the NPN stage (Transistor Q5 and Transistor Q6) is needed for input voltages up to and including the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as is shown in Figure 12. Notice that the bias current switches direction at approximately 1.2 V to 1.3 V below the positive rail. At voltages below this, the bias current flows out of the OP291, indicating a PNP input stage. Above this voltage, however, the bias current enters the device, revealing the NPN stage. The actual mechanism within the amplifier for switching between the input stages comprises Transistor Q3, Transistor Q4, and Transistor Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually, the emitters of Q1 and Q2 are high enough to turn on Q3, which diverts the 8 μA of tail current away from the PNP input stage, turning it off. Instead, the current is mirrored through Q4 and Q7 to activate the NPN input stage.

Notice that the input stage includes 5 kΩ series resistors and differential diodes, a common practice in bipolar amplifiers to protect the input transistors from large differential voltages. These diodes turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current flows between the input pins, limited only by the two 5 kΩ resistors. This characteristic is important in circuits where the amplifier may be operated open-loop, such as a comparator. Evaluate each circuit carefully to make sure that the increase in current does not affect the performance.

The output stage in OP191 devices uses a PNP and an NPN transistor, as do most output stages; however, Q32 and Q33, the output transistors, are actually connected with their collectors to the output pin to achieve the rail-to-rail output swing. As the output voltage approaches either the positive or negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage does have inherent gain arising from the collectors and any external load impedance. Because of this, the open-loop gain of the amplifier is dependent on the load resistance.

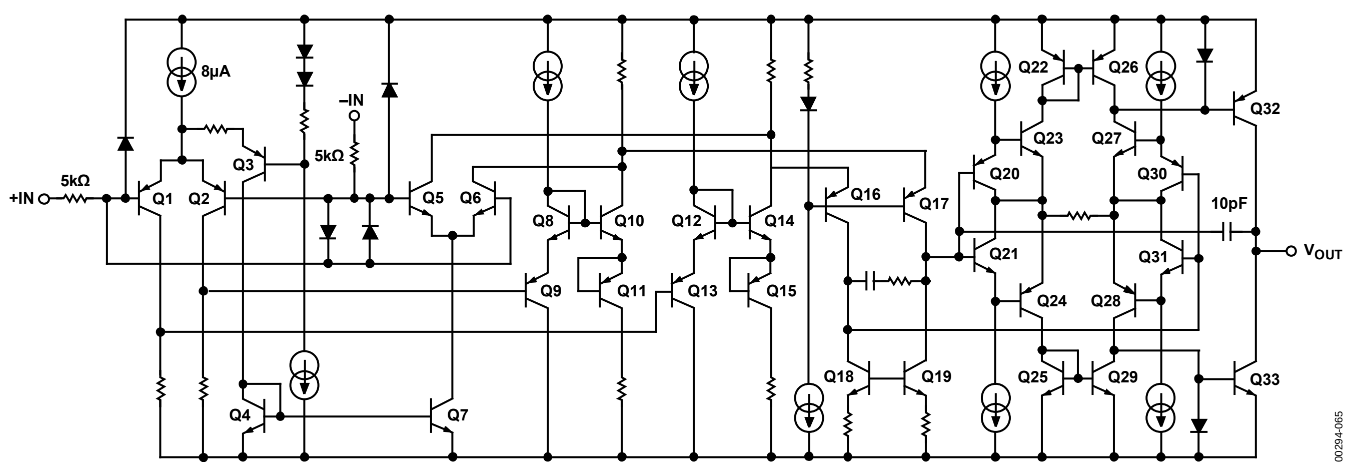


Figure 61. Simplified Schematic

INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, check the input overvoltage characteristic. When an overvoltage occurs, the amplifier could be damaged depending on the voltage level and the magnitude of the fault current. Figure 62 shows the characteristics for the OP191 family. This graph was generated with the power supplies at ground and a curve tracer connected to the input. When the input voltage exceeds either supply by more than 0.6 V, internal PN junctions energize, allowing current to flow from the input to the supplies. As described, the OP291/OP491 do have 5 kΩ resistors in series with each input to help limit the current. Calculating the slope of the current vs. voltage in the graph confirms the 5 kΩ resistor.

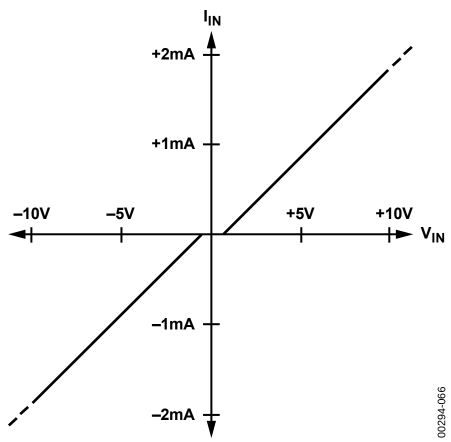


Figure 62. Input Overvoltage Characteristics

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. For an input of 10 V over the supply, the current is limited to 1.8 mA. If the voltage is large enough to cause more than 5 mA of current to flow, then an external series resistor should be added. The size of this resistor is calculated by dividing the maximum overvoltage by 5 mA and subtracting the internal 5 kΩ resistor. For example, if the input voltage could reach 100 V, the external resistor should be (100 V/5 mA) − 5 kΩ = 15 kΩ. This resistance should be placed in series with either or both inputs if they are subjected to the overvoltages.

OUTPUT VOLTAGE PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically, for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes with the anode connected to ground and the cathode to the inputs prevent input signal excursions from exceeding the device's negative supply (that is, GND), preventing a condition that could cause the output voltage to change phase. JFET input amplifiers can also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The OP191 is free from reasonable input voltage range restrictions due to its novel input structure. In fact, the input signal can exceed the supply voltage by a significant amount without causing damage to the device. As shown in Figure 64, the OP191 family can safely handle a 20 V p-p input signal on ±5 V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. Thus, no external clamping diodes are required.

OVERDRIVE RECOVERY

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large transient event, such as a comparator. The circuit shown in Figure 63 was used to evaluate the OPx91 overdrive recovery time. The OPx91 takes approximately 8 µs to recover from positive saturation and approximately 6.5 µs to recover from negative saturation.

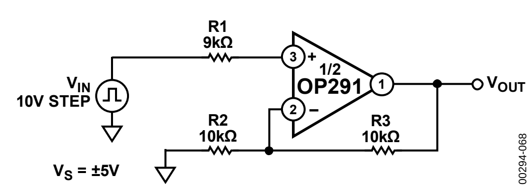


Figure 63. Overdrive Recovery Time Test Circuit

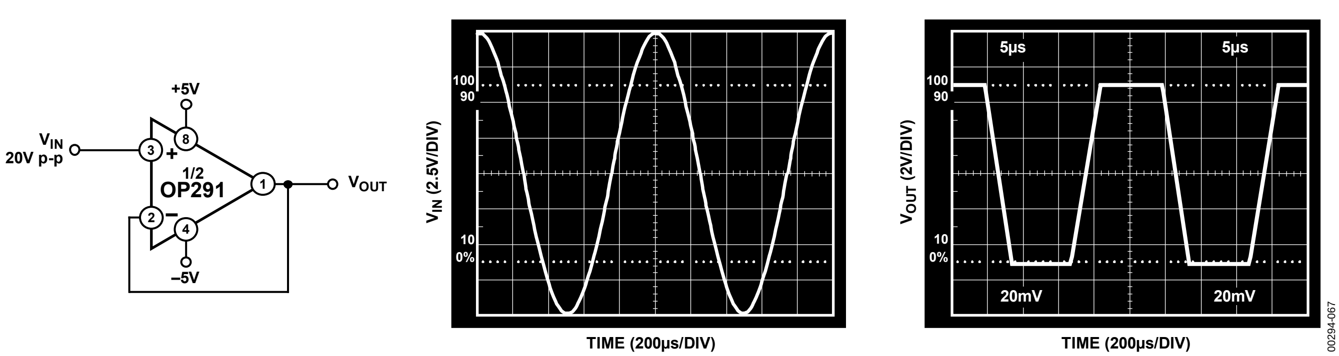


Figure 64. Output Voltage Phase Reversal Behavior

APPLICATIONS INFORMATION

SINGLE 3 V SUPPLY, INSTRUMENTATION AMPLIFIER

The OP291 low supply current and low voltage operation make it ideal for battery-powered applications, such as the instrumentation amplifier shown in Figure 65. The circuit uses the classic two op amp instrumentation amplifier topology, with four resistors to set the gain. The equation is simply that of a noninverting amplifier, as shown in Figure 65. The two resistors labeled R1 should be closely matched both to each other and to the two resistors labeled R2 to ensure good common-mode rejection performance. Resistor networks ensure the closest matching as well as matched drifts for good temperature stability. Capacitor C1 is included to limit the bandwidth and, therefore, the noise in sensitive applications. The value of this capacitor should be adjusted depending on the desired closed-loop bandwidth of the instrumentation amplifier. The RC combination creates a pole at a frequency equal to 1/(2π × R1C1). If AC-CMRR is critical, then a matched capacitor to C1 should be included across the second resistor labeled R1.

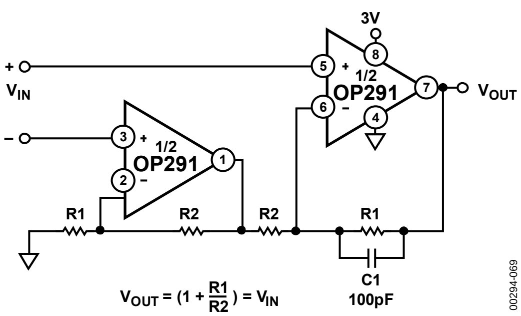


Figure 65. Single 3 V Supply Instrumentation Amplifier

Because the OP291 accepts rail-to-rail inputs, the input common-mode range includes both ground and the positive supply of 3 V. Furthermore, the rail-to-rail output range ensures the widest signal range possible and maximizes the dynamic range of the system. Also, with its low supply current of 300 µA/device, this circuit consumes a quiescent current of only 600 µA yet still exhibits a gain bandwidth of 3 MHz.

A question may arise about other instrumentation amplifier topologies for single-supply applications. For example, a variation on this topology adds a fifth resistor between the two inverting inputs of the op amps for gain setting. While that topology works well in dual-supply applications, it is inherently inappropriate for single-supply circuits. The same could be said for the traditional three op amp instrumentation amplifier. In both cases, the circuits simply cannot work in single-supply situations unless a false ground between the supplies is created.

SINGLE-SUPPLY RTD AMPLIFIER

The circuit in Figure 66 uses three op amps of the OP491 to develop a bridge configuration for an RTD amplifier that operates from a single 5 V supply. The circuit takes advantage of the OP491 wide output swing range to generate a high bridge excitation voltage of 3.9 V. In fact, because of the rail-to-rail output swing, this circuit works with supplies as low as 4.0 V. Amplifier A1 servos the bridge to create a constant excitation current in conjunction with the AD589, a 1.235 V precision reference. The op amp maintains the reference voltage across the parallel combination of the 6.19 kΩ and 2.55 MΩ resistors, which generate a 200 µA current source. This current splits evenly and flows through both halves of the bridge. Thus, 100 µA flows through the RTD to generate an output voltage based on its resistance. A 3-wire RTD is used to balance the line resistance in both 100 Ω legs of the bridge to improve accuracy.

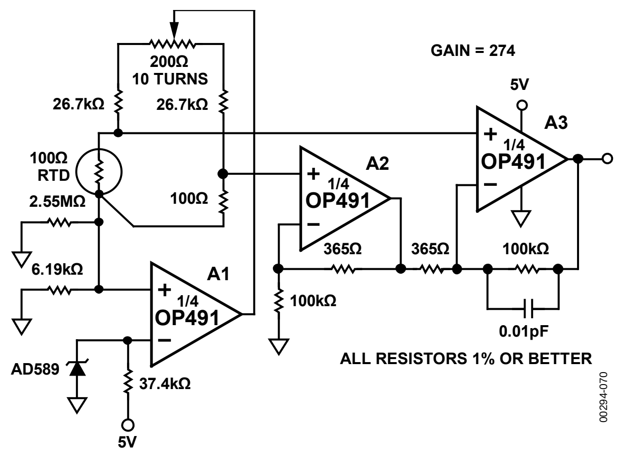


Figure 66. Single-Supply RTD Amplifier

Amplifier A2 and Amplifier A3 are configured in the two op amp instrumentation amplifier topology described in the Single 3 V Supply, Instrumentation Amplifier section. The resistors are chosen to produce a gain of 274, such that each 1°C increase in temperature results in a 10 mV change in the output voltage, for ease of measurement. A 0.01 µF capacitor is included in parallel with the 100 kΩ resistor on Amplifier A3 to filter out any unwanted noise from this high gain circuit. This particular RC combination creates a pole at 1.6 kHz.

A 2.5 V REFERENCE FROM A 3 V SUPPLY

In many single-supply applications, the need for a 2.5 V reference often arises. Many commercially available monolithic 2.5 V references require a minimum operating supply voltage of 4 V. The problem is exacerbated when the minimum operating system supply voltage is 3 V. The circuit illustrated in Figure 67 is an example of a 2.5 V reference that operates from a single 3 V supply. The circuit takes advantage of the OP291 rail-to-rail input and output voltage ranges to amplify an AD589 1.235 V output to 2.5 V. The OP291 low TCV_{OS} of 1 μV/°C helps maintain an output voltage temperature coefficient of less than 200 ppm/°C. The circuit overall temperature coefficient is dominated by the temperature coefficient of R2 and R3. Lower temperature coefficient resistors are recommended. The entire circuit draws less than 420 μA from a 3 V supply at 25°C.

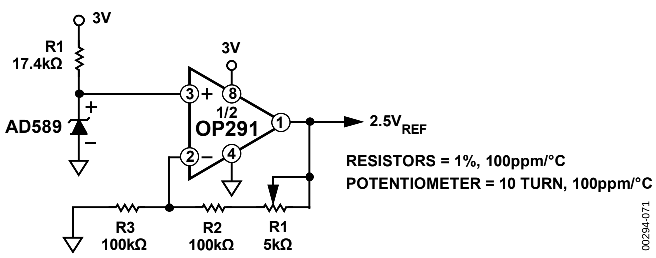


Figure 67. A 2.5 V Reference that Operates on a Single 3 V Supply

5 V ONLY, 12-BIT DAC SWINGS RAIL-TO-RAIL

The OPx91 family is ideal for use with a CMOS DAC to generate a digitally controlled voltage with a wide output range. Figure 68 shows the DAC8043 used in conjunction with the AD589 to generate a voltage output from 0 V to 1.23 V. The DAC is operated in voltage switching mode, where the reference is connected to the current output, I_{OUT}, and the output voltage is taken from the V_{REF} pin. This topology is inherently noninverting as opposed to the classic current output mode, which is inverting and, therefore, unsuitable for single supply.

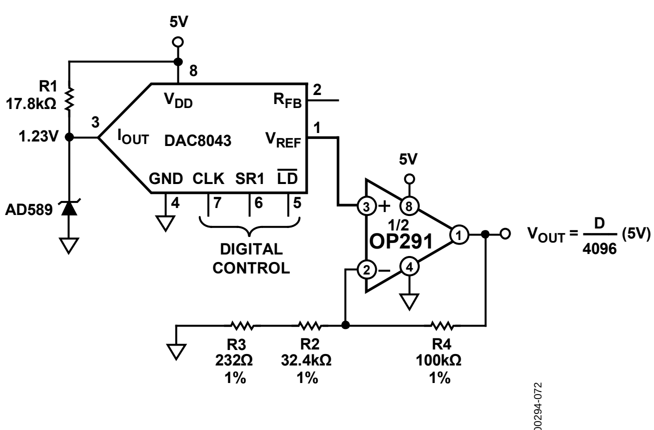


Figure 68. 5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP291 serves two functions. First, it is required to buffer the high output impedance of the DAC V_{REF} pin, which is on the order of 10 kΩ. The op amp provides a low impedance output to drive any following circuitry. Second, the op amp amplifies the output signal to provide a rail-to-rail output swing. In this particular case, the gain is set to 4.1 to generate a 5.0 V output when the DAC is at full scale. If other output voltage ranges are needed, such as 0 V to 4.095 V, the gain can easily be adjusted by altering the value of the resistors.

A HIGH-SIDE CURRENT MONITOR

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 69 is an example of a 5 V, single-supply, high-side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP291 rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET used as the feedback element in the circuit converts the op amp differential input voltage into a current. This current is then applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1}\right) \times I_L$$

For the element values shown, the monitor output transfer characteristic is 2.5 V/A.

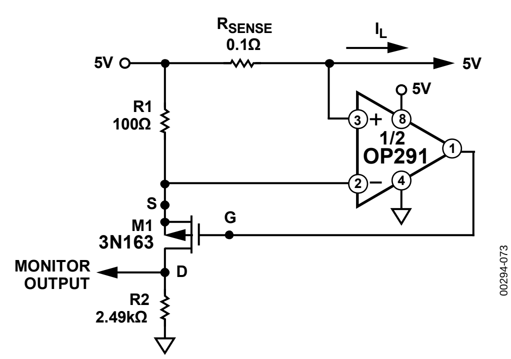


Figure 69. A High-Side Load Current Monitor

A 3 V, COLD JUNCTION COMPENSATED THERMOCOUPLE AMPLIFIER

The OP291 low supply operation makes it ideal for 3 V battery-powered applications such as the thermocouple amplifier shown in Figure 70. The K-type thermocouple terminates in an isothermal block where the junction ambient temperature is continuously monitored using a simple 1N914 diode. The diode corrects the thermal EMF generated in the junctions by feeding a small voltage, scaled by the 1.5 MΩ and 475 Ω resistors, to the op amp.

To calibrate this circuit, immerse the thermocouple measuring junction in a 0°C ice bath and adjust the 500 Ω potentiometer to 0 V out. Next, immerse the thermocouple in a 250°C temperature bath or oven and adjust the scale adjust potentiometer for an output voltage of 2.50 V. Within this temperature range, the K-type thermocouple is accurate to within ±3°C without linearization.

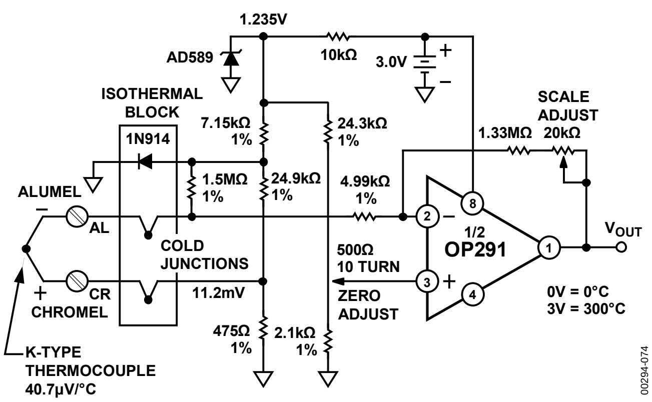


Figure 70. A 3 V, Cold Junction Compensated Thermocouple Amplifier

SINGLE-SUPPLY, DIRECT ACCESS ARRANGEMENT FOR MODEMS

An important building block in modems is the telephone line interface. In the circuit shown in Figure 71, a direct access arrangement is used to transmit and receive data from the telephone line. Amplifier A1 is the receiving amplifier; Amplifier A2 and Amplifier A3 are the transmitters. The fourth amplifier, A4, generates a pseudo ground halfway between the supply voltage and ground. This pseudo ground is needed for the ac-coupled bipolar input signals.

The transmit signal, TXA, is inverted by A2 and then reinverted by A3 to provide a differential drive to the transformer, where each amplifier supplies half the drive signal. This is needed because of the smaller swings associated with a single supply as opposed to a dual supply. Amplifier A1 provides some gain for the received signal, and it also removes the transmit signal present at the transformer from the received signal. To do this, the drive signal from A2 is also fed to the noninverting input of A1 to cancel the transmit signal from the transformer.

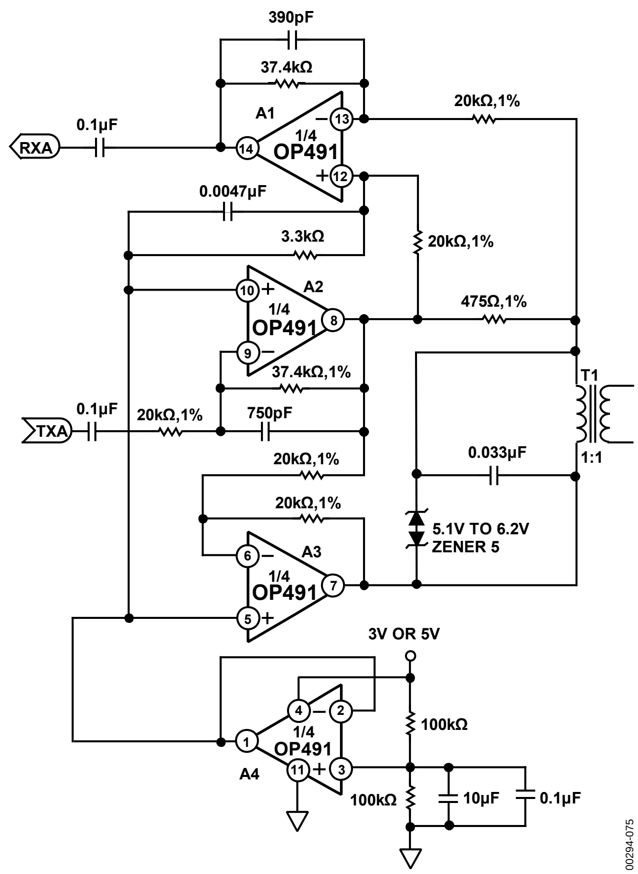


Figure 71. Single-Supply, Direct Access Arrangement for Modems

The OP491 bandwidth of 3 MHz and rail-to-rail output swings ensure that it can provide the largest possible drive to the transformer at the frequency of transmission.

3 V, 50 HZ/60 HZ ACTIVE NOTCH FILTER WITH FALSE GROUND

To process ac signals in a single-supply system, it is often best to use a false ground biasing scheme. Figure 72 illustrates a circuit that uses this approach. In this circuit, a false-ground circuit biases an active notch filter used to reject 50 Hz/60 Hz power line interference in portable patient monitoring equipment. Notch filters are quite commonly used to reject power line frequency interference that often obscures low frequency physiological signals, such as heart rates, blood pressure readings, EEGs, and EKGs. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. Substituting 3.16 kΩ resistors for the 2.67 kΩ resistors in the twin-T section (R1 through R5) configures the active filter to reject 50 Hz interference.

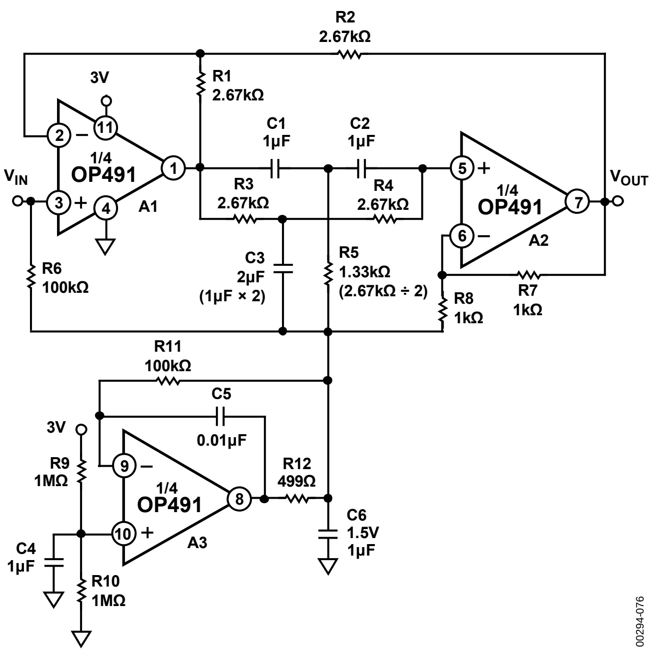


Figure 72. A 3 V Single-Supply, 50 Hz/60 Hz Active Notch Filter with False Ground

Amplifier A3 is the heart of the false ground bias circuit. It buffers the voltage developed by R9 and R10 and is the reference for the active notch filter. Because the OP491 exhibits a rail-to-rail input common-mode range, R9 and R10 are chosen to split the 3 V supply symmetrically. An in-the-loop compensation scheme used around the OP491 allows the op amp to drive C6, a 1 µF capacitor, without oscillation. C6 maintains a low impedance ac ground over the operating frequency range of the filter.

The filter section uses a pair of OP491s in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the pass band symmetry of the filter. Using 1% resistors and 5% capacitors produces satisfactory results.

SINGLE-SUPPLY, HALF-WAVE, AND FULL-WAVE RECTIFIERS

An OPx91 device configured as a voltage follower operating on a single supply can be used as a simple half-wave rectifier in low frequency (<2 kHz) applications. A full-wave rectifier can be configured with a pair of OP291s, as illustrated in Figure 73. The circuit works in the following way. When the input signal is above 0 V, the output of Amplifier A1 follows the input signal. Because the noninverting input of Amplifier A2 is connected to the output of A1, op amp loop control forces the inverting input of the A2 to the same potential. The result is that both terminals of R1 are equipotential; that is, no current flows. Because there is no current flow in R1, the same condition exists for R2; thus, the output of the circuit tracks the input signal. When the input signal is below 0 V, the output voltage of A1 is forced to 0 V. This condition now forces A2 to operate as an inverting voltage follower because the noninverting terminal of A2 is also at 0 V. The output voltage at $V_{OUT}A$ is then a full-wave rectified version of the input signal. If needed, a buffered, half-wave rectified version of the input signal is available at $V_{OUT}B$.

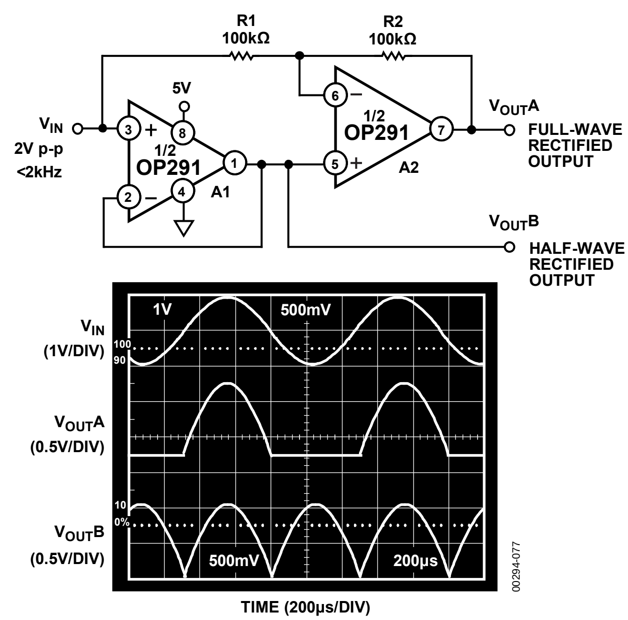
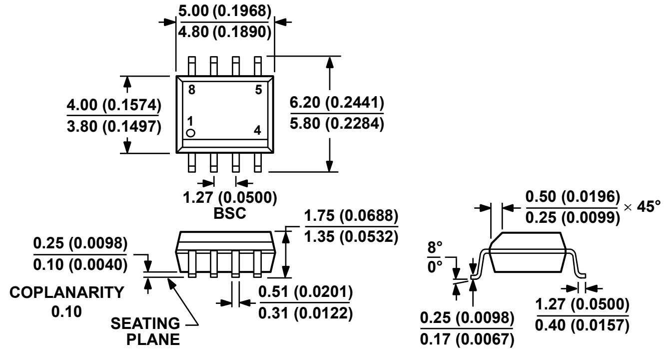


Figure 73. Single-Supply, Half-Wave, and Full-Wave Rectifiers Using an OP291

OUTLINE DIMENSIONS

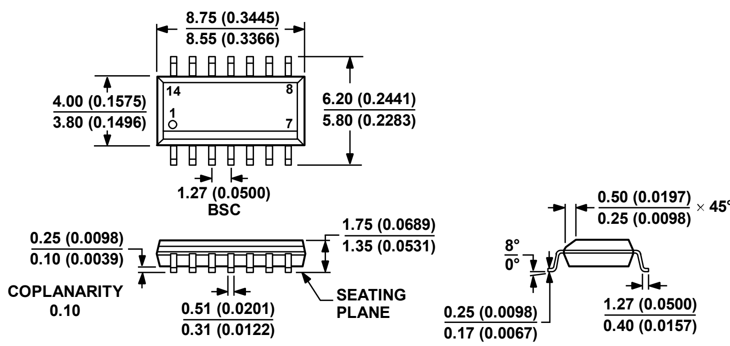


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 74. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8) [S-Suffix]
Dimensions shown in millimeters and (inches)

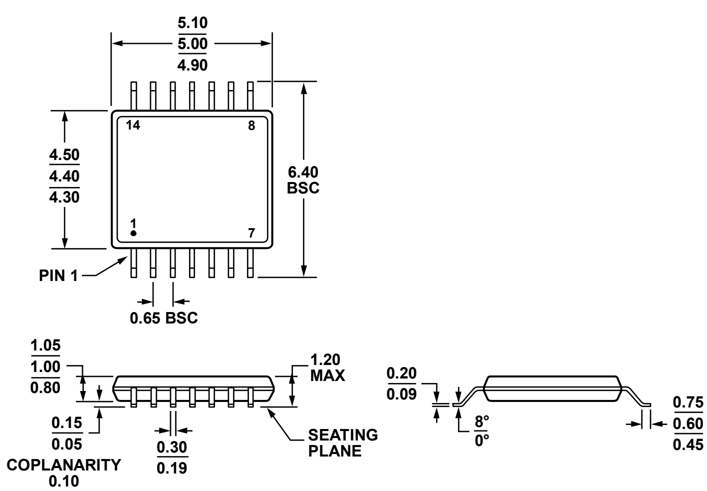


COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 75. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14) [S-Suffix]
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

061908-A

Figure 76. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

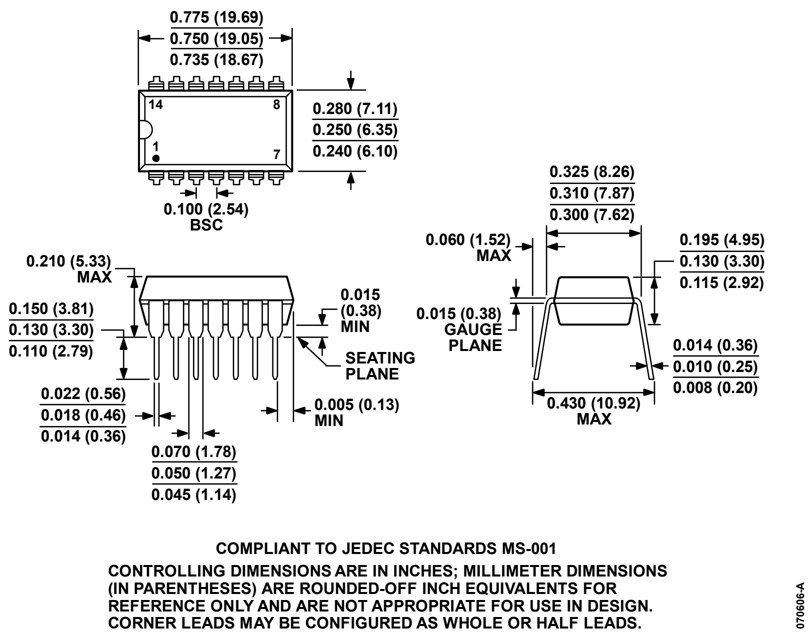


Figure 77. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
[P-Suffix]
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP191GS	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP191GS-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP191GS-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP191GSZ	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP191GSZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP191GSZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GS	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GS-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GS-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GSZ	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GSZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP291GSZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8 [S-Suffix]
OP491GP	−40°C to +125°C	14-Lead PDIP	N-14 [P-Suffix]
OP491GPZ	−40°C to +125°C	14-Lead PDIP	N-14 [P-Suffix]
OP491GRU-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14
OP491GRUZ-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14
OP491GS	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]
OP491GS-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]
OP491GS-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]
OP491GSZ	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]
OP491GSZ-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]
OP491GSZ-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14 [S-Suffix]

[1] Z = RoHS Compliant Part.

D00294-0-4/10(E)

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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