ML610Q178

The low power micro controller corresponding to 5v for household appliances

GENERAL DESCRIPTION

Equipped with a 8-bit CPU nX-U8/100, the ML610Q178 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Battery level detect circuit, LCD driver. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture.
In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system:16-bit instructions
  - Instruction set:Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 μs (at 32.768kHz system clock)
    Approx 0.122 μs (at 8.192MHz system clock)@V_{DD} = 2.2 to 5.5V

- Internal memory
  - Has 128-Kbyte flash ROM(64K × 16-bit) built in. (1K byte of test domain that it cannot be used is included)
  - Has 4-Kbyte RAM (4096 × 8 bits) built in.

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 23 maskable interrupt sources (Internal source: 19, External source: 4)

- Time base counter
  - Low-speed time base counter × 1 channel
  - High-speed time base counter × 1 channel

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 6ch (16-bit configuration available)

- PWM
  - Resolution 16 bits × 2 channel(IGBT control)

- Synchronous serial port
  - 2ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-duplex
  - TXD/RXD × 2 channels
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400kbit/s@4MHz), Standard mode (100kbit/s@4MHz)

- Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 16ch（Maximum）
  - Conversion time: 12.75μs per channel

- General-purpose ports ×74（Maximum）
  - Non-maskable interrupt input port × 1ch
  - Input-only port × 6ch
  - Output-only port × 8ch (including secondary functions)
  - Input/output × 27ch (including secondary functions)
  - Input/output × 32ch (including LCD driver functions)

- LCD driver
  - 160 dots max. (40 seg × 4 com), 1/1 to 1/4 duty
  - Frame frequency selecable (approx. 64Hz, 73Hz, 85Hz, 102Hz, 32Hz, 128Hz, 171Hz, and 256Hz)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Power supply voltage detect function
  - Judgment voltages: One of 4 levels
  - Judgment accuracy: ±2% (Typ.)

- Reset
  - Reset through the RESET_N pin
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.7kHz)
  - High-speed clock
    Built-in oscillation (8.192MHz), Crystal/Ceramic oscillation (8MHz), external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

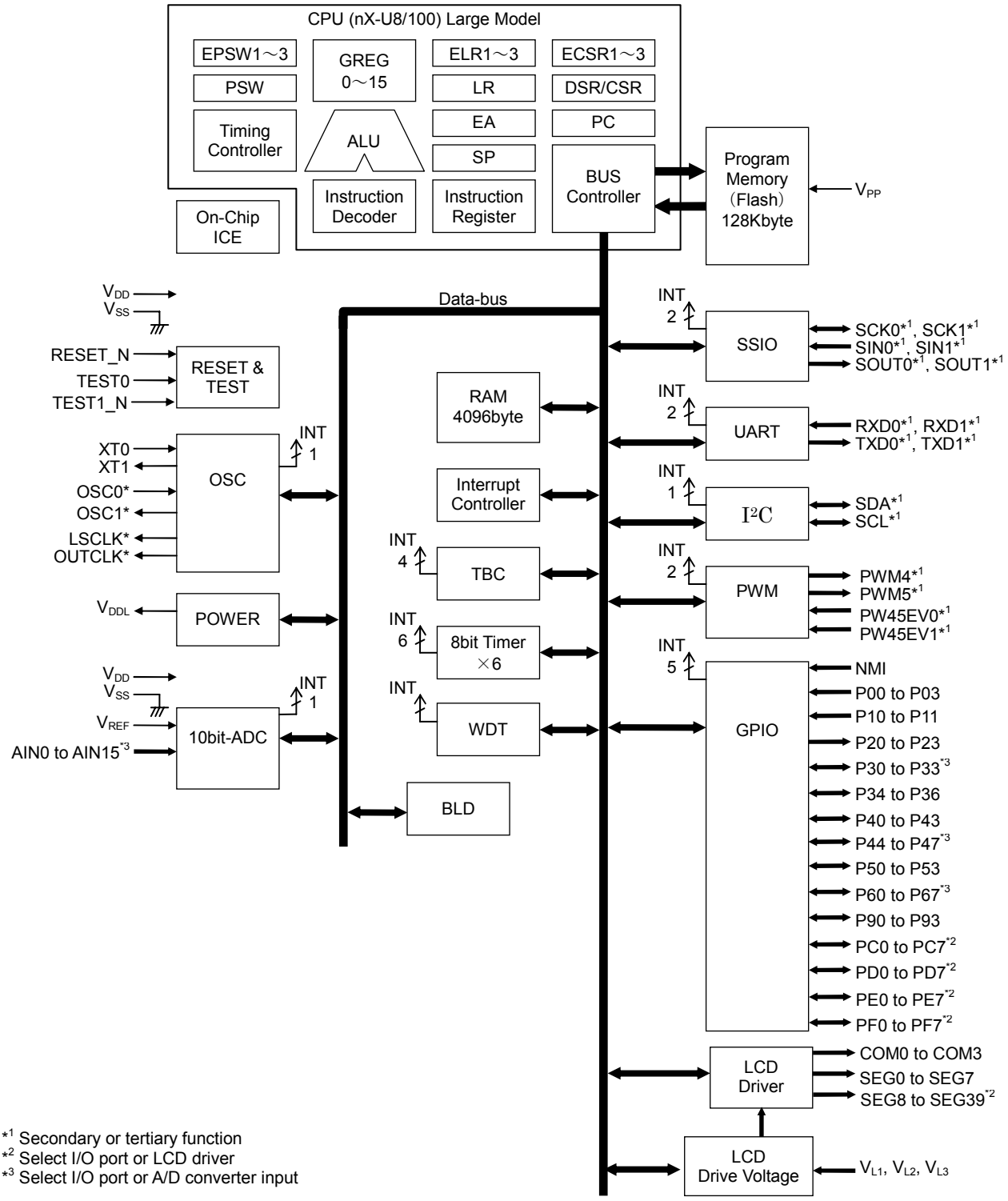
- Shipment
  - 100-pin QFP (QFP100-P-1420-0.65-BK)
  - ML610Q178-xxxGA (blank product: ML610Q178-NNNGA)

    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –40°C to 85°C
  - Operating voltage: V_{DD} = 2.2V to 5.5V, V_{REF} = 4.5V to 5.5V

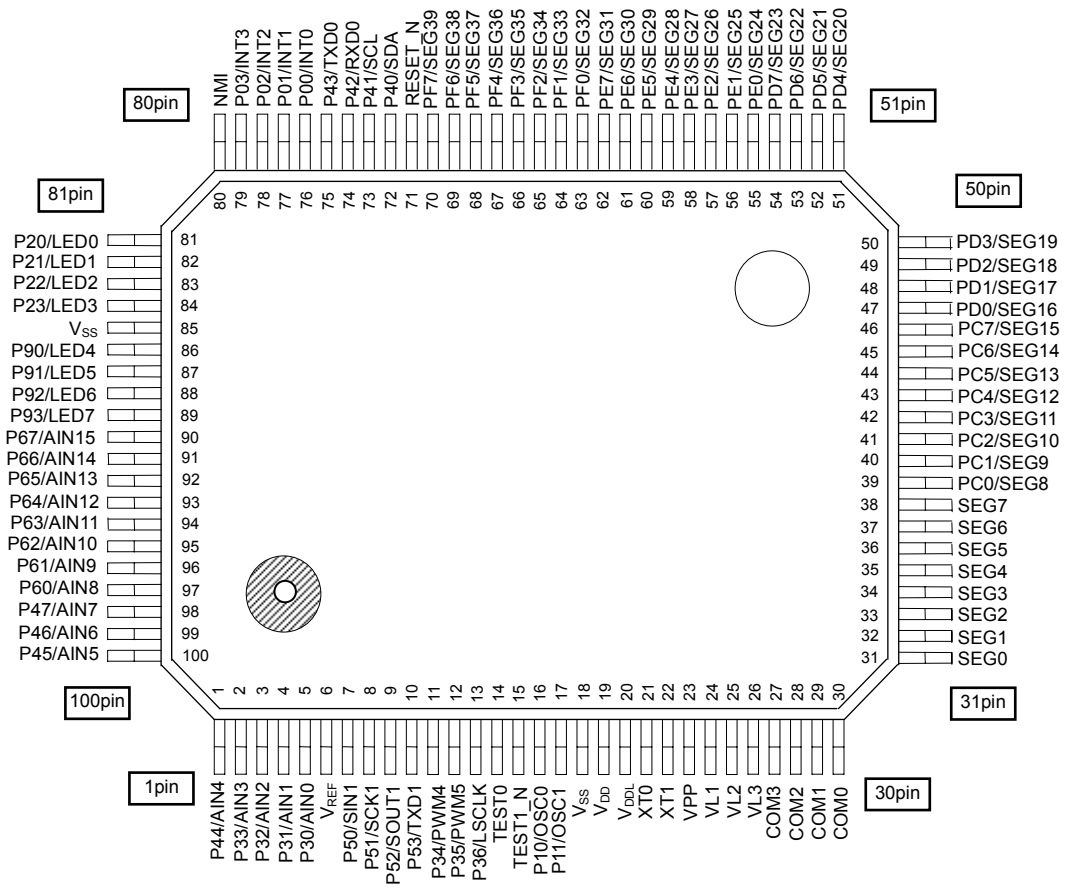
BLOCK DIAGRAM

Figure 1-1 is a block diagram of the ML610Q178.
Symbols with an asterisk "*" indicate that each of them is the secondary or tertiary function of the corresponding port.



PIN CONFIGURATION

ML610Q178 QFP package product



NC: No Connection

LIST OF PINS

Pin No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
18,85	Vss	—	Negative power supply pin	—	—	—	—	—	—
19	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
20	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
23	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
24	V_{L1}	—	Power supply pin for LCD bias	—	—	—	—	—	—
25	V_{L2}	—	Power supply pin for LCD bias	—	—	—	—	—	—
26	V_{L3}	—	Power supply pin for LCD bias	—	—	—	—	—	—
14	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—
15	TEST1_N	I/O	Input/output pin for testing	—	—	—	—	—	—
71	RESET_N	I	Reset input pin	—	—	—	—	—	—
21	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
22	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
6	V_{REF}	I	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—
80	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—
76	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—
77	P01/EXI1	I	Input port / External interrupt	—	—	—	—	—	—
78	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—
79	P03/EXI3/ RXD1	I	Input port / External interrupt / UART1 data input	—	—	—	—	—	—
16	P10	I	Input port	OSC0	I	High-speed clock oscillation pin	—	—	—
17	P11	I	Input port	OSC1	O	High-speed clock oscillation pin	—	—	—
81	P20/ LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	—	—	—
82	P21/ LED1	O	Output port / LED drive	OUTCLK	O	Low-speed clock output	—	—	—
83	P22/ LED2	O	Output port / LED drive	—	—	—	TM9OUT	O	Timer9 output
84	P23/ LED3	O	Output port / LED drive	—	—	—	TMBOUT	O	TimerB output

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
5	P30/ PW45EV1 /AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
4	P31/AIN1	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
3	P32/AIN2	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
2	P33/AIN3	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
11	P34	I/O	Input/output port	—	—	—	PWM4	O	PWM4 output	—	—	—
12	P35	I/O	Input/output port	—	—	—	PWM5	O	PWM5 output	—	—	—
13	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
72	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input	—	—	—
73	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
74	P42	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
75	P43	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UAR1 data output
1	P44/ T0P4CK/ AIN4	I/O	Input port / Timer0 / PWM4 external clock input/ Successive approximation type ADC input				SIN0	I	SSIO0 data input	—	—	—
100	P45/ T1P5CK/ AIN5	I/O	Input port / Timer1 / PWM5 external clock input/ Successive approximation type ADC input				SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
99	P46/ T8ACK/ AIN6	I	Input port / Timer8 / TimerA external clock input / Successive approximation type ADC input				SOUT0	O	SSIO0 data output	—	—	—
98	P47/ T9BCK/ AIN7	I	Input port / Timer9 / TimerB external clock input / Successive approximation type ADC input				PWM5	O	PWM5 output	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
7	P50	I/O	Input/output port	—	—	—	SIN1	I	SSIO1 data input	—	—	—
8	P51	I/O	Input/output port	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output	—	—	—
9	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT1	O	SSIO1 data output	—	—	—
10	P53	I/O	Input/output port	TXD1	O	UART1 data input	—	—	—	TXD0	O	UAR0 data output
97	P60/ AIN8	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
96	P61/ AIN9	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
95	P62/ AIN10	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
94	P63/ AIN11	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
93	P64/ AIN12	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
92	P65/ AIN13	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
91	P66/ AIN14	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
90	P67/ AIN15	I/O	Input/output port/ Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
86	P90/ LED4	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
87	P91/ LED5	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
88	P92/ LED6	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
89	P93/ LED7	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
30	COM0	O	LCD common pin	—	—	—	—	—	—	—	—	—
29	COM1	O	LCD common pin	—	—	—	—	—	—	—	—	—
28	COM2	O	LCD common pin	—	—	—	—	—	—	—	—	—
27	COM3	O	LCD common pin	—	—	—	—	—	—	—	—	—
31	SEG0	O	LCD segment pin	—	—	—	—	—	—	—	—	—
32	SEG1	O	LCD segment pin	—	—	—	—	—	—	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
33	SEG2	O	LCD segment pin	—	—	—	—	—	—	—	—	—
34	SEG3	O	LCD segment pin	—	—	—	—	—	—	—	—	—
35	SEG4	O	LCD segment pin	—	—	—	—	—	—	—	—	—
36	SEG5	O	LCD segment pin	—	—	—	—	—	—	—	—	—
37	SEG6	O	LCD segment pin	—	—	—	—	—	—	—	—	—
38	SEG7	O	LCD segment pin	—	—	—	—	—	—	—	—	—
39	PC0	I/O	Input/output port	SEG8	O	LCD segment pin	—	—	—	—	—	—
40	PC1	I/O	Input/output port	SEG9	O	LCD segment pin	—	—	—	—	—	—
41	PC2	I/O	Input/output port	SEG10	O	LCD segment pin	—	—	—	—	—	—
42	PC3	I/O	Input/output port	SEG11	O	LCD segment pin	—	—	—	—	—	—
43	PC4	I/O	Input/output port	SEG12	O	LCD segment pin	—	—	—	—	—	—
44	PC5	I/O	Input/output port	SEG13	O	LCD segment pin	—	—	—	—	—	—
45	PC6	I/O	Input/output port	SEG14	O	LCD segment pin	—	—	—	—	—	—
46	PC7	I/O	Input/output port	SEG15	O	LCD segment pin	—	—	—	—	—	—
47	PD0	I/O	Input/output port	SEG16	O	LCD segment pin	—	—	—	—	—	—
48	PD1	I/O	Input/output port	SEG17	O	LCD segment pin	—	—	—	—	—	—
49	PD2	I/O	Input/output port	SEG18	O	LCD segment pin	—	—	—	—	—	—
50	PD3	I/O	Input/output port	SEG19	O	LCD segment pin	—	—	—	—	—	—
51	PD4	I/O	Input/output port	SEG20	O	LCD segment pin	—	—	—	—	—	—
52	PD5	I/O	Input/output port	SEG21	O	LCD segment pin	—	—	—	—	—	—
53	PD6	I/O	Input/output port	SEG22	O	LCD segment pin	—	—	—	—	—	—
54	PD7	I/O	Input/output port	SEG23	O	LCD segment pin	—	—	—	—	—	—
55	PE0	I/O	Input/output port	SEG24	O	LCD segment pin	—	—	—	—	—	—
56	PE1	I/O	Input/output port	SEG25	O	LCD segment pin	—	—	—	—	—	—
57	PE2	I/O	Input/output port	SEG26	O	LCD segment pin	—	—	—	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
58	PE3	I/O	Input/output port	SEG27	O	LCD segment pin	—	—	—	—	—	—
59	PE4	I/O	Input/output port	SEG28	O	LCD segment pin	—	—	—	—	—	—
60	PE5	I/O	Input/output port	SEG29	O	LCD segment pin	—	—	—	—	—	—
61	PE6	I/O	Input/output port	SEG30	O	LCD segment pin	—	—	—	—	—	—
62	PE7	I/O	Input/output port	SEG31	O	LCD segment pin	—	—	—	—	—	—
63	PF0	I/O	Input/output port	SEG32	O	LCD segment pin	—	—	—	—	—	—
64	PF1	I/O	Input/output port	SEG33	O	LCD segment pin	—	—	—	—	—	—
65	PF2	I/O	Input/output port	SEG34	O	LCD segment pin	—	—	—	—	—	—
66	PF3	I/O	Input/output port	SEG35	O	LCD segment pin	—	—	—	—	—	—
67	PF4	I/O	Input/output port	SEG36	O	LCD segment pin	—	—	—	—	—	—
68	PF5	I/O	Input/output port	SEG37	O	LCD segment pin	—	—	—	—	—	—
69	PF6	I/O	Input/output port	SEG38	O	LCD segment pin	—	—	—	—	—	—
70	PF7	I/O	Input/output port	SEG39	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C_L) (see Measuring Circuit 1) between this pin and V_{SS} .	—	—
V_{PP}	—	Power supply pin for programming Flash ROM.	—	—
V_{L1}	—	Power supply pins for LCD bias (external input)	—	—
V_{L2}	—	Power supply pins for LCD bias (external input)	—	—
V_{L3}	—	Power supply pins for LCD bias (external input)	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I/O	Input/output pin for testing. Has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	—	—
XT1	O		—	—
OSC0	I	External input pin for high-speed clock. This function is allocated to the secondary function of the P10 pin.	Secondary	—
OSC1	O		Secondary	—
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20/P36 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P10 to P11	I			
General-output input port				
P20 to P23	O	General-purpose output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P90 to P93	O	General-purpose output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30 to P36	I/O	General-purpose input/output ports.Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P40 to P47				
P50 to P53				
PC0 to PC7		General-purpose input/output ports.Provided with a LCD segment for each port. Cannot be used as ports if LCD segment are used.		
PD0 to PD7				
PE0 to PE7				
PF0 to PF7				

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P43 pin and the fourthly function of the P53 pin.	Secondary Fourthly	Positive
RXD0	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the secondary function of the P42 pin.	Secondary	Positive
TXD1	O	UART1 data output pin. Allocated to the secondary function of the P53 pin and the fourthly function of the P43 pin.	Secondary Fourthly	Positive
RXD1	I	UART1 data input pin. Allocated to the primary function of the P03 pin and the secondary function of the P52 pin.	Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P44 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and P45 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and P46 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P50 pin .	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P51 pin.	Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P52 pin.	Tertiary	Positive
PWM				
PWM4	O	PWM4 output pin. Allocated to the tertiary function of the P34 and P43 pins.	Tertiary	Positive
PWM5	O	PWM5 output pin. Allocated to the tertiary function of the P35and P47 pins.	Tertiary	Positive
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
PW45EV0 PW45EV1	I	Control start /stop pin for PWM4 and PWM5. Allocated to the primary function of the P00 pin and P30 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0–EXI3	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P03 pins.	Primary	Positive/ Negative

Pin name	I/O	Description	Primary/ Secondary	Logic
Timer				
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
T8ACK	I	External clock input pin for timer 8 and timer A. Allocated to the primary function of the P46 pin.	Primary	—
T9BCK	I	External clock input pin for timer 9 and timer B. Allocated to the primary function of the P47 pin.	Primary	—
TM9OUT	O	Timer9 overflow output pin. Allocated to the secondary function of the P22 pin.	Tertiary	Positive
TMBOUT	O	TimerB overflow output pin. Allocated to the secondary function of the P23 pin.	Tertiary	Positive
LED drive				
LED0-LED7	O	Pins for LED driving. Allocated to the primary function of the P20–P23 pins and P90–P93 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0–AIN15	I	Analog inputs to Ch0–Ch15 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P33 and P44 to P47 and P60 to P67 pins.	Primary	—
LCD driver				
COM0 to COM3	O	LCD common output pins.	Primary	—
SEG0 to SEG7	O	LCD segment output pins.	Primary	—
SEG8 to SEG39	O	LCD segment output pins. Allocated to the secondary function of the PC0 to PC7 and PD0 to PD7 and PE0 to PE7 and PF0 to PF7 pins.	Secondary	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
V_{PP}	open
RESET_N	open
TEST0	open
TEST1_N	open
V_{REF}	Connect to V_{DD}
P00 to P03	Connect V_{DD} or V_{SS}
P10 to P11	Connect V_{DD} or V_{SS}
P20 to P23	open
P30 to P33 (AIN0 to AIN3)	open
P34 to P36	open
P40 to P43	open
P44 to P47 (AIN4 to AIN7)	open
P50 to P53	open
P60 to P67 (AIN8 to AIN15)	open
P90 to P93	open
COM0 to COM3	open
SEG0 to SEG7	open
PC0 to PC7（SEG8 to15）	open
PD0 to PD7（SEG16 to 23）	open
PE0 to PE7（SEG24 to 31）	open
PF0 to PF7（SEG32 to 39）	open

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 3	V_{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V_{L1}	Ta = 25°C	−0.3 to +2.33	V
Power supply voltage 5	V_{L2}	Ta = 25°C	−0.3 to +4.66	V
Power supply voltage 6	V_{L3}	Ta = 25°C	−0.3 to +7.0	V
Reference voltage	V_{REF}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3,4,5,6,C,D,E,F Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2,9 Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T_{STG}	—	−55 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +85	°C
Operating voltage	V_{DD}	—	2.2 to 5.5	V
Reference voltage	V_{REF}	—	4.5 to V_{DD}	V
Analog input voltage	V_{AI}	—	V_{SS} to V_{REF}	
Operating frequency (CPU)	f_{OP}	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Capacitor externally connected to V_{DD} pin	C_V	—	10±30%	μF
Capacitor externally connected to V_{PP} pin	C_1	—	1±30%	μF
Capacitor externally connected to V_{ref} pin	C_{AV}	—	1±30%	μF
Low-speed crystal oscillation external capacitor	C_{DL}	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C_{GL}		12 to 25	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	8M/8.192M	Hz
High-speed crystal oscillation external capacitor*	C_{DH}	—	47±30%	pF
	C_{GH}	—	47±30%	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	μF

* C_{GH} and C_{DH} are built into, external capacity is unnecessary for CSTLS8M00G56 (made by Murata Mfg.).

Flash Memory Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.7 to 5.5	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase[1]	7.7 to 8.3	
Maximum rewrite count	C_{EP}	—	80	times
Data retention period	Y_{DR}	—	10	years

*1: At the writing of a flash ROM, it is necessary to supply voltage to V_{DDL} pin within the limits of the above-mentioned regulation. Pulldown resistance is built in the V_{PP} pin.

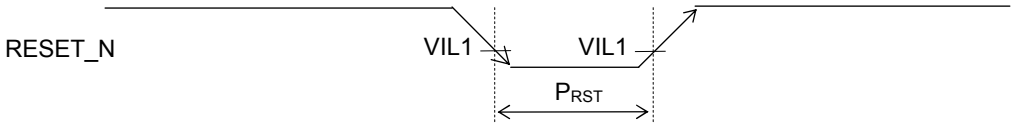
DC Characteristics (1 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed crystal oscillation start time	T_{XTH}	—	—	2	20	ms	1
Low-speed crystal oscillation start time*2	T_{XTL}	—	—	0.6	2	s	
Low-speed RC oscillator frequency	f_{LCR}	Ta= -10 to 60°C	Typ -5%	32.7k	Typ +5%	Hz	
PLL oscillation frequency	f_{PLL}	LSCLK=32.768kHz 100 clock average	Typ -1%	8.192	Typ +1%	MHz	
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		

*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance C_{GL}/C_{DL}＝12pF.

Reset



Reset by RESET_N pin

DC Characteristics (2 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	Ta = 25°C	LD3 to 0 = 0H	Typ. -2%	2.35	Typ. +2%	V	1
			LD3 to 0 = 3H		2.80			
			LD3 to 0 = 9H		3.70			
			LD3 to 0 = FH		4.60			

DC Characteristics (3 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state Low-speed/high-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	0.7	6	μA	1
			-40 to +85°C	—	0.7	22		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WBC: Operating*2) High-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	2.0	7		
			-40 to +85°C	—	2.0	24		
Supply current 3	IDD3	CPU: Running at 32kHz*1 High-speed oscillation: Stopped V_{DD}=3.0V	-40 to +35°C	—	13	20		
			-40 to +85°C	—	13	42		
Supply current 4	IDD4	CPU: Running at 8.192MHz Crystal/ceramic oscillating mode*2 V_{DD} = SPV_{DD} = 5.0V		—	5	8	mA	

*1: Case when the CPU operating rate is 100% (with no HALT state)
*2 : Significant bits of BLKCON0 to BLKCON4 registers are all “1”.

DC Characteristics (4 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23) (P90-P93)	VOL2	When LED drive mode is selected	IOL2 = +10mA $V_{DD} \geq 4.5V$	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	When I^2C mode is selected	IOL3 = +3mA	—	—	0.4		
Output leakage current (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Output current 1 COM0 to COM3	IOL1	VL3=3V、VOL=0.3V		15	40	—	μA	3
		VL3=5V、VOL=0.5V		100	200	—		
	IOH1	VL3=3V、VOH=2.7V		—	-30	-15		
		VL3=5V、VOH=4.5V		—	-90	-45		
Output current 2 SEG0 to SEG39	IOL2	VL3=3V、VOL=0.3V		15	30	—		
		VL3=5V、VOL=0.5V		70	150	—		
	IOH2	VL3=3V、VOH=2.7V		—	-13	-6		
		VL3=5V、VOH=4.5V		—	-40	-20		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}		–1500	–300	–20		
Input current 2 (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P47) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	IIH2	VIH2 = V_{DD} (when pulled down)		2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)		–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		-1	—	—		
Input current 3 (TEST0)	IIH3	VIH3 = V_{DD}		20	300	1500		
	IIL3	VIL3 = V_{SS}		-1	—	—		

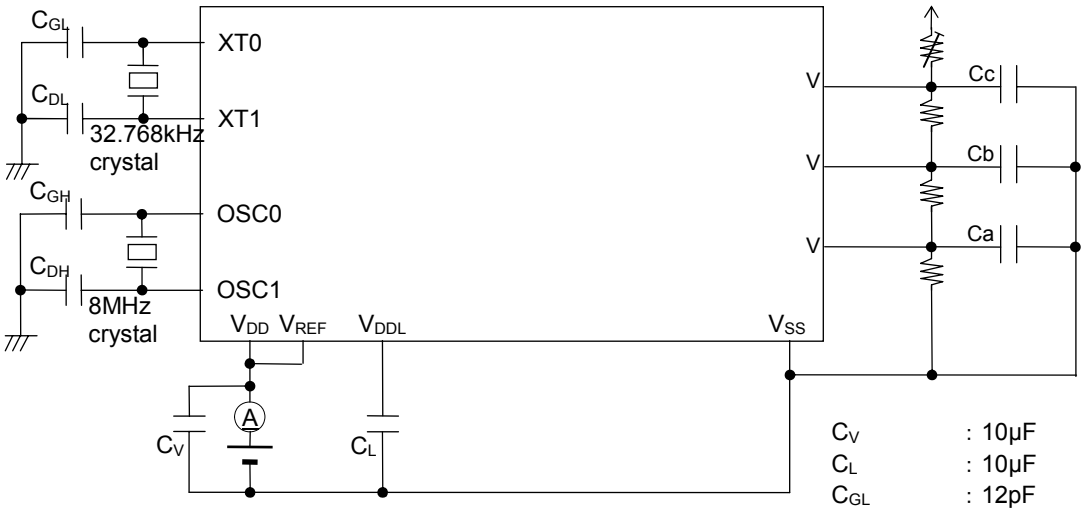
DC Characteristics (5 of 5)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P43) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Input pin capacitance (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P43) (P50 to P53) (PC0 to PC7) (PD0 to PD7) (PE0 to PE7) (PF0 to PF7)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

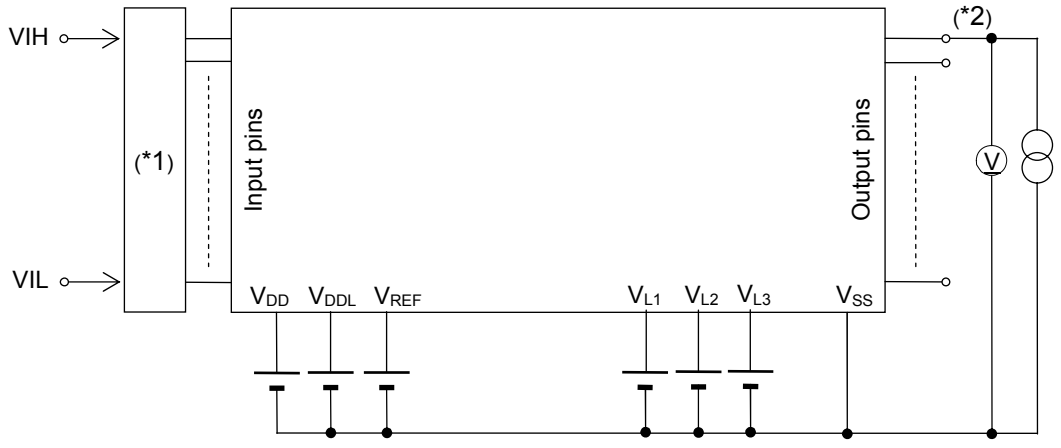
Measuring Circuits

Measuring circuit 1



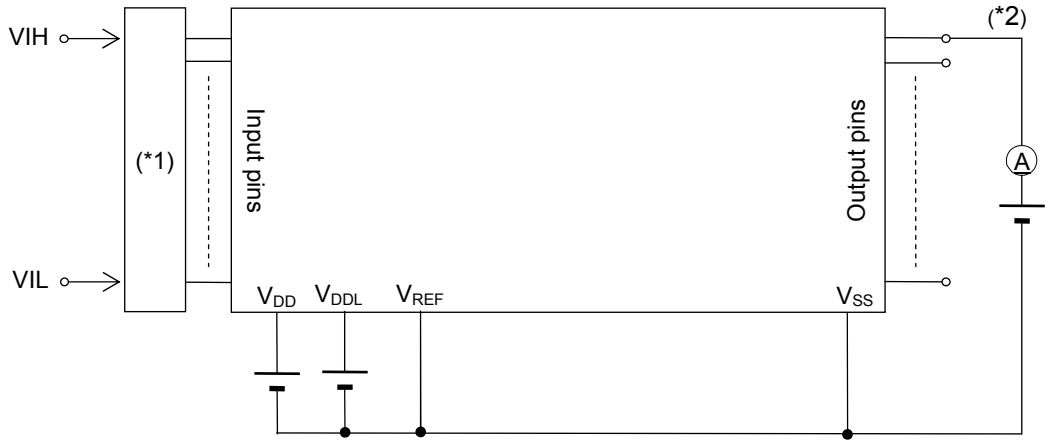
C_V : 10µF
C_L : 10µF
C_{GL} : 12pF
C_{DL} : 12pF
C_{GH} : 47pF
C_{DH} : 47pF
C_{L1},C_{L2},C_{L3} : 0.22µF
32.768kHz Crystal oscillator
(DMX-26 DAISHINKU Corp.)
8MHz Crystal oscillator
CSTLS8M00G56（MURATA Corp.）
it has built-in C_{GH}, and C_{DH}

Measuring circuit 2



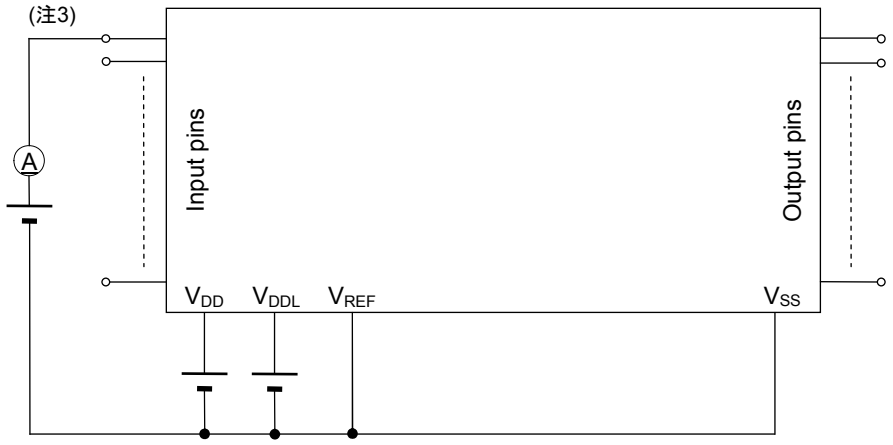
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



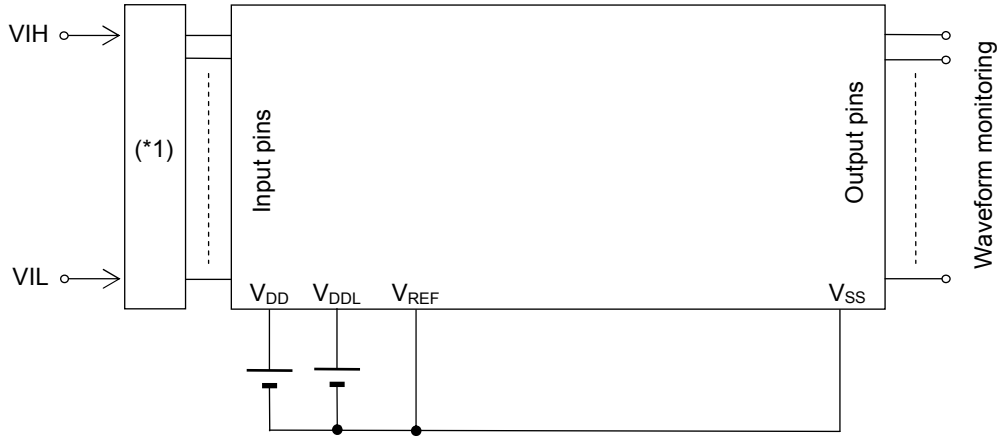
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

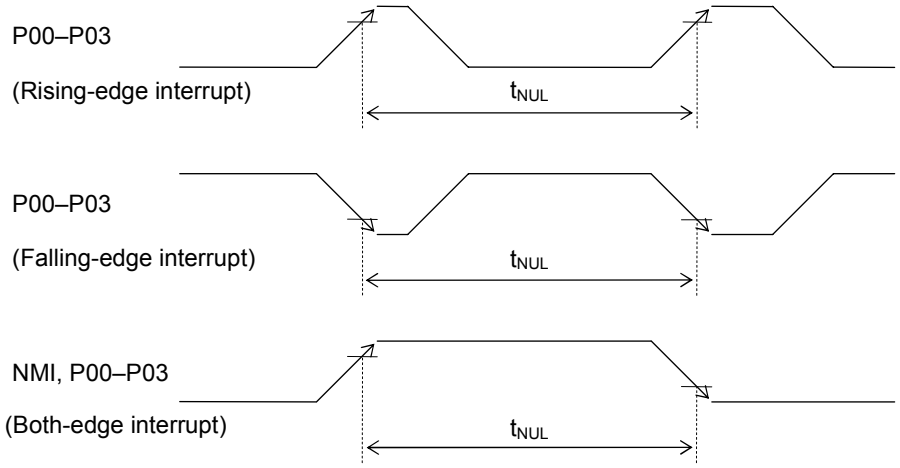


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× sysclk	—	3.5× sysclk	µs

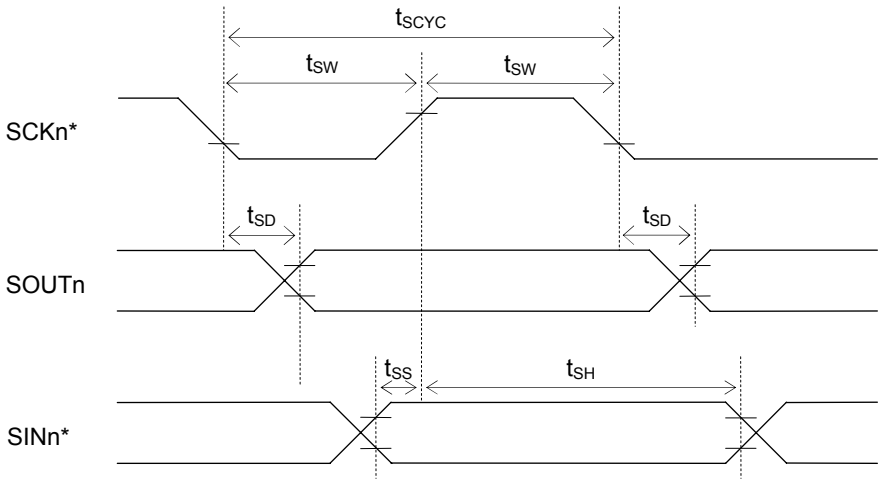


AC Characteristics (Synchronous Serial Port)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIOnMOD1)



*: Indicates the secondary function of the corresponding port.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode 100kHz)

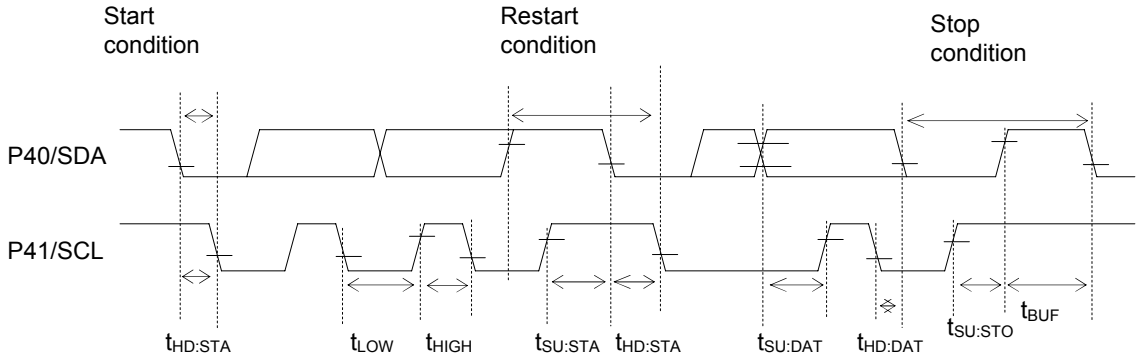
(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL ”L” level time	t_{LOW}	—	4.7	—	—	µs
SCL ”H” level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

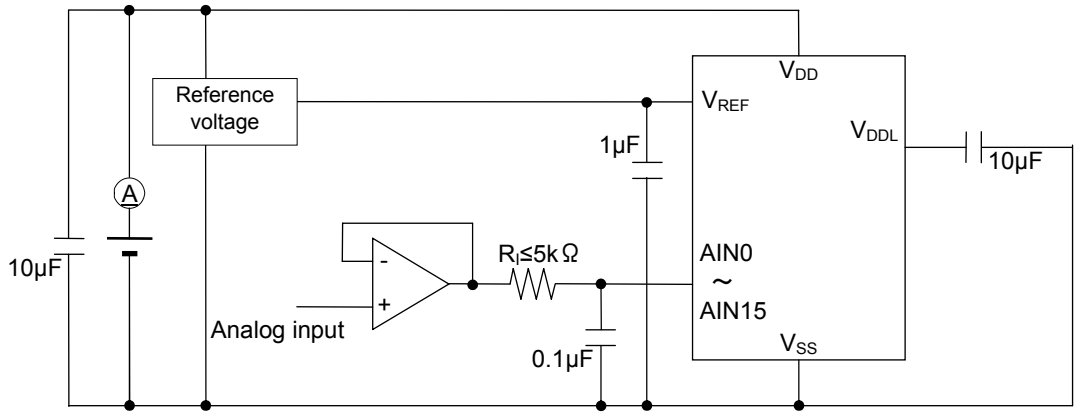


Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 5.5V	−4	—	+4	LSB
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	−3	—	+3	
Zero-scale error	V_{OFF}	—	−4	—	+4	
Full-scale error	FSE	—	−4	—	+4	
Input impedance	R_I	—	—	—	5k	Ω
Reference voltage	V_{REF}		4.5	—	V_{DD}	V
Conversion time	t_{CONV}	HSCLK=3.0M to 8.4MHz	—	102	—	φ/CH

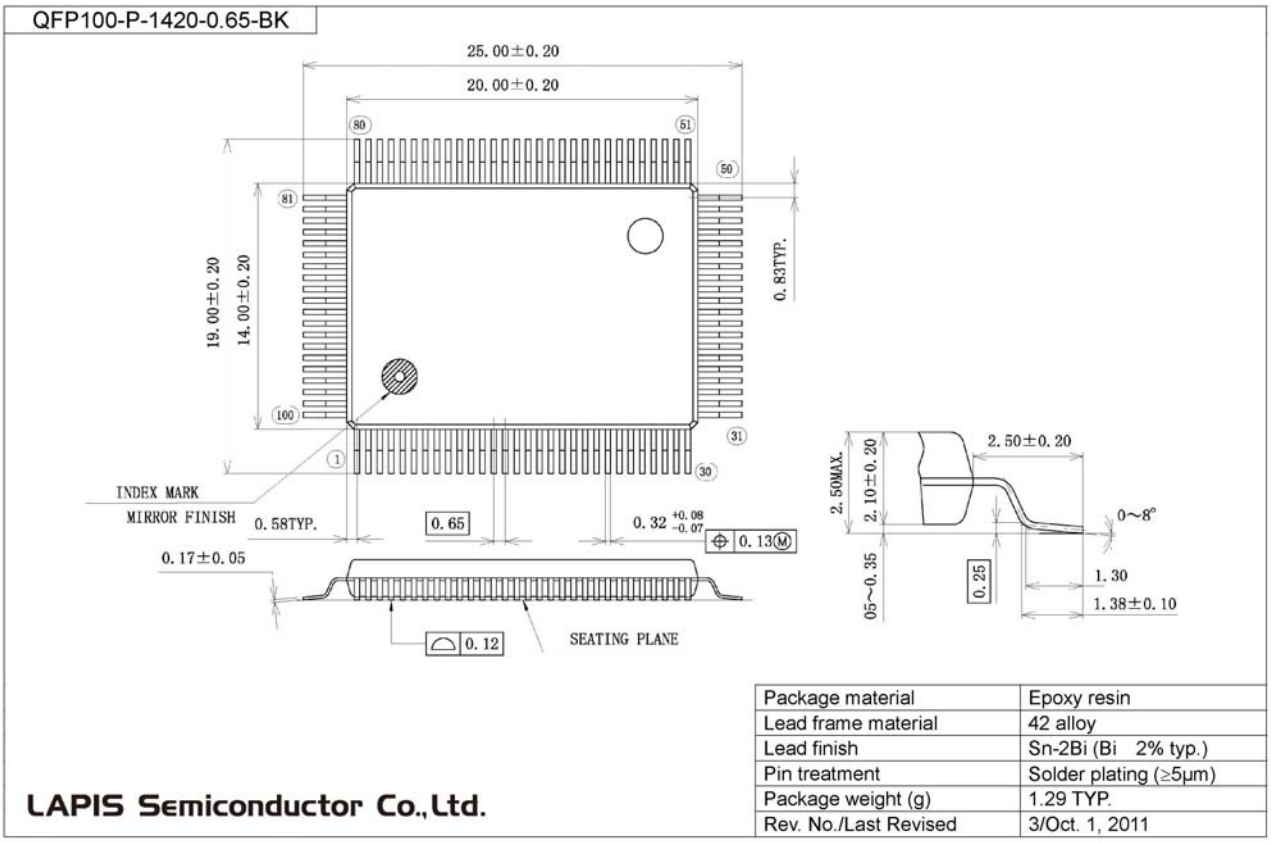
φ: Period of high-speed clock (HSCLK)



PACKAGE DIMENSIONS

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact LAPIS SEMICONDUCTOR's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.29 TYP.
Rev. No./Last Revised	3/Oct. 1, 2011

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q178FULL-01	May 18, 2012	–	–	Formal edition 1

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ML610Q178 reference board ML610Q178-NNNGAZ0AAL

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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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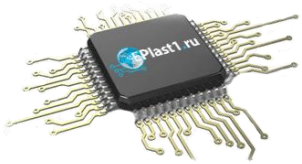
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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