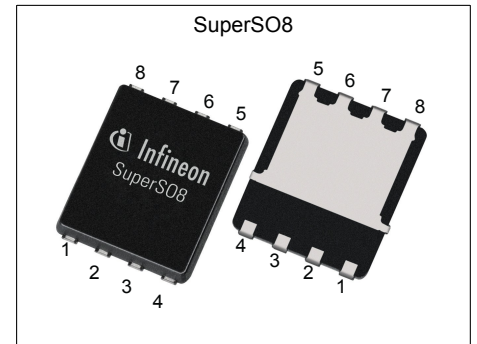


# MOSFET

## OptiMOS™3 Power-Transistor, 120 V

### Features

- N-channel, normal level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	120	V
$R_{DS(on),max}$	7.7	mΩ
$I_D$	98	A



Type / Ordering Code	Package	Marking	Related Links
BSC077N12NS3 G	PG-TDSON-8	077N12NS	-

<sup>1)</sup> J-STD20 and JESD22

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	3
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Package Outlines .....	10
Revision History .....	13
Trademarks .....	13
Disclaimer .....	13

## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	98 61 13.4	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=45\text{ K/W}^{(1)}$
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	330	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	139	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	18	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	75	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>(1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> see Diagram 3

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$ , $I_D=110\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.01 10	1 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.6	7.7	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1	1.5	$\Omega$	-
Transconductance	$g_{fs}$	40	80	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	4300	5700	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	550	730	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	28	49	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=60\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Rise time	$t_r$	-	8	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$
Fall time	$t_f$	-	7	-	ns	$V_{DD}=60\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=2.7\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	21	-	nC	$V_{DD}=60\text{ V}$ , $I_D=25\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	15	-	nC	$V_{DD}=60\text{ V}$ , $I_D=25\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	29	-	nC	$V_{DD}=60\text{ V}$ , $I_D=25\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	66	88	nC	$V_{DD}=60\text{ V}$ , $I_D=25\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	$V_{DD}=60\text{ V}$ , $I_D=25\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	76	100	nC	$V_{DD}=60\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition.

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	98	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	98	-	ns	$V_R=60\text{ V}, I_F=25, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	264	-	nC	$V_R=60\text{ V}, I_F=25, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

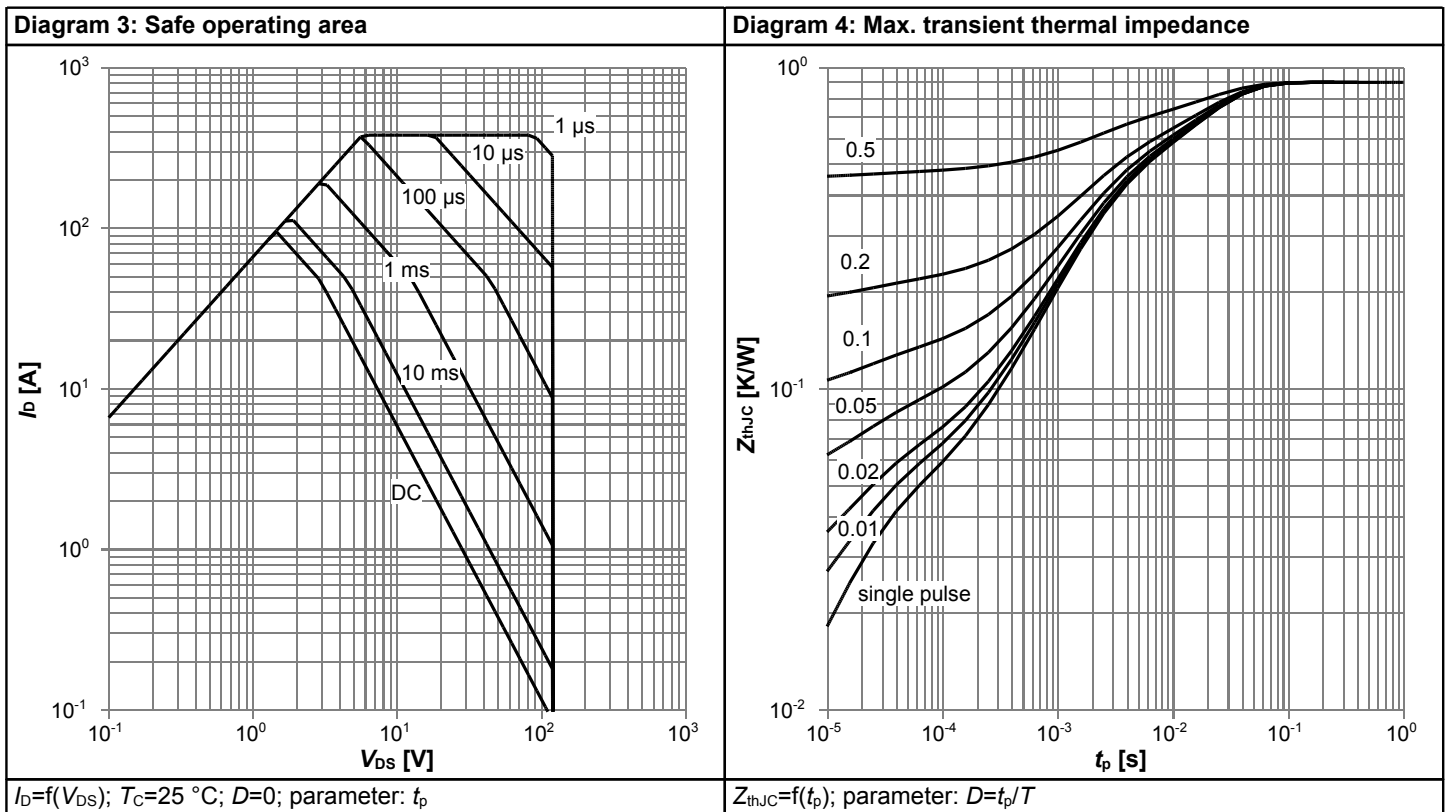
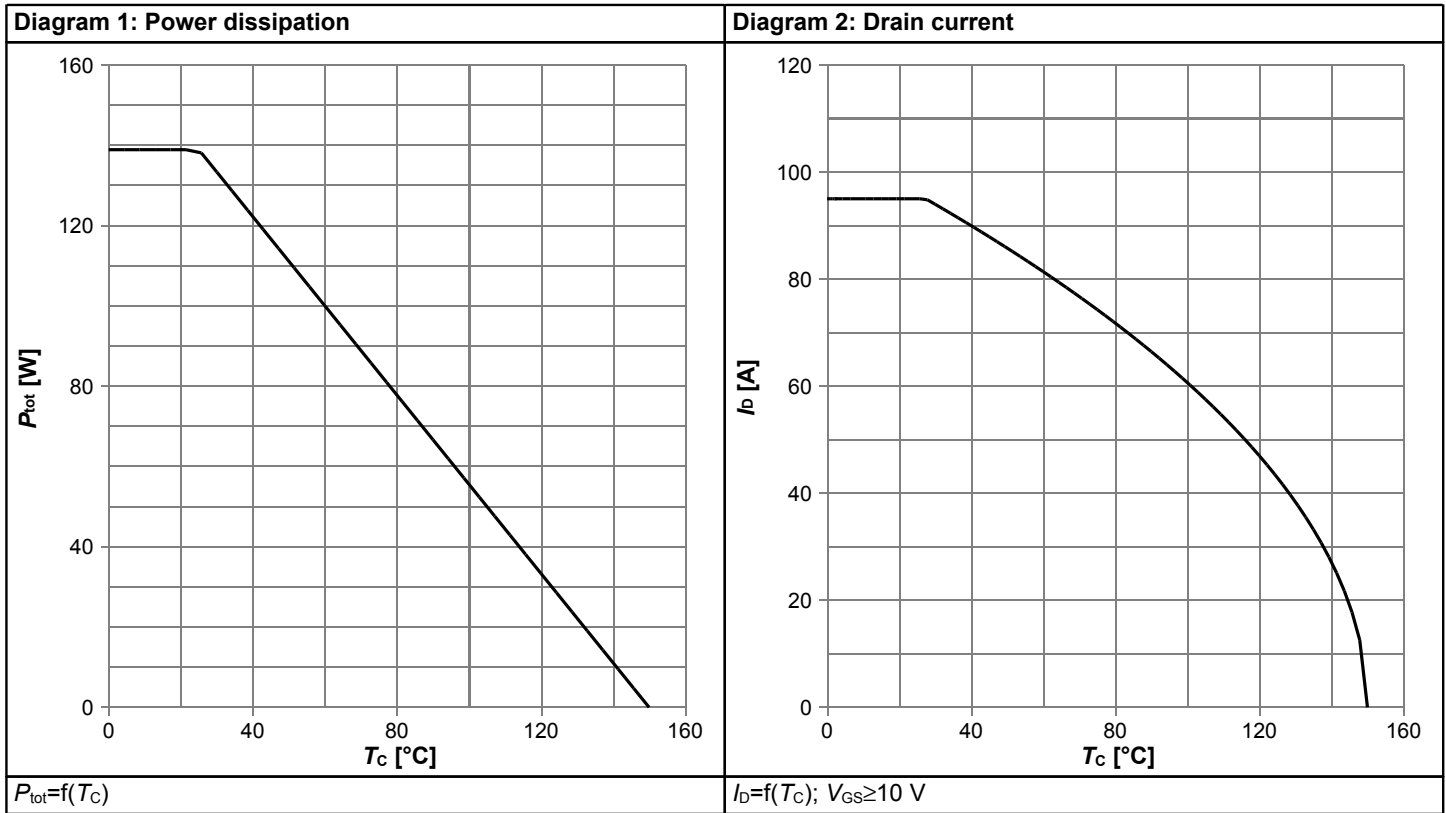
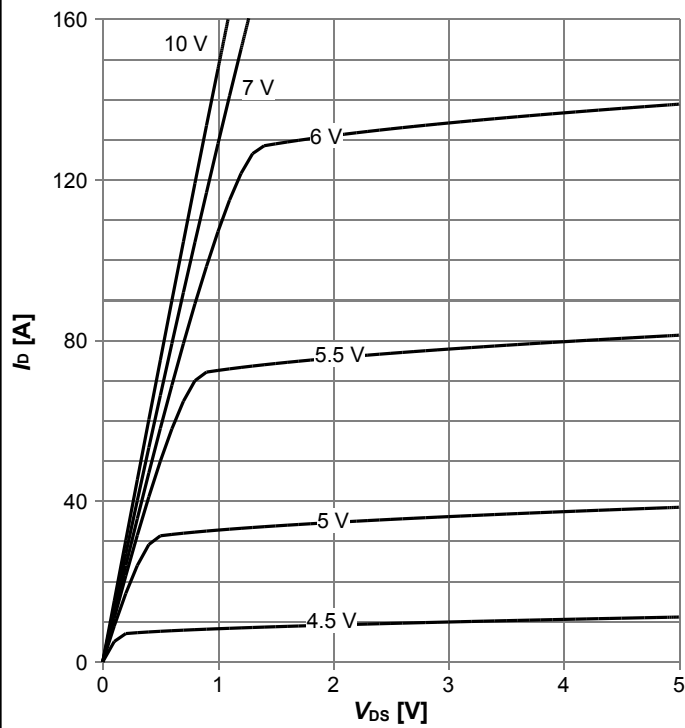
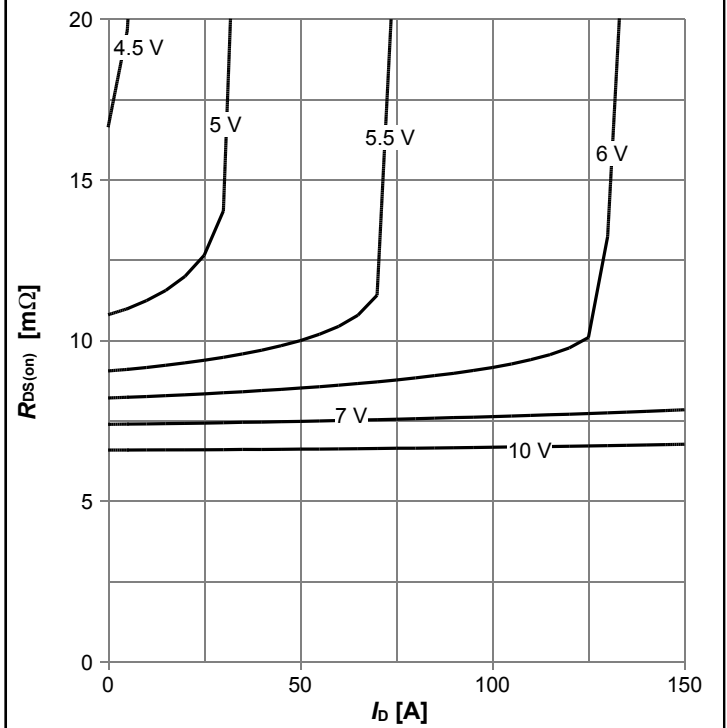


Diagram 5: Typ. output characteristics



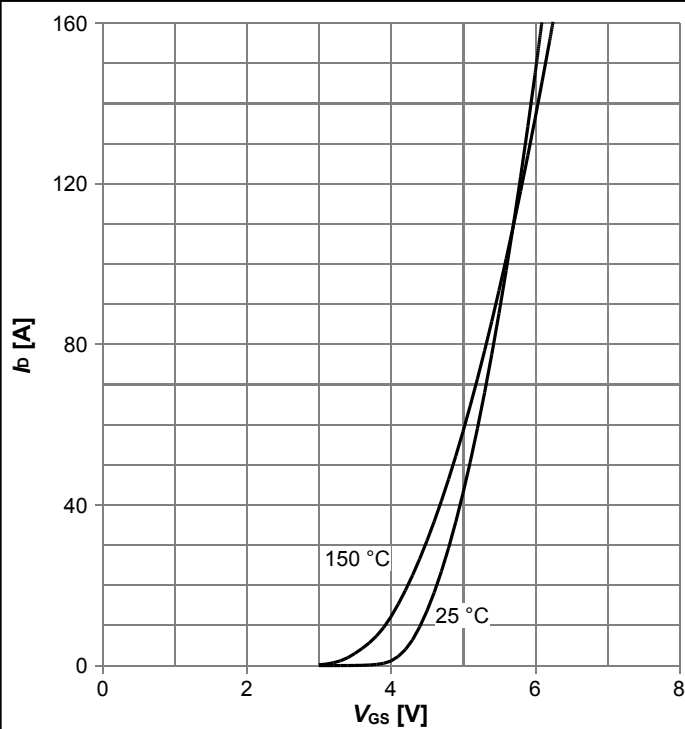
$I_D = f(V_{DS})$ ;  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



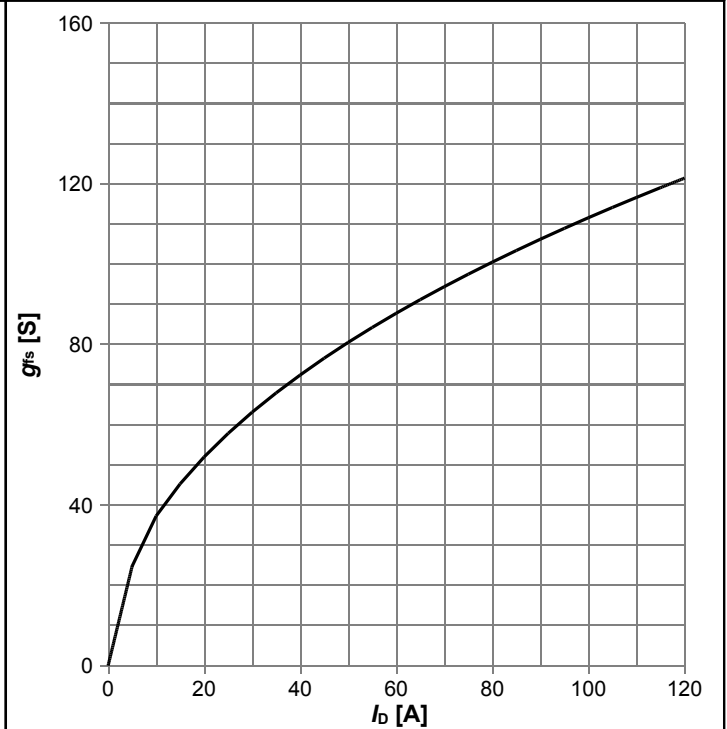
$R_{DS(on)} = f(I_D)$ ;  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



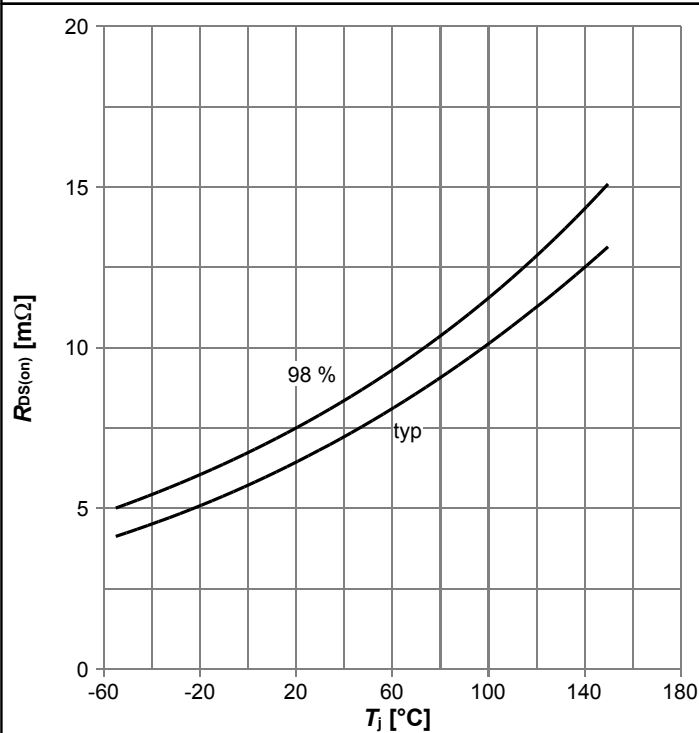
$I_D = f(V_{GS})$ ;  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. forward transconductance



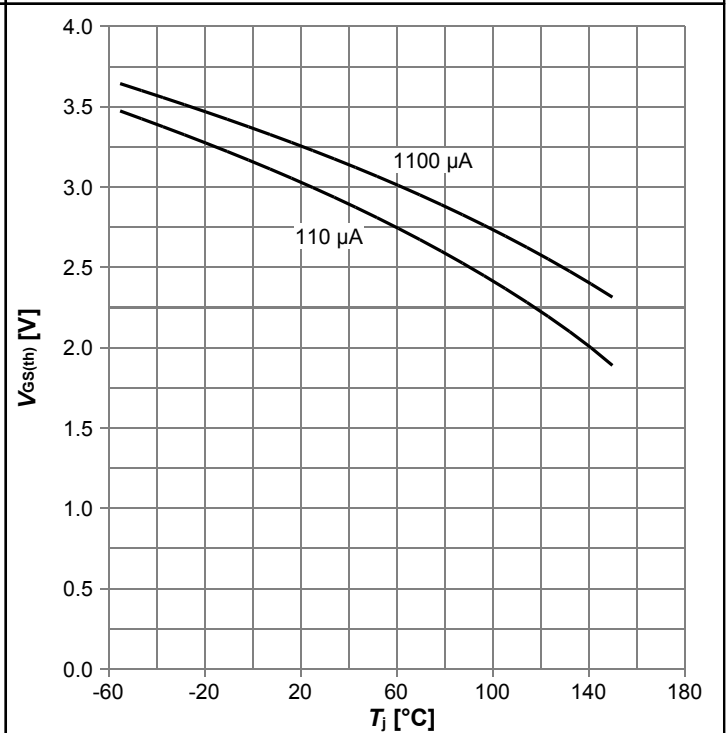
$g_{fs} = f(I_D)$ ;  $T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



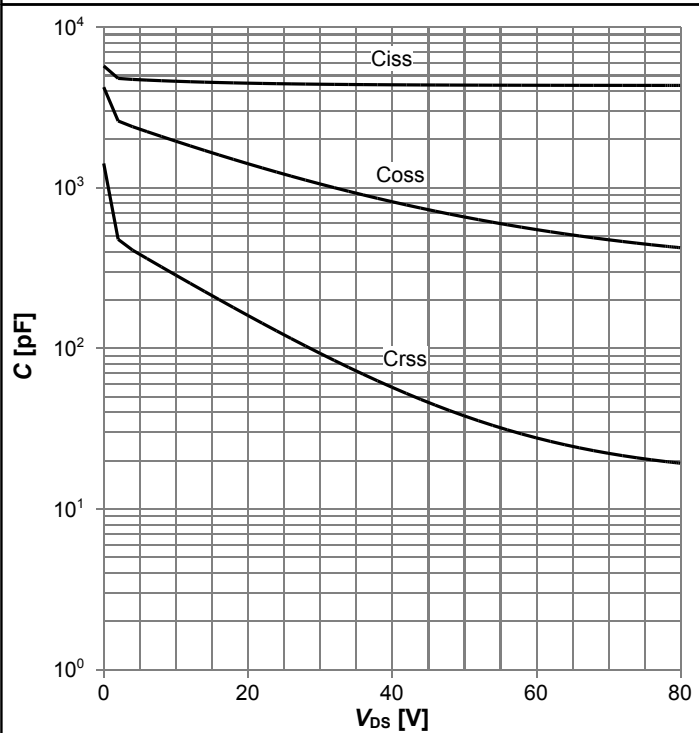
$R_{DS(on)}=f(T_j)$ ;  $I_D=50\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



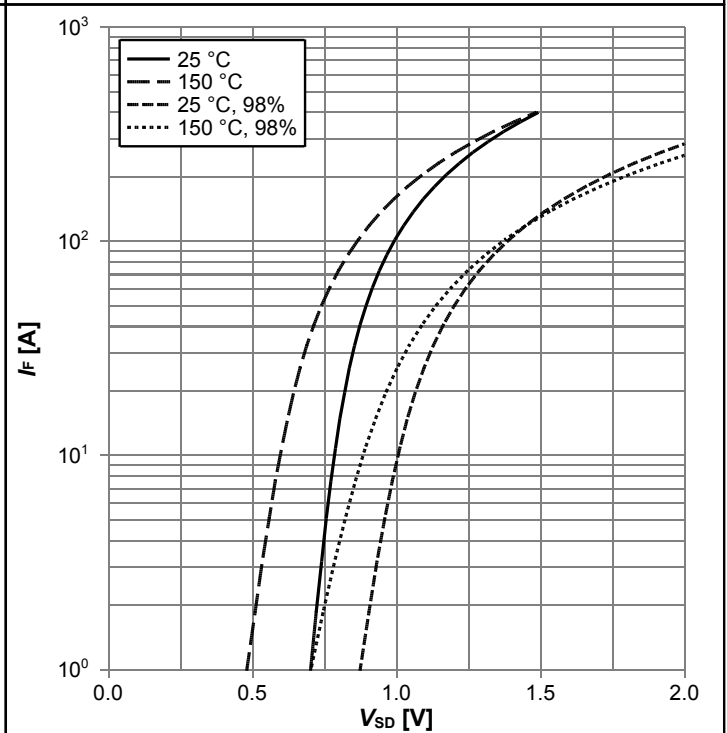
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

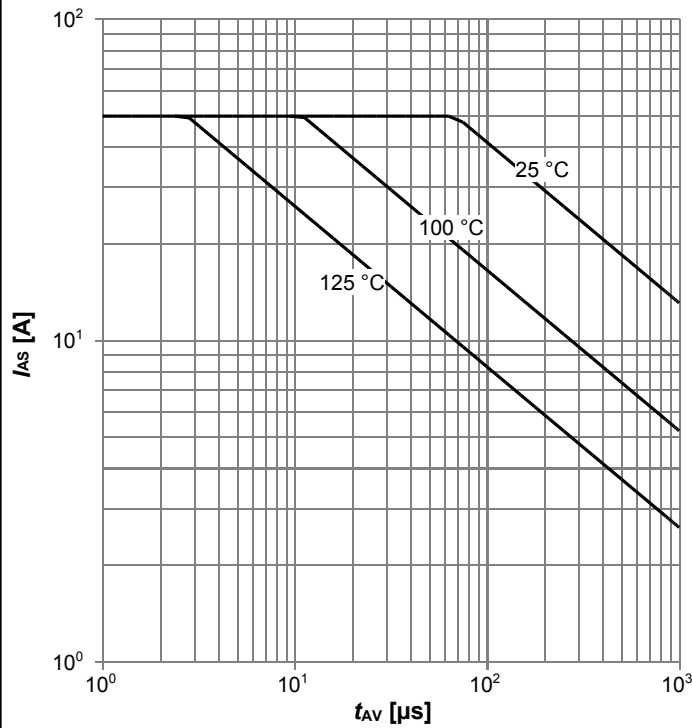
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

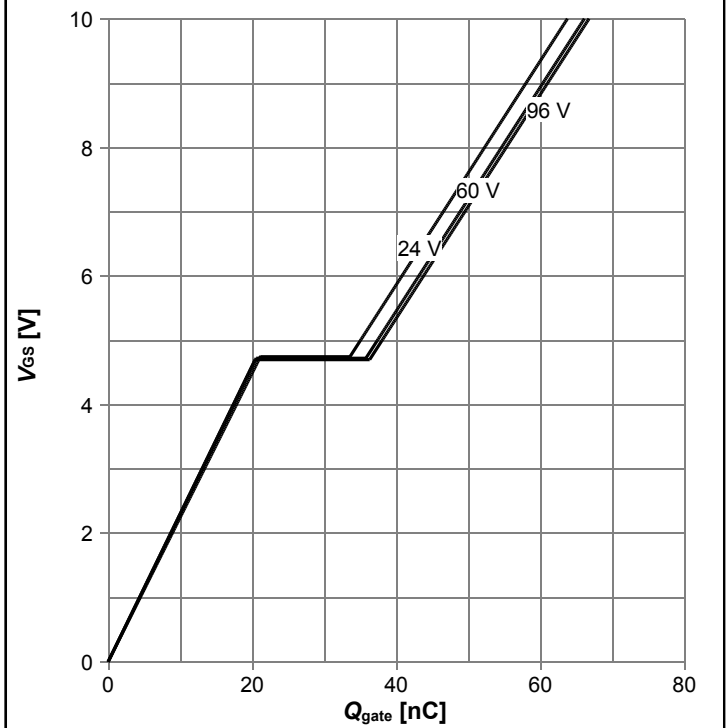


**Diagram 13: Avalanche characteristics**



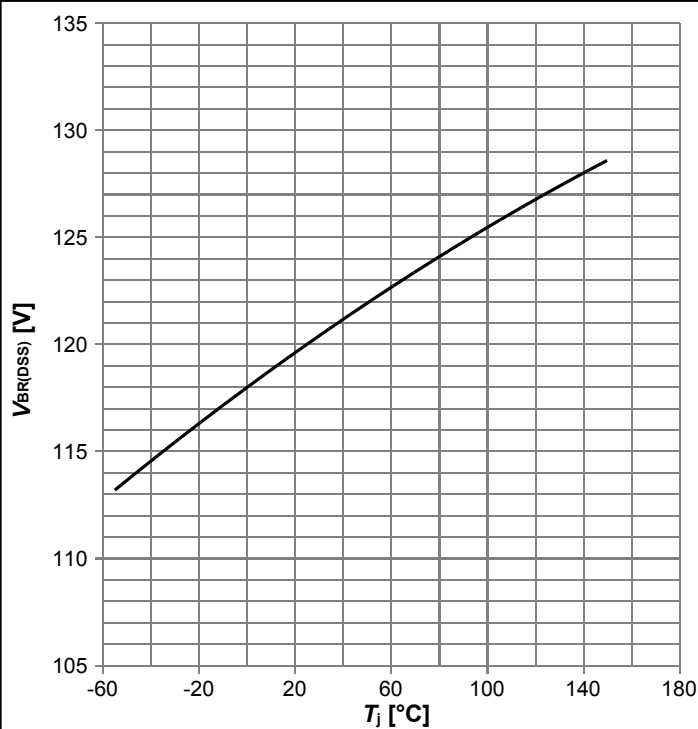
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



$V_{GS}=f(Q_{gate}); I_D=25 \text{ A pulsed}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



**5 Package Outlines**



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
theta	8.5°	12°
aaa	0.25	
eee	0.08	

**DOCUMENT NO.**  
Z8B00003332

**SCALE**

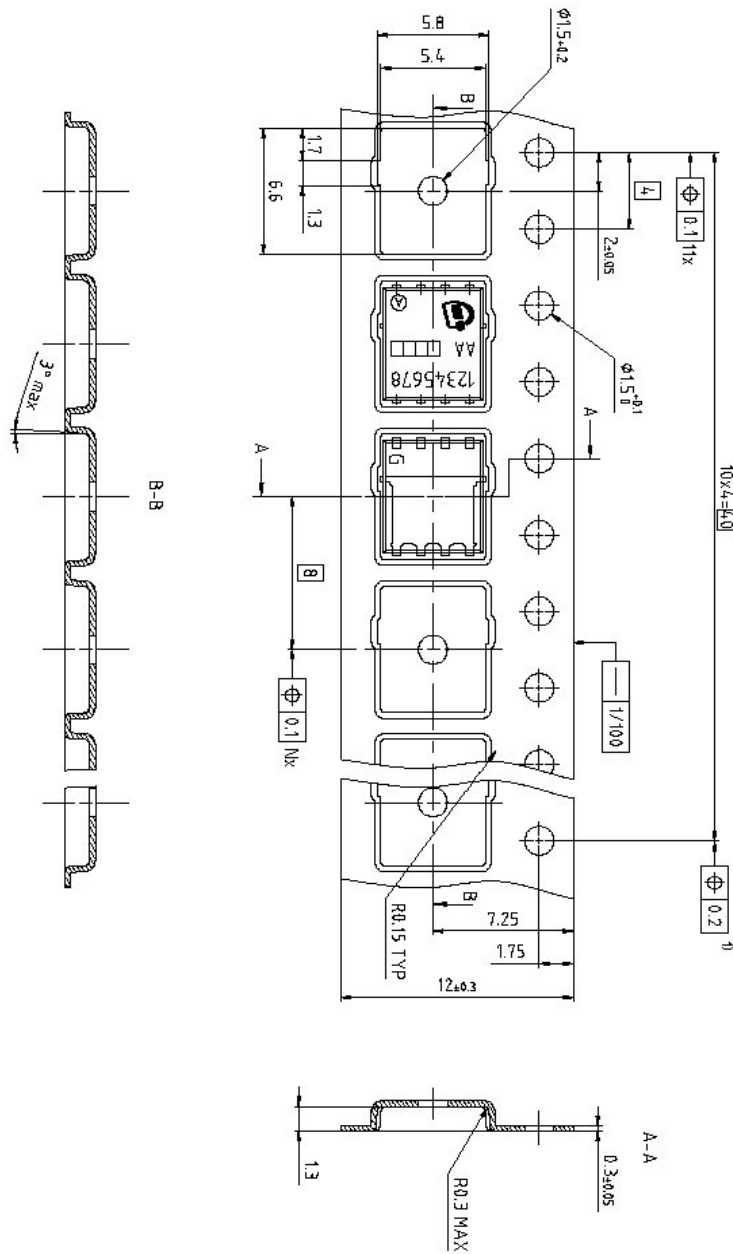
**EUROPEAN PROJECTION**

**ISSUE DATE**  
10-04-2013

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04

**Figure 1 Outline PG-TDSON-8, dimensions in mm**

OptiMOS™3 Power-Transistor, 120 V  
 BSC077N12NS3 G



Dimension in mm

Figure 2 Outline TDSON-8 Tape

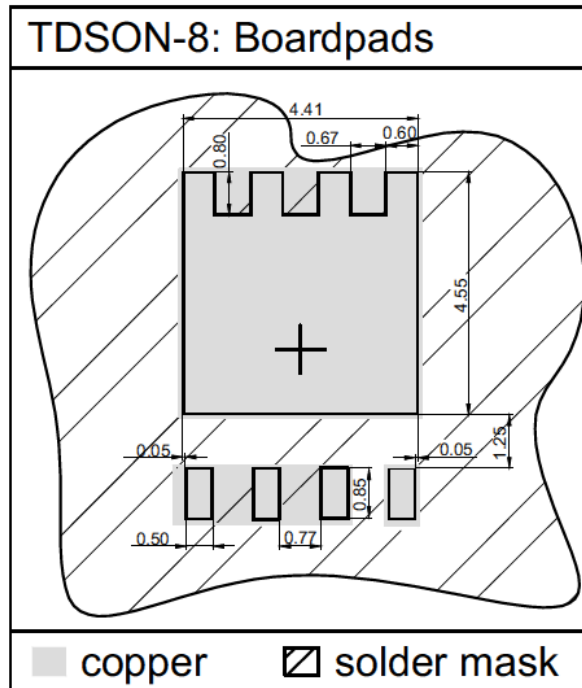


Figure 3 Outline Footprint TDSO-8

## Revision History

BSC077N12NS3 G

**Revision: 2015-12-15, Rev. 2.8**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.7	2014-10-02	Rev. 2.7
2.8	2015-12-15	Update of dynamic parameters td(on), td(off), tr, tf

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