

40MHz to 500MHz VGA and I/Q Demodulator with 17MHz Baseband Bandwidth

FEATURES

- 17MHz I/Q Lowpass Output Noise Filters
- Wide Range 1.8V to 5.25V Supply Voltage
- Frequency Range: 40MHz to 500MHz
- THD < 0.14% (–57dBc)
at 800mV_{p-p} Differential Output Level
- IF Overload Detector
- Log Linear Gain Control Range: –7dB to 56dB
- Baseband I/Q Amplitude Imbalance: 0.2dB
- Baseband I/Q Phase Imbalance: 0.6°
- 7.8dB Noise Figure at Max Gain
- Input IP3 at Low Gain: –1dBm
- Low Supply Current: 24mA
- Low Delay Shift Over Gain Control Range: 2ps/dB
- Outputs Biased Up While in Standby
- 16-Lead QFN 4mm × 4mm Package with Exposed Pad

APPLICATIONS

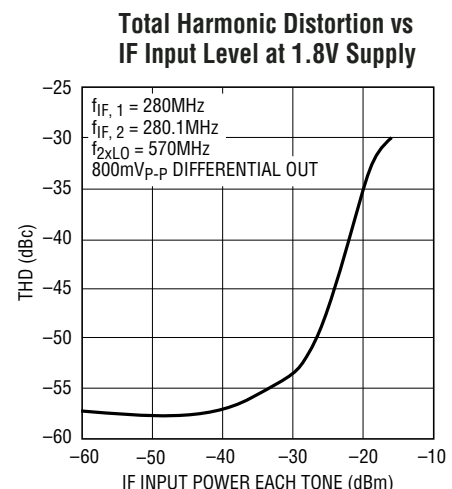
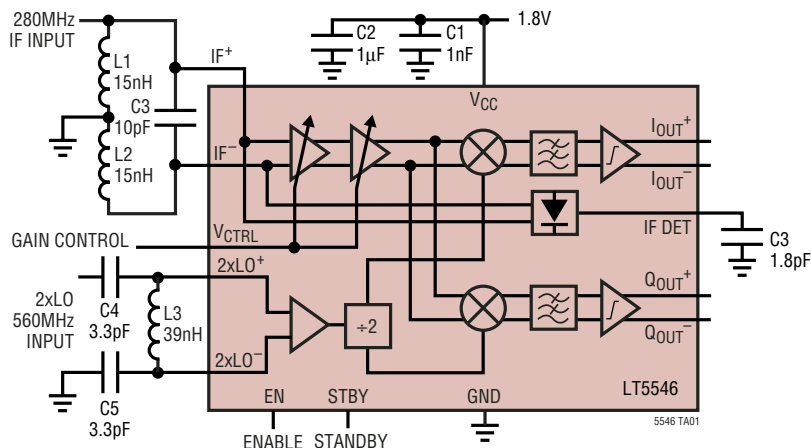
- GPS IF Receivers
- Satellite IF Receivers
- VHF/UHF Receivers
- Wireless Local Loop

DESCRIPTION

The LT[®]5546 is a 40MHz to 500MHz monolithic integrated quadrature demodulator with variable gain amplifier (VGA) and 17MHz I/Q baseband bandwidth designed for low voltage operation. It supports standards that use a linear modulation format. The chip consists of a VGA, quadrature down-converting mixers and 17MHz lowpass noise filters (LPF). The LO port consists of a divide-by-two stage and LO buffers. The IC provides all building blocks for IF down-conversion to I and Q baseband signals with a single supply voltage of 1.8V to 5.25V. The VGA gain has a linear-in-dB relationship to the control input voltage. Hard-clipping amplifiers at the mixer outputs reduce the recovery time from a signal overload condition. The lowpass filters reduce the out-of-band noise and spurious frequency components. The –3dB corner frequency of the noise filters is approximately 17MHz and has a first order roll-off. The standby mode provides reduced supply current and fast transient response into the normal operating mode when the I/Q outputs are AC-coupled to a baseband chip.

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TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	5.5V
Differential Voltage Between 2xLO ⁺ and 2xLO ⁻	4V
IF ⁺ , IF ⁻	-500mV to 500mV
I _{OUT} ⁺ , I _{OUT} ⁻ , Q _{OUT} ⁺ , Q _{OUT} ⁻	V _{CC} - 1.8V to V _{CC}
Operating Ambient Temperature (Note 2)	-40°C to 85°C
Storage Temperature Range	-65°C to 125°C
Voltage on Any Pin Not to Exceed	-500mV to V _{CC} + 500mV

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>16-LEAD (4mm × 4mm) PLASTIC QFN</p> <p>T_{JMAX} = 125°C, θ_{JA} = 37°C/W EXPOSED PAD IS GND (PIN 17) (MUST BE SOLDERED TO PCB)</p>	ORDER PART NUMBER
	LT5546EUF
	UF PART MARKING
	5546

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V, f_{2xLO} = 570MHz, P_{2xLO} = -5dBm (Note 5), f_{IF} = 284MHz, P_{IF} = -30dBm, I and Q outputs 800mV_{p-p} into 4kΩ differential load, T_A = 25°C, EN = V_{CC}, STBY = V_{CC}, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF Input						
f _{IF}	Frequency Range			40 to 500		MHz
	Nominal Input Level	R _{SOURCE} = 200Ω Differential		-76 to -19		dBm
	Input Impedance	IF ⁺ , IF ⁻ to GND, EN = V _{CC} IF ⁺ , IF ⁻ to GND, EN = GND		100Ω//1.2pF 1pF		
NF	Noise Figure at Max Gain	V _{CTRL} = 1.7V		7.8		dB
G _L	Min Gain (Note 4)	V _{CTRL} = 0.2V		1.6	6	dB
G _H	Max Gain (Note 4)	V _{CTRL} = 1.7V	49	56		dB
IIP3	Input IP3, Min Gain Input IP3, Max Gain	P _{IF} = -22.5dBm (Note 7) P _{IF} = -75dBm (Note 7)		-1 -49		dBm dBm
IIP2	Input IP2, Min Gain Input IP2, Max Gain	V _{CTRL} = 0.2V (Note 9) V _{CTRL} = 1.7V (Note 9)		36 -25		dBm dBm
Demodulator I/Q Output						
	Nominal Voltage Swing	(Note 6)		0.8		V _{p-p}
	Clipping Level	(Note 6)		1.47		V _{p-p}
	DC Common Mode Voltage			V _{CC} - 1.19		V
	I/Q Amplitude Imbalance	(Note 8)		0.14	0.6	dB
	I/Q Phase Imbalance	(Note 8)		0.6	3	Deg
	DC Offset	(Notes 6, 8)		21		mV
	Output Driving Capability	Single Ended, C _{LOAD} ≤ 10pF	2	1.5		kΩ
r _o	Small-Signal Output Impedance	(Note 6)		180		Ω
	STBY to Turn-On Delay			0.3		μs
	I/Q Output 1dB Compression			-10		dBm
	I/Q Output IM3	P _{IF,1} = -25.5dBm, 280MHz P _{IF,2} = -25.5dBm, 280.1MHz (Note 7)		-49		dBc

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ELECTRICAL CHARACTERISTICS

$V_{CC} = 3V$, $f_{2xLO} = 570MHz$, $P_{2xLO} = -5dBm$ (Note 5), $f_{IF} = 284MHz$, $P_{IF} = -30dBm$, I and Q outputs 800mV_{P-P} into 4k Ω differential load, $T_A = 25^\circ C$, $EN = V_{CC}$, $STBY = V_{CC}$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Variable Gain Amplifier (VGA)						
	Gain Slope Linearity Error	$V_{CTRL} = 0V$ to 1.4V		± 0.5		dB
	Temperature Gain Shift	$T = -40^\circ C$ to $85^\circ C$, $V_{CTRL} = 0V$ to 1.4V		± 0.4		dB
	Gain Control Response Time	Settled within 10% of Final Value		90		ns
	Gain Control Voltage Range			0 to 1.7		V
	Gain Control Slope			41		dB/V
	Gain Control Input Impedance	To Internal 0.2V Reference		25		k Ω
	Delay Shift Over Gain Control	Measured Over 10dB Step		2		ps/dB
Baseband Lowpass Filter (LPF)						
	-3dB Cutoff Frequency		13	17		MHz
	Amplitude Roll-Off at 50MHz			-9		dB
	Group Delay Ripple			1		ns
2xLO Input						
f_{2xLO}	Frequency Range			80 to 1000		MHz
P_{2xLO}	Input Power	1:2 Transformer with 240 Ω Shunt Resistor (Note 5)	-20	-5		dBm
	Input Power	LC Balun (Note 5)		-10		dBm
	Input Impedance	Differential Between 2xLO ⁺ and 2xLO ⁻		800 Ω /0.4pF		
	DC Common Mode Voltage			$V_{CC} - 0.4$		V
IF Detector						
	IF Detector Range	Referred to IF Input		-30 to 8		dBm
	Output Voltage Range	For $P_{IF} = -30dBm$ to 8dBm		0.27 to 1.2		V
	Detector Response Time	With External 1.8pF Load, Settling within 10% of Final Value		80		ns
Power Supply						
V_{CC}	Supply Voltage		1.8		5.25	V
I_{CC}	Supply Current	$EN = High$, $STBY = Low$ or $High$		24	34	mA
I_{OFF}	Shutdown Current	EN , $STBY < 350mV$		0.2	30	μA
I_{STBY}	Standby Current	$EN = Low$; $STBY = High$		3.6	6	mA
Mode						
Enable	Enable Pin Voltage	$EN = High$	1			V
Disable	Enable Pin Voltage	$EN = Low$			0.5	V
Standby	Standby Pin Voltage	$STBY = High$	1			V
No Standby	Standby Pin Voltage	$STBY = Low$			0.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Specifications over the $-40^\circ C$ to $85^\circ C$ temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 6. The IF input transformer loss is subtracted from the measured values.

Note 4: Power gain is defined here as the I (or Q) output power into a 4k Ω differential load, divided by the IF input power in dB. To calculate the voltage gain between the differential I output (or Q output) and the IF input, including ideal matching network, $10 \cdot \log(4k\Omega/50) = 19dB$ has to be added to this power gain.

Note 5: If a narrow-band match is used in the 2xLO path instead of a 1:2 transformer with 240 Ω shunt resistor, 2xLO input power can be reduced to $-10dBm$, without degrading the phase imbalance. See Figure 11 and Figure 6.

Note 6: Differential between I_{OUT}^+ and I_{OUT}^- (or differential between Q_{OUT}^+ and Q_{OUT}^-).

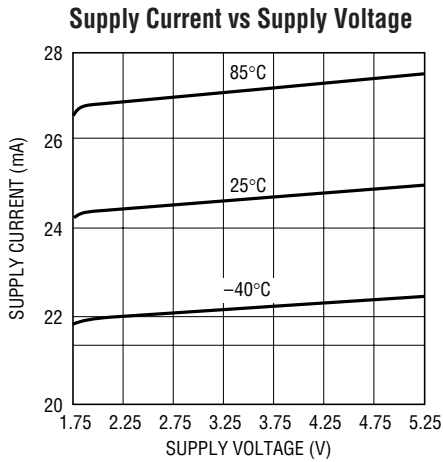
Note 7: The gain control voltage V_{CTRL} is set in such a way that the differential output voltage between I_{OUT}^+ and I_{OUT}^- (or differential between Q_{OUT}^+ and Q_{OUT}^-) is 800mV_{P-P}, with the given input power P_{IF} . IF frequencies are 280MHz and 280.1MHz, with $f_{2xLO} = 570MHz$.

Note 8: The typical parameter is defined as the mean of the absolute values of the data distribution.

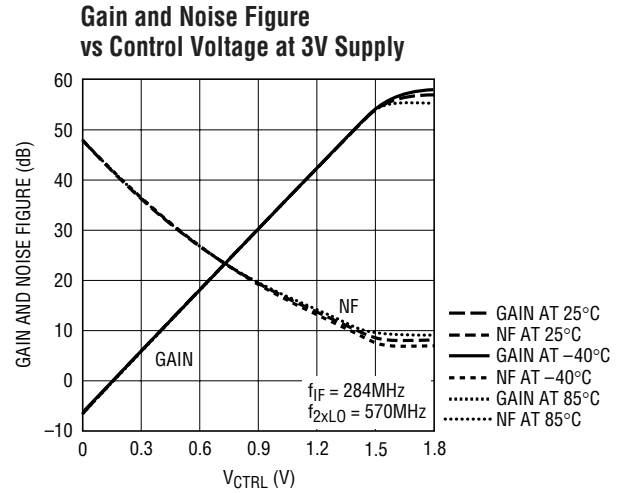
Note 9: IF frequency is 125MHz, with $f_{2xLO} = 502MHz$.

TYPICAL PERFORMANCE CHARACTERISTICS

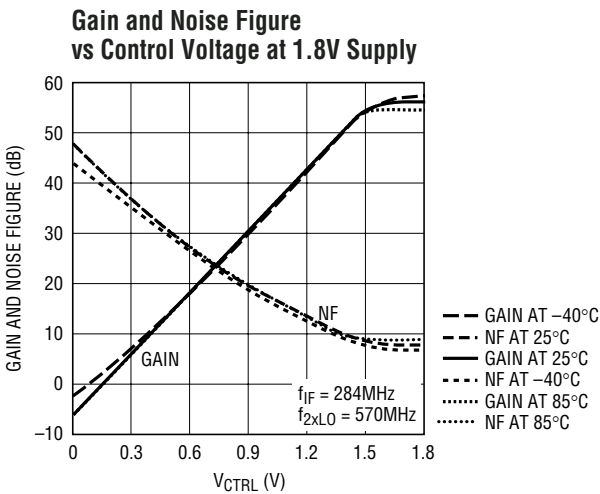
(Note 5), $f_{IF} = 284\text{MHz}$, $P_{IF} = -30\text{dBm}$, I and Q outputs 800mV_{P-P} into $4\text{k}\Omega$ differential load, $T_A = 25^\circ\text{C}$, $EN = V_{CC}$, $STBY = V_{CC}$, unless otherwise noted. (Note 3)



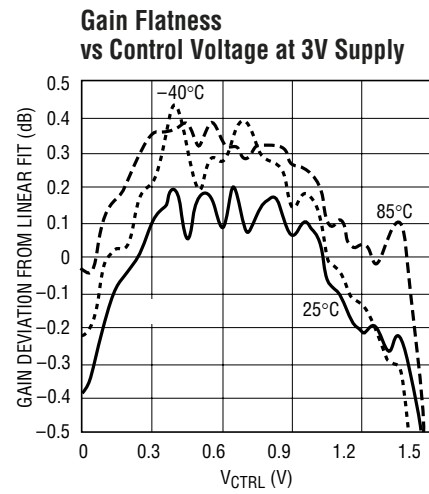
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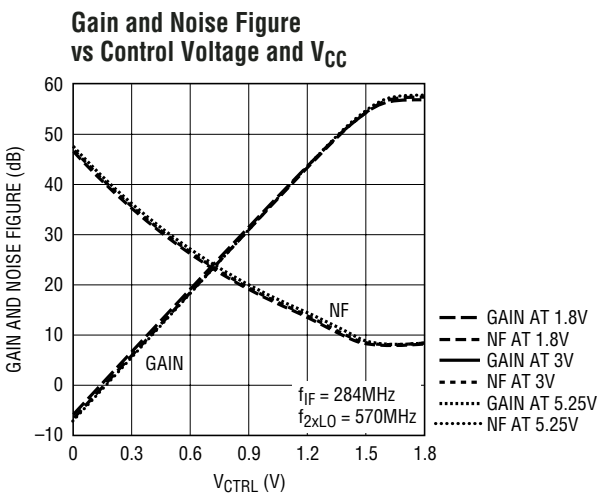
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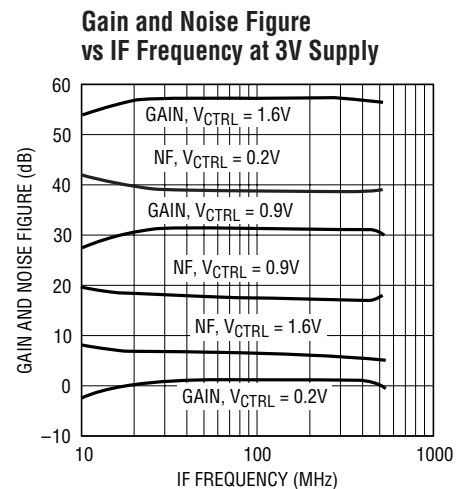
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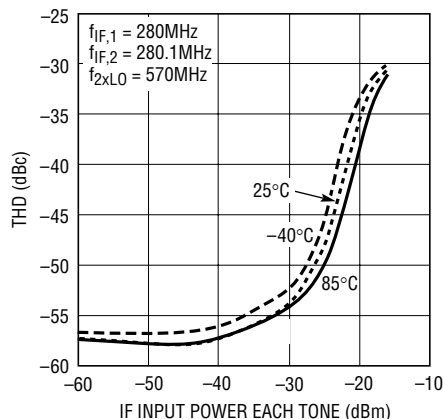


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TYPICAL PERFORMANCE CHARACTERISTICS

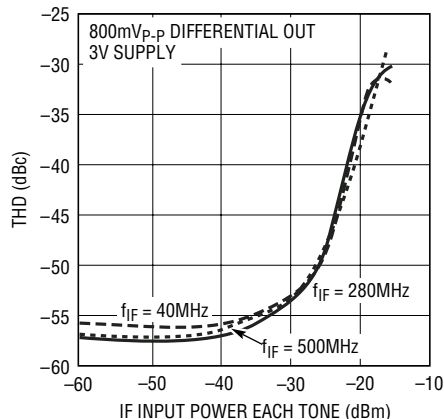
(Note 5), $f_{IF} = 284\text{MHz}$, $P_{IF} = -30\text{dBm}$, I and Q outputs 800mV_{P-P} into $4\text{k}\Omega$ differential load, $T_A = 25^\circ\text{C}$, $EN = V_{CC}$, $STBY = V_{CC}$, unless otherwise noted. (Note 3)

Total Harmonic Distortion vs IF Input Power at 3V Supply and 800mV_{P-P} Differential Out



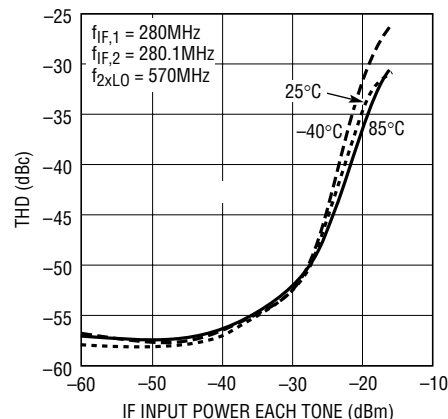
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Total Harmonic Distortion vs IF Input Power and IF Frequency



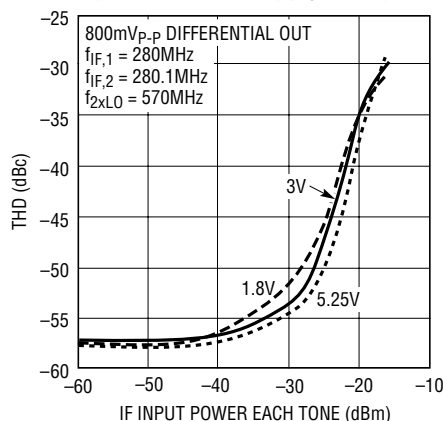
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Total Harmonic Distortion vs IF Input Power at 1.8V Supply and 800mV_{P-P} Differential Out



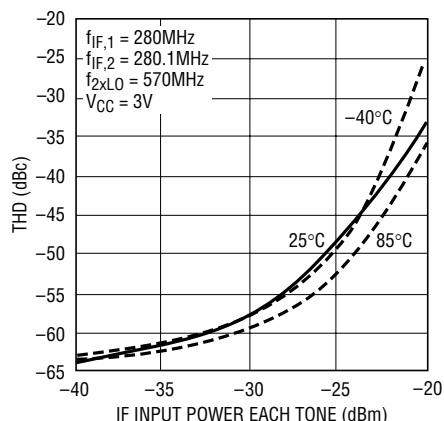
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Total Harmonic Distortion vs IF Input Power and Supply Voltage



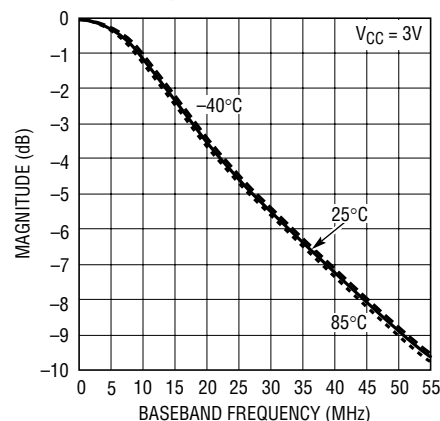
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Total Harmonic Distortion vs IF Input Power at 500mV_{P-P} Differential Out



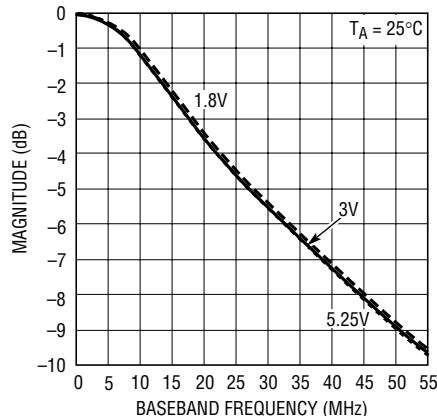
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LPF Frequency Response vs Baseband Frequency and Temperature



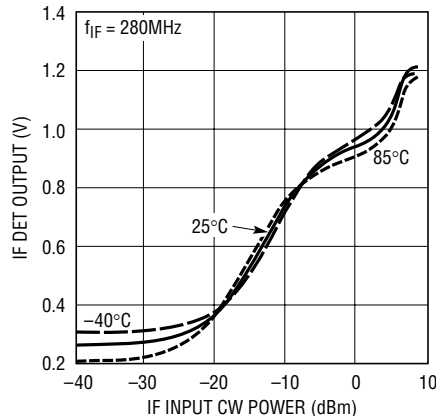
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LPF Frequency Response vs Baseband Frequency and Supply Voltage



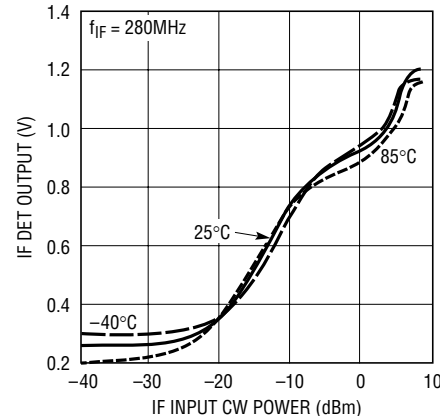
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IF Detector Output Voltage vs IF Input CW Power at 3V Supply



5546 G14

IF Detector Output Voltage vs IF Input CW Power at 1.8V Supply

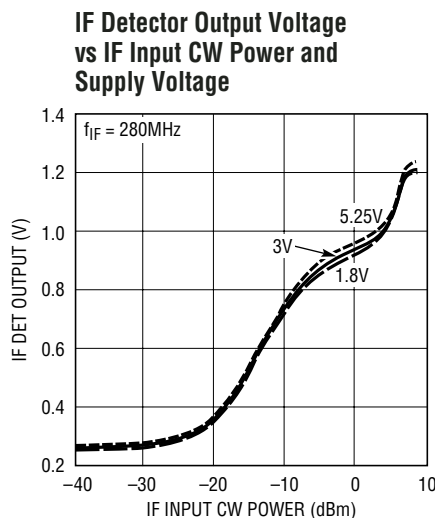


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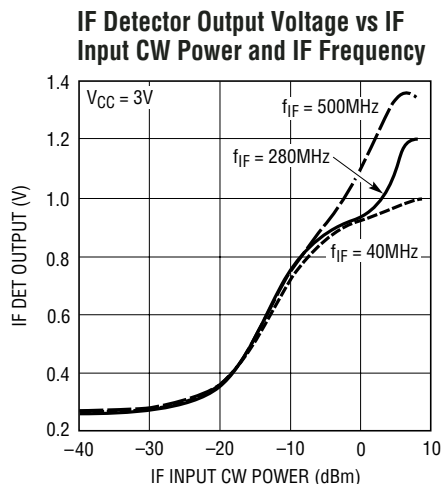
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TYPICAL PERFORMANCE CHARACTERISTICS

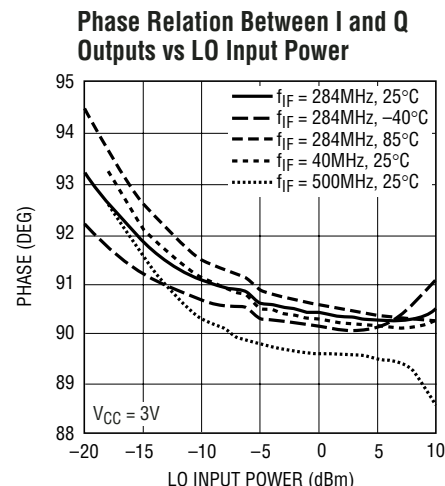
$V_{CC} = 3V$, $f_{2 \times LO} = 570MHz$, $P_{2 \times LO} = -5dBm$
 (Note 5), $f_{IF} = 284MHz$, $P_{IF} = -30dBm$, I and Q outputs $800mV_{P-P}$ into $4k\Omega$ differential load, $T_A = 25^\circ C$, $EN = V_{CC}$, $STBY = V_{CC}$,
 unless otherwise noted. (Note 3)



5546 G16



5546 G17



5546 G18

PIN FUNCTIONS

GND (Pins 1, 4 and 17): Ground. Pins 1 and 4 are connected to each other internally. The exposed pad (Pin 17) is not connected internally to Pins 1 and 4. For chip functionality, the exposed pad and either Pin 1 or Pin 4 must be connected to ground. For best RF performance, Pin 1, Pin 4 and the exposed pad should be connected to RF ground.

IF⁺, IF⁻ (Pins 2, 3): Differential Inputs for the IF Signal. Each pin must be DC grounded through an external inductor or RF transformer with central ground tap. This path should have a DC resistance lower than 2Ω to ground.

V_{CC} (Pins 5 and 8): Power Supply. These pins should be decoupled to ground using 1000pF and 0.1μF capacitors.

V_{CTRL} (Pin 6): VGA Gain Control Input. This pin controls the IF gain and its typical input voltage range is 0.2V to 1.7V. It is internally biased via a 25k resistor to 0.2V, setting a low gain if the V_{CTRL} pin is left floating.

IF DET (Pin 7): IF Detector Output. For strong IF input signals, the DC level at this pin is a function of the IF input signal level.

EN (Pin 9): Enable Input. When the enable pin voltage is higher than 1V, the IC is completely turned on. When the input voltage is less than 0.5V, the IC is turned off, except the part of the circuit associated with standby mode.

2xLO⁻, 2xLO⁺ (Pins 10, 11): Differential Inputs for the 2xLO Input. The 2xLO input frequency must be twice that of the IF frequency. The internal bias voltage is $V_{CC} - 0.4V$.

STBY (Pin 12): Standby Input. When the STBY pin is higher than 1V, the standby mode circuit is turned on to prebias the I/Q buffers. When the STBY pin is less than 0.5V, the standby mode circuit is turned off.

Q_{OUT}⁻, Q_{OUT}⁺ (Pins 13, 14): Differential Baseband Outputs of the Q Channel. Internally biased at $V_{CC} - 1.19V$.

I_{OUT}⁻, I_{OUT}⁺ (Pins 15, 16): Differential Baseband Outputs of the I Channel. Internally biased at $V_{CC} - 1.19V$.

APPLICATIONS INFORMATION

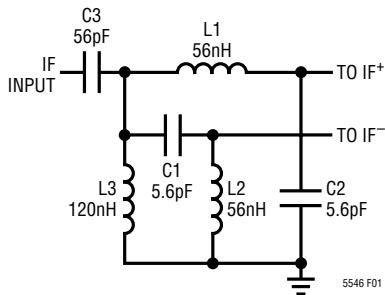


Figure 1. Example L-C IF Input Matching Network at 280MHz

Table 1. The Component Values of Matching Network L1, L2, L3, C1, C2 and C3.

f_{IF} (MHz)	L1, L2(nH)	C1, C2(pF)	L3(nH)	C3(pF)
50	340	34	1800	820
100	159	15.9	470	220
150	106	10.6	470	220
200	80	8.0	470	220
250	64	6.4	120	56
300	53	5.3	120	56
350	45	4.5	120	56
400	40	4.0	120	56
450	35	3.5	120	56
500	32	3.2	120	56

To keep the DC resistance of L3 below 2Ω , 120nH is used. This disturbs the matching network slightly by causing the frequency where the S11 is minimal to be lower than the frequency where the amplitudes of IF⁺ and IF⁻ are equal. To compensate for this, the value of coupling capacitor C3 is lowered and will contribute some correcting reactance. For low frequencies, it might not be possible to find any practical inductor value for L3 with DC resistance smaller than 2Ω . In that case it is recommended to use a transformer with a center tap. The tolerance for the components in Figure 1 can be 10% for a return loss higher than 16dB and a gain reduction due to mismatch less than 0.3dB.

It is possible to simplify the input matching circuit and compromise the performance. In Figure 2a, the simplified matching network is given.

This matching network can deliver equal amplitudes to the IF⁺ and IF⁻ inputs for a narrow frequency region, but the phase difference between the inputs will not be exactly 180 degrees. In practice, the phase shift will be around 145

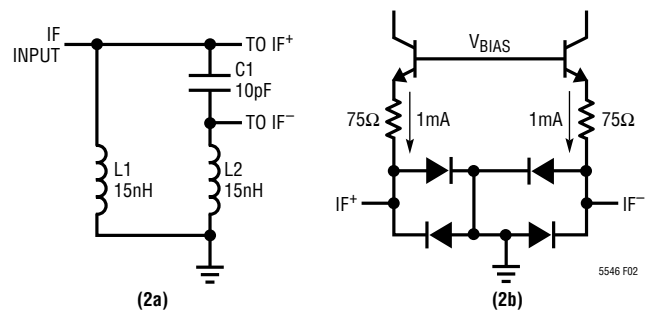


Figure 2a. Simplified IF Input Matching Network at 280MHz and Figure 2b. Simplified Circuit Schematic of the IF Inputs

degrees, depending on the quality factor of the network. This will result in a reduction in the gain. The higher the chosen quality factor, the closer the phase difference will approach 180 degrees. However, a higher quality factor will reduce bandwidth and create more loss in the matching network. For minimum board space, 0402 components are used. The measured noise figure for maximum gain with this matching network is about 9.4dB, and the maximum gain is about 55dB. Assuming 0402 inductors with $Q = 35$, the insertion loss of this network is about 2.5dB. The tolerance for the components in Figure 2a can be 10% for a return loss higher than 10dB and a gain reduction due to mismatch less than 0.5dB. The measured input sensitivity for this matching network (see also Figure 11) is about -78.3dBm for a 10dB signal-to-noise ratio.

The gain of the VGA is set by the voltage at the V_{CTRL} pin. For high gain settings, both the noise figure and the input IP3 will be low. From a noise figure point of view, it is advantageous to work as closely as possible to the maximum gain point. However, if the voltage at the V_{CTRL} pin is increased beyond the maximum gain point (where additional increase in control voltage does not give an increase in gain), the response time of the gain control circuit is increased. If control speed is crucial, a few dB of gain margin should be allowed from the highest gain point to be sure that at all temperatures, the maximum gain setting is not crossed. At low gain settings, the noise figure and the input IP3 will be high. Optionally, the control voltage V_{CTRL} can be set lower than 0.2V. The normal range is from $V_{CTRL} = 0.2\text{V}$ to 1.7V, which results in a nominal gain range from 1.6dB to 56.8dB. The linear-in-dB gain relation with the V_{CTRL} voltage still holds for control voltages as low as -0.35V . This results in an

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extended gain control range of -23dB to 57dB . The V_{CTRL} pin is a very sensitive input because of its high input impedance and therefore should be well shielded. Signal pickup on the V_{CTRL} pin can lead to spurs and increased noise floor in the I/Q baseband outputs. It can degrade the linearity performance and it can cause asymmetry in the two-tone test. If control speed is not important, $1\mu\text{F}$ bypass capacitors are recommended between V_{CTRL} and ground.

A fast responding peak detector is connected to the VGA input, sensitive to signal levels above the signal levels where the VGA is operating in the linear range. It is active from -22dBm up to 5dBm IF input signal levels. The DC output voltage of this detector (IF DET) can be used by the baseband controller to quickly determine the presence of a strong input level at the desired channel, and adjust gain accordingly. Figure 3a shows the simplified circuit schematic of the IF DET output.

I/Q Demodulators

The quadrature demodulators are double balanced mixers, down-converting the amplified IF signal from the VGA into I/Q baseband signals. The quadrature LO signals are generated internally from a double frequency external CW signal. The nominal output voltage of the differential I/Q baseband signals should be set to $0.8V_{\text{P-P}}$ or lower, depending on the linearity requirements. The magnitudes of I and Q are well matched and their phases are 90° apart.

Quadrature LO Generator

The quadrature LO generator consists of a divide-by-two circuit and LO buffers. An input signal ($2x\text{LO}$) with twice the desired IF signal frequency is used as the clock for the divide-by-two circuit, producing the quadrature LO signals for the demodulators. The outputs are buffered and then drive the down-converting mixers. With a fully differential approach, the quadrature LO signals are well matched. Second harmonic content (or higher order even harmonics) in the external $2x\text{LO}$ signal can degrade the 90° phase shift between I and Q. Therefore, such content should be minimized. In disable or standby mode, the divide-by-two stage is powered down. After enabling the circuit, the phase relation between the IF signal and the baseband (I or Q) signals can be either 0° or 180° , since the circuit cannot distinguish between the two subsequent identical sinusoidal

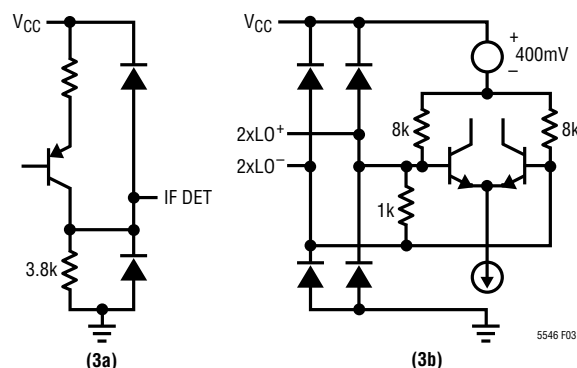


Figure 3a. Simplified Circuit Schematic of the IF DET Output and Figure 3b. The $2x\text{LO}$ Inputs

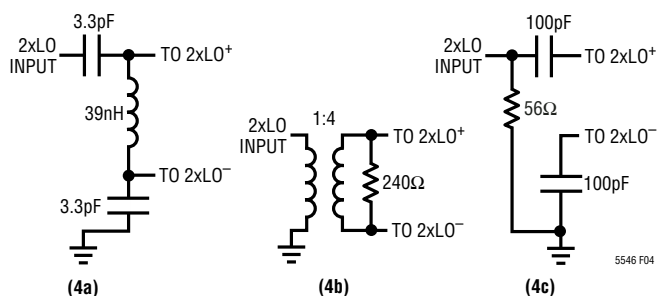


Figure 4. $2x\text{LO}$ Input Matching Networks for 4a) Narrow Band Tuned to 570MHz , 4b) Wide Band, 4c) Single-Ended Wide Band

dal waveforms of the $2x\text{LO}$ input signal. The phase relation between I and Q is always 90° , i.e. I always leads Q by 90° for $f_{\text{IF}} > 1/2 \cdot f_{2x\text{LO}}$. Figure 3b shows the simplified circuit schematic of the $2x\text{LO}$ inputs. Depending on the application, different $2x\text{LO}$ input matching networks can be chosen. In Figure 4, three examples are given. The first network provides the best $2x\text{LO}$ input sensitivity because it can boost the $2x\text{LO}$ differential input signal using a narrow-band resonant approach. The second network gives a wide-band match, but the $2x\text{LO}$ input sensitivity is about 2dB lower. The third network gives a simple and less expensive wide-band match, but $2x\text{LO}$ input sensitivity drops by about 9dB . The IF input sensitivity doesn't change significantly using any of the three $2x\text{LO}$ matching networks.

Baseband Circuit

The baseband circuit consists of I/Q low-pass filters, I/Q hard limiters (clippers) and I/Q output buffers. The hard limiters operate as linear amplifiers normally. However, if a high level input temporarily overloads a linear amplifier,

APPLICATIONS INFORMATION

then the circuit will limit symmetrically, which will help to prevent the output buffer from overloading. This speeds up recovery from an overload event, which can occur during the gain settling. The clipping level is approximately constant over temperature. The first order integrated lowpass filters are used for noise filtering of the down-converted baseband signals for both the I channel and the Q channel. These filters are well matched in gain response. The -3dB corner frequency is typically 17MHz . The I/Q outputs can drive $2\text{k}\Omega$ in parallel with a maximum capacitive loading of 10pF at 5MHz , from all four pins to ground. The outputs are internally biased at $V_{CC} - 1.19\text{V}$. Figure 5 shows the simplified output circuit schematic of the I channel or Q channel.

The I/Q baseband outputs can be DC-coupled to the inputs of a baseband chip. For AC-coupled applications with large capacitors, the STBY pin can be used to pre-bias the outputs to nominal $V_{CC} - 1.19\text{V}$ at much reduced current. This mode draws only 3.6mA supply current. When the EN pin is then driven high ($>1\text{V}$), the chip is quickly switched to normal operating mode, avoiding the introduction of

large charging time constants. Table 2 shows the logic of the EN pin and STBY pin. In both normal operating mode and standby mode, the maximum discharging current is about $300\mu\text{A}$, and the maximum charging current is more than 4mA . In Figure 5 the simplified circuit schematic of the STBY (or EN) input is shown.

Table 2. The Logic of Different Operating Modes

EN	STBY	Comments
Low	Low	Shutdown Mode
Low	High	Standby Mode
High	Low or High	Normal Operation Mode

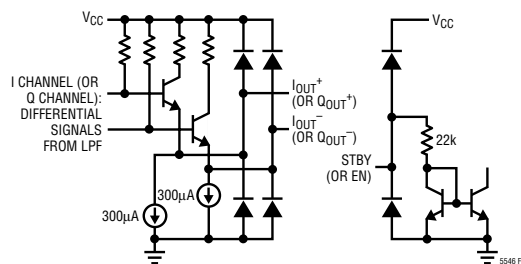


Figure 5. Simplified Circuit Schematic of I Channel (or Q Channel) Outputs and STBY (or EN) Input

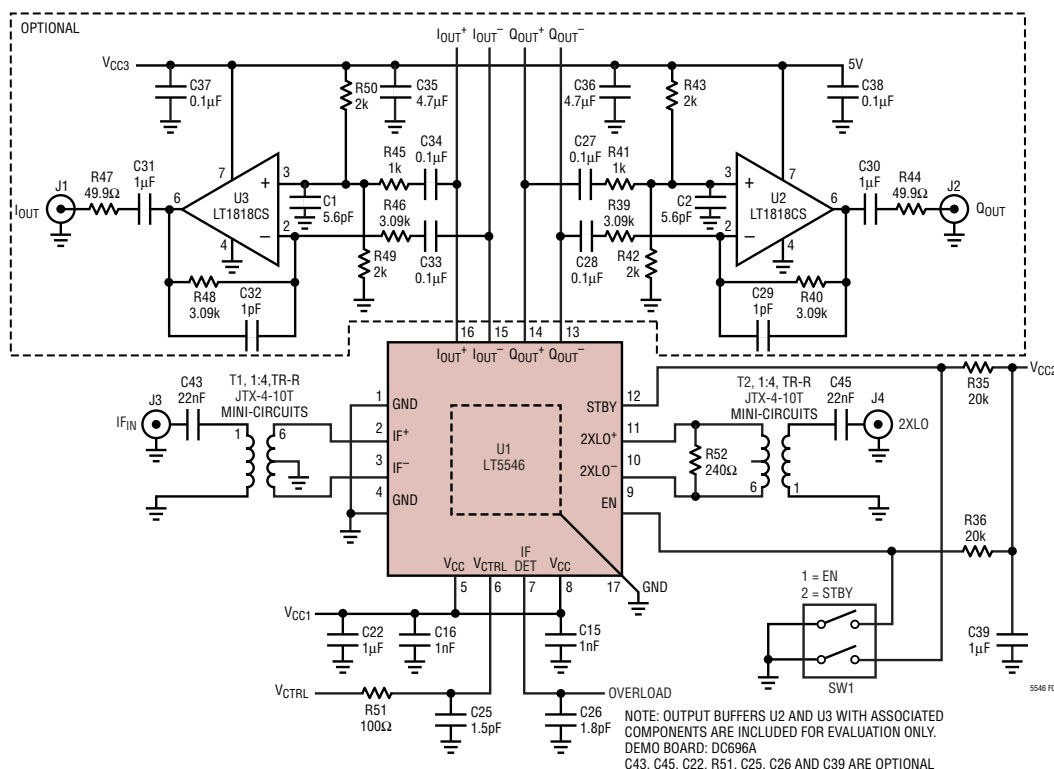


Figure 6. Evaluation Circuit Schematic with I/Q Output Buffers

The evaluation circuit schematic is drawn in Figure 6. The components associated with buffers U2 and U3 are included to drive a 50Ω load for evaluation purposes only.

The diagram shows the internal circuitry of the DC696A L75546EUF receiver, a 16-pin DIP package. The pins are numbered 1 through 16 around the perimeter. Key components and connections include:

- Pin 1:** Vcc3 (3.3V-3.25V), connected to a 10k resistor (R3) and a 100pF capacitor (C3).
- Pin 2:** VoutI, connected to a 100pF capacitor (C2).
- Pin 3:** GND.
- Pin 4:** Vcc1 (1.8V-2.25V), connected to a 10k resistor (R1) and a 100pF capacitor (C1).
- Pin 5:** Voutm, connected to a 100pF capacitor (C4).
- Pin 6:** Voutpq, connected to a 100pF capacitor (C5).
- Pin 7:** Voutmq, connected to a 100pF capacitor (C6).
- Pin 8:** IFin, connected to a 100pF capacitor (C7).
- Pin 9:** Vcc2 (1.8V-2.25V), connected to a 10k resistor (R2) and a 100pF capacitor (C8).
- Pin 10:** Vctrl, connected to a 100pF capacitor (C9).
- Pin 11:** E1, connected to a 100pF capacitor (C10).
- Pin 12:** E2, connected to a 100pF capacitor (C11).
- Pin 13:** E3, connected to a 100pF capacitor (C12).
- Pin 14:** E4, connected to a 100pF capacitor (C13).
- Pin 15:** E5, connected to a 100pF capacitor (C14).
- Pin 16:** E6, connected to a 100pF capacitor (C15).

The schematic also shows various internal components like resistors (R1-R3), capacitors (C1-C15), and a central IC block labeled DC696A L75546EUF. The package is identified as a DIP16.

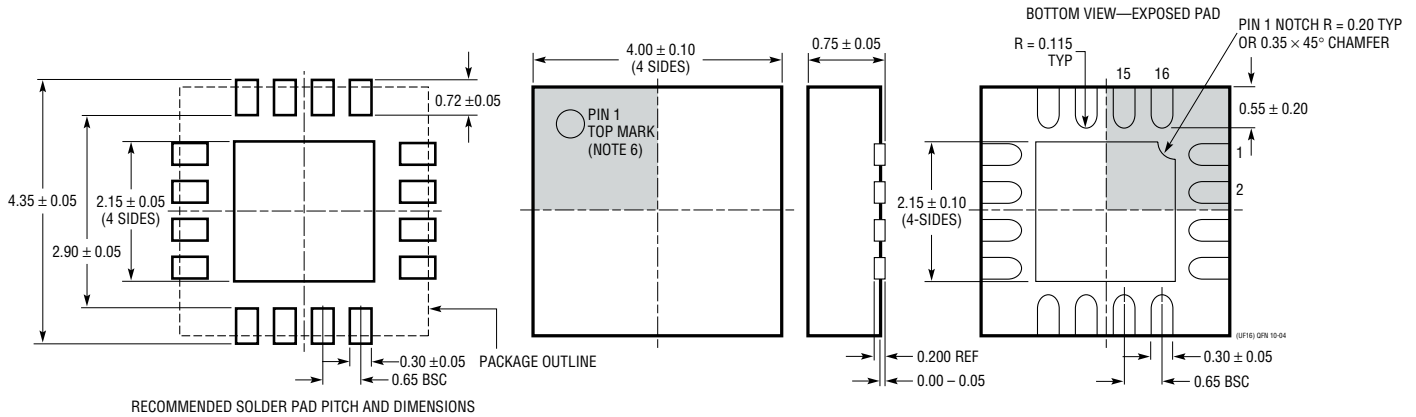
Figure 1 shows the pin connections for the 16-pin DIP package. The top view shows pins 1 through 16 arranged in two rows of eight. The bottom view shows pins 1 through 16 arranged in two rows of eight. The pin numbers are indicated next to the corresponding pins.

[illegible]

11

PACKAGE DESCRIPTION

UF Package 16-Lead Plastic QFN (4mm × 4mm) (Reference LTC DWG # 05-08-1692)


NOTE:

1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WG6C)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Signal Level Upconverting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	High Signal Level Downconverting Mixer	DC-3GHz, 20dBm IIP3, Integrated LO Buffer
LT5515	1.5GHz to 2.5GHz Direct-Conversion Quadrature Demodulator	20dBm IIP3, NF = 16.8dB, Integrated LO Quadrature Generator
LT5516	800MHz to 1.5GHz Direct-Conversion Quadrature Demodulator	4V to 5.25V Supply, 21.5dBm IIP3, NF = 12.8dB, Integrated LO Quadrature Generator
LT5522	600MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
RF Power Detectors		
LT5504	800MHz to 2.7GHz RF Measuring Receiver	2.7V to 5.25V Supply, 80dB Dynamic Range, Temperature Compensated
LTC5505	RF Power Detectors with >40dB Dynamic Range	2.7V to 6V Supply, 300MHz to 3.5GHz, Temperature Compensated
LTC5507	100kHz to 1000MHz RF Power Detector	2.7V to 6V Supply, 48dB Dynamic Range, Temperature Compensated
LTC5508	0.3GHz to 7GHz RF Power Detector	2.7V to 6V Supply, 44dB Dynamic Range, Temperature Compensated
LTC5509	300MHz to 3GHz RF Power Detector	–30dBm to 6dBm, 600μA Supply Current, Temperature Compensated
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
RF Receiver Building Blocks		
LT5500	1.8GHz to 2.7GHz Receiver Front End	1.8V to 5.25V Supply, Dual-Gain LNA, Mixer
LT5502	400MHz Quadrature IF Demodulator with RSSI	1.8V to 5.25V Supply, 70MHz to 400MHz IF, 84dB Limiting Gain, 90dB RSSI Range
LT5503	1.2GHz to 2.7GHz Direct IQ Modulator and Mixer	1.8V to 5.25V Supply, Four Step RF Power Control, 120MHz Modulation Bandwidth
LT5506	40MHz to 500MHz Quadrature IF Demodulator with VGA	1.8V to 5.25V, I/Q Baseband Bandwidth 8.8MHz, –40dB to 57dB Linear Power Gain



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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