PSMN0R7-25YLD

N-channel 25 V, 0.72 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

25 July 2017 Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- 100% Avalanche tested at $I_{(AS)}$ = 190 A
- Ultra low Q_G, Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 150 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	25	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	300	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	158	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	0.76	0.92	mΩ

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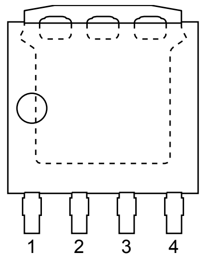
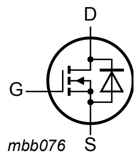
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	11.9	-	nC

[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	Gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN0R7-25YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56); 4 leads	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN0R7-25YLD	0D725L

8. Limiting values

Table 5. Limiting values

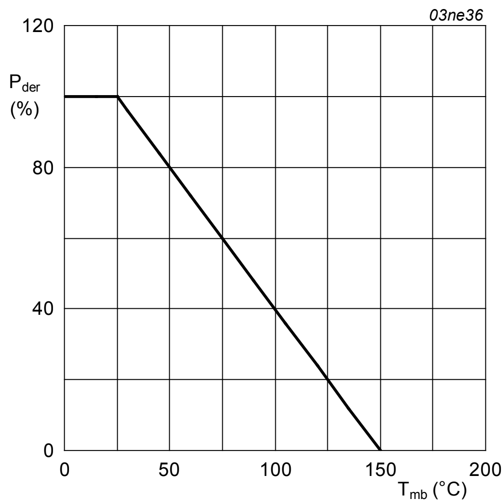
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	25	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	25	V
V_{GS}	gate-source voltage			-20	20	V

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	158	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	300	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	235	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1482	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	132	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1482	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 300 A; V_{sup} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 36 µs		-	174	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 25 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[2]	-	190	A

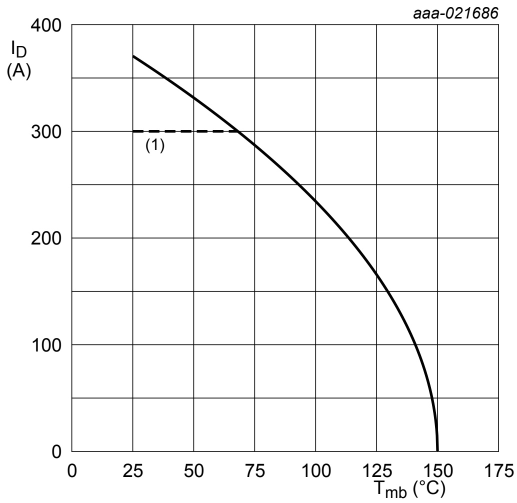
[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature

[2] Protected by 100% test



$$P_{der} = \frac{P_{(tot)}}{P_{tot(25°C)}} \times 100\,\%$$

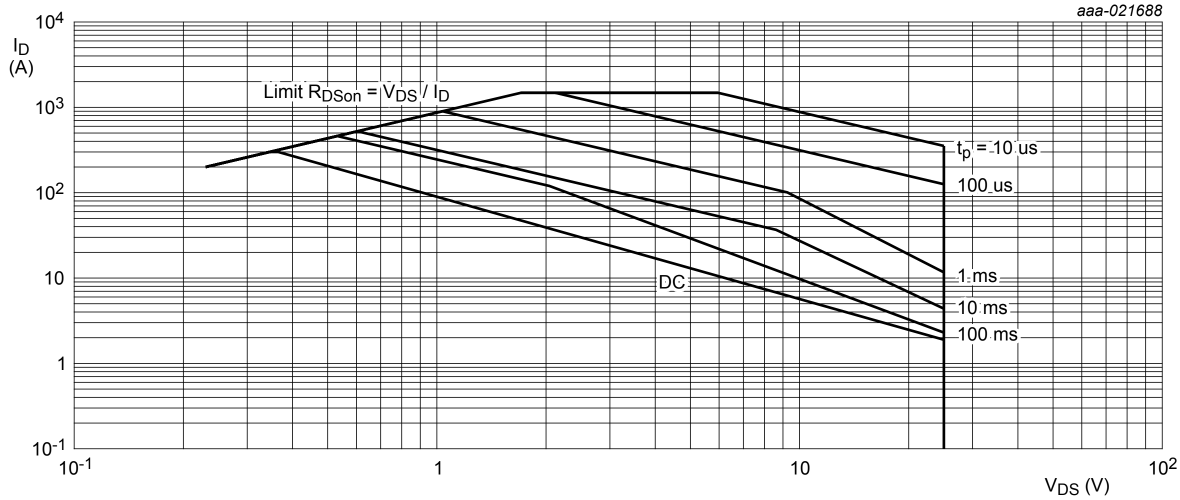
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

(1) 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB thermal design and operating temperature

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.59	0.79	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	50	-	K/W
		Fig. 6		-	125	-	K/W

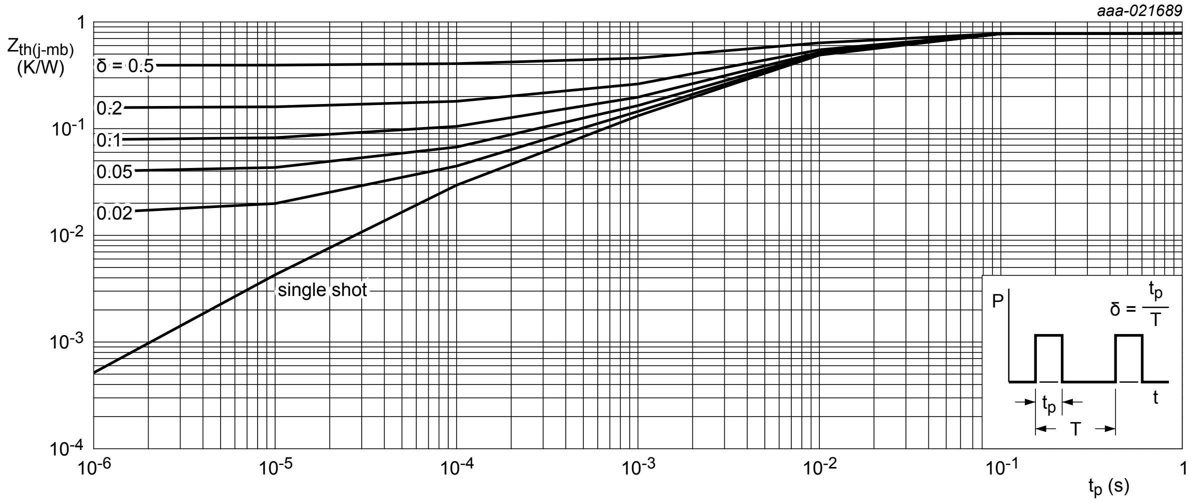
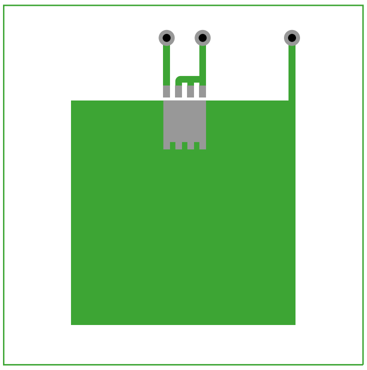
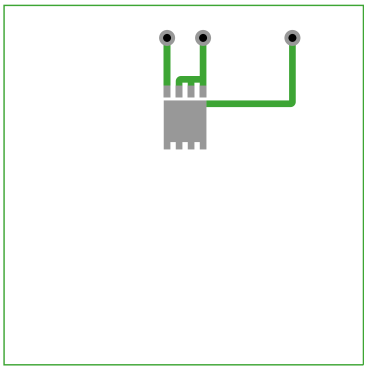


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-005750

Fig. 5. PCB layout for thermal impedance junction to ambient 1" square pad; FR4 Board; 2oz copper



aaa-005751

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

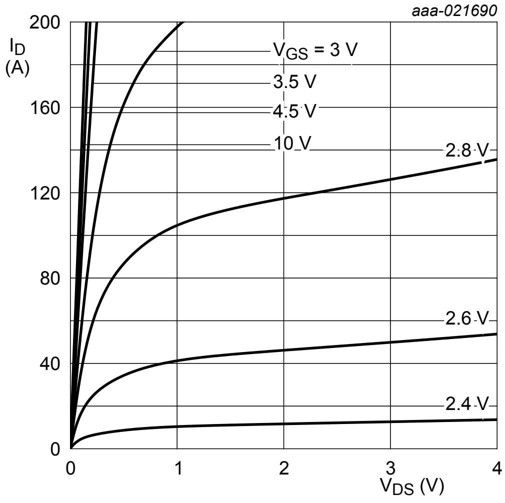
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		25	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		1.2	1.66	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-5.1	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 125 °C		-	68.5	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	0.76	0.92	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	1.47	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 10		-	0.57	0.72	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	1.15	mΩ
R_G	gate resistance	f = 1 MHz		-	1.35	-	Ω

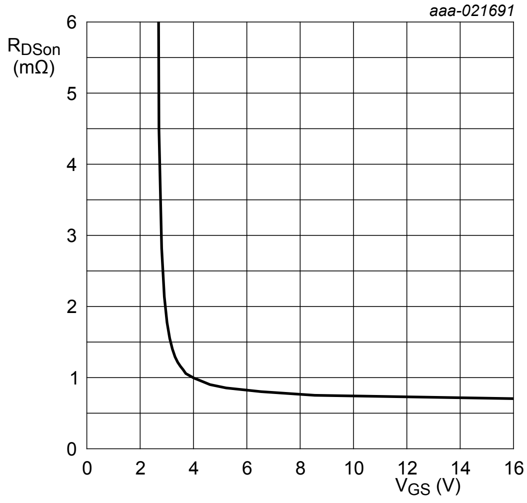
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	110.2	-	nC
		I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	50.9	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	45.8	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	18.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	11.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	6.9	-	nC
Q_{GD}	gate-drain charge			-	11.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 12 V; Fig. 12; Fig. 13		-	2.6	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	8320	-	pF
C_{oss}	output capacitance			-	2982	-	pF
C_{rss}	reverse transfer capacitance			-	522	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	42.2	-	ns
t_r	rise time			-	48.3	-	ns
$t_{d(off)}$	turn-off delay time			-	53.1	-	ns
t_f	fall time			-	38.2	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; T_j = 25 °C		-	54	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.77	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 12 V; Fig. 16		-	57.7	-	ns
Q_r	recovered charge		[1]	-	83.2	-	nC
t_a	reverse recovery rise time			-	30.5	-	ns
t_b	reverse recovery fall time			-	27.2	-	ns
S	softness factor			-	0.9	-	

[1] includes capacitive recovery



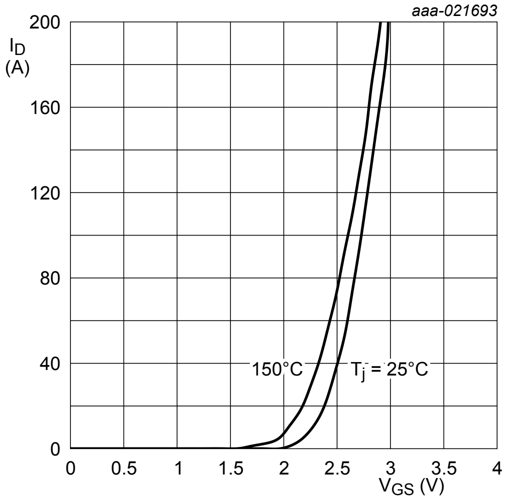
T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



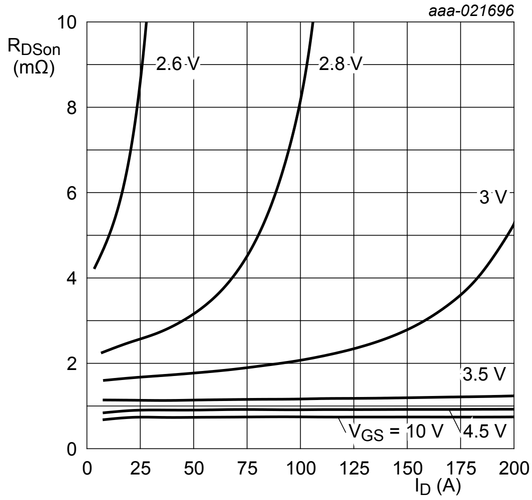
T_j = 25 °C; I_D = 25 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



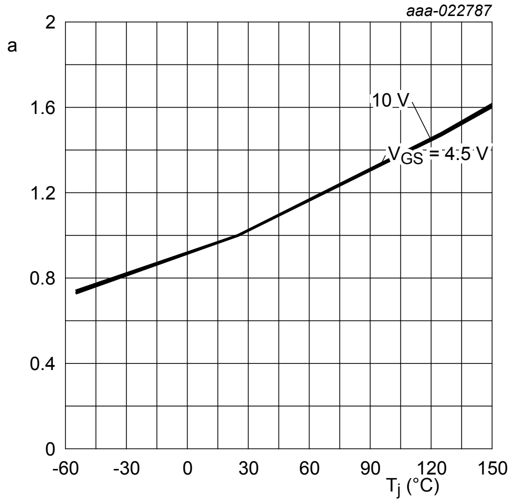
V_{DS} = 12 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



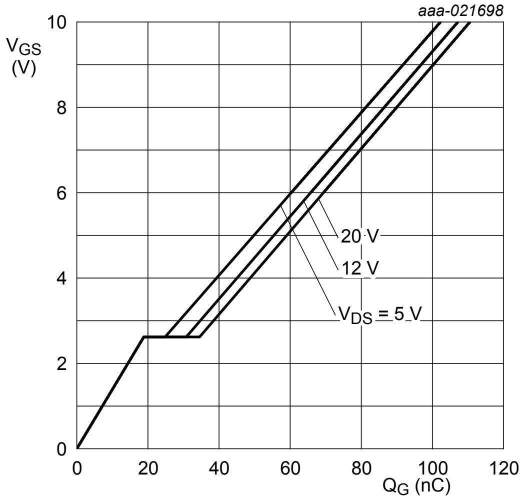
T_j = 25 °C

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}\ (25°C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 12. Gate-source voltage as a function of gate charge; typical values

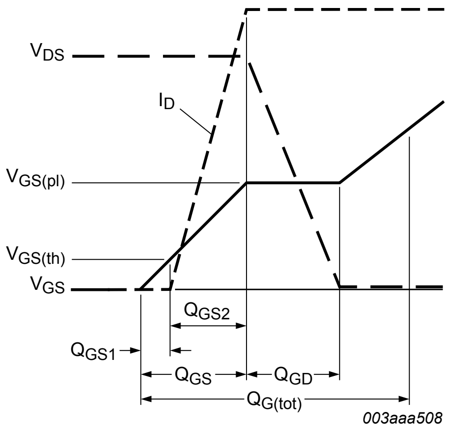
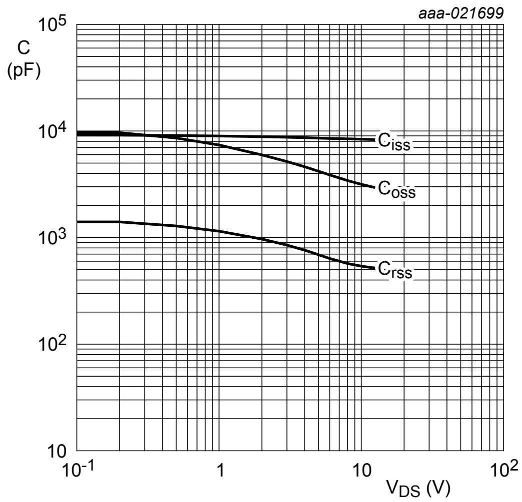
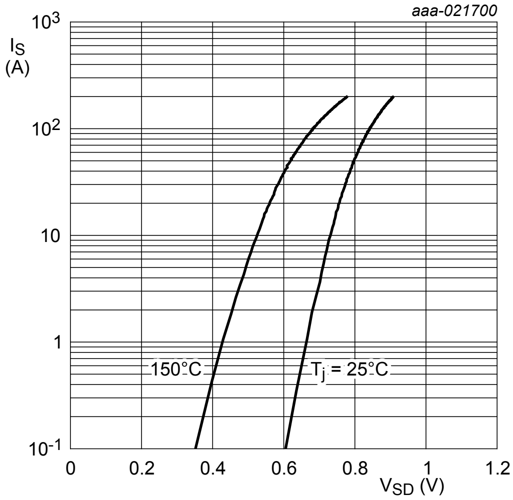


Fig. 13. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

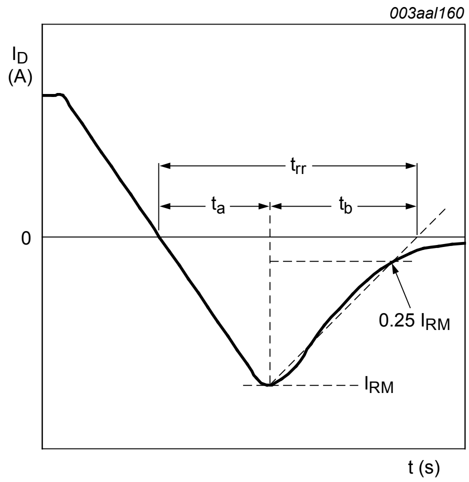
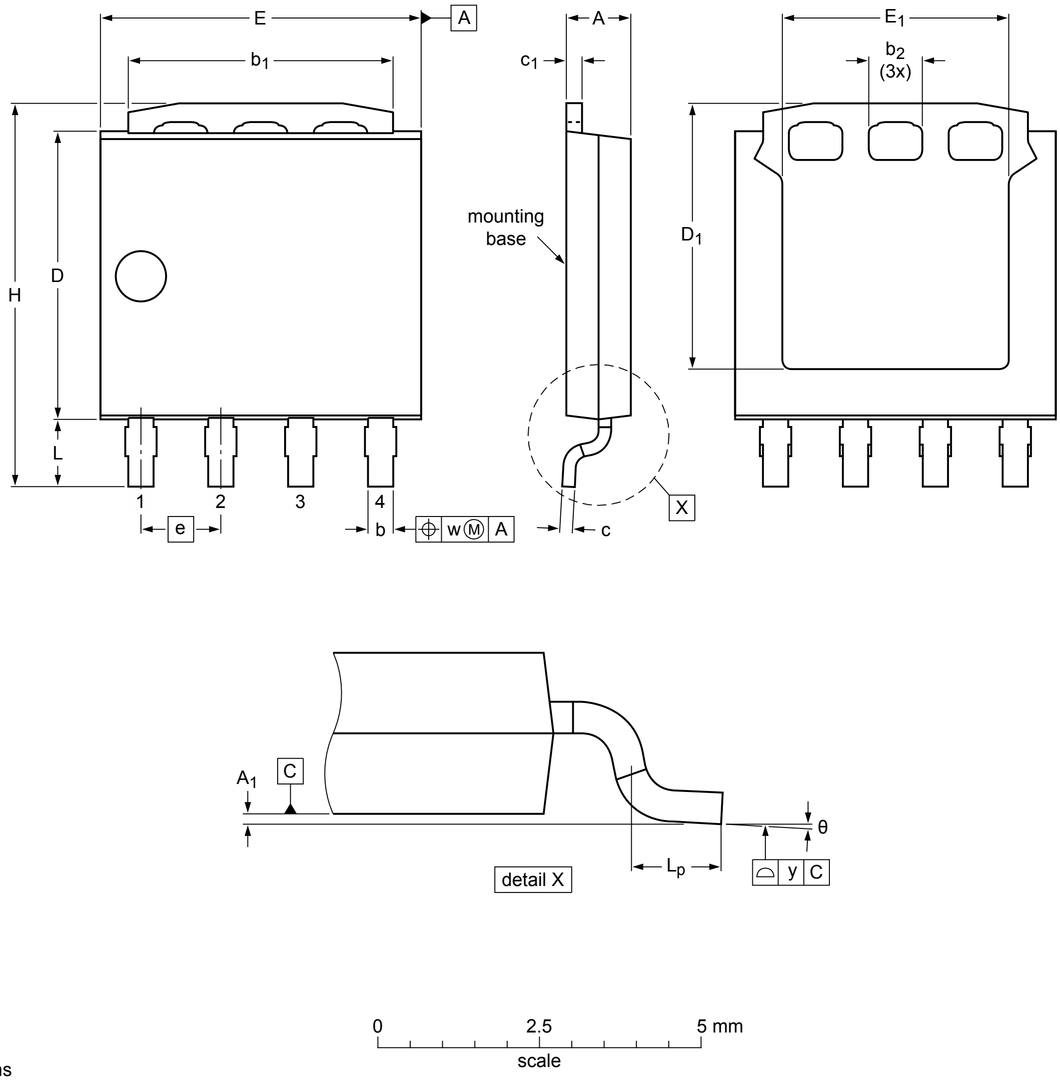


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~11-12-09~~ 13-03-05

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT1023)

12. Soldering

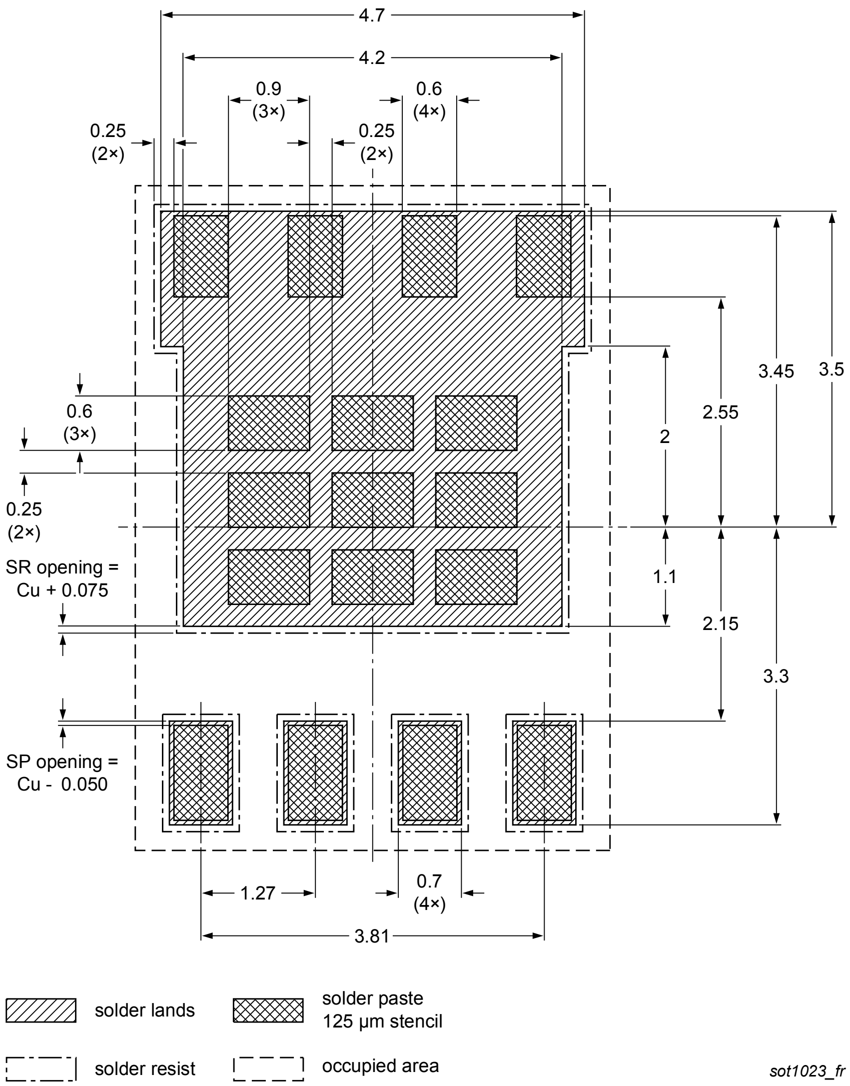


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT1023)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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