PICO-IMX6UL-EMMC

PICO Compute Module with NXP i.MX6Ultralite SoC

REV. A1 – VER. 1.00

March 28, 2016

REVISION HISTORY

Revision	Date	Originator	Notes
1.00	March 28, 2016	TechNexion	Initial Public release

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1. Introduction

1.1. General Introduction

The PICO-IMX6UL-EMMC is a high performance highly integrated PICO Compute Module designed around the NXP i.MX6Ultralite ARM Cortex-A7. The PICO-IMX6UL-EMMC provides an ideal building block that easily integrates with a wide range of target markets requiring compact, cost effective with low power consumption.

The modular approach offered by the PICO Compute Module gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

1.2. General Care and Maintenance

Your device is a product of superior design and craftsmanship and should be treated with care.

The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

Regulatory information

Disposal of Waste Equipment by Users in Private Household in the European Union
This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15

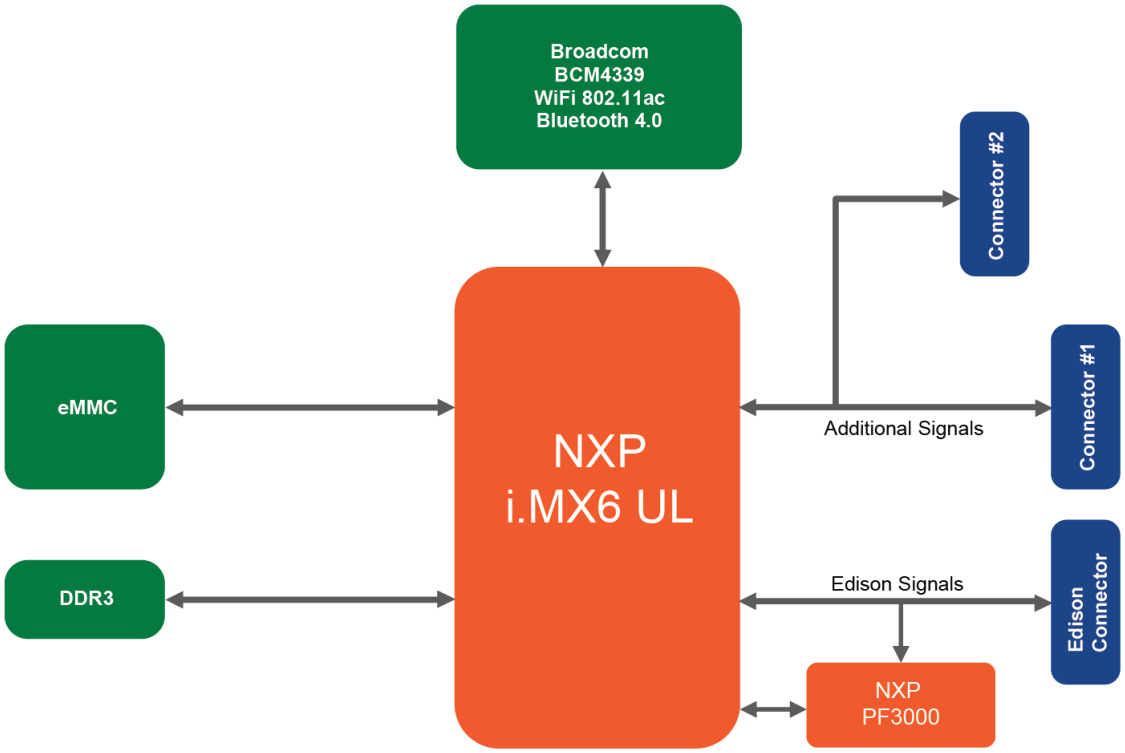
This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

1.3. Block Diagram

Figure 1 - PICO-IMX6UL-EMMC Block Diagram



1.4. PICO Compute Module Compatibility

The PICO-IMX6UL-EMMC is function compatible with Intel® Edison and adds additional multimedia I/O Interfaces on two additional expansion interfaces.

Many of the pins on PICO-IMX6UL-EMMC can be used for other functions. **Chapter 5. PICO Compute Module Pinmux Overview** of this manual provides a complete overview.

Figure 2 - PICO-IMX6UL-EMMC Compatibility Chart

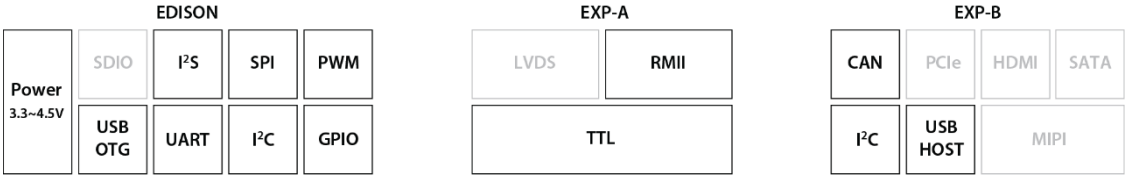


Table 1 - PICO Compatibility Overview

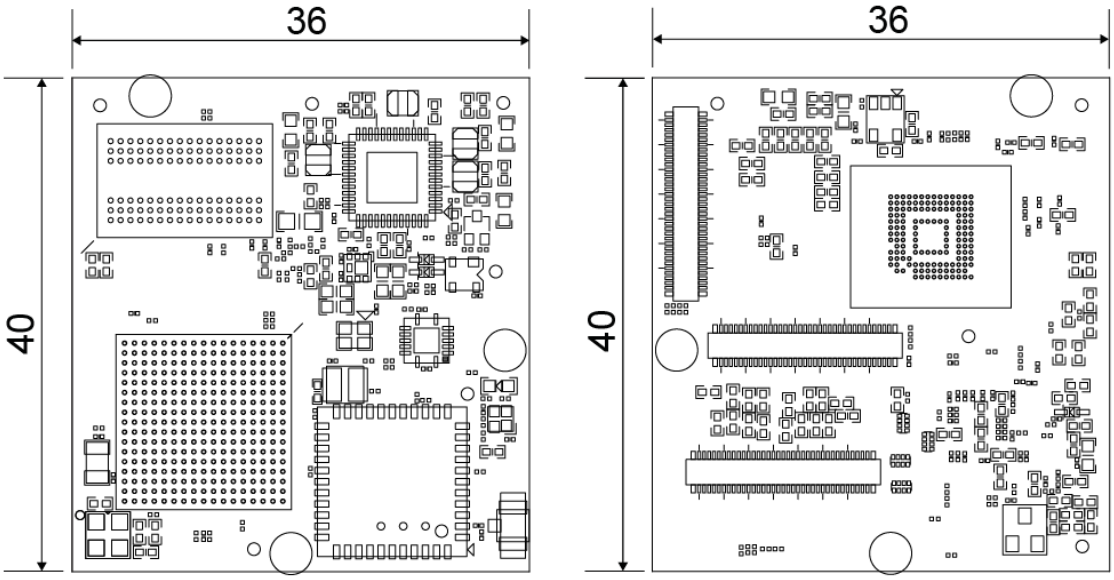
Interface	Description
LAN	1 Fast Ethernet
LVDS	Not available
HDMI	Not available
TTL Display	1 TTL 18/24 bit Display
PCIe	Not available
SATA	Not available
USB Host	1 USB 2.0 Host port
USB OTG	1 USB 2.0 OTG port (possible to use in Host mode)
I^2S	1 I^2S interface
CAN Bus	2 FlexCAN CAN 2.0B protocol compliant interfaces
UART	1 UART (2 wire) 1 UART (4 wire)
SDIO	Not available
SPI	1 SPI interface
I^2C	3 independent I^2C channels
GPIO	10 dedicated GPIO's available
PWM	4 PWM available

1.5. Dimensional Drawing

The PICO-IMX6UL-EMMC Compute Module is partly size compatible with Intel® Edison and adds several additional I/O expansion interfaces on an enlarged footprint.

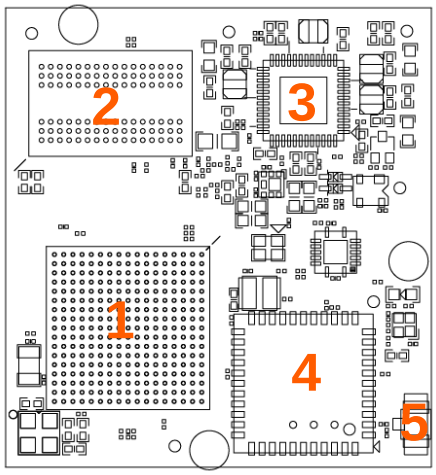
2D and 3D files can be obtained from the **www.technexion.com** homepage.

Figure 3 - PICO-IMX6UL-EMMC Dimensional Drawing



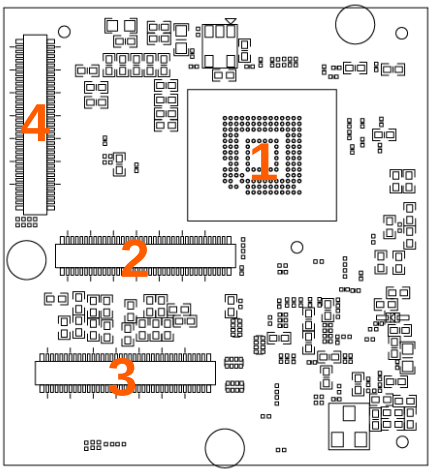
1.6. Component Location

Figure 4 - PICO-IMX6UL-EMMC Top view



Item	Description	Item	Description
1	NXP i.MX6Ultralite Processor	2	Memory IC
3	NXP PF300 Power Management IC	4	BCM4339 WiFi/Bluetooth IC
5	Antenna connector		

Figure 5 - PICO-IMX6UL-EMMC Bottom view



Item	Description	Item	Description
1	eMMC Storage IC	2	Intel® Edison Compatible Connector
3	Expansion Connector 1	4	Expansion Connector 2

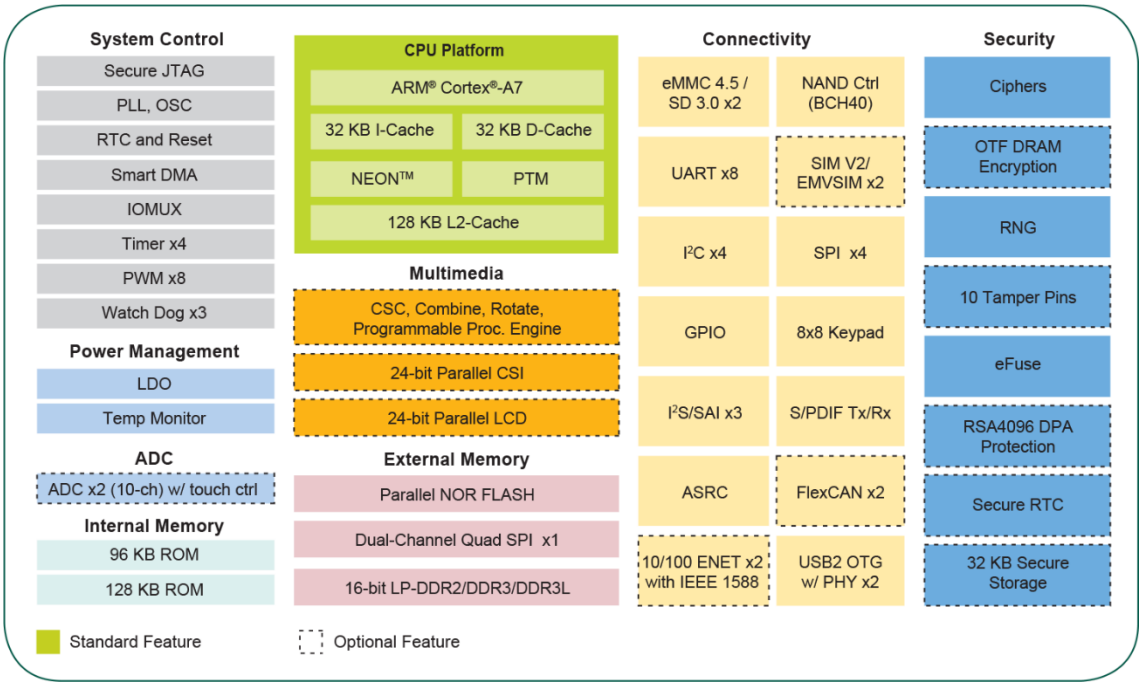
2. Core Components

2.1. NXP i.MX6Ultralite Cortex-A7 Processor

The i.MX 6UltraLite is an ultra-efficient processor family with featuring Freescale's advanced implementation of the single ARM Cortex®-A7 core, which operates at speeds of up to 528 MHz.

- The device is composed of the following major subsystems:
  - Single-core ARM Cortex-A7 MPCore™ Platform
  - 32 KBytes L1 Instruction Cache
  - 32 KBytes L1 Data Cache
  - Private Timer and Watchdog
  - TrustZone support
  - Cortex-A7 NEON MPE (Media Processing Engine) Co-processor
- PXP—PiXel Processing Pipeline for imagine resize, rotation, overlay and CSC. Offloading key pixel processing operations are required to support the LCD display applications.

Figure 6 - NXP i.MX6Ultralite Processor Blocks



2.2. Power Management IC (NXP PF3000)

The PICO-IMX6UL-EMMC has on onboard NXP PF3000 power management integrated circuit (PMIC) that features a configurable architecture supporting the numerous outputs with various current ratings as well as programmable voltage and sequencing required by the components on the PICO-IMX6UL-EMMC module.

Table 2 - PMIC Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	V	I/O	Description
L17	GPIO1_IO03	i2c1.SDA (mode0)	SDA	3V3	I/O	I²C bus data line
L14	GPIO1_IO02	i2c1.SCL (mode0)	SCL	3V3	I/O	I²C bus clock line
T9	SNVS_PMIC_ON_REQ	snvs_lp_wrapper.PMIC_ON_REQ (mode0)	PWRON	3V3	I	PMIC Power ON/OFF Input from processor
P9	SNVS_TAMPER4	gpio5.IO[4] (mode5)	INT	3V3	I	PMIC Interupt Signal
P8	POR_B	src.POR_B (mode0)	RESETBMCU	3V3	I	PMIC Reset Signal
U9	CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ (mode0)	STANDBY	3V3	I	PMIC Standby Input Signal

2.2.1. NXP PF3000 Reset Signal

To perform a hard-reset of the PICO-IMX6UL-EMMC a software reset signal can be implemented.

Table 3 - PMIC Reset Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	V	I/O	Description
E9	LCD_RESET	lcdif.RESET (mode0)	RESET	3V3	I	Connected to the PWRON signal of PMIC

To perform a hard-reset of the PICO-IMX6UL-EMMC an external circuit (for example a button or external watchdog IC) can be integrated on the carrier board.

Table 4 - PMIC Reset Signal Description

Connector	Signal	V	I/O	Description
E1_36	RESET	3V3	I	Connected to the PWRON signal of PMIC on the PICO Compute Module. Connected to the RESET Button on the Hobbitboard.

2.3. Memory

The PICO-IMX6UL-EMMC integrates Double Data Rate III (DDR3) Synchronous DRAM in a single (16 bit) channel configuration.

The following memory chips have been validated and tested on the PICO-IMX6UL-EMMC Compute Module:

2.3.1 SK Hynix

SK Hynix low power Double Data Rate III (DDR3L) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density, high bandwidth and low power operation at 1.35V.

SK Hynix DDR3L SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

SK Hynix memory features:

- VDD=VDDQ=1.35V + 0.100 / - 0.067V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10 and 11, 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0o C~ 95 o C)
  - 7.8 µs at 0 o C ~ 85 o C
  - 3.9 µs at 85 o C ~ 95 o C
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- 8 bit pre-fetch

More information can be retrieved from SKHynix.

2.3.2. Micron

Micron 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Unless stated otherwise, the DDR3L SDRAM device meets the functional and timing specifications listed in the equivalent density standard or automotive DDR3 SDRAM data sheet located on www.micron.com.

Micron memory features:

- VDD = VDDQ = 1.35V (1.283–1.45V)
- Backward-compatible to VDD = VDDQ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self-refresh mode
- TC of 0°C to +95°C
  – 64ms, 8192-cycle refresh at 0°C to +85°C
  – 32ms at +85°C to +95°C
- Self-refresh temperature (SRT)

More information can be retrieved from Micron.

2.4. eMMC Storage

The PICO-IMX6UL-EMMC can be ordered with onboard eMMC storage in different configurations and capacity.

The onboard eMMC device is connected on the SD1 pins of the i.MX6Ultralite processor in an 8 bit width configuration.

The following eMMC chips have been validated and tested on the PICO-IMX6UL-EMMC Compute Module:

2.4.1. Sandisk iNAND

iNAND Ultra is an Embedded Flash Drive (EFD) designed for mobile handsets and consumer electronic devices. iNAND Ultra is a hybrid device combining an embedded thin flash controller and standard MLC NAND flash memory, with an industry standard e.MMC 4.511 interface. Empowered with a new e.MMC4.51 feature set such as Power Off Notifications and Packed commands, as well as legacy e.MMC4.41 features such as Boot and RPMB partitions, HPI, and HW Reset the iNAND Ultra e.MMC is the optimal device for reliable code and data storage.

iNAND provides mass storage of up to 128GB in JEDEC compatible form factors, with low power consumption and high performance.

In addition to the high reliability and high system performance, it offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as advanced power management scheme.

iNAND Ultra uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by embedded flash management software running as firmware on the flash controller.
The architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-levelling, and automatic block management to ensure high data reliability and maximize flash life expectancy.

SanDisk iNAND Extreme, with MMC interface, features include the following:

- Memory controller and NAND flash
- Complies with e.MMC Specification Ver. 4.512
- Mechanical design complies with JEDED MO-276C Specification
- Offered in two TFBGA packages of e.MMC 4.513
- Operating temperature range: -25C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6v
- I/O (VCCQ) voltage 2.7-3.6v
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed)
- Up to 104 MB/sec bus transfer rate, using 8 parallel data lines at 52 MHz, DDR Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage

More information can be retrieved from SanDisk.

2.4.2. Kingston EMMC

Kingston e•MMC™ products follow the JEDEC e•MMC™ 4.5 standard. It is an ideal universal storage solutions for many electronic devices, including smartphones, tablet PCs, PDAs, eBook readers, digital
cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. E•MMC™ encloses the MLC NAND and e•MMC™ controller inside as one JEDEC standard package, providing a standard interface to the host. The e•MMC™ controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

The Kingston NAND Device is fully compatible with the JEDEC Standard Specification No.JESD84-B45.
This datasheet describes the key and specific features of the Kingston e•MMC™ Device. Any additional
information required interfacing the Device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

Kingston e•MMC™, with MMC interface, features include the following:

- Packaged NAND flash memory with e•MMC™ 4.5 interface
- Compliant with e•MMC™ Specification Ver.4.4, 4.41 & 4.5
- Bus mode
    - High-speed e•MMC™ protocol
    - Provide variable clock frequencies of 0-200MHz.
    - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits
    - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
    - Single data rate : up to 200Mbyte/s @ HS200(Host clock @ 200MHz)
    - Dual data rate : up to 104Mbyte/s @ 52MHz
- Supports (Alternate) Boot Operation Mode to provide a simple boot sequence method
- Supports SLEEP/AWAKE (CMD5).
- Host initiated explicit sleep mode for power saving
- Enhanced Write Protection with Permanent and Partial protection options
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Supports Background Operations & High Priority Interrupt (HPI)
- Supports enhanced storage media feature for better reliability
- Operating voltage range :
    - VCCQ = 1.8 V/3.3 V
    - VCC = 3.3 V
- Error free memory access
    - Internal error correction code (ECC) to protect data communication
    - Internal enhanced data management algorithm
    - Solid protection of sudden power failure safe-update operations for data content
- Security
    - Support secure bad block erase commands
    - Enhanced write Protection with permanent and partial protection options

More information can be retrieved from Kingston.

Table 5 - eMMC Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	V	I/O	Description
B3	SD1_DATA0	usdhc1.DATA0 (mode0)	eMMC_DATA0	3V3	I/O	MMC/SDIO Data bit 0
B2	SD1_DATA1	usdhc1.DATA1 (mode0)	eMMC_DATA1	3V3	I/O	MMC/SDIO Data bit 1
B1	SD1_DATA2	usdhc1.DATA2 (mode0)	eMMC_DATA2	3V3	I/O	MMC/SDIO Data bit 2
A2	SD1_DATA3	usdhc1.DATA3 (mode0)	eMMC_DATA3	3V3	I/O	MMC/SDIO Data bit 3
A3	NAND_READY_B	usdhc1.DATA4 (mode1)	eMMC_DATA4	3V3	I/O	MMC/SDIO Data bit 4
C5	NAND_CE0_B	usdhc1.DATA5 (mode1)	eMMC_DATA5	3V3	I/O	MMC/SDIO Data bit 5
B5	NAND_CE1_B	usdhc1.DATA6 (mode1)	eMMC_DATA6	3V3	I/O	MMC/SDIO Data bit 6
A4	NAND_CLE	usdhc1.DATA7 (mode1)	eMMC_DATA7	3V3	I/O	MMC/SDIO Data bit 7
C2	SD1_CMD	usdhc1.CMD (mode0)	eMMC_CMD	3V3	I/O	MMC/SDIO Command
C1	SD1_CLK	usdhc1.CLK (mode0)	eMMC_CLK	3V3	O	MMC/SDIO Clock

2.5. Broadcom BCM4339 WiFi/Bluetooth SiP Module

The PICO-IMX6UL-EMMC can be ordered with an optional onboard WiFI/Bluetooth SIP module. The 802.11ac + BT SiP module is a small sized BGA mounted module that provides full function of 802.11ac and Bluetooth class 4.0 +HS

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11ac Wi-Fi + Bluetooth features.

The SIP module is based on Broadcom BCM4339 chipset which is a WiFi + BT SOC. The Radio architecture & high integration MAC/BB chip provide excellent sensitivity with rich system performance.

In addition to WEP 64/128, WPA and TKIP, AES, CCX is supported to provide the latest security requirement on your network.

The SiP module is designed to operate with a single antenna for WiFi and Bluetooth to be connected to the u.FL connector available on the PICO-IMX6UL-EMMC.

For the software and driver development, TechNexion provides extensive technical document and reference software code for the system integration under the agreement of Broadcom International Ltd.

Figure 7 - PICO-IMX6UL-EMMC Antenna u.FL Connector Location

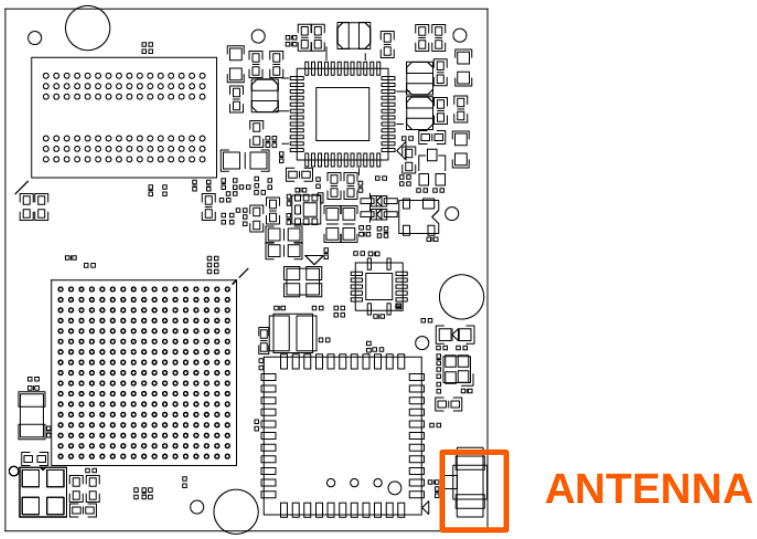


Table 6 - BCM4339 WiFi Signal Description

CPU BALL	PAD NAME	Pinmux (mode)	Signal	I/O	Description
D7	NAND_DATA00	usdhc2.DATA0 (mode1)	SDIO_D0	I/O	MMC/SDIO Data bit 0
B7	NAND_DATA01	usdhc2.DATA1 (mode1)	SDIO_D1	I/O	MMC/SDIO Data bit 1
A7	NAND_DATA02	usdhc2.DATA2 (mode1)	SDIO_D2	I/O	MMC/SDIO Data bit 2
D6	NAND_DATA03	usdhc2.DATA3 (mode1)	SDIO_D3	I/O	MMC/SDIO Data bit 3
C8	NAND_WE_B	usdhc2.CMD (mode1)	SDIO_CMD	I/O	MMC/SDIO Command
D8	NAND_RE_B	usdhc2.CLK (mode1)	SDIO_CLK	I/O	MMC/SDIO Clock
C6	NAND_DATA04	gpio4.IO[6] (mode5)	WL_HOST_WAKE	O	General purpose interface pin. This pin is high-impedance on power up and reset. Subsequently, it becomes an input or output through software control. This pin has a programmable weak pull-up/down.
A6	NAND_DATA06	gpio4.IO[8] (mode5)	WL_REG_ON	I	Used by PMU (OR-gated with BT_REG_ON) to power up or power down internal BCM4339 regulators used by the WLAN section. This pin is also a low-asserting reset for WLAN only (Bluetooth is not affected by this pin).

Table 7 - BCM4339 Bluetooth Signal Description

CPU BALL	PAD NAME	Pinmux (mode)	Signal	I/O	Description
M16	GPIO1_IO04	uart5.TX (mode8)	BT_UART_RXD	I	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface
M17	GPIO1_IO05	uart5.RX (mode8)	BT_UART_TXD	O	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
M15	GPIO1_IO09	uart5.CTS_B (mode8)	BT_UART_CTS	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
N17	GPIO1_IO08	uart5.RTS_B (mode8)	BT_UART_RTS	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
N14	JTAG_TRST_B	sai2.TX_DATA (mode2)	BT_PCM_IN	I	PCM data input
M14	JTAG_TCK	sai2.RX_DATA (mode2)	BT_PCM_OUT	O	PCM data output
N16	JTAG_TDI	sai2.TX_BCLK (mode2)	BT_PCM_CLK	I/O	PCM clock
N15	JTAG_TDO	sai2.TX_SYNC (mode2)	BT_PCB_SYNC	I/O	PCM sync signal
N9	SNVS_TAMPER8	gpio5.IO[8] (mode5)	BT_WAKE	I	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
R6	SNVS_TAMPER9	gpio5.IO[9] (mode5)	BT_RST_N	I	Low asserting reset for BT core
B6	NAND_DATA05	gpio4.IO[7] (mode5)	BT_HOST_WAKE	O	Host UART wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

3. PICO Compute Module Connector Interfaces

3.1 Ethernet

The PICO-IMX6UL-EMMC implements a 10/100 Mbit/s Fast Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs.

The Ethernet MAC supports the following features:

- Integrated PHY for 10/100 Mbps
- IEEE 802.3 Auto-Negotiation support.
- IEEE 802.3ab PHY compliance and compatibility
- Supports automatic MDI/MDIX functions
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Seamless interface to commercial Ethernet PHY devices via one of the following:
    - 4-bit Media Independent Interface (MII) operating at 2.5/25MHz.
    - 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25MHz.
    - 2-bit Reduced MII (RMII) operating at 50MHz.

For additional details, please refer to the “10/100 Mbps Ethernet MAC (ENET)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 8 - Ethernet Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_33	F15	ENET1_TXEN	ENET2_MDIC	3V3		Management data clock reference
X1_35	E14	ENET1_TXD1	ENET2_MDIO	3V3		Management data
X1_37	D16	ENET2_RXER	GPIO2_IO15	3V3		Ethernet reset
X1_39	N11	SNVS_TAMPER6	GPIO5_IO06	3V3		Ethernet interrupt output
X1_41	L16	GPIO1_IO07	ANATOP_ENET_ REF_CLK2	3V3		Synchronous Ethernet recovered clock
X1_43	B15	ENET2_TXEN	ENET2_TX_EN	3V3		RMII transmit enable
X1_45	B17	ENET2_CRS_DV	ENET2_RX_EN	3V3		RMII receive data valid
X1_49	D17	ENET2_TXCLK	ENET2_TX_CLK	3V3	O	RMII transmit clock
X1_51	A15	ENET2_TXD0	ENET2_TX_DATA0	3V3	O	RMII transmit data 0
X1_53	A16	ENET2_TXD1	ENET2_TX_DATA1	3V3	O	RMII transmit data 1
X1_63	C17	ENET2_RXD0	ENET2_RX_DATA0	3V3	I	RMII receive data 0
X1_65	C16	ENET2_RXD1	ENET2_RX_DATA1	3V3	I	RMII receive data 1

3.2. Digital Display Sub-System (DSS) or TTL Interface

The Parallel Display interface of PICO-IMX6UL-EMMC is derived from the eLCDIF subsystem. The eLCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The eLCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.

The block has several major features:

- Bus master interface to source frame buffer data for display refresh. This interface can also be used to drive data for "Smart" displays.
- PIO interface to manage data transfers between "Smart" displays and SoC.
- 8/16/18/24/32 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

For additional details, please refer to the “Enhanced LCD Interface” chapter and the “Pixel Pipeline (PXP)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 9 - TTL Display Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_8	B16	LCD_DATA23	LCDIF_DATA23	3V3	O	LCD Pixel Data bit 23
X1_10	A14	LCD_DATA22	LCDIF_DATA22	3V3	O	LCD Pixel Data bit 22
X1_12	B14	LCD_DATA21	LCDIF_DATA21	3V3	O	LCD Pixel Data bit 21
X1_14	C14	LCD_DATA20	LCDIF_DATA20	3V3	O	LCD Pixel Data bit 20
X1_16	D14	LCD_DATA19	LCDIF_DATA19	3V3	O	LCD Pixel Data bit 19
X1_18	A13	LCD_DATA18	LCDIF_DATA18	3V3	O	LCD Pixel Data bit 18
X1_20	B13	LCD_DATA17	LCDIF_DATA17	3V3	O	LCD Pixel Data bit 17
X1_22	C13	LCD_DATA16	LCDIF_DATA16	3V3	O	LCD Pixel Data bit 16
X1_24	D13	LCD_DATA15	LCDIF_DATA15	3V3	O	LCD Pixel Data bit 15
X1_26	A12	LCD_DATA14	LCDIF_DATA14	3V3	O	LCD Pixel Data bit 14
X1_28	B12	LCD_DATA13	LCDIF_DATA13	3V3	O	LCD Pixel Data bit 13
X1_30	C12	LCD_DATA12	LCDIF_DATA12	3V3	O	LCD Pixel Data bit 12
X1_32	D12	LCD_DATA11	LCDIF_DATA11	3V3	O	LCD Pixel Data bit 11
X1_34	E12	LCD_DATA10	LCDIF_DATA10	3V3	O	LCD Pixel Data bit 10
X1_36	A11	LCD_DATA9	LCDIF_DATA9	3V3	O	LCD Pixel Data bit 9
X1_38	B11	LCD_DATA8	LCDIF_DATA8	3V3	O	LCD Pixel Data bit 8
X1_40	D11	LCD_DATA7	LCDIF_DATA7	3V3	O	LCD Pixel Data bit 7
X1_42	A10	LCD_DATA6	LCDIF_DATA6	3V3	O	LCD Pixel Data bit 6
X1_44	B10	LCD_DATA5	LCDIF_DATA5	3V3	O	LCD Pixel Data bit 5
X1_46	C10	LCD_DATA4	LCDIF_DATA4	3V3	O	LCD Pixel Data bit 4
X1_48	D10	LCD_DATA3	LCDIF_DATA3	3V3	O	LCD Pixel Data bit 3
X1_50	E10	LCD_DATA2	LCDIF_DATA2	3V3	O	LCD Pixel Data bit 2
X1_52	A9	LCD_DATA1	LCDIF_DATA1	3V3	O	LCD Pixel Data bit 1
X1_54	B9	LCD_DATA0	LCDIF_DATA0	3V3	O	LCD Pixel Data bit 0
X1_56	N8	SNVS_TAMPER5	GPIO5_IO05	3V3	O	LCD backlight enable/disable
X1_58	D9	LCD_HSYNC	LCDIF_HSYNC	3V3	O	LCD Horizontal Synchronization
X1_60	B8	LCD_ENABLE	LCDIF_ENABLE	3V3	O	LCD dot enable pin signal
X1_62	C9	LCD_VSYNC	LCDIF_VSYNC	3V3	O	LCD Vertical Synchronization
X1_64	A8	LCD_CLK	LCDIF_CLK	3V3	O	LCD Pixel Clock
X1_66	B4	NAND_ALE	PWM3_OUT	3V3	O	LCD Backlight brightness Control
X1_68	P14	JTAG_TMS	GPIO1_IO11	3V3	O	LCD Voltage On

3.3. Audio Interface

The PICO-IMX6UL-EMMC incorporates one I²S / AUDMUX instance. The synchronous audio interface (SAI) supports full-duplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

Key features of the audio signal block include:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Maximum Frame Size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel
- Supports graceful restart after FIFO error

For additional details, please refer to the “Synchronous Audio Interface (SAI)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 10 - I²S Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_50	D2	CSI_DATA06	SAI1_RX_DATA	1V8	I	Integrated Interchip Sound (I²S) channel receive data line
E1_52	D3	CSI_DATA05	SAI1_TX_BCLK	1V8	O	Integrated Interchip Sound (I²S) channel word clock signal
E1_54	D4	CSI_DATA04	SAI1_TX_SYNC	1V8	O	Integrated Interchip Sound (I²S) channel frame synchronization signal
E1_56	D1	CSI_DATA07	SAI1_TX_DATA	1V8	O	Integrated Interchip Sound (I²S) channel transmit data line

NOTE: SAI2 signals are connected to the onboard Bluetooth/WiFi interface on the PICO-IMX6UL-EMMC

3.4. Universal Serial Bus (USB) Interface

The PICO-IMX6UL-EMMC incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:
USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 11 - USB Host Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_46	T13	USB_OTG2_DN	USB_OTG2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_48	U13	USB_OTG2_DP	USB_OTG2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_50	U12	USB_OTG2_VBUS	USB_OTG2_VBUS	5V	I/O	Universal Serial Bus power
X2_52	R10	SNVS_TAMPER0	GPIO5_IO00	3V3	I	Active low input, to inform USB overcurrent condition (low = overcurrent detected)

Table 12 - USB OTG Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_3	K13	GPIO1_IO00	USB_OTG1_PWR	3V3	I	USB OTG ID Pin
E1_16	U15	USB_OTG1_DP	USB_OTG_DP	USB	I/O	Universal Serial Bus differential pair positive signal
E1_18	T15	USB_OTG1_DN	USB_OTG1_DN	USB	I/O	Universal Serial Bus differential pair negative signal
E1_19	L15	GPIO1_IO01	GPIO1_IO01	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	T12	USB_OTG1_VBUS	USB_OTG1_VBUS	5V	I/O	Universal Serial Bus power
E1_21	K17	GPIO1_IO06	USB_OTG_ PWR_WAKE	USB	I	Universal Serial Bus power enable

NOTE: While using USB OTG in USB HOST mode. The USB_ID pin should have a pull-down resistor to GND.

3.5. CAN BUS Interface signals

The PICO-IMX6UL-EMMC features two CAN bus interfaces. The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported.

FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

Integration of a CAN Bus transceiver and optional galvanic isolation should be incorporated on your carrier board.

For additional details, please refer to the “Flexible Controller Area Network (FLEXCAN)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 13 - CAN Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_19	F16	ENET1_RXD0	CAN1_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_21	E17	ENET1_RXD1	CAN1_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_25	E16	ENET1_RX_EN	CAN2_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_27	E15	ENET1_TXD0	CAN2_RX	3V3	I/O	CAN (controller Area Network) receive signal

3.6. Universal Asynchronous Receiver/Transmitter (UART) Interface

The PICO-IMX6UL-EMMC Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter.

The i.MX6Ultralite processor integrated UARTs support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 14 - UART Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_22	E5	CSI_PIXCLK	UART6_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_27	F5	CSI_MCLK	UART6_TX	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_46	H17	UART3_TXD	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_61	H16	UART3_RXD	UART3_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_63	G14	UART3_RTS	UART3_RTS	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_65	H15	UART3_CTS	UART3_CTS	1V8	O	Universal Asynchronous Receive Transmit clear to send signal

NOTE: it is recommended to use the UART6 interface as system debug where possible and use the UART3 signals in applications where one serial port is required.

NOTE: UART5 is not listed in this section. This interface is connected from the i.MX6Ultralite processor towards the WiFi/Bluetooth interface present on PICO-IMX6UL-EMMC and can be found in the WiFi/Bluetooth section of this manual.

3.7. Serial Peripheral Interface (SPI)

The PICO-IMX6UL-EMMC features an Enhanced Configurable Serial Peripheral Interface (ECSPI) full-duplex, synchronous, four-wire serial communication block.

The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency.

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 15 - SPI Channel Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_53	J17	UART2_TXD	ECSPI3_SS0	1V8		Serial Peripheral Interface Chip Select 1 signal
E1_55	J16	UART2_RXD	ECSPI3_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_57	H14	UART2_CTS	ECSPI3_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal
E1_59	J15	UART2_RTS	ECSPI3_MISO	1V8	I	Serial Peripheral Interface master input slave output signal

3.8. I²C Bus

The PICO-IMX6UL-EMMC incorporates several I²C interfaces. I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the “I2C Controller (I2C)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 16 - I²C Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_41	F17	UART5_TXD	I2C2_SCL	1V8	I/O	I²C bus clock line
E1_43	G13	UART5_RXD	I2C2_SDA	1V8	I/O	I²C bus data line
E1_45	K14	UART1_TXD	I2C3_SCL	1V8	I/O	I²C bus clock line
E1_47	K16	UART1_RXD	I2C3_SDA	1V8	I/O	I²C bus data line
X2_13	L14*	GPIO1_IO02	I2C1_SCL	3V3	I/O	I²C bus clock line
X2_15	L17*	GPIO1_IO03	I2C1_SDA	3V3	I/O	I²C bus data line

NOTE: All 1V8 I²C bus data and clock lines for all I²C interfaces have 2.2K Ω pull-up resistors present on the PICO-IMX6UL-EMMC module.

NOTE: All 3V3 I²C bus data and clock lines for all I²C interfaces have 1.5K Ω pull-up resistors present on the PICO-IMX6UL-EMMC module.

NOTE: I²C1 is connected to the PICO-IMX6UL-EMMC onboard NXP PF3000 Power Management IC and cannot be set in another pinmux mode.

3.9. General Purpose Input/Output (GPIO)

The PICO-IMX6UL-EMMC has 10 dedicated GPIO pins at 1.8V. Many of the other pins used on the PICO Compute Module can be put in GPIO module however doing so might break scalability with other PICO Compute Modules. An overview can be found in **chapter 5. PICO Compute Module Pinmux** Overview of this manual.

The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input/Output (GPIO)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 17 - GPIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_24	F2	CSI_VSYNC	GPIO4_IO19	1V8	I/O	General Purpose Input Output
E1_25	F3	CSI_HSYNC	GPIO4_IO20	1V8	I/O	General Purpose Input Output
E1_26	E4	CSI_DATA00	GPIO4_IO21	1V8	I/O	General Purpose Input Output
E1_28	E3	CSI_DATA01	GPIO4_IO22	1V8	I/O	General Purpose Input Output
E1_30	E2	CSI_DATA02	GPIO4_IO23	1V8	I/O	General Purpose Input Output
E1_32	E1	CSI_DATA03	GPIO4_IO24	1V8	I/O	General Purpose Input Output
E1_34	K15	UART1_CTS	GPIO4_IO18	1V8	I/O	General Purpose Input Output
E1_42	G17	UART4_TXD	GPIO4_IO28	1V8	I/O	General Purpose Input Output
E1_44	G16	UART4_RXD	GPIO4_IO29	1V8	I/O	General Purpose Input Output
E1_48	P11	SNVS_TAMPER2	GPIO5_IO02	1V8	I/O	General Purpose Input Output

3.10. Pulse Width Modulation (PWM)

The PICO-IMX6UL-EMMC has 3 dedicated PWM pins at 1.8V and 1 PWM for LCD brightness control at 3.3V.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

For additional details, please refer to the “Pulse Width Modulation (PWM)” chapter of the “i.MX6Ultralite Application Processor Reference Manual”.

Table 18 - PWM Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_33	D15	ENET1_RX_ER	PWM8_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_35	F14	ENET1_TX_CLK	PWM7_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_37	J14	UART1_RTS	USDHC1_CD_B	1V8	I/O	General Purpose Input Output with PWM control
X1_66	B4	NAND_ALE	PWM3_OUT	3V3	O	LCD Backlight brightness Control

3.11. Manufacturing and Boot Control

The PICO-IMX6UL-EMMC has a number of pins to override the default boot media present on the PICO-IMX6UL-EMMC Compute Module or enable debug serial loader functionality.

Table 19 - Boot Selection Pins

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_3	T10	BOOT_MODE0	BOOT_MODE0	1V8	I	Boot Select pin
X2_5	U10	BOOT_MODE1	BOOT_MODE1	1V8	I	Boot Select pin
X2_7	B12	LCD_DATA13	BT_CFG13	1V8	I	Boot Select pin
X2_9	A12	LCD_DATA14	BT_CFG14	1V8	I	Boot Select pin

3.11.1. Boot Modes

The PICO-IMX6UL-EMMC Compute Module automatically boot from the internal eMMC if the above signals keep floating. Only when Serial Downloader Mode is required the signals need to be connected as **Table 20 - Serial Downloader Boot Mode Configuration** below.

Table 20 - Serial Downloader Boot Mode Configuration

PIN	CPU BALL	Serial Downloader Mode
X2_3	T10	HIGH
X2_5	U10	LOW
X2_7	B12	Not Connected
X2_9	A12	Not Connected

Table 21 - Internal Downloader Boot Mode Configuration

PIN	CPU BALL	Internal (eMMC) Boot Mode
X2_3	T10	LOW
X2_5	U10	HIGH
X2_7	B12	Not Connected
X2_9	A12	Not Connected

3.12. Input Power Requirements

The PICO-IMX6UL-EMMC is designed to be driven with a single input power rail.

The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VSYS pins should be connected to the main power source.

Table 22 - Input Power Signals

Power Rail	Nominal Input	Input Range	Maximum Input Ripple
VSYS (4 pin)	5V	+4.2V - +5.25V	±50 mV

3.12.1. Power Management Signals

The PICO-IMX6UL-EMMC has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states.

Table 23 - Power Management Signals

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_17	R8	ONOFF	SRC_RESET_B	3V3	I	Power ON button input signal
E1_36	PMIC	RESET	RESET	1V8	I	Reset power signal

NOTE: Pin E1_36 is described in detail in **chapter 2.2. Power Management IC** of this manual

3.12.2. Power Sequence

PICO-IMX6UL-EMMC input power sequencing requirements are as follow:

If a backup Real Time Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the PICO carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I²C can be used.

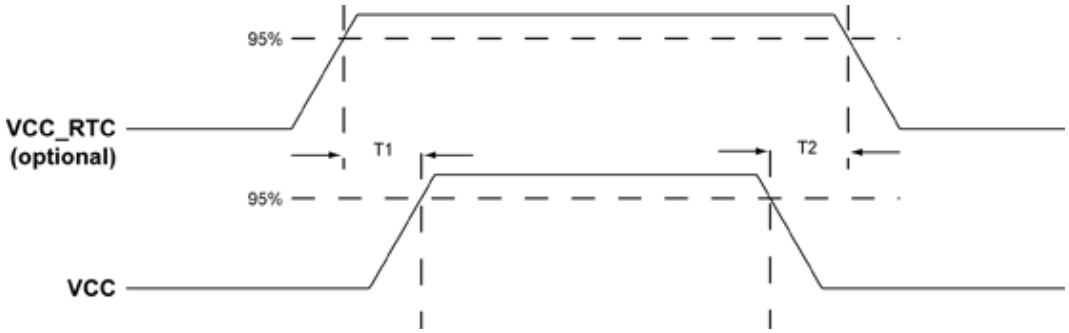
Start Sequence:
VCC_RTC must come up at the same time or before VCC comes up.

Stop Sequence:
VCC must go down at the same time or before VCC_RTC goes down

Table 24 - Input Power Sequencing for AT based configurations

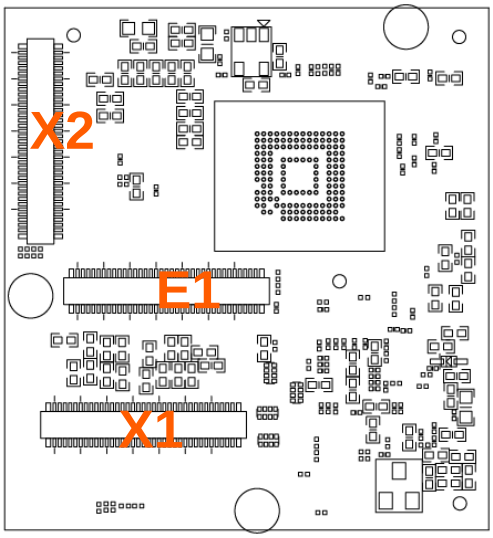
Item	Description	Value
T1	VCC_RTC rise to VCC rise	≥ 0 ms
T2	VCC fall to VCC_RTC fall	≥ 0 ms

Figure 8 - Input Power sequence for AT based configurations



4. PICO Compute Module Pin Assignment

The PICO-IMX6UL-EMMC has three 70-pin Hirose board to board connectors.



PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_1			GND		P	Ground
E1_2			VSYS		P	System input power (4.0 to 5.25V)
E1_3	K13	GPIO1_IO00	USB_OTG1_PWR	3V3	I	USB OTG ID Pin
E1_4			VSYS		P	System input power (4.0 to 5.25V)
E1_5			GND		P	Ground
E1_6			VSYS		P	System input power (4.0 to 5.25V)
E1_7			NC			Not Connected
E1_8			3V3		P	System 3.3V Output
E1_9			GND		P	Ground
E1_10			3V3		P	System 3.3V Output
E1_11			GND		P	Ground
E1_12			1V8		P	System 1.8V Output (same as E1 connector I/O voltage levels)
E1_13			GND		P	Ground
E1_14			VSYS		P	System input power (4.0 to 5.25V)
E1_15			GND		P	Ground
E1_16	U15	USB_OTG1_DP	USB_OTG_DP	USB	I/O	Universal Serial Bus differential pair positive signal

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_17	R8	ONOFF	SRC_RESET_B	3V3	I	Power ON button input signal
E1_18	T15	USB_OTG1_DN	USB_OTG1_DN	USB	I/O	Universal Serial Bus differential pair negative signal
E1_19	L15	GPIO1_IO01	GPIO1_IO01	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	T12	USB_OTG1_VBUS	USB_OTG1_VBUS	5V	I/O	Universal Serial Bus power
E1_21	K17	GPIO1_IO06	USB_OTG_ PWR_WAKE	USB	I	Universal Serial Bus power enable
E1_22	E5	CSI_PIXCLK	UART6_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_23			NC			Not Connected
E1_24	F2	CSI_VSYNC	GPIO4_IO19	1V8	I/O	General Purpose Input Output
E1_25	F3	CSI_HSYNC	GPIO4_IO20	1V8	I/O	General Purpose Input Output
E1_26	E4	CSI_DATA00	GPIO4_IO21	1V8	I/O	General Purpose Input Output
E1_27	F5	CSI_MCLK	UART6_TX	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_28	E3	CSI_DATA01	GPIO4_IO22	1V8	I/O	General Purpose Input Output
E1_29			NC			Not Connected
E1_30	E2	CSI_DATA02	GPIO4_IO23	1V8	I/O	General Purpose Input Output
E1_31			NC			Not Connected
E1_32	E1	CSI_DATA03	GPIO4_IO24	1V8	I/O	General Purpose Input Output
E1_33	D15	ENET1_RX_ER	PWM8_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_34	K15	UART1_CTS	GPIO4_IO18	1V8	I/O	General Purpose Input Output
E1_35	F14	ENET1_TX_CLK	PWM7_OUT	1V8	I/O	General Purpose Input Output with PWM control
E1_36	PMIC	RESET	RESET	1V8	I	Reset power signal
E1_37	J14	UART1_RTS	USDHC1_CD_B	1V8	I/O	General Purpose Input Output with PWM control
E1_38			NC			Not Connected
E1_39			NC			Not Connected
E1_40			NC			Not Connected
E1_41	F17	UART5_TXD	I2C2_SCL	1V8	I/O	I^2C bus clock line
E1_42	G17	UART4_TXD	GPIO4_IO28	1V8	I/O	General Purpose Input Output
E1_43	G13	UART5_RXD	I2C2_SDA	1V8	I/O	I^2C bus data line
E1_44	G16	UART4_RXD	GPIO4_IO29	1V8	I/O	General Purpose Input Output
E1_45	K14	UART1_TXD	I2C3_SCL	1V8	I/O	I^2C bus clock line

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_46	H17	UART3_TXD	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_47	K16	UART1_RXD	I2C3_SDA	1V8	I/O	I²C bus data line
E1_48	P11	SNVS_TAMPER2	GPIO5_IO02	1V8	I/O	General Purpose Input Output
E1_49			NC			Not Connected
E1_50	D2	CSI_DATA06	SAI1_RX_DATA	1V8	I	Integrated Interchip Sound (I²S) channel receive data line
E1_51			NC			Not Connected
E1_52	D3	CSI_DATA05	SAI1_TX_BCLK	1V8	O	Integrated Interchip Sound (I²S) channel word clock signal
E1_53	J17	UART2_TXD	ECSPI3_SS0	1V8		Serial Peripheral Interface Chip Select 1 signal
E1_54	D4	CSI_DATA04	SAI1_TX_SYNC	1V8	O	Integrated Interchip Sound (I²S) channel frame synchronization signal
E1_55	J16	UART2_RXD	ECSPI3_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_56	D1	CSI_DATA07	SAI1_TX_DATA	1V8	O	Integrated Interchip Sound (I²S) channel transmit data line
E1_57	H14	UART2_CTS	ECSPI3_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal
E1_58			NC			Not Connected
E1_59	J15	UART2_RTS	ECSPI3_MISO	1V8	I	Serial Peripheral Interface master input slave output signal
E1_60			NC			Not Connected
E1_61	H16	UART3_RXD	UART3_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_62			NC			Not Connected
E1_63	G14	UART3_RTS	UART3_RTS	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_64			NC			Not Connected
E1_65	H15	UART3_CTS	UART3_CTS	1V8	O	Universal Asynchronous Receive Transmit clear to send signal
E1_66			NC			Not Connected
E1_67			NC			Not Connected
E1_68			NC			Not Connected
E1_69			NC			Not Connected
E1_70			NC			Not Connected

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_1			GND		P	Ground
X1_2			GND		P	Ground
X1_3			NC			Not Connected
X1_4			NC			Not Connected
X1_5			NC			Not Connected
X1_6			NC			Not Connected
X1_7			GND		P	Ground
X1_8	B16	LCD_DATA23	LCDIF_DATA23	3V3	O	LCD Pixel Data bit 23
X1_9			NC			Not Connected
X1_10	A14	LCD_DATA22	LCDIF_DATA22	3V3	O	LCD Pixel Data bit 22
X1_11			NC			Not Connected
X1_12	B14	LCD_DATA21	LCDIF_DATA21	3V3	O	LCD Pixel Data bit 21
X1_13			GND		P	Ground
X1_14	C14	LCD_DATA20	LCDIF_DATA20	3V3	O	LCD Pixel Data bit 20
X1_15			NC			Not Connected
X1_16	D14	LCD_DATA19	LCDIF_DATA19	3V3	O	LCD Pixel Data bit 19
X1_17			NC			Not Connected
X1_18	A13	LCD_DATA18	LCDIF_DATA18	3V3	O	LCD Pixel Data bit 18
X1_19			GND		P	Ground
X1_20	B13	LCD_DATA17	LCDIF_DATA17	3V3	O	LCD Pixel Data bit 17
X1_21			NC			Not Connected
X1_22	C13	LCD_DATA16	LCDIF_DATA16	3V3	O	LCD Pixel Data bit 16
X1_23			NC			Not Connected
X1_24	D13	LCD_DATA15	LCDIF_DATA15	3V3	O	LCD Pixel Data bit 15
X1_25			GND		P	Ground
X1_26	A12	LCD_DATA14	LCDIF_DATA14	3V3	O	LCD Pixel Data bit 14
X1_27			NC			Not Connected
X1_28	B12	LCD_DATA13	LCDIF_DATA13	3V3	O	LCD Pixel Data bit 13
X1_29			NC			Not Connected
X1_30	C12	LCD_DATA12	LCDIF_DATA12	3V3	O	LCD Pixel Data bit 12
X1_31			GND		P	Ground
X1_32	D12	LCD_DATA11	LCDIF_DATA11	3V3	O	LCD Pixel Data bit 11
X1_33	F15	ENET1_TXEN	ENET2_MDIC	3V3		Management data clock reference
X1_34	E12	LCD_DATA10	LCDIF_DATA10	3V3	O	LCD Pixel Data bit 10
X1_35	E14	ENET1_TXD1	ENET2_MDIO	3V3		Management data
X1_36	A11	LCD_DATA9	LCDIF_DATA9	3V3	O	LCD Pixel Data bit 9
X1_37	D16	ENET2_RXER	GPIO2_IO15	3V3		Ethernet reset
X1_38	B11	LCD_DATA8	LCDIF_DATA8	3V3	O	LCD Pixel Data bit 8
X1_39	N11	SNVS_TAMPER6	GPIO5_IO06	3V3		Ethernet interrupt output
X1_40	D11	LCD_DATA7	LCDIF_DATA7	3V3	O	LCD Pixel Data bit 7
X1_41	L16	GPIO1_IO07	ANATOP_ENET_ REF_CLK2	3V3		Synchronous Ethernet recovered clock
X1_42	A10	LCD_DATA6	LCDIF_DATA6	3V3	O	LCD Pixel Data bit 6
X1_43	B15	ENET2_TXEN	ENET2_TX_EN	3V3		RMII transmit enable
X1_44	B10	LCD_DATA5	LCDIF_DATA5	3V3	O	LCD Pixel Data bit 5
X1_45	B17	ENET2_CRS_DV	ENET2_RX_EN	3V3		RMII receive data valid
X1_46	C10	LCD_DATA4	LCDIF_DATA4	3V3	O	LCD Pixel Data bit 4

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_47			GND		P	Ground
X1_48	D10	LCD_DATA3	LCDIF_DATA3	3V3	O	LCD Pixel Data bit 3
X1_49	D17	ENET2_TXCLK	ENET2_TX_CLK	3V3	O	RMII transmit clock
X1_50	E10	LCD_DATA2	LCDIF_DATA2	3V3	O	LCD Pixel Data bit 2
X1_51	A15	ENET2_TXD0	ENET2_TX_DATA0	3V3	O	RMII transmit data 0
X1_52	A9	LCD_DATA1	LCDIF_DATA1	3V3	O	LCD Pixel Data bit 1
X1_53	A16	ENET2_TXD1	ENET2_TX_DATA1	3V3	O	RMII transmit data 1
X1_54	B9	LCD_DATA0	LCDIF_DATA0	3V3	O	LCD Pixel Data bit 0
X1_55			NC			Not Connected
X1_56	N8	SNVS_TAMPER5	GPIO5_IO05	3V3	O	LCD backlight enable/disable
X1_57			NC			Not Connected
X1_58	D9	LCD_HSYNC	LCDIF_HSYNC	3V3	O	LCD Horizontal Synchronization
X1_59			GND		P	Ground
X1_60	B8	LCD_ENABLE	LCDIF_ENABLE	3V3	O	LCD dot enable pin signal
X1_61			NC			Not Connected
X1_62	C9	LCD_VSYNC	LCDIF_VSYNC	3V3	O	LCD Vertical Synchronization
X1_63	C17	ENET2_RXD0	ENET2_RX_DATA0	3V3	I	RMII receive data 0
X1_64	A8	LCD_CLK	LCDIF_CLK	3V3	O	LCD Pixel Clock
X1_65	C16	ENET2_RXD1	ENET2_RX_DATA1	3V3	I	RMII receive data 1
X1_66	B4	NAND_ALE	PWM3_OUT	3V3	O	LCD Backlight brightness Control
X1_67			NC			Not Connected
X1_68	P14	JTAG_TMS	GPIO1_IO11	3V3	O	LCD Voltage On
X1_69			NC			Not Connected
X1_70			GND		P	Ground

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_1			GND		P	Ground
X2_2			GND		P	Ground
X2_3	T10	BOOT_MODE0	BOOT_MODE0	1V8	I	Boot Select pin
X2_4			NC			Not Connected
X2_5	U10	BOOT_MODE1	BOOT_MODE1	1V8	I	Boot Select pin
X2_6			NC			Not Connected
X2_7	B12	LCD_DATA13	BT_CFG13	1V8	I	Boot Select pin
X2_8			GND		P	Ground
X2_9	A12	LCD_DATA14	BT_CFG14	1V8	I	Boot Select pin
X2_10			NC			Not Connected
X2_11			GND		P	Ground
X2_12			NC			Not Connected
X2_13	L14	GPIO1_IO02	I2C1_SCL	3V3	I/O	I^2C bus clock line
X2_14			GND		P	Ground
X2_15	L17	GPIO1_IO03	I2C1_SDA	3V3	I/O	I^2C bus data line
X2_16			NC			Not Connected
X2_17			GND		P	Ground
X2_18			NC			Not Connected
X2_19	F16	ENET1_RXD0	CAN1_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_20			GND		P	Ground
X2_21	E17	ENET1_RXD1	CAN1_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_22			NC			Not Connected
X2_23			GND		P	Ground
X2_24			NC			Not Connected
X2_25	E16	ENET1_RX_EN	CAN2_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_26			GND		P	Ground
X2_27	E15	ENET1_TXD0	CAN2_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_28			NC			Not Connected
X2_29			GND		P	Ground
X2_30			NC			Not Connected
X2_31			NC			Not Connected
X2_32			GND		P	Ground
X2_33			NC			Not Connected
X2_34			NC			Not Connected
X2_35			NC			Not Connected
X2_36			NC			Not Connected
X2_37			NC			Not Connected
X2_38			GND		P	Ground
X2_39			NC			Not Connected
X2_40			NC			Not Connected
X2_41			NC			Not Connected
X2_42			NC			Not Connected
X2_43			NC			Not Connected
X2_44			GND		P	Ground
X2_45			NC			Not Connected

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_46	T13	USB_OTG2_DN	USB_OTG2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_47			NC			Not Connected
X2_48	U13	USB_OTG2_DP	USB_OTG2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_49			NC			Not Connected
X2_50	U12	USB_OTG2_VBUS	USB_OTG2_VBUS	5V	I/O	Universal Serial Bus power
X2_51			GND		P	Ground
X2_52	R10	SNVS_TAMPER0	GPIO5_IO00	3V3	I	Active low input, to inform USB overcurrent condition (low = overcurrent detected)
X2_53			NC			Not Connected
X2_54			GND		P	Ground
X2_55			NC			Not Connected
X2_56			NC			Not Connected
X2_57			NC			Not Connected
X2_58			NC			Not Connected
X2_59			NC			Not Connected
X2_60			GND		P	Ground
X2_61			NC			Not Connected
X2_62			NC			Not Connected
X2_63			NC			Not Connected
X2_64			NC			Not Connected
X2_65			NC			Not Connected
X2_66			GND		P	Ground
X2_67			NC			Not Connected
X2_68			NC			Not Connected
X2_69			NC			Not Connected
X2_70			NC			Not Connected

5. PICO Compute Module Pinmux Overview

Many signals on the PICO-IMX6UL-EMMC can be configured to support other interfaces. The table below gives an overview of all pins that can be modified.

The default operation mode which is compatible with other PICO Compute Modules has been highlighted.

PIN	CPU BALL	PADNAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE8
E1_3	K13	GPIO1_IO00	i2c2.SCL	gpt1.CAPTURE1	usb.OTG1_PWR	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio1.IO[0]	enet1.1588_EVENT0_IN	wdog3.WDOG_B
E1_17	R8	ONOFF	src.RESET_B							
E1_19	L15	GPIO1_IO01	i2c2.SDA	gpt1.COMPARE1	usb.OTG1_OC	anatop.ENET_REF_CLK2	mqs.LEFT	gpio1.IO[1]	enet1.1588_EVENT0_OUT	wdog2.WDOG_B
E1_21	K17	GPIO1_IO06	enet1.MDIO	anatop.ENET_REF_CLK1	usb.OTG_PWR_WAKE	csi.MCLK	usdhc2.WP	gpio1.IO[6]	enet2.1588_EVENT1_IN	uart1.CTS_B
E1_22	E5	CSI_PIXCLK	csi.PIXCLK	usdhc2.WP	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[18]	enet1.MDC	uart6.RX
E1_24	F2	CSI_VSYNC	csi.VSYNC	usdhc2.CLK	sim1.PORT1_CLK	i2c2.SDA	weim.RW	gpio4.IO[19]	enet2.MDIO	uart6.RTS_B
E1_25	F3	CSI_HSYNC	csi.HSYNC	usdhc2.CMD	sim1.PORT1_PD	i2c2.SCL	weim.LBA_B	gpio4.IO[20]	enet2.MDC	uart6.CTS_B
E1_26	E4	CSI_DATA00	csi.DATA[2]	usdhc2.DATA0	sim1.PORT1_RST_B	ecspi2.SCLK	weim.AD[0]	gpio4.IO[21]	wdog3.WDOG_B	uart5.TX
E1_27	F5	CSI_MCLK	csi.MCLK	usdhc2.CD_B	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio4.IO[17]	enet1.MDIO	uart6.TX
E1_28	E3	CSI_DATA01	csi.DATA[3]	usdhc2.DATA1	sim1.PORT1_SVEN	ecspi2.SS0	weim.AD[1]	gpio4.IO[22]	sai1.MCLK	uart5.RX
E1_30	E2	CSI_DATA02	csi.DATA[4]	usdhc2.DATA2	sim1.PORT1_TRXD	ecspi2.MOSI	weim.AD[2]	gpio4.IO[23]	sai1.RX_SYNC	uart5.RTS_B
E1_32	E1	CSI_DATA03	csi.DATA[5]	usdhc2.DATA3	sim2.PORT1_PD	ecspi2.MISO	weim.AD[3]	gpio4.IO[24]	sai1.RX_BCLK	uart5.CTS_B
E1_33	D15	ENET1_RXER	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	csi.DATA[23]	weim.CRE	gpio2.IO[7]		global wdog
E1_34	K15	UART1_CTS	uart1.CTS_B	enet1.RX_CLK	usdhc1.WP	csi.DATA[4]	kpp.ROW[1]	gpio1.IO[18]	src.INT_BOOT	usdhc2.WP
E1_35	F14	ENET1_TXCLK	enet1.TX_CLK	uart7.CTS_B	pwm7.OUT	csi.DATA[22]	anatop.ENET_REF_CLK2	gpio2.IO[6]		gpt1.CLK
E1_37	J14	UART1_RTS	uart1.RTS_B	enet1.TX_ER	usdhc1.CD_B	csi.DATA[5]	kpp.COL[1]	gpio1.IO[19]	gpt1.CAPTURE1	usdhc2.CD_B
E1_41	F17	UART5_TXD	uart5.TX	enet2.CRS	i2c2.SCL	csi.DATA[14]	kpp.ROW[7]	gpio1.IO[30]	csu.CSU_ALARM_AUT[0]	ecspi2.MOSI
E1_42	G17	UART4_TXD	uart4.TX	enet2.TDATA[2]	i2c1.SCL	csi.DATA[12]	kpp.ROW[6]	gpio1.IO[28]	csu.CSU_ALARM_AUT[2]	ecspi2.SCLK
E1_43	G13	UART5_RXD	uart5.RX	enet2.COL	i2c2.SDA	csi.DATA[15]	kpp.COL[7]	gpio1.IO[31]	csu.CSU_INT_DEB	ecspi2.MISO
E1_44	G16	UART4_RXD	uart4.RX	enet2.TDATA[3]	i2c1.SDA	csi.DATA[13]	kpp.COL[6]	gpio1.IO[29]	csu.CSU_ALARM_AUT[1]	ecspi2.SS0
E1_45	K14	UART1_TXD	uart1.TX	enet1.RDATA[2]	i2c3.SCL	csi.DATA[2]	kpp.ROW[0]	gpio1.IO[16]	snvs_hp_wrapper.VIO_5_CTL	spdif.OUT
E1_46	H17	UART3_TXD	uart3.TX	enet2.RDATA[2]	can2.TX	csi.DATA[1]	kpp.ROW[4]	gpio1.IO[24]	gpt1.COMPARE3	anatop.OTG1_ID
E1_47	K16	UART1_RXD	uart1.RX	enet1.RDATA[3]	i2c3.SDA	csi.DATA[3]	kpp.COL[0]	gpio1.IO[17]	snvs_hp_wrapper.VIO_5	spdif.IN
E1_48	P11	SNVS_TAMPER2	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[2]		
E1_50	D2	CSI_DATA06	csi.DATA[8]	usdhc2.DATA6	sim2.PORT1_SVEN	ecspi1.MOSI	weim.AD[6]	gpio4.IO[27]	sai1.RX_DATA	usdhc1.RESET_B
E1_52	D3	CSI_DATA05	csi.DATA[7]	usdhc2.DATA5	sim2.PORT1_RST_B	ecspi1.SS0	weim.AD[5]	gpio4.IO[26]	sai1.TX_BCLK	usdhc1.CD_B
E1_53	J17	UART2_TXD	uart2.TX	enet1.TDATA[2]	i2c4.SCL	csi.DATA[6]	kpp.ROW[2]	gpio1.IO[20]	gpt1.CAPTURE2	ecspi3.SS0
E1_54	D4	CSI_DATA04	csi.DATA[6]	usdhc2.DATA4	sim2.PORT1_CLK	ecspi1.SCLK	weim.AD[4]	gpio4.IO[25]	sai1.TX_SYNC	usdhc1.WP
E1_55	J16	UART2_RXD	uart2.RX	enet1.TDATA[3]	i2c4.SDA	csi.DATA[7]	kpp.COL[2]	gpio1.IO[21]	gpt1.COMPARE1	ecspi3.SCLK
E1_56	D1	CSI_DATA07	csi.DATA[9]	usdhc2.DATA7	sim2.PORT1_TRXD	ecspi1.MISO	weim.AD[7]	gpio4.IO[28]	sai1.TX_DATA	usdhc1.VSELECT
E1_57	H14	UART2_CTS	uart2.CTS_B	enet1.CRS	sim1.PORT0_PD	csi.DATA[8]	kpp.ROW[3]	gpio1.IO[22]	gpt1.CLK	ecspi3.MOSI
E1_59	J15	UART2_RTS	uart2.RTS_B	enet1.COL	sim2.PORT0_PD	csi.DATA[9]	kpp.COL[3]	gpio1.IO[23]	gpt1.COMPARE2	ecspi3.MISO
E1_61	H16	UART3_RXD	uart3.RX	enet2.RDATA[3]	can2.RX	csi.DATA[0]	kpp.COL[4]	gpio1.IO[25]	caam_wrapper.RNG_OSC_OBS	epit1.OUT
E1_63	G14	UART3_CTS	uart3.CTS_B	enet2.RX_CLK	can1.TX	csi.DATA[10]	kpp.ROW[5]	gpio1.IO[26]	ccm.WAIT	epit2.OUT
E1_65	H15	UART3_RTS	uart3.RTS_B	enet2.TX_ER	can1.RX	csi.DATA[11]	kpp.COL[5]	gpio1.IO[27]	ccm.STOP	wdog1.WDOG_B

PIN	CPU BALL	PADNAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE8
X1_8	B16	LCD_DATA23	lcdif.DATA[23]	uart8.RTS_B	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[28]	src.BT_CFG[31]	usdhc1.DATA3
X1_10	A14	LCD_DATA22	lcdif.DATA[22]	uart8.CTS_B	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[27]	src.BT_CFG[30]	usdhc1.DATA2
X1_12	B14	LCD_DATA21	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[26]	src.BT_CFG[29]	usdhc1.DATA1
X1_14	C14	LCD_DATA20	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[25]	src.BT_CFG[28]	usdhc1.DATA0
X1_16	D14	LCD_DATA19	lcdif.DATA[19]	uart7.RTS_B	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[24]	src.BT_CFG[27]	usdhc1.CLK
X1_18	A13	LCD_DATA18	lcdif.DATA[18]	uart7.CTS_B	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[23]	src.BT_CFG[26]	usdhc1.CMD
X1_20	B13	LCD_DATA17	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[22]	src.BT_CFG[25]	usdhc1.DATA7
X1_22	C13	LCD_DATA16	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[21]	src.BT_CFG[24]	usdhc1.DATA6
X1_24	D13	LCD_DATA15	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[20]	src.BT_CFG[15]	usdhc1.DATA5
X1_26*	A12	LCD_DATA14	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	usdhc1.DATA4
X1_28*	B12	LCD_DATA13	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	usdhc1.RESET_B
X1_30	C12	LCD_DATA12	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[17]	src.BT_CFG[12]	ecspi1.RDY
X1_32	D12	LCD_DATA11	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[16]	src.BT_CFG[11]	can2.RX
X1_33	F15	ENET1_TXEN	enet1.TX_EN	uart6.RTS_B	pwm6.OUT	csi.DATA[21]	enet2.MDC	gpio2.IO[5]		mqs.LEFT
X1_34	E12	LCD_DATA10	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[15]	src.BT_CFG[10]	can2.TX
X1_35	E14	ENET1_TXD1	enet1.TDATA[1]	uart6.CTS_B	pwm5.OUT	csi.DATA[20]	enet2.MDIO	gpio2.IO[4]		GPIO1_IO04
X1_36	A11	LCD_DATA09	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[14]	src.BT_CFG[9]	can1.RX
X1_37	D16	ENET2_RXER	enet2.RX_ER	uart8.RTS_B	sim2.PORT0_SVEN	ecspi4.SS0	weim.ADDR[25]	gpio2.IO[15]		global wdog
X1_38	B11	LCD_DATA08	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[13]	src.BT_CFG[8]	can1.TX
X1_39	N11	SNVS_TAMPER6	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[6]		
X1_40	D11	LCD_DATA07	lcdif.DATA[7]	pwm8.OUT	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[12]	src.BT_CFG[7]	ecspi1.SS3
X1_41	L16	GPIO1_IO07	enet1.MDC	anatop.ENET_REF_CLK2	usb.OTG_HOST_MODE	csi.PIXCLK	usdhc2.CD_B	gpio1.IO[7]	enet2.1588_EVENT1_OUT	uart1.RTS_B
X1_42	A10	LCD_DATA06	lcdif.DATA[6]	pwm7.OUT	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[11]	src.BT_CFG[6]	ecspi1.SS2
X1_43	B15	ENET2_TXEN	enet2.TX_EN	uart8.RX	sim2.PORT0_CLK	ecspi4.MOSI	weim.ACLK_FREERUN	gpio2.IO[13]		usb.OTG2_OC
X1_44	B10	LCD_DATA05	lcdif.DATA[5]	pwm6.OUT	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[10]	src.BT_CFG[5]	ecspi1.SS1
X1_45	B17	ENET2_CRS_DV	enet2.RX_EN	uart7.TX	sim1.PORT0_RST_B	i2c4.SCL	weim.ADDR[26]	gpio2.IO[10]		usb.OTG1_PWR
X1_46	C10	LCD_DATA04	lcdif.DATA[4]	pwm5.OUT	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	spdif.SR_CLK	gpio3.IO[9]	src.BT_CFG[4]	sai1.TX_DATA
X1_48	D10	LCD_DATA03	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[8]	src.BT_CFG[3]	sai1.RX_DATA
X1_49	D17	ENET2_TXCLK	enet2.TX_CLK	uart8.CTS_B	sim2.PORT0_RST_B	ecspi4.MISO	anatop.ENET_REF_CLK1	gpio2.IO[14]		anatop.OTG2_ID
X1_50	E10	LCD_DATA02	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[7]	src.BT_CFG[2]	sai1.TX_BCLK
X1_51	A15	ENET2_TXD0	enet2.TDATA[0]	uart7.RX	sim1.PORT0_SVEN	i2c4.SDA	weim.EB_B[2]	gpio2.IO[11]		usb.OTG1_OC
X1_52	A9	LCD_DATA01	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[6]	src.BT_CFG[1]	sai1.TX_SYNC
X1_53	A16	ENET2_TXD1	enet2.TDATA[1]	uart8.TX	sim2.PORT0_TRXD	ecspi4.SCLK	weim.EB_B[3]	gpio2.IO[12]		usb.OTG2_PWR
X1_54	B9	LCD_DATA00	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[5]	src.BT_CFG[0]	sai1.MCLK
X1_56	N8	SNVS_TAMPER5	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[5]		
X1_58	D9	LCD_HSYNC	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[2]		ecspi2.SS1
X1_60	B8	LCD_ENABLE	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS3_B	gpio3.IO[1]		ecspi2.RDY
X1_62	C9	LCD_VSYNC	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[3]		ecspi2.SS2
X1_63	C17	ENET2_RXD0	enet2.RDATA[0]	uart6.TX	sim1.PORT0_TRXD	i2c3.SCL	enet1.MDIO	gpio2.IO[8]		wdog1.WDOG_RST_B_DEB
X1_64	A8	LCD_CLK	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	weim.CS2_B	gpio3.IO[0]		wdog1.WDOG_RST_B_DEB
X1_65	C16	ENET2_RXD1	enet2.RDATA[1]	uart6.RX	sim1.PORT0_CLK	i2c3.SDA	enet1.MDC	gpio2.IO[9]		wdog2.WDOG_RST_B_DEB
X1_66	B4	NAND_ALE	rawnand.ALE	usdhc2.RESET_B	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[10]		ecspi3.SS1
X1_68	P14	JTAG_TMS	sjc.TMS	gpt2.CAPTURE1	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[11]	sdma.EXT_EVENT[1]	epit1.OUT

PIN	CPU BALL	PADNAME	MODE0	MODE1	MODE2	MODE3	MODE4	MODE5	MODE6	MODE8
X2_3	T10	BOOT_MODE0	src.BOOT_MODE[0]					gpio5.IO[11]		
X2_5	U10	BOOT_MODE1	src.BOOT_MODE[1]					gpio5.IO[12]		
X2_7*	B12	LCD_DATA13	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	usdhc1.RESET_B
X2_9*	A12	LCD_DATA14	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	usdhc1.DATA4
X2_13**	L14	GPIO1_IO02	i2c1.SCL	gpt1.COMPARE2	usb.OTG2_PWR	anatop.ENET_REF_CLK_25M	usdhc1.WP	gpio1.IO[2]	enet1.1588_EVENT1_IN	uart1.TX
X2_15**	L17	GPIO1_IO03	i2c1.SDA	gpt1.COMPARE3	usb.OTG2_OC	osc32k.32K_OUT	usdhc1.CD_B	gpio1.IO[3]	enet1.1588_EVENT1_OUT	uart1.RX
X2_19	F16	ENET1_RXD0	enet1.RDATA[0]	uart4.RTS_B	pwm1.OUT	csi.DATA[16]	can1.TX	gpio2.IO[0]		usdhc1.LCTL
X2_21	E17	ENET1_RXD1	enet1.RDATA[1]	uart4.CTS_B	pwm2.OUT	csi.DATA[17]	can1.RX	gpio2.IO[1]		usdhc2.LCTL
X2_25	E16	ENET1_CRS_DV	enet1.RX_EN	uart5.RTS_B	osc32k.32K_OUT	csi.DATA[18]	can2.TX	gpio2.IO[2]		usdhc1.VSELECT
X2_27	E15	ENET1_TXD0	enet1.TDATA[0]	uart5.CTS_B	anatop.24M_OUT	csi.DATA[19]	can2.RX	gpio2.IO[3]		usdhc2.VSELECT
X2_52	R10	SNVS_TAMPER0	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[0]		

NOTE*: Pin X1_26 and X1_28 are also routed to pin X2_7 and X2_9

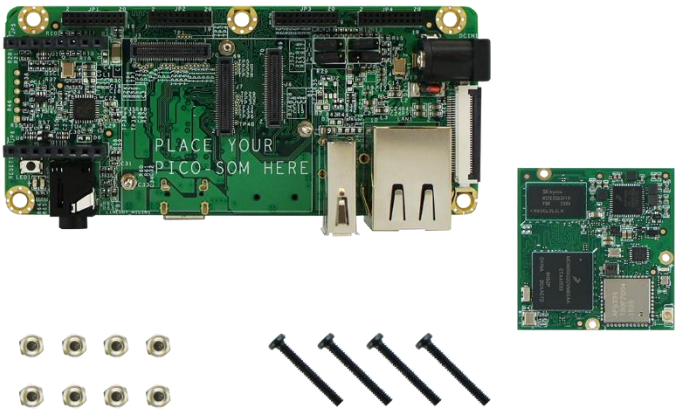
NOTE**: Pin X2_13 and X2_15 can only be used for I^2C function and should not be used in another pinmux mode.

6. Development Kits, Proto-type Components and Accessories

To evaluate the PICO-IMX6UL-EMMC TechNexion has made available a large number of evaluation kits and accessories available.

6.1. PICO-IMX6UL-EMMC Evaluation Kits

6.1.1. PICO Evaluation Start Kit Pack Content



Partnumber	Description
PICOHBIMX6G205R256E04BW	PICO Compute Module NXP i.MX6Ultralite + 256MB RAM + 4GB eMMC + 802.11ac + Bluetooth 4.0
	PICODWARFFL Carrierboard
	4 mounting screws + 8 mounting nuts

6.2. PICO Compatible Displays

6.2.1. Multi Touch PCAP Displays

Partnumber	Description
TDEJ050NAPCAPKIT	5 inch LVDS interface LCD display 800*480 resolution 350 nits with PCAP multitouch touchsensor.
	TLL Adaptor interface board
	Touch panel link cable

Partnumber	Description
TDAT070TN94PCAPKIT	7 inch LVDS interface LCD display 800*480 resolution 350 nits with PCAP multitouch touchsensor.
	TLL Adaptor interface board
	Touch panel link cable

NOTE: Many other display and touch solutions are available. Please connect with your TechNexion distributor or account manager for conditions and availability.

6.3. Accessories

6.3.1. EDMANTP150A138045D2450BK Pack Content.

Partnumber	Description
EDMANTP150A138045D2450BK	4.5 dB, 2.4/5 GHz, black color antenna
	u.FL to SMA patch cable

6.4. PICO Compute Module Product Ordering Part Numbers

The PICO-IMX6UL-EMMC is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

6.4.1 Standard Part Numbers

Standard PICO-IMX6UL-EMMC System-on-Modules part numbers can be ordered in multiples of 10 units in the following configurations.

Standard Part numbers featuring NXP i.MX6Ultralite with 256MB DDR3

Part Number	Description
PICOIMX6G205R256E04	PICO Compute Module NXP i.MX6Ultralite + 256MB RAM + 4GB eMMC
PICOIMX6G205R256E04BW	PICO Compute Module NXP i.MX6Ultralite + 256MB RAM + 4GB eMMC + 802.11ac + Bluetooth 4.0

6.4.2. Custom Part Number Creation Rules

The PICO-IMX6UL-EMMC can be ordered in custom tailored to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry minimum order quantities. Please connect with your TechNexion distributor or account manager for conditions and availability.

Part number format:

PICO-IMX6G205-R512-Exx-BW- xx-xxxx

Interface	Code	Description
Processor	G2	i.MX6Ultralite
Proccesor speed	05	528 Mhz
Memory	R256	256 MB DDR3L
	R512	512 MB DDR3L
Storage	Exx	eMMC (4GB = 04 , 8GB = 08 , 16GB = 16 , 32GB = 32)
Wireless Networking	-	No
	BW	802.11ac + Bluetooth 4.0
Temperature Range	-	Commercial Temperature range (0~60°C) (Default)
	TE	Extended Temperature range (-20~70°C)
	TI	Industrial Temperature range (-35~85°C)
	TEC	Certified Extended Temperature range (-20~70°C)
	TIC	Certified Industrial Temperature range (-35~85°C)
Custom ID	XXXX	Custom Partnumber ID for customized software loader and special component (BOM)

NOTE: Wireless networking option is not available in “TI” Industrial Temperature Range.

7. Important Notice

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8. DISCLAIMER

TechNexion Ltd.
16F-5, No. 736, Zhongzheng Road,
ZhongHe District, 23511, New Taipei City, Taiwan
Phone : +886-2-82273585
Fax : +886-2-82273590
E-mail : sales@technexion.com
Web : http://www.technexion.com/

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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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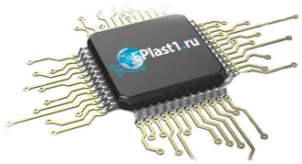
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.