EVALUATION KIT AVAILABLE

MAX14571/MAX14572/MAX14573
Adjustable Overvoltage and Overcurrent Protectors with High Accuracy

General Description

The MAX14571/MAX14572/MAX14573 adjustable overvoltage- and overcurrent-protection devices are ideal to protect systems against positive and negative input voltage faults up to ±40V and feature low 100mΩ (typ) R_{ON} FETs.

The overvoltage-protector (OVP) feature protects voltages between 6V and 36V, while the undervoltage-protector (UVP) feature protects voltages between 4.5V and 24V. The overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds are set using optional external resistors. The factory-preset internal OVLO threshold is 33V (typ) and the preset internal UVLO threshold is 19.2V (typ).

The ICs also feature programmable current-limit protection up to 4.2A. Once current reaches the threshold, the MAX14571 turns off after the 20.7ms (typ) blanking time and stays off during the retry period. The MAX14572 latches off after the blanking time, and the MAX14573 limits the current continuously. In addition, these devices feature reverse current and thermal-shutdown protection.

The ICs are available in a small 14-pin TSSOP (5mm x 6.5mm) package and are specified over the extended -40°C to +85°C temperature range.

Applications

Industrial Equipment
Consumer Electronics
Marine Equipment
Battery-Powered Applications

Features

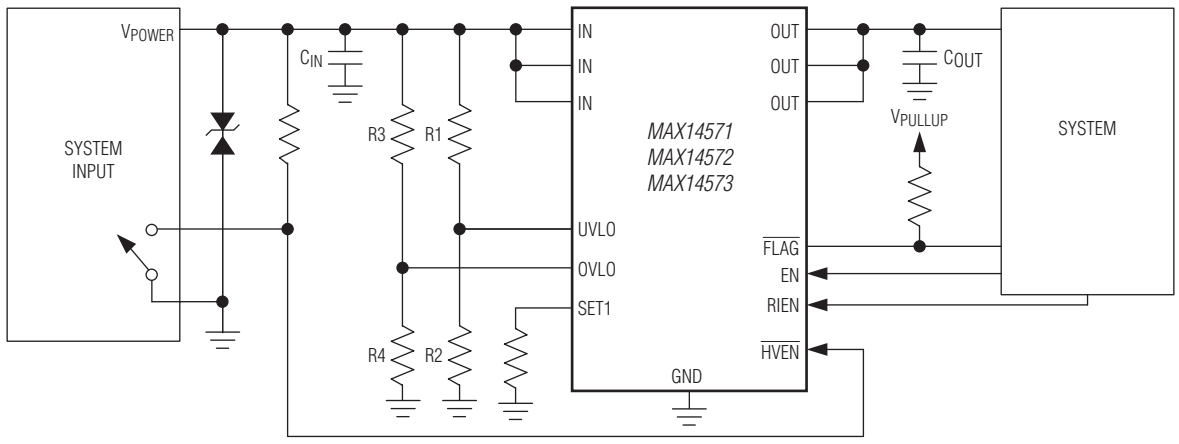
- **Wide 4.5V to 36V Operating Input Range**
- **Adjustable OVLO and UVLO Thresholds**
  ±3% Accurate Preset Thresholds
  Automatic Internal and External Selection
- **Programmable Forward Current Limit**
  Adjustable Current Limit Up to 4.2A
  ±15% Accuracy Limit
- **100mΩ (typ) On-Resistance FET**
- **Dual-Enable Inputs**
  High-Voltage-Capable Input, $\overline{HVEN}$
  Microprocessor Input, EN
- **Reverse Current Flow Control Input, RIEN**
- **Thermal-Shutdown Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OVERCURRENT PROTECTION
MAX14571EUD+T	-40°C to +85°C	14 TSSOP-EP*	Autoretry
MAX14572EUD+T	-40°C to +85°C	14 TSSOP-EP*	Latchoff
MAX14573EUD+T	-40°C to +85°C	14 TSSOP-EP*	Continuous

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Typical Operating Circuit



NOTE: R1, R2, R3, AND R4 ARE ONLY REQUIRED FOR ADJUSTABLE OVLO/UVLO; OTHERWISE, CONNECT UVLO/OVLO TO GND.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6470; Rev 1; 12/12

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN, $\overline{HVEN}$ .....-40V to +40V
IN to OUT .....-40V to +40V
OUT .....-0.3V to +40V
OVLO, UVLO, $\overline{FLAG}$, EN, RIEN.....-0.3V to +6.0V
Current into IN (DC Operating) (Note 1)..... .....4.2A
SETI ....-0.3V to Min (V_{IN}, 1.22V) + 0.3V

Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 25.6mW/°C above +70°C)..... ….2051.3mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: DC current is also limited by the thermal design of the system.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... +39°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... +3°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4.5V to 36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 24V, R_{ISET} = 12kΩ, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		4.5		36	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V			15	µA
Shutdown Output Current	I_{OFF}	V_{OUT} = 0V			2	µA
Reverse Input Current	I_{IN_RVS}	V_{IN} = -40V, V_{OUT} = V_{GND} = 0V	-35			µA
Supply Current	I_{IN}	V_{IN} = 15V, R_{ISET} = 12kΩ		490	700	µA
Internal Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	32	33	34	V
		V_{IN} falling		32		
Internal Undervoltage Trip Level	V_{UVLO}	V_{IN} falling	17.5	18.5	19.5	V
		V_{IN} rising	18.2	19.2	20.2	
Overvoltage-Lockout Hysteresis		% of typical OVLO		3		%
External OVLO Adjustment Range		(Note 4)	6		36	V
External OVLO Select Voltage	$V_{OVLOSEL}$		0.3		0.50	V
External OVLO Leakage Current	I_{OVLO_LEAK}	V_{OVLO} < 1.2V (Note 5)	-100		+100	nA
External UVLO Adjustment Range			4.5		24	V
External UVLO Select Voltage	$V_{OVLOSEL}$		0.3		0.50	V
External UVLO Leakage Current	I_{UVLO_LEAK}	(Note 5)	-100		+100	nA
BG Reference Voltage	V_{BG}		1.186	1.210	1.234	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 4.5V to 36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 24V, $R_{ISET.}$ = 12kΩ, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL FETs						
Internal FET On-Resistance	R_{ON}	I_{LOAD} = 100mA, $V_{IN} \geq$ 8V		100	160	mΩ
Current-Limit Adjustment Range	I_{LIM}	(Notes 5, 6)	0.7		4.2	A
Current-Limit Accuracy			-15		+15	%
$\overline{FLAG}$ Assertion Drop Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V		560		mV
Reverse Current Blocking Threshold	V_{RIB}	V_{OUT} - V_{IN}	40	100	160	mV
Reverse Blocking Leakage Current	I_{RBL}	V_{OUT} - V_{IN} > 160mV, current into OUT		400	600	µA
$\overline{FLAG}$ OUTPUT						
$\overline{FLAG}$ Output Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
$\overline{FLAG}$ Output Leakage Current		V_{IN} = $V_{\overline{FLAG}}$ = 5V, $\overline{FLAG}$ desasserted			2	µA
LOGIC INPUT						
$\overline{HVEN}$ Threshold Voltage	$V_{\overline{HVEN}_TH}$		1	2	3.5	V
$\overline{HVEN}$ Threshold Hysteresis				2		%
$\overline{HVEN}$ Input Leakage Current	$I_{\overline{HVEN}_LEAK}$	$V_{\overline{HVEN}}$ = 36V		26	40	µA
$\overline{HVEN}$ Input Reverse Leakage Current	$I_{\overline{HVEN}_RLEAK}$	V_{IN} = $V_{\overline{HVEN}}$ = -36V	-45	-27		µA
EN, RIEN Input Logic-High	V_{IH}		1.4			V
EN, RIEN Input Logic-Low	V_{IL}				0.4	V
EN, RIEN Input Leakage Current	I_{EN_LEAK}, I_{RIEN_LEAK}	V_{EN} = V_{RIEN} = 5.0V	-1		+1	µA
THERMAL PROTECTION						
Thermal Shutdown	T_{JC_MAX}	Low-to-high temperature		150		°C
Thermal-Shutdown Hysteresis	T_{JC_HYST}	High-to-low temperature		30		°C
TIMING CHARACTERISTICS (Note 7)						
Switch Turn-On Time	t_{ON}	From OFF to IN, see Table 1. R_{LOAD} = 240Ω, C_{OUT} = 470µF		25		ms
Switch Turn-Off Time	t_{OFF}	R_{LOAD} = 47Ω		3		µs
Overvoltage Switch Turn-Off Time	t_{OFF_OVP}	V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{OVLO}, R_{LOAD} = 47Ω, R_{SETI} = 10kΩ		3		µs
Overcurrent Switch Turn-Off Time	t_{OFF_OCP}	I_{IN} > I_{LIM}, after t_{BLANK}, I_{LIM} = 1A		3		µs
IN Debounce Time	t_{DEB}	V_{IN} changes from 0V to greater than V_{UVLO} to V_{OUT} = 10% of V_{IN}	15.0	16.7	18.4	ms
Blanking Time	t_{BLANK}		18.6	20.7	22.8	ms
Autoretry Time	t_{RETRY}	After blanking time from I_{OUT} > I_{LIM} to $\overline{FLAG}$ clear (deassertion) (Note 8)	540	600	660	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 4.5V to 36V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 24V, $R_{ISET.}$ = 12kΩ, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
IN		Human Body Model, IN bypassed to GND with a 1µF low-ESR ceramic capacitor		±15		kV

Note 3: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization; not production tested.
Note 4: Not production tested, user settable. See overvoltage/undervoltage lockout instructions.
Note 5: Guaranteed by design; not production tested. UVLO and OVLO are internally clamped to BG reference voltage.
Note 6: The current limit can be set below 700mA with a decreased accuracy.
Note 7: All timing is measured using 20% and 80% levels.
Note 8: The ratio between the autoretry time and blanking time is fixed and equal to 30.

Timing Diagrams

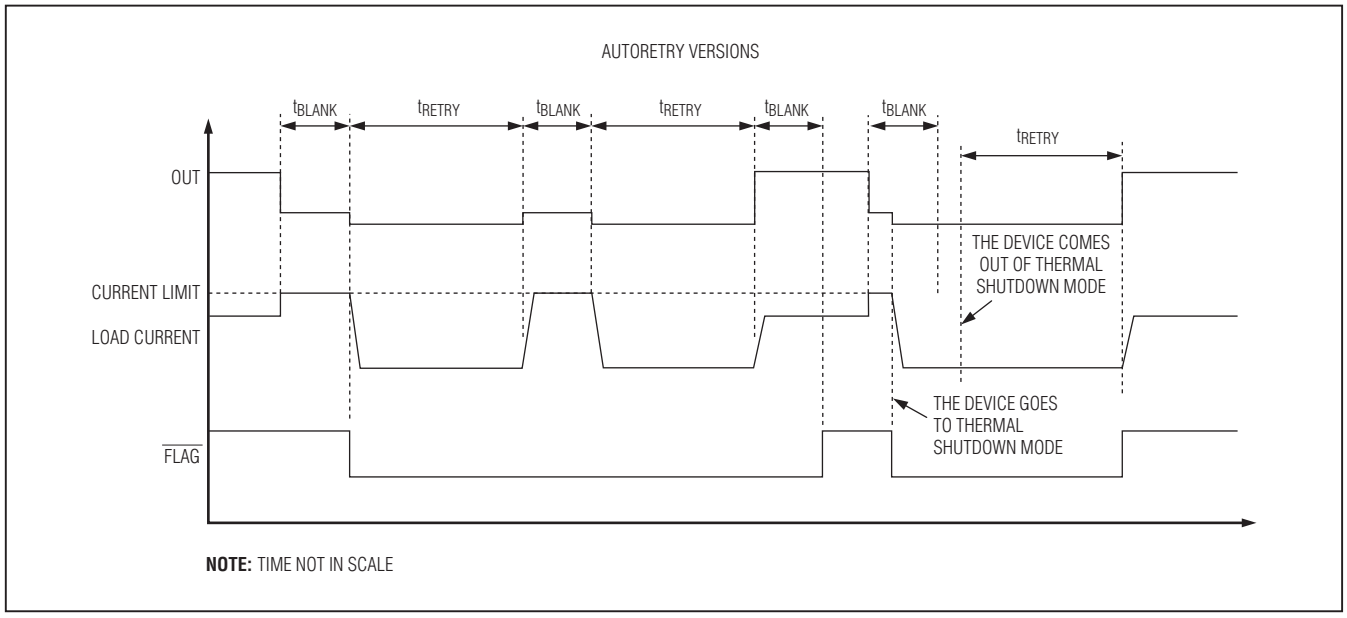


Figure 1. Autoretry Fault Diagram

Timing Diagrams (continued)

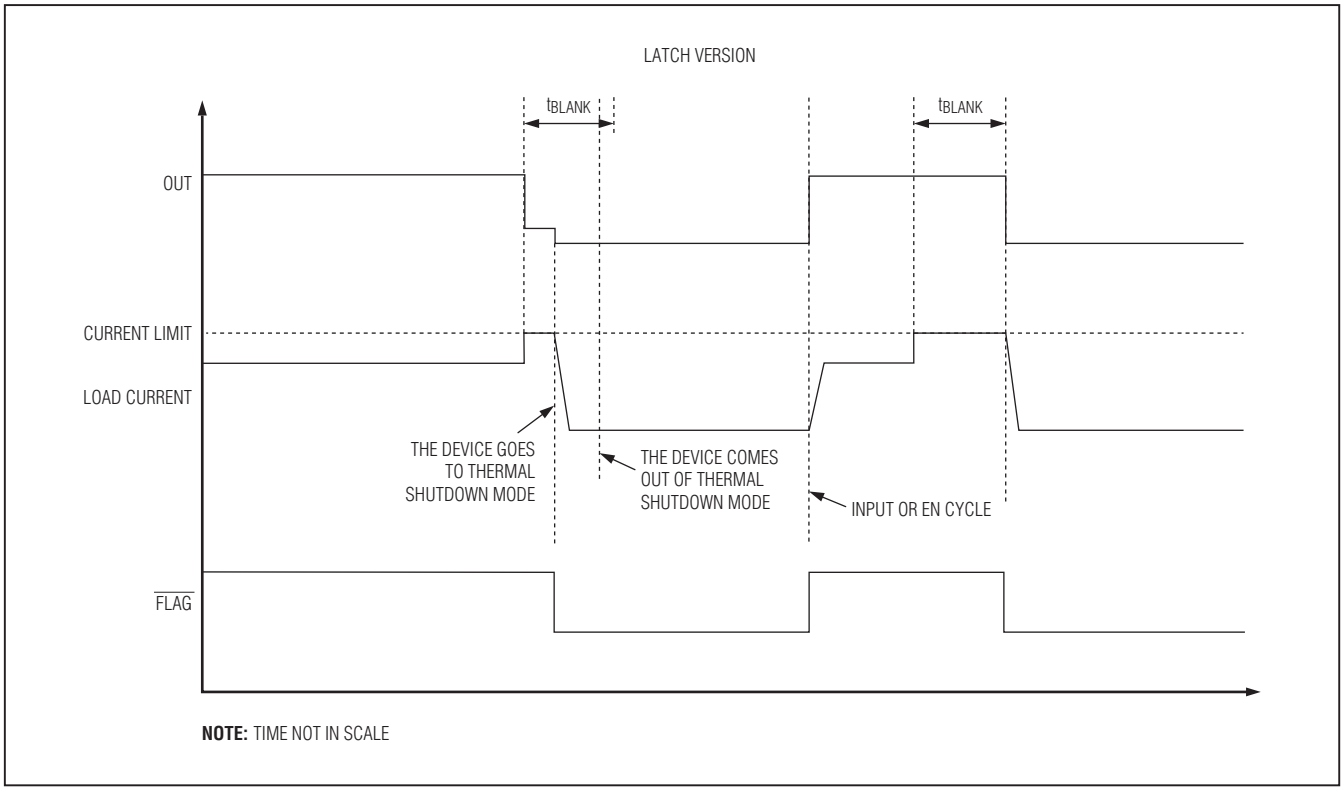


Figure 2. Latch-Off Fault Diagram

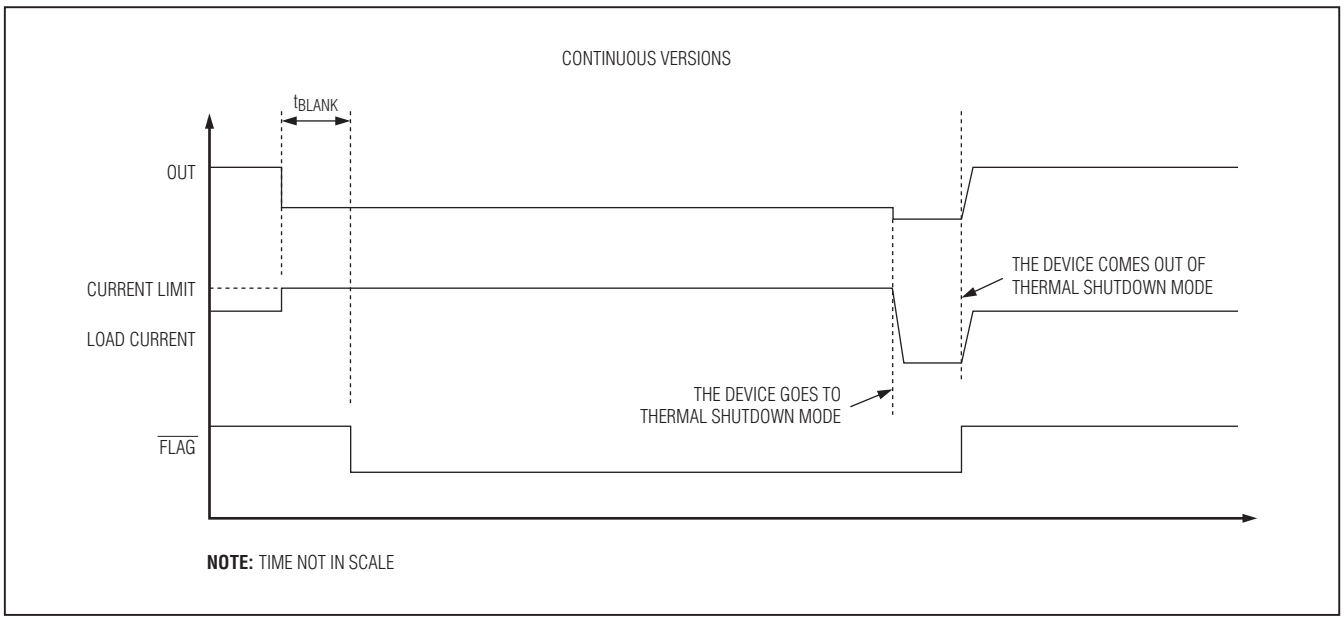


Figure 3. Continuous Fault Diagram

Timing Diagrams (continued)

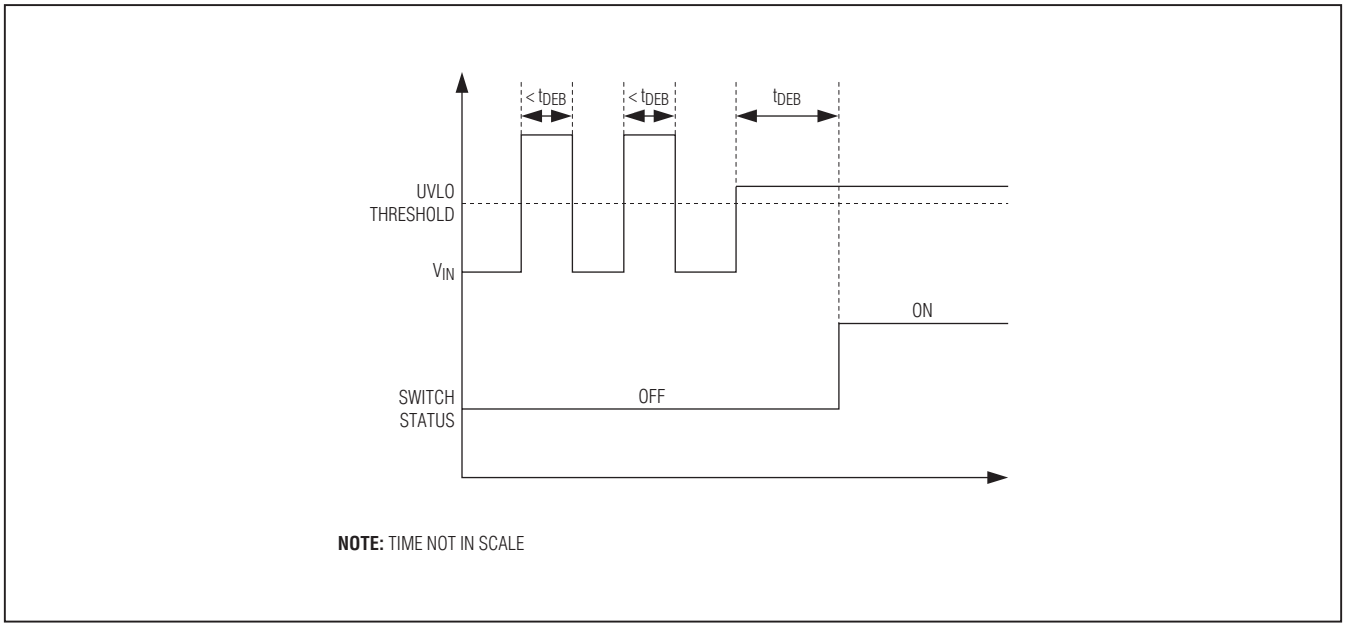
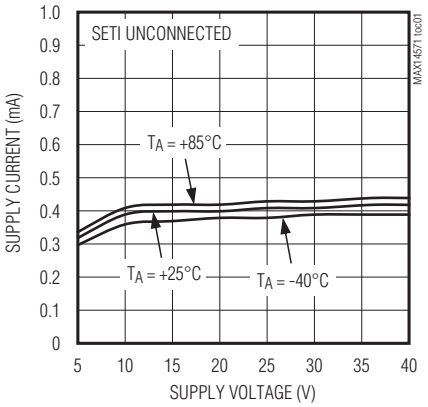


Figure 4. Debounce Timing

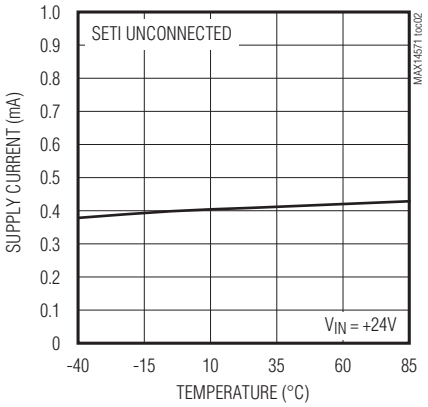
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

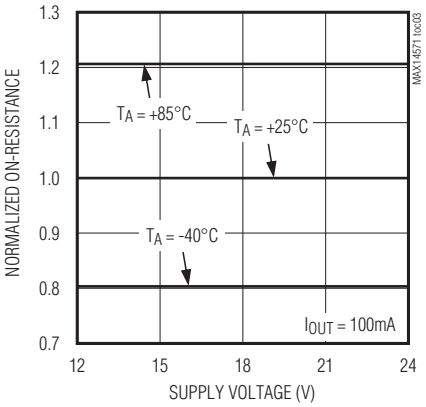
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



IN SUPPLY CURRENT vs. TEMPERATURE



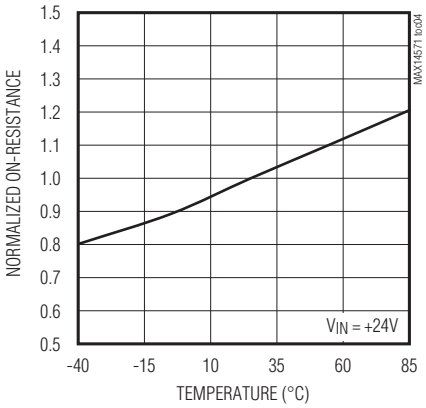
NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



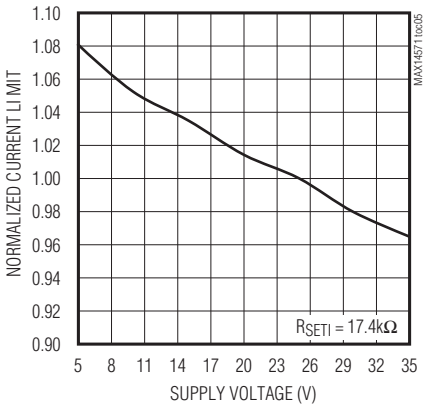
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

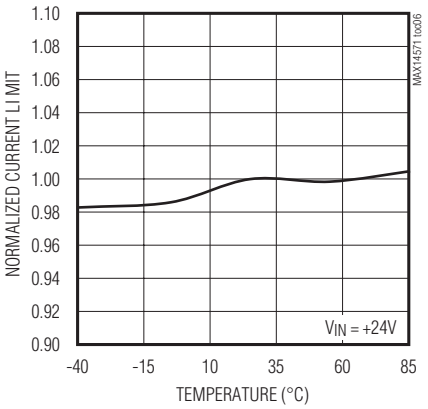
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



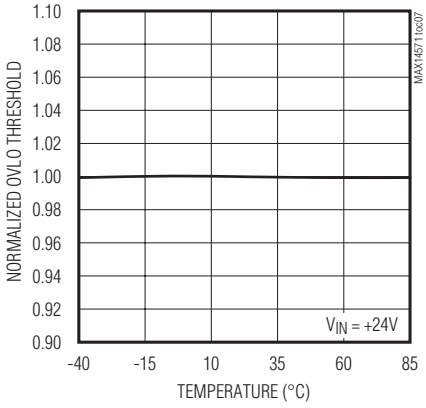
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



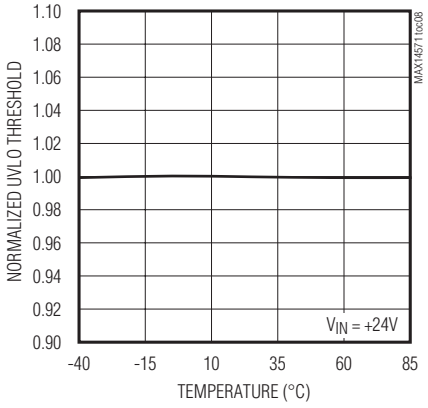
NORMALIZED CURENT LIMIT vs. TEMPERATURE



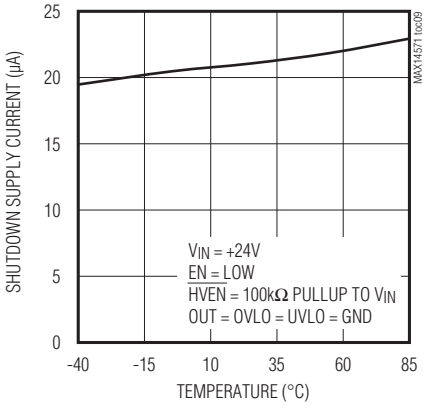
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



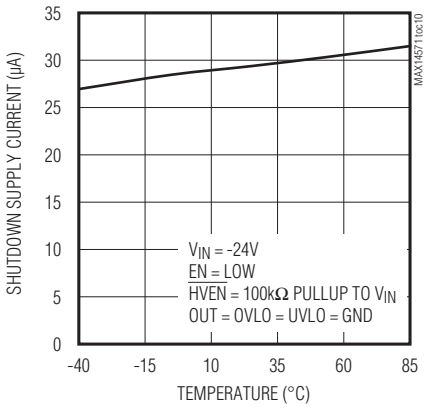
NORMALIZED UVLO THRESHOLD vs. TEMPERATURE



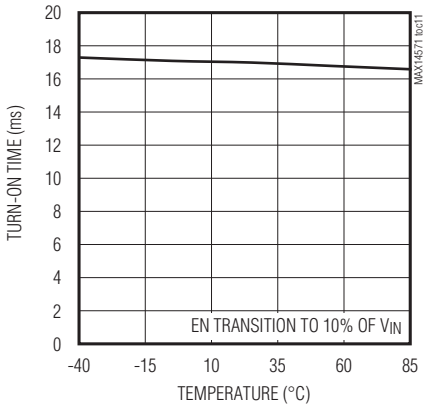
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



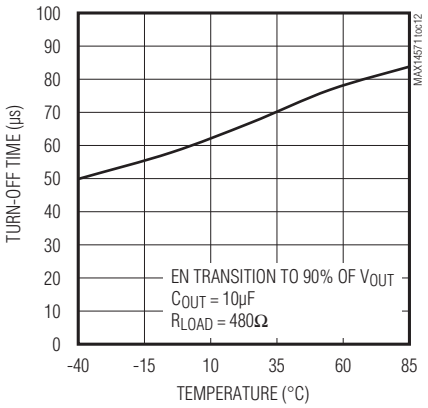
SHUTDOWN REVERSE CURRENT vs. TEMPERATURE



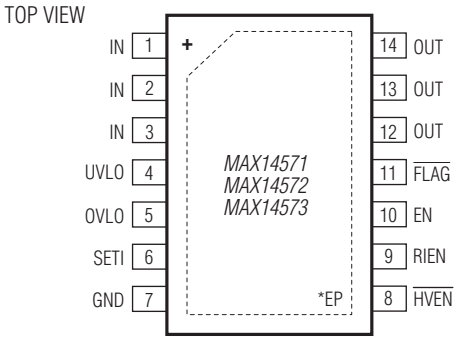
TURN-ON TIME vs. TEMPERATURE



TURN-OFF TIME vs. TEMPERATURE



Pin Configuration



TSSOP

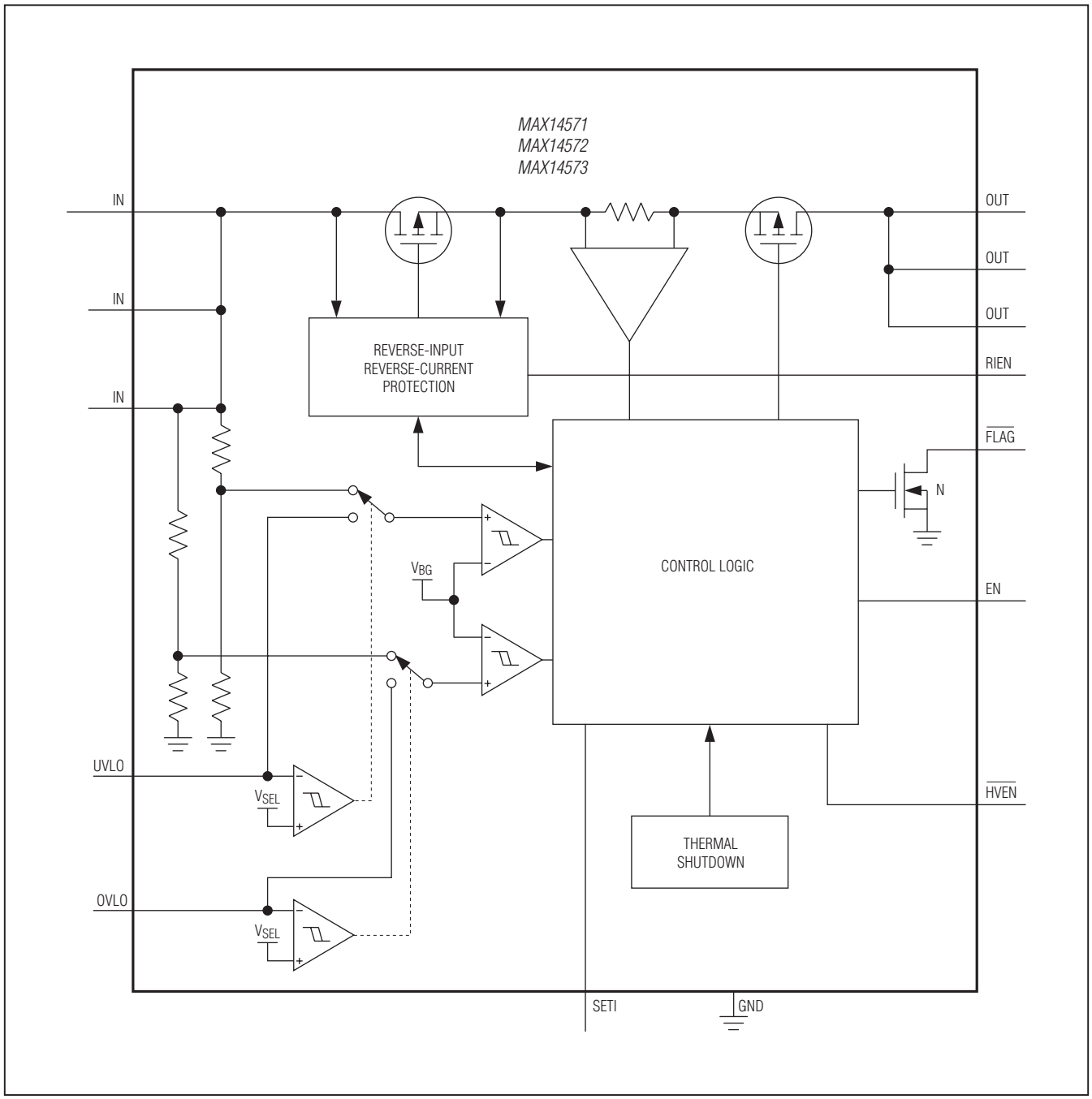
*CONNECT EXPOSED PAD TO GND

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	IN	Overvoltage-Protection Input. Bypass IN to GND with a 1µF ceramic capacitor placed as close as possible to the device. Use a 1µF, low-ESR ceramic capacitor to enable ±15kV (HBM) ESD protection on IN. For hot-plug applications, see the *Applications Information* section.
4	UVLO	Externally Programmable Undervoltage-Lockout Threshold. Connect UVLO to GND to use the default internal UVLO threshold. Connect UVLO to an external resistor-divider to define a threshold externally and override the preset internal UVLO threshold.
5	OVLO	Externally Programmable Overvoltage-Lockout Threshold. Connect OVLO to GND to use the default internal OVLO threshold. Connect OVLO to an external resistor-divider to define a threshold externally and override the preset internal OVLO threshold.
6	SETI	Overload Current-Limit Adjust. Connect a resistor from SETI to GND to program the overcurrent limit. If SETI is unconnected, the current limit is set to 0A. If SETI is connected to GND, the FETs turn off and $\overline{FLAG}$ is asserted. Do not connect more than 10pF to SETI.
7	GND	Ground
8	$\overline{HVEN}$	Active-Low Enable Input. $\overline{HVEN}$ is a high-voltage-capable enable input. Drive $\overline{HVEN}$ low for normal operation. Drive $\overline{HVEN}$ high to disable the device. $\overline{HVEN}$ has up to 36V overvoltage protection at the input (Table 1).
9	RIEN	Reverse-Current Enable Input. Connect RIEN to GND to disable the reverse-current flow protection. Connect RIEN to logic-high to activate the reverse-current flow protection.
10	EN	Active-High Enable Input. Drive EN high for normal operation. Drive EN low to disable the device (Table 1).
11	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when the fault duration exceeds the blanking time, reverse current is detected, thermal-shutdown mode is active, OVLO threshold is reached, or SETI is connected to GND.
12, 13, 14	OUT	Output Voltage. Output of internal FETs. Bypass OUT to GND with a 1µF ceramic capacitor placed as close as possible to the device. For a long output cable or inductive lead, see the *Applications Information* section.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. Do not use EP as the single GND connection.

Adjustable Overvoltage and Overcurrent Protectors with High Accuracy

Functional Diagram



Detailed Description

The MAX14571/MAX14572/MAX14573 are adjustable overvoltage- and overcurrent-protection devices designed to protect systems against positive and negative input voltage faults up to ±40V, and feature low 100mΩ (typ) on-resistance FETs. If the input voltage exceeds the OVLO threshold or falls below the UVLO, the internal FETs are turned off to prevent damage to the protected components. If the OVLO or the UVLO pin is set below the external OVLO or UVLO select thresholds ($V_{OVLOSEL}$ and $V_{UVLOSEL}$), the device automatically selects the internal ±3% (typ) accurate trip thresholds. The internal OVLO threshold is preset to 33V (typ), and the internal UVLO threshold is preset to 19.2V (typ).

The ICs feature programmable current-limit protection up to 4.2A. Once current reaches the threshold, the MAX14571 turns off after 20.7ms (typ) blanking time and stays off during the retry period. The MAX14572 latches off after the blanking time, and the MAX14573 limits the current continuously.

Programmable Current Limit/Threshold

A resistor from SETI to GND sets the current limit/threshold for the switch (see the *Setting the Current Limit/Threshold* section). If the output current is limited at the current threshold value for a time equal to or longer than t_{BLANK}, the output $\overline{FLAG}$ asserts and the MAX14571 enters the autoretry mode, the MAX14572 latches off the switch, and the MAX14573 enters the continuous current-limit mode.

Autoretry (MAX14571)

When the current threshold is reached, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK}. The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. A retry time delay, t_{RETRY}, is started immediately after t_{BLANK} has elapsed and during t_{RETRY} time, the FETs are off. At the end of t_{RETRY}, the FETs are turned on again. If the fault still exists, the cycle is repeated and the $\overline{FLAG}$ stays low. When the fault is removed, the FETs stay on. If the die temperature exceeds +150°C (typ) due to self-heating, the MAX14571 enables thermal shutdown until the die temperature drops by approximately 30°C (Figure 1).

The autoretry feature reduces the system power in case of overcurrent or short-circuit conditions. During t_{BLANK} time, when the switch is on, the supply current is held at the current limit. During t_{RETRY} time, when the switch is off, there is no current through the switch. Thus, the output current is much less than the programmed current limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK}}{t_{BLANK} + t_{RETRY}}\right]$$

With a 20.7ms (typ) t_{BLANK} and 600ms (typ) t_{RETRY}, the duty cycle is 3.3%, resulting in a 96.7% power savings.

Latch-Off (MAX14572)

When the current threshold is reached, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK}. The timer resets when the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond the blanking time. To reset the switch, either toggle the control logic EN or $\overline{HVEN}$ or cycle the input voltage. If the die temperature exceeds +150°C (typ) due to self-heating, the MAX14572 latches off (Figure 2.)

Continuous Current Limit (MAX14573)

When the current threshold is reached, the MAX14573 limits the output current to the programmed current limit. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK} and deasserts when the overload condition is removed. If the die temperature exceeds +150°C (typ) due to self-heating, the MAX14573 enables thermal shutdown until the die temperature drops by approximately 30°C (Figure 3).

Reverse-Current Enable (RIEN)

This feature disables the reverse-current protection and enables reverse-current flow from OUT to IN. The reverse-current enable feature is useful in applications with inductive loads.

Fault Flag Output

$\overline{FLAG}$ is an open-drain fault indicator output and requires an external pullup resistor to a DC supply. $\overline{FLAG}$ goes low when any of the following conditions occur:

- The blanking time has elapsed.
- The reverse-current protection has tripped.
- The die temperature exceeds +150°C.
- SETI is connected to ground.
- OVLO threshold is reached.

Thermal-Shutdown Protection

The devices have a thermal-shutdown feature to protect them from overheating. The devices turn off and the $\overline{FLAG}$ asserts when the junction temperature exceeds +150°C (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools by 30°C (typ), except for the MAX14572, which remains latched off.

The thermal limit behaves similarly to the current limit. For the MAX14571 (autoretry), the thermal limit works with the autoretry timer. When the device comes out of the thermal limit, it starts after the retry time. For the MAX14572 (latch off), the device latches off until power or EN cycle. For the MAX14573 (continuous), the device only disables while the temperature is over the limit. There is no blanking time for thermal protection.

Overvoltage Lockout (OVLO)

The devices have a 33V (typ) preset OVLO threshold when the voltage at OVLO is set below the external OVLO select voltage ($V_{OVLOSEL}$). Connect OVLO to GND to activate the preset OVLO threshold. Connect the external resistors to the OVLO pin as shown in the *Typical Operating Circuit* to externally adjust the OVLO threshold. Use the following equation to adjust the OVLO threshold. The recommended value for R3 is 2.2MΩ:

$$V_{OVLO} = V_{BG} \times \left[1 + \frac{R3}{R4}\right]$$

Undervoltage Lockout (UVLO)

The devices have a 19.2V (typ) preset UVLO threshold when the voltage at UVLO is set below the external UVLO select voltage ($V_{UVLOSEL}$). Connect UVLO to GND to activate the preset UVLO threshold. Connect the external resistors to the UVLO pin as shown in the *Typical Operating Circuit* to externally adjust the UVLO threshold. Use the following equation to adjust the UVLO threshold. The recommended value for R1 is 2.2MΩ:

$$V_{UVLO} = V_{BG} \times \left[1 + \frac{R1}{R2}\right]$$

Switch Control

There are two independent enable inputs ($\overline{HVEN}$ and EN) for the devices. $\overline{HVEN}$ is a high-voltage-capable input. Toggle $\overline{HVEN}$ or EN to reset the fault condition once a short circuit is detected and the devices shut down (Table 1).

Input Debounce Protection

The ICs feature input debounce protection. When the input voltage is higher than the UVLO threshold voltage for a period greater than the debounce time (t_{DEB}), the internal FETs are turned on. This feature is intended for applications where the EN or $\overline{HVEN}$ signal is present when the power supply ramps up (Figure 4).

Applications Information

Setting the Current Limit/Threshold

A resistor from SETI to ground programs the current limit/threshold value for the devices. Leaving SETI unconnected selects a 0A current limit/threshold. Connecting SETI to ground asserts $\overline{FLAG}$. Use the following formula to calculate the current limit:

$$R_{SETI}(k\Omega) = \frac{11500}{I_{LIM}(mA)}$$

IN Bypass Capacitor

Connect a minimum of 1µF capacitor from IN to GND to limit the input voltage drop during momentary output short-circuit conditions. Larger capacitor values further reduce the voltage undershoot at the input.

Hot-Plug IN

In many system powering applications, an input-filtering capacitor is required to lower the radiated emission, enhance the ESD capability, etc. In hot-plug applications, parasitic cable inductance, along with the input capacitor, cause overshoot and ringing when the powered cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. An input voltage of 24V can easily exceed the absolute maximum rating of 40V, which may permanently damage the device. A transient voltage suppressor (TVS) is often used for industrial applications to protect the system from these conditions. We recommend using a TVS that is capable of limiting surge to 40V placed close to the input terminal.

Table 1. Switch Control

$\overline{HVEN}$	EN	SWITCH STATUS
0	0	On
1	0	Off
0	1	On
1	1	On

OUT Bypass Capacitor

For stable operation over the full temperature range and over the entire programmable current-limit range, connect a 1µF ceramic capacitor from OUT to ground. Excessive output capacitance can cause a false overcurrent condition due to decreased dV/dt across the capacitor. Calculate the maximum capacitive load (C_{MAX}) value that can be connected to OUT by using the following formula:

$$C_{MAX}(\mu F) = \frac{I_{LIM}(mA) \times t_{BLANK(MIN)}\ (ms)}{V_{IN}(V)}$$

For example, for V_{IN} = 24V, t_{BLANK} = 15ms, and I_{LIM} = 4.2A, C_{MAX} equals 2625µF.

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection form a sudden short to ground with an inductive load or long cable, a Schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal. If the output is continuously shorted to ground at the maximum supply voltage, the switches with the autoretry option do not cause thermal-shutdown detection to trip:

$$P_{(MAX)} = \frac{V_{IN(MAX)} \times I_{OUT(MAX)} \times t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

Attention must be given to the MAX14573 continuous current-limit version when the power dissipation during a fault condition can cause the device to reach the thermal-shutdown threshold. Thermal vias from the exposed pad to ground plane are highly recommended to increase the system thermal capacitance while reducing the thermal resistance to the ambient.

ESD Test Conditions

The devices are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 1µF low-ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) typical ESD on IN. All the pins have a ±2kV (HBM) typical ESD protection.

HBM ESD Protection

Figure 5a shows the Human Body Model, and Figure 5b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

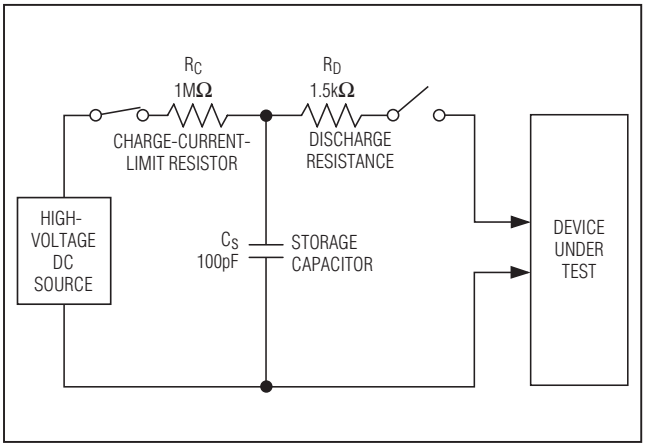


Figure 5a. Human Body ESD Test Model

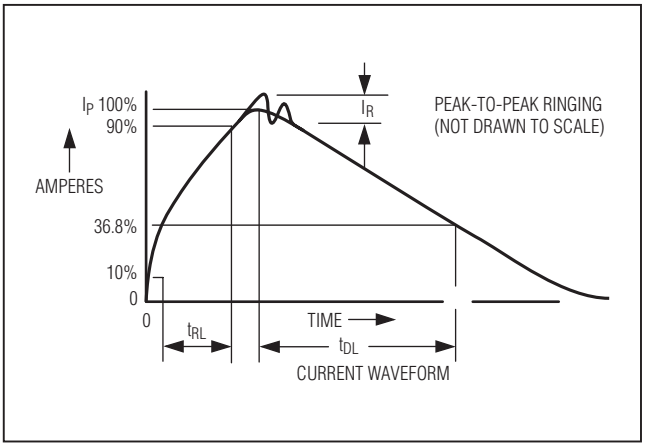


Figure 5b. Human Body Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP-EP	U14E+3	21-0108	90-0119

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	—
1	12/12	Removed future product asterisk and notes for the MAX14571/MAX14573, style edits.	1–6, 8, 10, 11, 14

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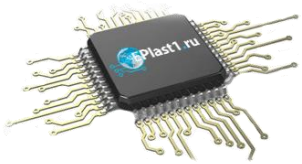
- Защита от снятия компонента с производства.



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