

Surround Sound Codec

Features

- Stereo 20-bit A/D converters
- Six 20-bit D/A converters
- S/PDIF receiver
 - AC-3 & MPEG auto-detect capability
- 108 dB DAC signal-to-noise ratio (EIAJ)
- Mono 20-bit A/D converter
- Programmable Input gain & output attenuation
- On-chip anti-aliasing and output smoothing filters
- De-emphasis for 32 kHz, 44.1 kHz, 48 kHz

Description

The CS4226 is a single-chip codec providing stereo analog-to-digital and six digital-to-analog converters using Delta-Sigma conversion techniques. This +5V device also contains volume control independently selectable for each of the six D/A channels. An S/PDIF receiver is included as a digital input channel. Applications include Dolby Pro-logic®, Dolby Digital AC-3®, THX® and DTS® home theater systems, DSP based car audio systems, and other multi-channel applications.

ORDERING INFORMATION

CS4226-KQ	-10° to +70° C	44-pin TQFP
CS4226-KQZ	-10° to +70° C	44-pin TQFP Lead Free
CS4226-BQ	-40° to +85° C	44-pin TQFP
CS4226-BQZ	-40° to +85° C	44-pin TQFP Lead Free
CS4226-DQ	-40° to +85° C	44-pin TQFP
CDB4226		Evaluation Board

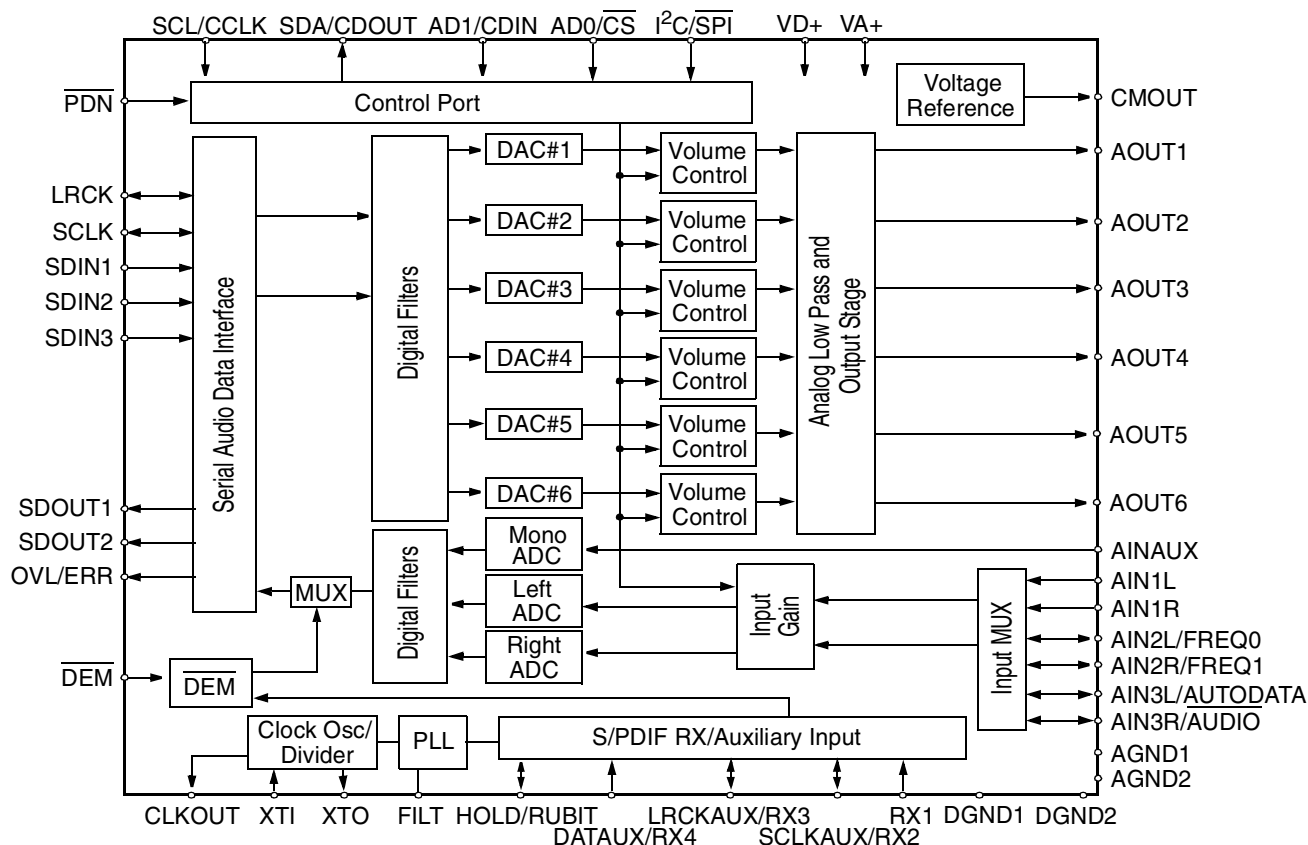


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Table 1. Change History

Revision	Date	Changes
F1	September 1998	Initial release.
F2	March 2003	Update drawings.
F3	September 2004	Added lead free part information.
F4	November 2004	Added lead free part information.

1 CHARACTERISTICS/SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A = 25^\circ\text{C}$.)

SPECIFIED OPERATING CONDITIONS

(AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Nom	Max	Units
Power Supplies	Digital	VD+	4.75	5.0	5.25	V
$I(VA+) - (VD+) < 0.4\text{V}$	Analog	VA+	4.75	5.0	5.25	V
Operating Ambient Temperature	CS4226-KQ/-KQZ	T_A	-10	-	70	$^\circ\text{C}$
	CS4226-BQ/-BQZ		-40	-	85	$^\circ\text{C}$
	CS4226-DQ		-40	-	85	$^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD+	-0.3	-	6.0	V
	Analog	VA+	-0.3	-	6.0	V
Input Current	(Note 1)		-	-	± 10	mA
Analog Input Voltage	(Note 2)		-0.7	-	$(VA+) + 0.7$	V
Digital Input Voltage	(Note 2)		-0.7	-	$(VD+) + 0.7$	V
Ambient Temperature	(Power Applied)		-55	-	+125	$^\circ\text{C}$
Storage Temperature			-65	-	+150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

- Notes:
- Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SCR latch-up.
 - The maximum over or under voltage is limited by the input current.

ANALOG CHARACTERISTICS

(Full Scale Input Sine wave, 990.52 Hz; $F_s = 44.1$ kHz (PLL in use); Measurement Bandwidth is 20 Hz to 20 kHz, unless specified otherwise.)

Parameter	Symbol	CS4226-KQ/-KQZ			CS4226-BQ/-BQZ/-DQ			Units	
		Min	Typ	Max	Min	Typ	Max		
Analog Input Characteristics - Minimum gain setting (0 dB) Differential Input; unless otherwise specified.									
ADC Resolution	Stereo Audio channels		16	-	20	16	-	20	Bits
	Mono channel		16	-	20	16	-	20	Bits
Total Harmonic Distortion	THD			0.003	-		0.003	-	%
Dynamic Range	(A weighted, Stereo)		92	95	-	90	93	-	dB
	(unweighted, Stereo)		-	92	-	-	90	-	dB
	(A weighted, Mono)		89	-	-	87	-	-	dB
Total Harmonic Distortion + Noise	-1 dB, Stereo (Note 3)	THD+N	-	-88	-82	-	-86	-80	dB
	-1 dB, Mono (Note 1)		-	-	-72	-	-	-70	dB
Interchannel Isolation			-	90	-	-	90	-	dB
Interchannel Gain Mismatch			-	0.1	-	-	0.1	-	dB
Programmable Input Gain Span			8	9	10	8	9	10	dB
Gain Step Size			2.7	3	3.3	2.7	3	3.3	dB
Offset Error (with high pass filter)			-	-	0	-	-	0	LSB
Full Scale Input Voltage (Single Ended):			0.90	1.0	1.10	0.90	1.0	1.10	Vrms
Gain Drift			-	100	-	-	100	-	ppm/°C
Input Resistance	(Note 4)		10	-	-	10	-	-	kΩ
Input Capacitance			-	-	15	-	-	15	pF
CMOUT Output Voltage			-	2.3	-	-	2.3	-	V
A/D Decimation Filter Characteristics									
Passband	(Note 5)		0.02	-	20.0	0.02	-	20.0	kHz
Passband Ripple			-	-	0.01	-	-	0.01	dB
Stopband	(Note 5)		27.56	-	5617.2	27.56	-	5617.2	kHz
Stopband Attenuation	(Note 6)		80	-	-	80	-	-	dB
Group Delay (Fs = Output Sample Rate)	(Note 7)	t _{gd}	-	15/Fs	-	-	15/Fs	-	s
Group Delay Variation vs. Frequency		Δ t _{gd}	-	-	0	-	-	0	μs

- Notes:
- Referenced to typical full-scale differential input voltage (2V_{rms}).
 - Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified
 - Filter characteristics scale with output sample rate.
 - The analog modulator samples the input at 5.6448 MHz for an output sample rate of 44.1 kHz. There is no rejection of input signals which are multiples of the sampling frequency ($n \times 5.6448$ MHz ± 20.0 kHz where $n = 0, 1, 2, 3, \dots$).
 - Group delay for $F_s = 44.1$ kHz, $t_{gd} = 15/44.1$ kHz = 340 μs

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	CS4226-KQ/-KQZ			CS4226-BQ/-BQZ/-DQ			Units	
		Min	Typ	Max	Min	Typ	Max		
High Pass Filter Characteristics									
Frequency Response:	-3 dB (Note 5)		-	3.4	-	-	3.4	-	Hz
	-0.13 dB		-	20	-	-	20	-	Hz
Phase Deviation	@ 20 Hz (Note 5)		-	10	-	-	10	-	Deg.
Passband Ripple			-	-	0	-	-	0	dB
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.									
DAC Resolution			16	-	20	16	-	20	Bits
Signal-to-Noise/Idle (DAC muted, A weighted)			101	108	-	99	106	-	dB
Channel Noise									
Dynamic Range (DAC not muted, A weighted)			93	98	-	91	96	-	dB
	(DAC not muted, unweighted)		-	95	-	-	93	-	dB
Total Harmonic Distortion	THD		-	0.003	-	-	0.003	-	%
Total Harmonic Distortion + Noise (Stereo)	THD+N		-	-88	-83	-	-86	-81	dB
Interchannel Isolation			-	90	-	-	90	-	dB
Interchannel Gain Mismatch			-	0.1	-	-	0.1	-	dB
Attenuation Step Size (All Outputs)			0.7	1	1.3	0.7	1	1.3	dB
Programmable Output Attenuation Span			-84	-86	-	-84	-86	-	dB
Offset Voltage (relative to CMOUT)			-	±15	-	-	±15	-	mV
Full Scale Output Voltage			0.92	1.0	1.08	0.92	1.0	1.08	Vrms
Gain Drift			-	100	-	-	100	-	ppm/°C
Out-of-Band Energy (Fs/2 to 2Fs)			-	-60	-	-	-60	-	dBFS
Analog Output Load	Resistance:		10	-	-	10	-	-	kΩ
	Capacitance:		-	-	100	-	-	100	pF
Combined Digital and Analog Filter Characteristics									
Frequency Response	10 Hz to 20 kHz		-	±0.1	-	-	±0.1	-	dB
Deviation from Linear Phase			-	±0.5	-	-	±0.5	-	Deg.
Passband: to 0.01 dB corner	(Notes 8, 9)		0	-	20.0	0	-	20.0	kHz
Passband Ripple	(Note 9)		-	-	±0.01	-	-	±0.01	dB
Stopband	(Notes 8, 9)		24.1	-	-	24.1	-	-	kHz
Stopband Attenuation	(Note 10)		70	-	-	70	-	-	dB
Group Delay (Fs = Input Word Rate)	(Note 5)	tgd	-	16/Fs	-	-	16/Fs	-	s
Analog Loopback Performance									
Signal-to-noise Ratio (CCIR-2K weighted, -20 dB input)	CCIR-2K		-	71	-	-	71	-	dB
Power Supply									
Power Supply Current	Operating		-	90	113	-	90	115	mA
	Power Down		-	1	3	-	1	3	mA
Power Supply Rejection	(1 kHz, 10 mV _{rms})		-	45	-	-	45	-	dB

Notes: 8. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 44.1 kHz, the 0.01 dB passband edge is 0.4535 $\times$ Fs and the stopband edge is 0.5465 $\times$ Fs.

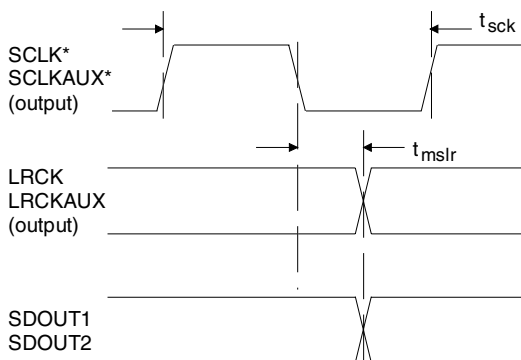
9. Digital filter characteristics.

10. Measurement bandwidth is 10 Hz to 3 Fs.

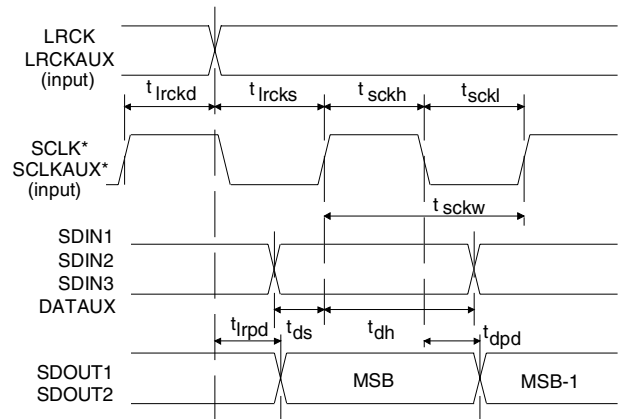
SWITCHING CHARACTERISTICS (Outputs loaded with 30 pF)

Parameter	Symbol	Min	Typ	Max	Units
Audio ADC's & DAC's Sample Rate	Fs	4	-	50	kHz
XTI Frequency (XTI = 256, 384, or 512 Fs)		1.024	-	26	MHz
XTI Pulse Width High XTI = 512 Fs XTI = 384 Fs XTI = 256 Fs		10	-	-	ns
		21	-	-	ns
		31	-	-	ns
XTI Pulse Width Low XTI = 512 Fs XTI = 384 Fs XTI = 256 Fs		10	-	-	ns
		21	-	-	ns
		31	-	-	ns
PLL Clock Recovery Frequency RX, XTI, LRCK, LRCKAUX		30	-	50	kHz
XTI Jitter Tolerance		-	500	-	ps
PDN Low Time (Note 11)		500	-	-	ns
SCLK Falling Edge to SDOUT Output Valid (DSCK = 0)	t _{dpd}	-	-	$\frac{1}{(384)Fs} + 20$	ns
LRCK edge to MSB valid	t _{lrpd}	-	-	40	ns
SDIN Setup Time Before SCLK Rising Edge (DSCK=0)	t _{ds}	-	-	25	ns
SDIN Hold Time After SCLK Rising Edge (DSCK=0)	t _{dh}	-	-	25	ns
Master Mode					
SCLK Period	t _{sck}	$\frac{1}{(256)Fs}$	-	-	ns
SCLK Falling to LRCK Edge (DSCK=0)	t _{mslr}	-	±10	-	ns
SCLK Duty Cycle		-	50	-	%
Slave Mode					
SCLK Period	t _{sckw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK High Time	t _{sckh}	40	-	-	ns
SCLK Low Time	t _{sckl}	40	-	-	ns
SCLK Rising to LRCK Edge (DSCK=0)	t _{lrckd}	20	-	-	ns
LRCK Edge to SCLK Rising (DSCK=0)	t _{lrcks}	40	-	-	ns

Notes: 11. After powering up the CS4226, $\overline{\text{PDN}}$ should be held low until the power supply is settled.



Audio Ports Master Mode Timing



*SCLK, SCLKAUX shown for DSCK = 0 and ASCK = 0.
SCLK & SCLKAUX inverted for DSCK = 1 and ASCK = 1, respectively.

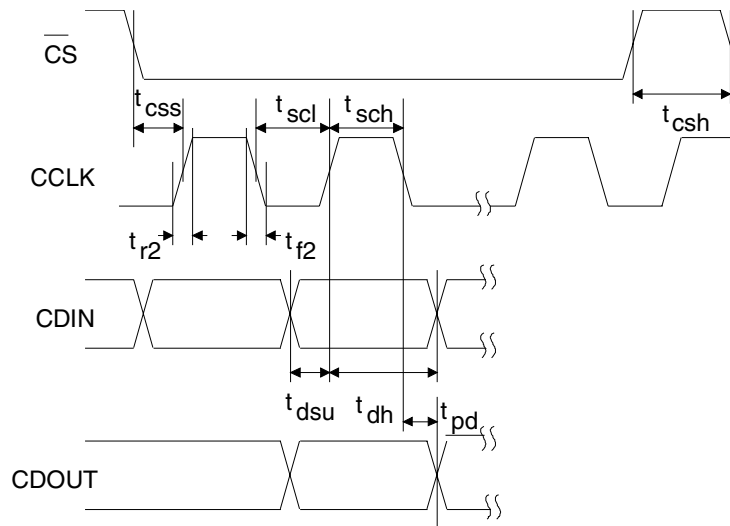
Audio Ports Slave Mode and Data I/O timing

SWITCHING CHARACTERISTICS - CONTROL PORT (Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
SPI Mode (SPI/I ² C = 0)				
CCLK Clock Frequency	f_{sck}	-	6	MHz
CS High Time Between Transmissions	t_{csh}	1.0		μ s
CS Falling to CCLK Edge	t_{css}	20		ns
CCLK Low Time	t_{scl}	66		ns
CCLK High Time	t_{sch}	66		ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40		ns
CCLK Rising to DATA Hold Time (Note 12)	t_{dh}	15		ns
CCLK Falling to CDOUT stable	t_{pd}		45	ns
Rise Time of CDOUT	t_{r1}		25	ns
Fall Time of CDOUT	t_{f1}		25	ns
Rise Time of CCLK and CDIN (Note 13)	t_{r2}		100	ns
Fall Time of CCLK and CDIN (Note 13)	t_{f2}		100	ns

Notes: 12. Data must be held for sufficient time to bridge the transition time of CCLK.

13. For $F_{SCK} < 1$ MHz



SWITCHING CHARACTERISTICS - CONTROL PORT (Inputs: logic 0 = DGND, logic 1 = VD+, C_L = 30 pF)

Parameter	Symbol	Min	Max	Units
I²C® Mode (SPI/I ² C = 1)				
SCL Clock Frequency	f _{scl}	-	100	kHz
Bus Free Time Between Transmissions	t _{buf}	4.7		μs
Start Condition Hold Time (prior to first clock pulse)	t _{hdst}	4.0		μs
Clock Low Time	t _{low}	4.7		μs
Clock High Time	t _{high}	4.0		μs
Setup Time for Repeated Start Condition	t _{sust}	4.7		μs
SDA Hold Time from SCL Falling (Note 14)	t _{hdd}	0		μs
SDA Setup Time to SCL Rising	t _{sud}	250		ns
Rise Time of Both SDA and SCL Lines	t _r		1	μs
Fall Time of Both SDA and SCL Lines	t _f		300	ns
Setup Time for Stop Condition	t _{susp}	4.7		μs

Notes: 14. Data must be held for sufficient time to bridge the 300 ns transition time of SCL

S/PDIF RECEIVER CHARACTERISTICS (RX1, RX2, RX3, RX4 pins only)

Parameter	Symbol	Min	Typ	Max	Units
Input Resistance	Z _N	-	10	-	kΩ
Input Voltage	V _{TH}	200	-	-	mVpp
Input Hysteresis	V _{HYST}	-	50	-	mV
Input Sample Frequency	F _S	30	-	50	kHz
CLKOUT Jitter (Note 15)		-	200	-	ps RMS
CLKOUT Duty Cycle (high time/cycle time) (Note 16)		40	50	60	%

Notes: 15. CLKOUT Jitter is for 256×F_S selected as output frequency measured from falling edge to falling edge. Jitter is greater for 384×F_S and 512×F_S as selected output frequency.

16. For CLKOUT frequency equal to 1×F_S, 384×F_S, and 512×F_S. See Master Clock Output section.

DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage (except RX1)	V _{IH}	2.8	-	(VD+)+0.3	V
Low-level Input Voltage (except RX1)	V _{IL}	-0.3	-	0.8	V
High-level Output Voltage at I _O = -2.0 mA	V _{OH}	(VD+)-1.0	-	-	V
Low-level Output Voltage at I _O = 2.0 mA	V _{OL}	-	-	0.4	V
Input Leakage Current (Digital Inputs)		-	-	10	μA
Output Leakage Current (High-Impedance Digital Outputs)		-	-	10	μA

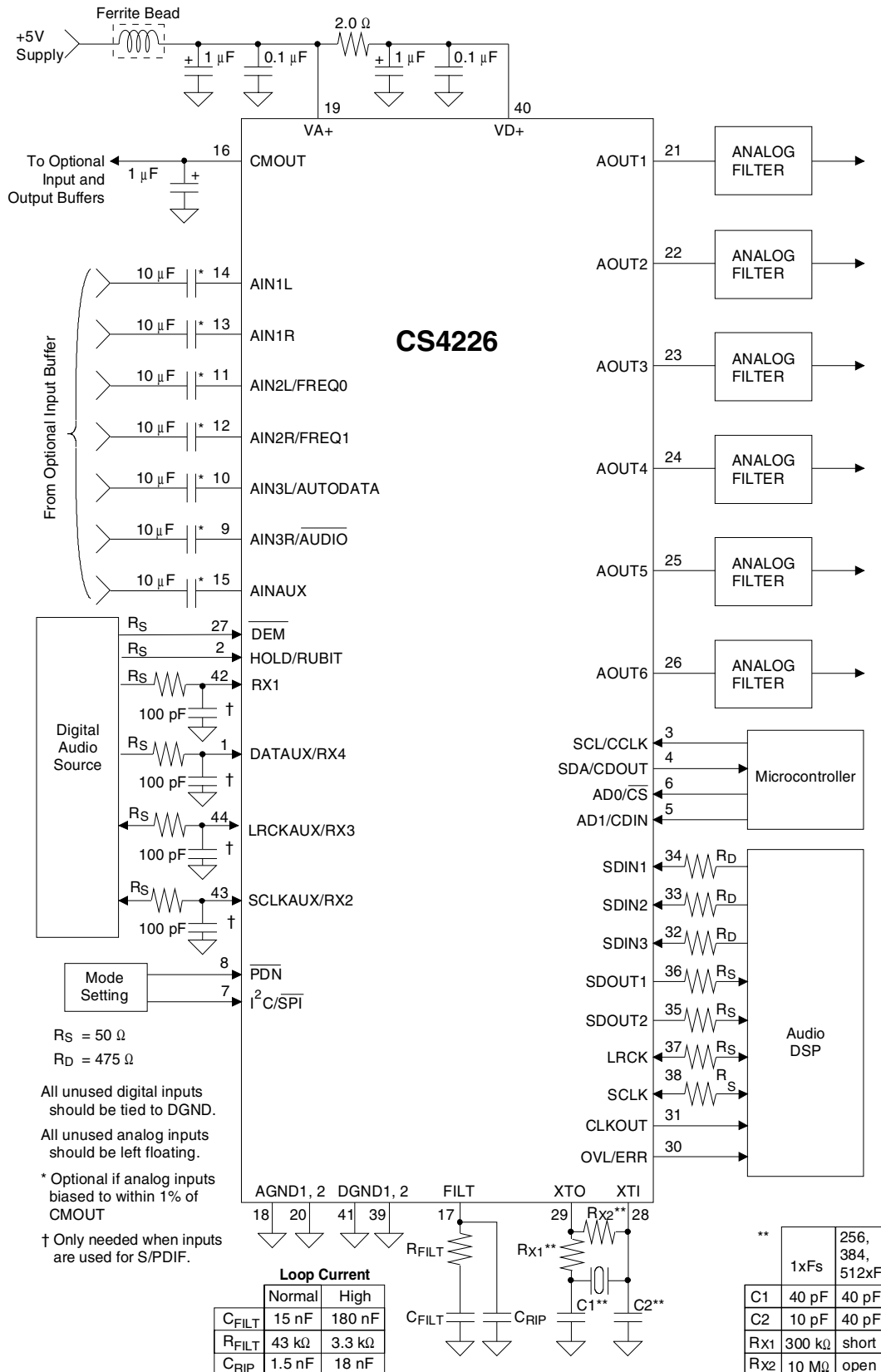


Figure 1. Recommended Connection Diagram

2 FUNCTIONAL DESCRIPTION

2.1 Overview

The CS4226 has 2 channels of 20-bit analog-to-digital conversion and 6 channels of 20-bit digital-to-analog conversion. A mono 20-bit ADC is also provided. All ADCs and DACs are delta-sigma converters. The stereo ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. The device also contains an S/PDIF receiver capable of receiving compressed AC-3/MPEG or uncompressed digital audio data.

Digital audio data for the DACs and from the ADCs is communicated over separate serial ports. This allows concurrent writing to and reading from the device. The CS4226 functions are controlled via a serial microcontroller interface. Figure 1 shows the recommended connection diagram for the CS4226.

2.2 Analog Inputs

2.2.1 Line Level Inputs

AIN1R, AIN1L, AIN2R, AIN2L, AIN3R, AIN3L and AINAUX are the line level input pins (See Figure 1). These pins are internally biased to the CMOUT voltage. A 10 μ F DC blocking capacitor placed in series with the input pins allows signals centered around 0V to be input to the CS4226. Figure 2 shows an optional dual op amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 Vrms to 1 Vrms. The CMOUT reference level is used to bias the op-amps to approximately one half the supply voltage. With this input circuit, the 10 μ F DC blocking caps in Figure 1 may be omitted. Any remaining DC offset will be removed by the internal high-pass filters.

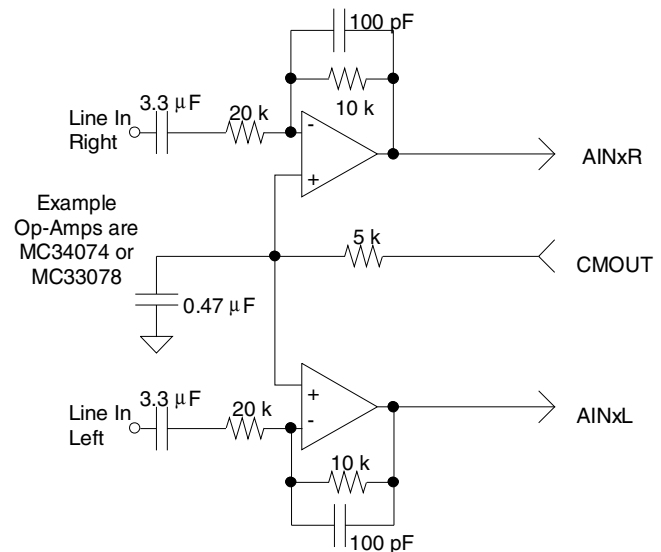


Figure 2. Optional Line Input Buffer

Selection of stereo the input pair (AIN1L/R, AIN2L/R or AIN3L/R) for the 20-bit ADC's is accomplished by setting the AIS1/0 bits (ADC analog input mux control), which are accessible in the ADC Control Byte. On-chip anti-aliasing filters follow the input mux providing anti-aliasing for all input channels.

The analog inputs may also be configured as differential inputs. This is enabled by setting bits AIS1/0=3. In the differential configuration, the left channel inputs reside on pins 10 and 11, and the right channel inputs reside on pins 12 and 13 as described in Table 2 below. In differential mode, the full scale input level is 2 Vrms.

Single-ended	Pin #	Differential Inputs
AIN3L	Pin 10	AINL+
AIN3R	Pin 9	unused
AIN2L	Pin 11	AINL-
AIN2R	Pin 12	AINR-
AIN1L	Pin 14	unused
AIN1R	Pin 13	AINR+

Table 2. Single-ended vs. Differential Input Pin Assignments

The analog signal is input to the mono ADC via the AINAUX pin.

Independent Muting of both the stereo ADC's and the mono ADC is possible through the ADC Control Byte with the MUTR, MUTL and MUTM bits.

2.2.2 Adjustable Input Gain

The signals from the line inputs are routed to a programmable gain circuit which provides up to 9 dB of gain in 3 dB steps. The gain is adjustable through the Input Control Byte. Right and left channel gain settings are controlled independently with the GNR1/0 and GNL1/0 bits. Level changes occur immediately on register updates. To minimize audible artifacts, level changes should be done with the channel muted.

The ADC Status Report Byte provides feedback of input level for each ADC channel. This register continuously monitors the ADC output and records the peak output level since the last register read. Reading this register causes it to reset to 0 and peak monitoring begins again.

2.2.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4226 may generate a small DC offset into the A/D converter. The CS4226 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multi-channel system.

The characteristics of this first-order high pass filter are outlined Table 3 below for an output

sample rate of 44.1 kHz. This filter response scales linearly with sample rate.

Frequency Response	-3 dB @ 3.4 Hz -0.13 dB @ 20 Hz
Phase Deviation	10 degrees @ 20 Hz
Passband Ripple	None

Table 3. High Pass Filter Characteristics

2.3 Analog Outputs

2.3.1 Line Level Outputs

The CS4226 contains an on-chip buffer amplifier producing single-ended outputs capable of driving 10 kΩ loads. Each output (A_{OUT} 1-6) will produce a nominal 2.83 V_{pp} (1 V_{rms}) output with a 2.3 volt quiescent voltage for a full scale digital input. The recommended off-chip analog filter is a 2nd order Butterworth with a -3 dB corner at F_s, see Figure 3. This filter provides out-of-band noise attenuation along with a gain of 2, providing a 2 V_{rms} output signal. A 3rd order Butterworth filter with a -3 dB corner at 0.75 F_s can be used if greater out of band noise filtering is desired. The CS4226 DAC interpolation filter is a linear phase design which has been pre-compensated for an external 2nd order Butterworth filter to provide a flat frequency response and linear phase response over the passband. If this filter is not used, small frequency response magnitude and phase errors will occur.

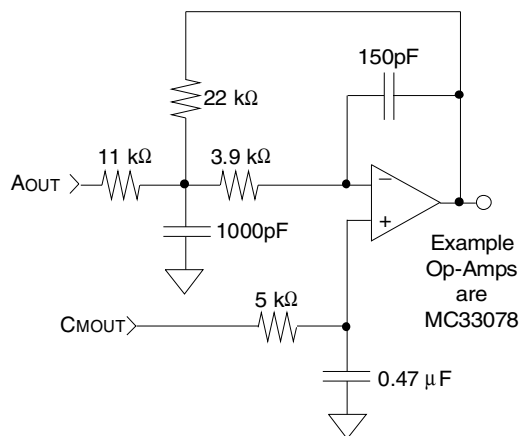
2.3.2 Output Level Attenuator

The DAC outputs are each routed through an attenuator which is adjustable in 1 dB steps. Output attenuation is available through the Output Attenuator Data Bytes. Level changes are implemented in the analog domain such that the noise is attenuated by the same amount as the signal, until the residual output noise is equal to the noise floor in the mute state; at this point attenuation is implemented

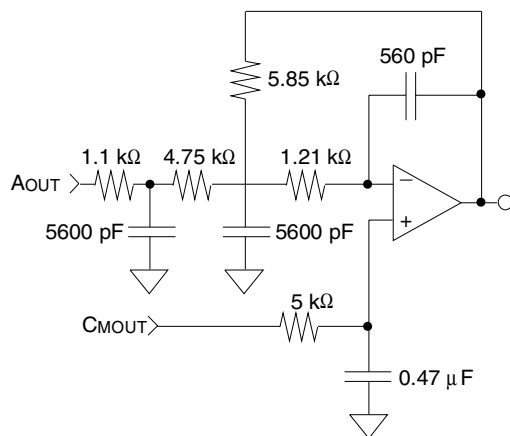
in the digital domain. The change from analog to digital attenuation occurs at -23 dB. Level changes only take effect on zero crossings to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out period between 512 and 1024 frames (11.6 ms to 23.2 ms at 44.1 kHz frame rate). There is a separate zero crossing detector for each channel. Each ACC bit (Acceptance bit) in the DAC Status Report Byte gives feedback on when a volume control change has taken effect. This bit goes high when a new setting is loaded and returns low when it has taken effect. Volume control

changes can be instantaneous by setting the Zero Crossing Disable (ZCD) bit in the DAC Control Byte to 1.

Each output can be independently muted via mute control bits, MUT6-1, in the DAC Control Byte. The mute also takes effect on a zero-crossing or after a timeout. In addition, the CS4226 has an optional mute on consecutive zeros feature, where all DAC outputs will mute if they receive between 512 and 1024 consecutive zeros (or -1 code) on all six channels. A single non-zero value will unmute the DAC outputs. This feature can be disabled with the MUTC bit in the DAC Control Byte. When using the internal PLL as the clock source, all DACs will instantly mute when the PLL detects an error.



2-Pole Butterworth Filter



3-Pole Butterworth Filter

Figure 3. Butterworth Filter Examples

2.4 Clock Generation

The master clock to operate the CS4226 may be generated by using the on-chip inverter and an external crystal, by using the on-chip PLL, or by using an external clock source. In all modes it is required to have SCLK and LRCK synchronous to the selected master clock.

2.4.1 Clock Source

The CS4226 requires a high frequency master clock to run the internal logic. The Clock Source bits, CS0/1/2 in Clock Mode Byte, determine the source of the clock. A high frequency crystal can be connected to XTI and XTO, or a high frequency clock can be applied to XTI. In both these cases, the internal PLL is disabled, and the VCO turns off. The externally supplied high frequency clock can be 256 Fs, 384 Fs or 512 Fs; this is set by the CI0/1 bits in the Clock Mode Byte. When using the on-chip crystal oscillator, external loading capacitors are required, see Figure 1. High frequency crystals (>8 MHz) should be parallel resonant, fundamental mode and designed for

20 pF loading (equivalent to 40 pF to ground on each leg).

Alternatively, the on-chip PLL may be used to generate the required high frequency clock. The PLL input clock is 1 Fs, and may be input from LRCKAUX, LRCK, or from XTI/XTO. In this last case, a 1 Fs clock may be input into XTI, or a 1 Fs crystal attached across XTI/XTO. When an external 1 Fs crystal is attached, extra components will be required, see Figure 1. The PLL will lock onto a new 1 Fs clock in about 90 ms. If the PLL input clock is removed, the VCO will drift to the low frequency end of its frequency range.

The PLL can also be used to lock to an S/PDIF data source on RX1, RX2, RX3, or RX4. Source selection is accomplished with the CS2/1/0 bits in the Clock Mode Byte. The PLL will lock to an S/PDIF source in about 90 ms.

Finally, the PLL has two filter loop current modes, normal and high current, that are selected via the LC bit in the Converter Control Byte. In the normal mode, the loop current is 25 μ A. In the high current mode, the loop current is 300 μ A. The high current mode allows the use of lower impedance filter components which minimizes the influences of board contamination. See the table in Figure 1 for filter component values in each mode.

2.4.2 Master Clock Output

CLKOUT is a master clock output provided to allow synchronization of external components. Available CLKOUT frequencies of 1 Fs, 256 Fs, 384 Fs, and 512 Fs, are selectable by the CO0/1 bits of the Clock Mode Byte.

Generation of CLKOUT for 384 Fs and 512 Fs is accomplished with an on chip clock multiplier and may contain clock jitter. The source of the 256 Fs CLKOUT is the output of the PLL or a divided down clock from the XTI/XTO input.

If 384 Fs is chosen as the input clock at XTI and 256 Fs is chosen as the output, CLKOUT will have approximately a 33% duty cycle. In all other cases CLKOUT will typically have a 50% duty cycle.

2.4.3 Synchronization

The DSP port and Auxiliary port must operate synchronously to the CS4226 clock source. The serial port will force a reset of the data paths in an attempt to resynchronize if non-synchronous data is input to the CS4226. It is advisable to mute the DACs when changing from one clock source to another to avoid the output of undesirable audio signals as the CS4226 resynchronizes.

2.5 Digital Interfaces

There are 3 digital audio interface ports: the audio DSP port, the auxiliary digital audio port, and the S/PDIF receiver. The serial data is represented in 2's complement format with the MSB-first in all formats.

2.5.1 Audio DSP Serial Interface Signals

The serial interface clock, SCLK, is used for transmitting and receiving audio data. The active edge of SCLK is chosen by setting the DSCK bit in the DSP Port Mode Byte. SCLK can be generated by the CS4226 (master mode) or it can be input from an external SCLK source (slave mode). Mode selection is set with the DMS1/0 bits in the DSP Port Mode Byte. The number of SCLK cycles in one system sample period is programmable to be 32, 48, 64, or 128 by setting the DCK1/0 bits in the DSP Port Mode Byte.

The Left/Right clock (LRCK) is used to indicate left and right data and the start of a new sample period. It may be output from the CS4226, or it may be generated from an external

controller. The frequency of LRCK must be equal to the system sample rate, F_s .

SDIN1, SDIN2, and SDIN3 are the data input pins, each of which drive a pair of DACs. SDOUT1 and SDOUT2 can carry the output data from the two 20-bit ADC's, the mono ADC, the auxiliary digital audio port, and the S/PDIF receiver. Selection depends on the IS1/0 bits in the ADC control byte. The audio DSP port may also be configured so that all 6 DAC's data is input on SDIN1, and all 3 ADC's data is output on SDOUT1. Table 4 outlines the serial interface ports.

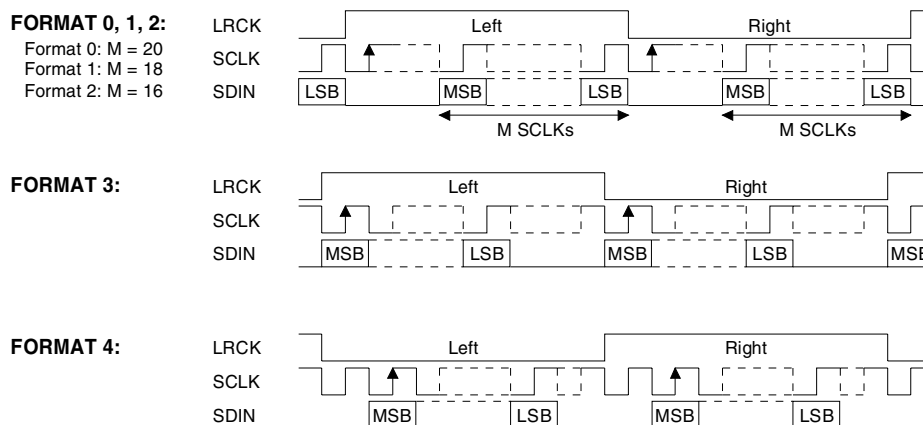
<i>DAC Inputs</i>		
SDIN1	left channel	DAC #1
	right channel	DAC #2
	single line	All 6 DAC channels
SDIN2	left channel	DAC #3
	right channel	DAC #4
SDIN3	left channel	DAC #5
	right channel	DAC #6

Table 4. DSP Serial Interface Ports

2.5.2 Audio DSP Serial Interface Formats

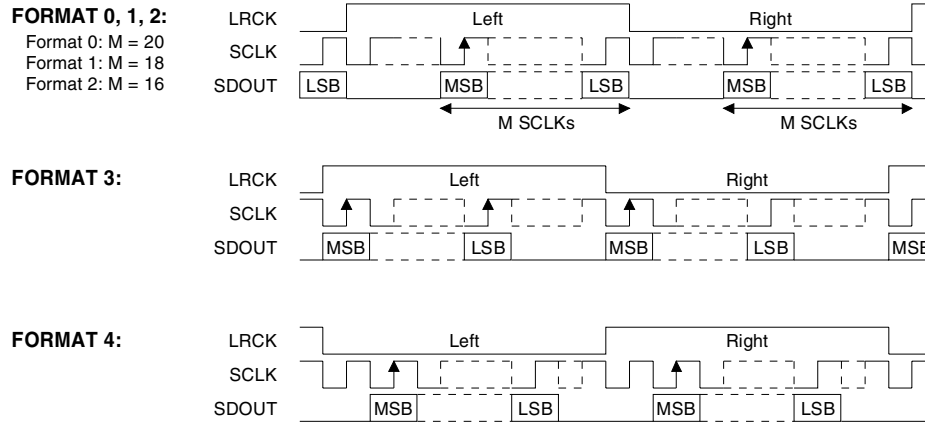
The audio DSP port supports 7 alternate formats, shown in Figures 4, 5, and 6. These formats are chosen through the DSP Port Mode Byte with the DDF2/1/0 bits.

Formats 5 and 6 are single line data modes where all DAC channels are combined onto a single input and all ADC channels are combined onto a single output. Format 6 is available in Master Mode only. See figure 6 for details.



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 4. Audio DSP and Auxiliary Port Data Input Formats



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 5. Audio DSP Port Data Output Formats

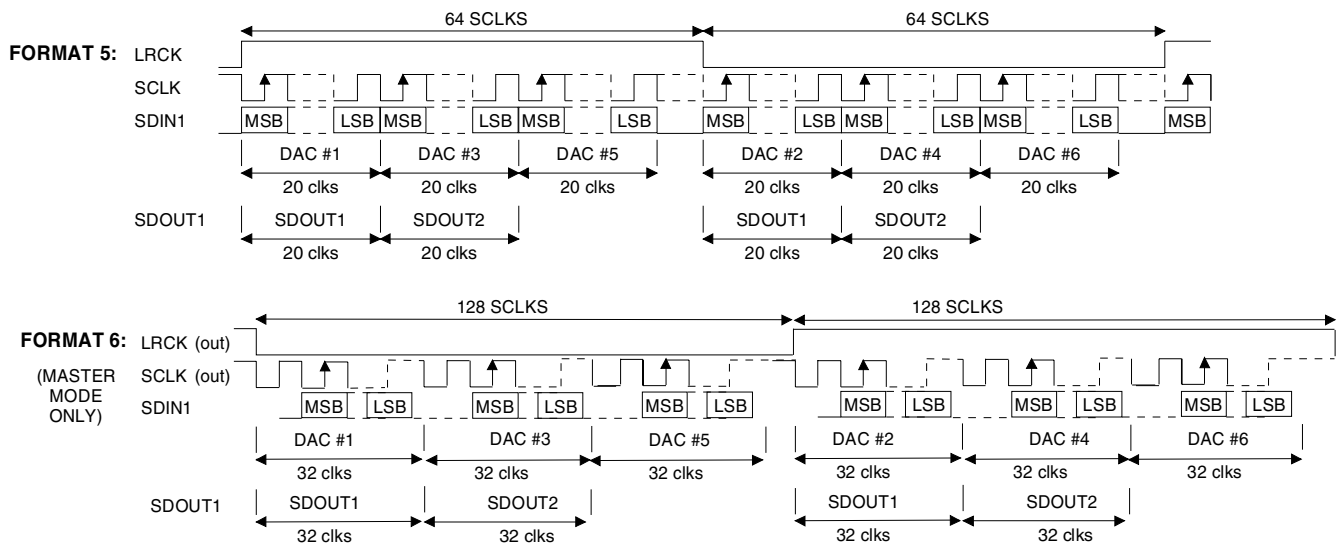


Figure 6. One data line modes

2.5.3 Auxiliary Audio Port Signals

The auxiliary port provides an alternate way to input digital audio signals into the CS4226, and allows the CS4226 to synchronize the system to an external digital audio source. This port consists of serial clock, data and left/right clock pins named, SCLKAUX, DATAUX and LRCKAUX. The Auxiliary Audio Port input is output on SDOUT1 when the IS bits are set to 1 or 2 in the ADC Control Byte. Additionally, setting IS to 2 routes the stereo ADC outputs to SDOUT2. There is approximately a two frame delay from DATAUX to SDOUT1. When the auxiliary port is used, the frequency of LRCKAUX must equal to the system sample rate, F_s , but no particular phase relationship is required.

De-emphasis and muting on error conditions can be performed on input data to the auxiliary audio port; this is controlled by the Auxiliary Port Control Byte.

2.5.4 Auxiliary Audio Port Formats

Data input on DATAUX is clocked into the part by SCLKAUX using the format selected in the Auxiliary Port Mode Byte. The auxiliary audio port supports the same 5 formats as the audio DSP port in multi-data line mode. LRCKAUX is used to indicate left and right data samples, and the start of a new sample period. SCLKAUX and LRCKAUX may be output from the CS4226, or they may be generated from an external source, as set by the AMS1/0 control bits in the Auxiliary Port Mode Byte.

2.5.5 S/PDIF Receiver

The CS4226 reconfigures its auxiliary digital audio port as an S/PDIF receiver if CS2/1/0 in the Clock Mode Byte are set to be 4, 5, 6, or 7. In this mode RX1, RX2, RX3, or RX4 can be chosen as the S/PDIF input source.

The PLL will lock to the requested data source and setting IS1/0 = 1 or 2 in the ADC Control Byte routes the recovered output to SDOUT1 (channel A to left, channel B to right). All 24 received data bits will pass through the part to SDOUT1 except when the serial port is configured with 32 SCLKs per frame or in Format 5. For these cases, the 16 or 20 MSBs respectively will be output.

The error flags are reported in the Receiver Status Byte. The LOCK bit indicates whether the PLL is locked to the incoming S/PDIF data. Parity, Biphase, or Validity errors (PAR=1, BIP=1 or V=1) will cause the last valid data sample to be held at the receiver input until the error condition no longer is present (see Hold section). Mute on extended hold can also be enabled through the Auxiliary Port Control Byte (see Hold section).

Other error flags include confidence, CONF, and cyclic redundancy check, CRC. The CONF flag occurs when the received data eye opening is less than half a bit period. This indicates that the quality of the transmission link is poor and does not meet the digital audio interface standards. The CRC flag is updated at the beginning of a channel status block and is only valid when the professional format of channel status data is received. This error indicates when the CS4226 calculated CRC value does not match the CRC byte of the received channel status block.

The OVL/ERR pin will go high to flag an error. It is a latched logical OR of the Parity, Biphase, Validity, and Lock error flags in the Receiver Status Byte which is reset at the end of each frame. However, Parity, Biphase, or Validity errors can be masked from the pin by clearing the PM, BM, and VM bits respectively, of the Input Control Byte.

The first four bytes of the Channel Status block for both channel A and B can be accessed in the Receiver Channel Status Bytes. When the CV bit is high, these bytes are being updated and may be invalid. Additionally, the audio/non-audio, AC-3/MPEG data stream indicator and sampling frequency channel status bits may be output to pins 9, 10, 11 and 12, respectively, see Table 5. This is accomplished by setting the CSP bit to 1 in the Auxiliary Status Output Byte. The FREQ0/1 channel status bit outputs are decoded from the sampling frequency channel status bits after first referencing channel status byte 0, bit 0 (PRO or consumer bit) which indicates the appropriate location of these bits in the channel status data stream.

The received user bit is output on the HOLD/RUBIT pin if the HPC bit in the AUX Port Control Byte is set to 1. It can be sampled with the rising or falling edge of LRCK if the audio DSP port is in Master Mode.

AUDIO	Pin 9	0 - Audio data 1 - Non-audio data
AUTODATA	Pin 10	0 - No preamble detected in last 4096 frames 1 - Preamble detected
FREQ0/1	Pin 11/12	00 - 44.1 kHz 01 - 48 kHz 10 - Reserved 11 - 32 kHz

Table 5. S/PDIF Receiver Status Outputs

2.5.6 AC-3/MPEG Auto Detection

For AC-3/MPEG applications, it is important to know whether the incoming S/PDIF data stream is digital audio or compressed AC-3/MPEG data. This information is typically conveyed by setting channel status bit 1 (audio/non-audio bit), but some AC-3/MPEG sources may not strictly adhere to this convention and the bit may not be properly set. The

CS4226 S/PDIF receiver has the capability to automatically detect whether the incoming data is a compressed AC-3/MPEG input. This is accomplished by looking for an AC-3/MPEG 96-bit sync code consisting of six 16-bit words. The 96-bit sync code consists of: 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, the AUTODATA indicator (pin 10) will go high. If no additional sync codes are detected within the next 4096 frames, the AUTODATA indicator pin will return low until another sync code is detected.

2.6 Control Port Signals

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS4226 as a slave device. The SPI mode is selected by setting the I²C/SPI pin low, and I²C is selected by setting the I²C/SPI pin high. The state of this pin is continuously monitored.

2.6.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4226 chip select signal, CCLK is the control port bit clock, (input into the CS4226 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller, and the chip address is 0010000. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 7 shows the control port timing in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and they must be 0010000. The eighth bit is a read/write indicator (R/W), which should be

low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. During writes, the CDOUT output stays in the high impedance state. It may be externally pulled high or low with a 47 kΩ resistor.

The CS4226 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive reads or writes. If INCR is set to a 1, then MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{\text{CS}}$ high) immediately after the MAP byte. The auto MAP increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{\text{CS}}$ low, send out the chip address and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

2.6.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 8. There is no $\overline{\text{CS}}$ pin. Pins AD0, AD1 form the partial chip address. The upper 5 bits of the 7 bit address field must be 00100. To communicate with a CS4226, the LSBs of the chip address field, which is the first byte sent to the CS4226, should match the settings of the AD1, AD0 pins. The eighth bit of the address bit is the R/W bit (high for a read, low for a write). The next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a write, the next byte is the data to be written to the register pointed to by the MAP. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. I²C bus is a registered trademark of Philips Semiconductors.

2.6.3 Control Port Bit Definitions

All registers can be written and read back, except the DAC Status Report Byte, ADC Status Report Byte, Receiver Status Byte, and the Receiver Channel Status Bytes, which are read only. See the bit definition tables for bit assignment information.

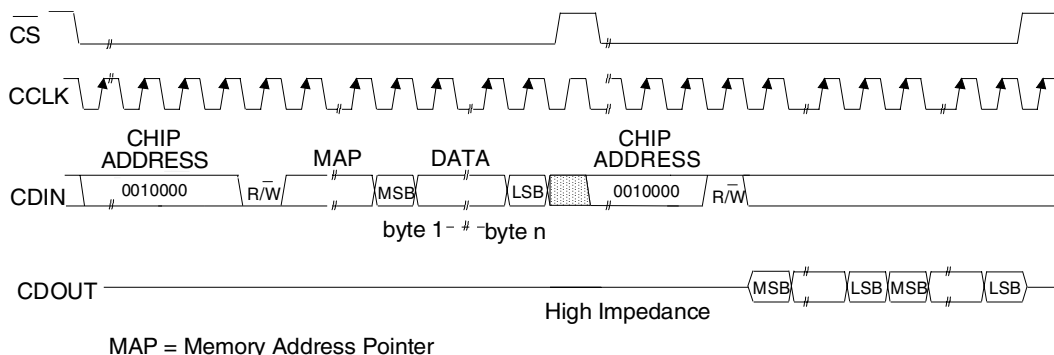


Figure 7. Control Port Timing, SPI mode

2.7 Power-up/Reset/Power Down Mode

Upon power up, the user should hold $\overline{\text{PDN}}=0$ until the system's power supply has stabilized. In this state, the control port is reset to its default settings. When $\overline{\text{PDN}}$ goes high, the device remains in a low power mode in which the control port is active, but CMOUT will not supply current. The desired settings should be loaded in while keeping the RS bit set to 1. Normal operation is achieved by setting the RS bit to zero in the Converter Control Byte. Once set to 0, the part powers up and an offset calibration occurs. This process lasts approximately 50 ms.

Reset/power down is achieved by lowering the $\overline{\text{PDN}}$ pin causing the part to enter power down. Once $\overline{\text{PDN}}$ goes high, the control port is functional and the desired settings should be loaded in while keeping the RS bit set to 1. The remainder of the chip remains in a low power reset state until the RS bit in the Converter Control Byte is set to 0.

The CS4226 will also enter a stand-by mode if the master clock source stops for approximately 10 μs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings when in stand-by mode.

2.8 DAC Calibration

Output offset voltage is minimized by an internal calibration cycle. A calibration will automat-

ically occur anytime the part comes out of reset, including the power-up reset, when the master clock source to the part changes by changing the CS or CI bits in the Clock Mode Byte or when the PLL goes out of lock and then re-locks.

The CS4226 can be re-calibrated whenever desired. A control bit, CAL, in the Converter Control Byte, is provided to initiate a calibration. The sequence is:

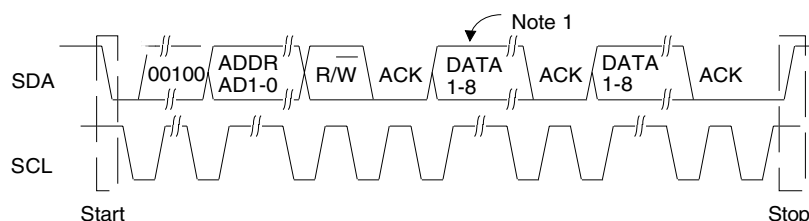
- 1) Set CAL to 1, the CS4226 sets CALP to 1 and begins to calibrate.
- 2) CALP will go to 0 when the calibration is completed.

Additional calibrations can be implemented by setting CAL to 0 and then to 1.

2.9 De-Emphasis

The S/PDIF receiver can be enabled to process 24 bits of received data (20 bits of audio data and four auxiliary bits) or process 20 bits of audio data (no auxiliary bits). Setting $\text{DEM24}=0$ in the Auxiliary Port Control Byte, will enable all 24 received data bits to be processed with de-emphasis when de-emphasis is enabled. When setting $\text{DEM24}=1$, the four auxiliary bits in the receiver data stream will pass through unchanged and only the 20 audio data bits will be processed.

The CS4226 is capable of digital de-emphasis for 32, 44.1, or 48 kHz sample rates. Implementation of digital de-emphasis requires re-



Note 1: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 8. Control Port Timing, I²C Mode

configuration of the digital filter to maintain the filter response shown in Figure 9 at multiple sample rates. The Auxiliary Port Control Byte selects the de-emphasis control method. De-emphasis may be enabled under hardware control, using the DEM pin (DEM2/1/0=4,5,6), by software control using the DEM bit (DEM2/1/0=0,1,2,3), or by the emphasis bits in the channel status data when the S/PDIF receiver is chosen as the clock source (DEM2/0/1=7). If no frequency information is present, the filter defaults to 44.1 kHz.

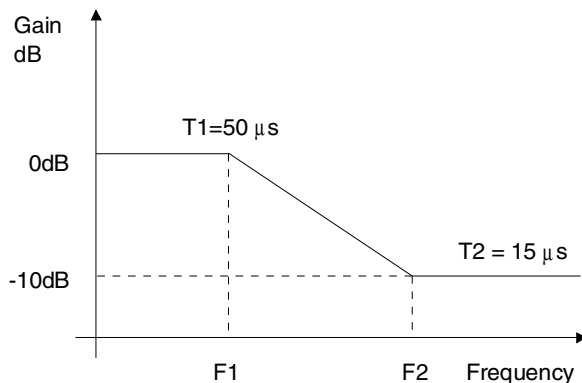


Figure 9. De-emphasis Curve

2.10 HOLD Function

If the digital audio source presents invalid data to the CS4226, the CS4226 may be configured to cause the last valid digital input sample to be held constant. Holding the previous output sample occurs when the user asserts the HOLD pin (HOLD=1) at any time during the stereo sample period, or if a parity, biphase, or validity error occurs when receiving S/PDIF data. Parity, biphase, and validity errors can be independently masked so that no hold occurs. This is done using the VM, PM, and BM bits in the Input Control Byte. During a HOLD condition, AUXPort (S/PDIF) input data is ignored.

DAC outputs can be automatically muted after an extended HOLD period (>15 samples) by setting the MOH (Mute On Hold) bit = 0 in the Auxiliary Port Control Byte. DACs will not be automatically muted when MOH=1. When the S/PDIF error condition is removed or the HOLD pin is de-asserted (HOLD=0), the DAC outputs will return to one of two different states controlled by the UMV (Unmute on Valid Data) bit in the Auxiliary Port Control Byte. When UMV=0, the DAC outputs will unmute when the error is removed. When UMV=1, the DACs must be unmuted in the DAC Control Byte after the error is removed. This allows the user to unmute the DAC after the invalid data has passed through the DSP.

2.11 Power Supply, Layout, and Grounding

As with any high resolution converter, the CS4226 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangement with VA connected to a clean +5V supply. VD should be derived from VA through a 2 ohm resistor. VD should not be used to power additional circuitry. Pins 18, 20, 39 and 41, AGND and DGND should be connected together at the CS4226. DGND for the CS4226 should not be confused with the ground for the digital section of the system. The CS4226 should be positioned over the analog ground plane near the digital/analog ground plane split. The analog and digital ground planes must be connected elsewhere in the system. The CS4226 evaluation board, CDB4226, demonstrates this layout technique. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors for VA, VD, and CMOUT should be located as close to the device package as possible. See Crystal's

Application Note AN018: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, and the CDB4226 evaluation board data sheet for recommended layout of the decoupling components.

The CS4226 will mute the analog outputs and enter the Power Down Mode if the supply drops below approximately 4V.

2.12 ADC and DAC Filter Response Plots

Figures 10 through 15 show the overall frequency response, passband ripple and transition band for the CS4226 ADC's and DAC's.

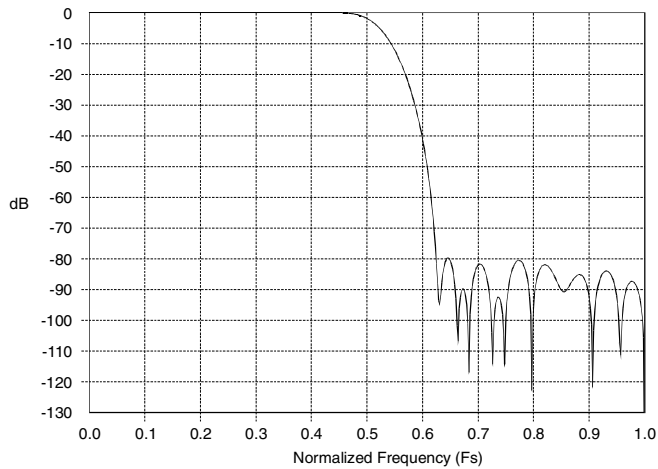


Figure 10. 20-bit ADC Filter Response

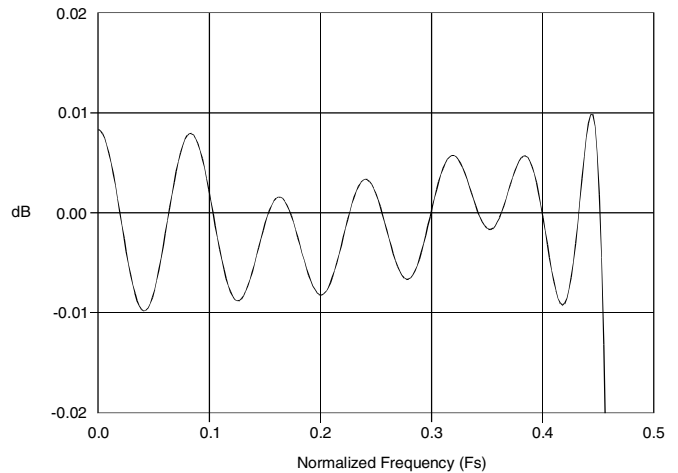


Figure 11. 20-bit ADC Passband Ripple

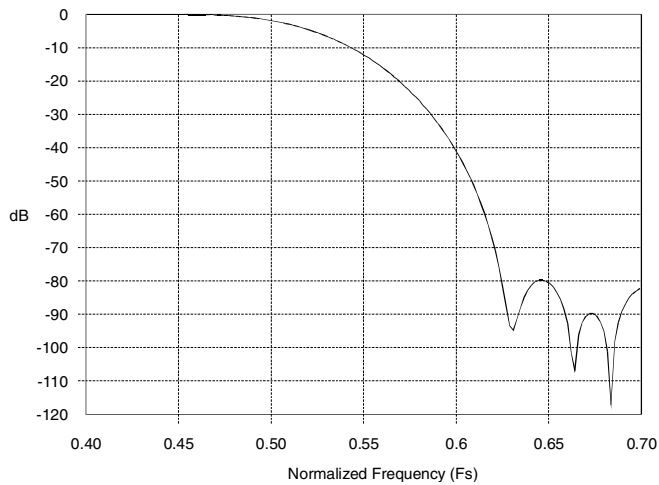


Figure 12. 20-bit ADC Transition Band

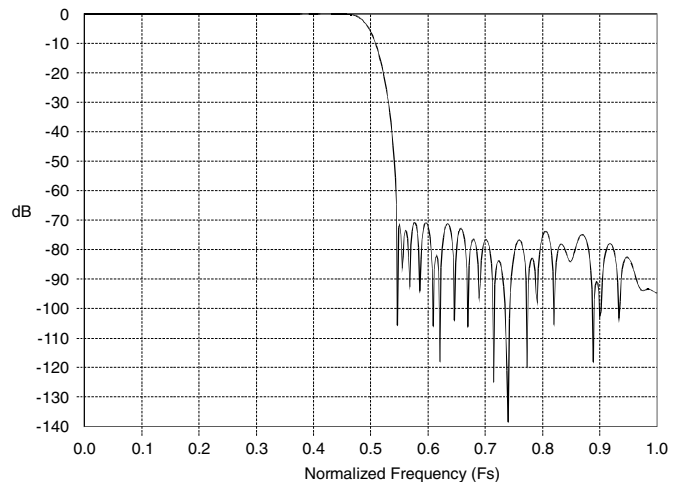


Figure 13. DAC Frequency Response

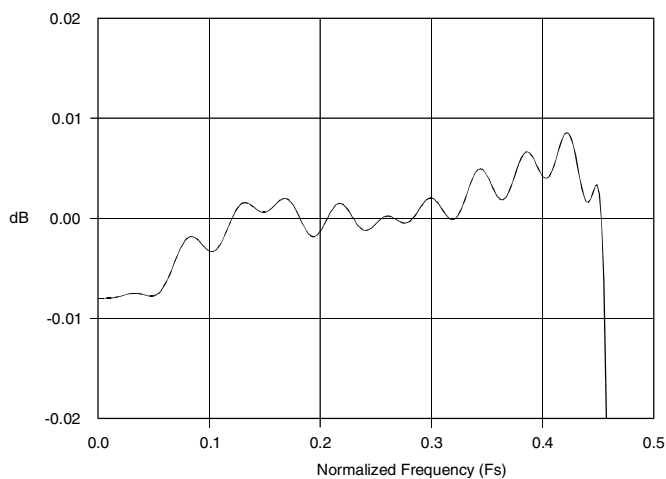


Figure 14. DAC Passband Ripple

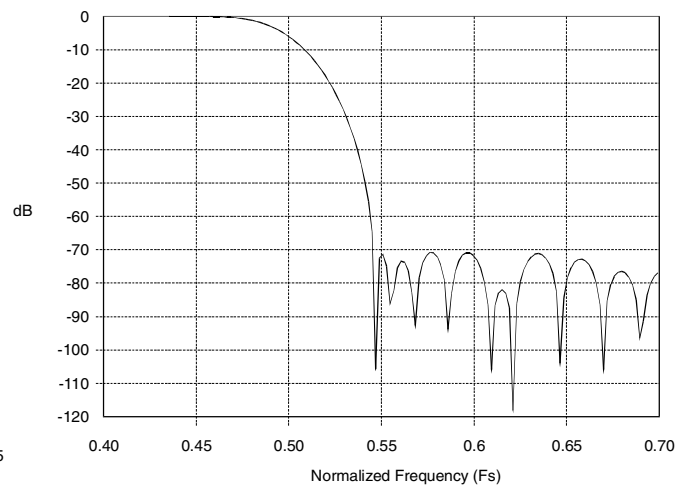


Figure 15. DAC Transition Band

3 REGISTER DESCRIPTION

3.1 Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	MAP4	MAP3	MAP2	MAP1	MAP0

MAP4-MAP0 Register Pointer

INCR Auto Increment Control Bit
 0 - No auto increment
 1 - Auto increment on

This register defaults to 01h.

3.2 Reserved Byte (00h)

This byte is reserved for internal use and must be set to 00h for normal operation.

This register defaults to 00h.

3.3 Clock Mode Byte (01h)

B7	B6	B5	B4	B3	B2	B1	B0
0	CO1	CO0	CI1	CI0	CS2	CS1	CS0

CS2-CS0 Sets the source of the master clock.
 0 - Crystal Oscillator or XTI at high frequency (PLL disabled)
 1 - PLL driven by LRCKAUX at 1 Fs
 2 - PLL driven by LRCK at 1 Fs
 3 - PLL driven by XTI at 1 Fs
 4 - PLL driven by RX1 data. This changes AUX port to S/PDIF port.
 5 - PLL driven by RX2 data. This changes AUX port to S/PDIF port.
 6 - PLL driven by RX3 data. This changes AUX port to S/PDIF port.
 7 - PLL driven by RX4 data. This changes AUX port to S/PDIF port.

CI1-CI0 Determines frequency of XTI when PLL is disabled (not used if CS ≠ 0)
 0 - 256 Fs
 1 - 384 Fs
 2 - 512 Fs
 3 - not used

CO1-CO0 Sets CLKOUT frequency
 0 - 256 Fs
 1 - 384 Fs
 2 - 512 Fs
 3 - 1 Fs

This register defaults to 01h.

NOTE: If the sample rate on an input pin changes while using the PLL with RX1, RX2, RX3 or RX4, the PLL will not resynchronize to the new sample rate. You must either change input pins or change the Clock Mode Byte to something else and then change it back to the correct value. This will cause the PLL to resync.

3.4 Converter Control Byte (02h)

B7	B6	B5	B4	B3	B2	B1	B0
CALP	CLKE	DU	AUTO	LC	0	CAL	RS

RS	Chip reset (Do not clear this bit until all registers have been configured as desired) 0 - No Reset 1 - Reset						
CAL	Calibration control bit 0 - Normal operation 1 - Rising edge initiates calibration						
LC	Loop Current 0 - Normal Mode, 25 μ A PLL loop current (See Figure 1 for filter component values) 1 - High Current Mode, 300 μ A PLL loop current (See Figure 1 for filter component values)						

The following bits are read only:

AUTO	AC3 and MPEG Automatic Detection 0 - No AC3/MPEG Detected 1 - AC3/MPEG detected on RX/AUX						
DU	Shows selected De-Emphasis setting used by DAC's 0 - Normal Flat DAC frequency response 1 - De-Emphasis selected						
CLKE	Clocking system status 0 - No errors 1 - PLL is not locked, crystal is not oscillating, or requesting clock change in progress						
CALP	Calibration status 1 - Calibration in progress 0 - Calibration done. This register defaults to 01h						

This register defaults to 01h

NOTE: The AC3 and MPEG detection for the AUTO bit does not look at the channel status bits. This bit is determined by looking for the AC3/MPEG header in the data stream. See the "AC3/MPEG Auto Detection" section earlier in the data sheet for more details.

3.5 DAC Control Byte (03h)

B7	B6	B5	B4	B3	B2	B1	B0
ZCD	MUTC	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1

MUT6-MUT1	Mute control bits 0 - Normal output level 1 - Selected DAC output muted						
MUTC	Controls mute on consecutive zeros function 0 - 512 consecutive zeros will mute DAC 1 - DAC output will not mute on zeros						
ZCD	Zero crossing disable 0 - DAC mutes and volume control changes occur on zero-crossings. 1 - DAC mutes and volume control changes occur immediately.						

This register defaults to 3Fh.

3.6 Output Attenuator Data Byte (04h, 05h, 06h, 07h, 08h, 09h)

B7	B6	B5	B4	B3	B2	B1	B0
0	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT6-ATT0 Sets attenuator level
 0 - No attenuation
 127 - 127 dB attenuation
 ATT0 represents 1.0 dB of attenuation

This register defaults to 7Fh.

3.7 DAC Status Report Byte (Read Only) (0Ah)

B7	B6	B5	B4	B3	B2	B1	B0
0	-	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1

ACC6-ACC1 Acceptance Bit
 1 - New setting is waiting for zero-crossing to be accepted.
 0 - ATT6-ATT0 has been accepted.

This register is read-only.

3.8 ADC Control Byte (0Bh)

B7	B6	B5	B4	B3	B2	B1	B0
IS1	IS0	0	AIS1	AIS0	MUTM	MUTR	MUTL

MUTL, MUTR, MUTM - Left, right and mono channel mute control
 0 - Normal output level
 1 - Selected ADC output muted

AIS1-AIS0 ADC analog input mux control
 0 - Selects stereo pair 1
 1 - Selects stereo pair 2
 2 - Selects stereo pair 3
 3 - Differential Input

IS1-IS0 Input mux selection
 0 - Stereo ADC output to SDOUT1, Mono ADC output to SDOUT2
 1 - Auxiliary Digital Input Port or S/PDIF Receiver to SDOUT1, Mono ADC output to SDOUT2
 2 - Auxiliary Digital Input Port or S/PDIF Receiver to SDOUT1, Stereo ADC output to SDOUT2
 3 - Not used.

This register defaults to 00h.

3.9 Input Control Byte (0Ch)

B7	B6	B5	B4	B3	B2	B1	B0
OVRM	VM	BM	PM	GNR1	GNR0	GNL1	GNL0

OVRM	ADC Overflow Mask 0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold 1- No Masking
VM	Validity Error Mask 0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold 1- No Masking
BM	Biphase Error Mask 0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold 1- No Masking
PM	Parity Error Mask 0- Error condition is masked at OLV/ERR pin and no DAC muting on extended hold 1- No Masking
GNL1-GNL0	Sets left input gain 0 - 0 dB 1 - 3 dB 2 - 6 dB 3 - 9 dB
GNR1-GNR0	Sets right input gain 0 - 0 dB 1 - 3 dB 2 - 6 dB 3 - 9 dB

This register defaults to 00h.

3.10 ADC Status Report Byte (Read Only) (0Dh)

B7	B6	B5	B4	B3	B2	B1	B0
LVM1	LVM0	LVR2	LVR1	LVR0	LVL2	LVL1	LVL0

LVL2-LVL0, LVR2-0	Left and Right ADC output level 0 - Normal output levels 1 - -6 dB level 2 - -5 dB level 3 - -4 dB level 4 - -3 dB level 5 - -2 dB level 6 - -1 dB level 7 - Clipping
LVL1-LVL0	Mono ADC output level 0 - Normal output level 1 - -6 dB level 2 - -3 dB level 3 - Clipping

These bits are 'sticky'. They constantly monitor the ADC output for the peak levels and hold the maximum output. They are reset to 0 when read.

This register is read only.

3.11 DSP Port Mode Byte (0Eh)

B7	B6	B5	B4	B3	B2	B1	B0
DCK1	DCK0	DMS1	DMS0	DSCK	DDF2	DDF1	DDF0

DDF2-DDF0	Data format 0 - Right justified, 20-bit 1 - Right justified, 18-bit 2 - Right justified, 16-bit 3 - Left justified, 20-bit in / 24-bit out 4 - I ² S compatible, 20-bit in / 24-bit out 5 - One Data Line Mode (Figure 6) 6 - One Data Line (Master Mode only, Figure 6) 7 - Not used
DSCK	Set the polarity of clocking data 0 - Data clocked in on rising edge of SCLK, out on falling edge of SCLK 1 - Data clocked in on falling edge of SCLK, out on rising edge of SCLK
DMS1-DMS0	Sets the mode of the port 0 - Slave 1 - Master Burst - SCLKs are gated 128 fs clocks 2 - Master Non-Burst - SCLKs are evenly distributed (No 48 fs SCLK) 3 - not used - default to Slave
DCK1-DCK0 *	Set number of bit clocks per Fs period 0 - 128 1 - 48 - Master Burst or Slave mode only 2 - 32 - All formats will default to 16 bits 3 - 64

This register defaults to 00h.

* DCK1-DCK0 are ignored in formats 5 and 6.

3.12 Auxiliary Port Mode Byte (0Fh)

B7	B6	B5	B4	B3	B2	B1	B0
ACK1	ACK0	AMS1	AMS0	ASCK	ADF2	ADF1	ADF0

This byte is not available when the receiver is functioning.

ADF2-ADF0	Data format 0 - Right justified, 20-bit data 1 - Right justified, 18-bit data 2 - Right justified, 16-bit data 3 - Left justified, 20-bit 4 - I ² S compatible, 20-bit 5 - Not used 6 - Not used 7 - Not used
ASCK	Sets the polarity of clocking data 0 - Data clocked in on rising edge of SCLKAUX 1 - Data clocked in on falling edge of SCLKAUX
AMS1-AMS0	Sets the mode of the port. 0 - Slave 1 - Master Burst - SCLKAUXs are gated 128 fs clocks 2 - Master Non-Burst - SCLKAUXs are evenly distributed in LRCKAUX frame 3 - Not used - default to slave
ACK1-ACK0	Set number of bit clocks per Fs period. 0 - 128 1 - 48 - Master Burst or Slave mode only 2 - 32 - All input formats will default to 16 bits. 3 - 64

This register defaults to 00h.

3.13 Auxiliary Port Control Byte (10h)

B7	B6	B5	B4	B3	B2	B1	B0
CSP	HPC	UMV	MOH	DEM24	DEM2	DEM1	DEM0

DEM 2-0	Selects de-emphasis response/source 0 - De-emphasis off 1 - De-emphasis on 32 kHz 2 - De-emphasis on 44.1 kHz 3 - De-emphasis on 48 kHz 4 - De-emphasis pin 32 kHz 5 - De-emphasis pin 44.1 kHz 6 - De-emphasis pin 48 kHz 7 - S/PDIF receiver channel status bits
DEM24	Process AUX data LSBs 0 - All received data bits (24 max) are processed 1 - Top 20 bits processed with De-emphasis filter. 4 AUX LSBs are passed unchanged.
MOH	Mute On Hold 0 - Extended Hold (16 frames) mutes DAC outputs 1 - DACs not muted
UMV	Unmute on Valid Data 0 - DACs unmute when ERROR is removed 1 - DACs must be unmuted in DAC control byte after ERROR is removed.
HPC	HOLD/RUBIT Pin Control 0 - HOLD/RUBIT is an input (HOLD) 1 - HOLD/RUBIT is an output (RUBIT)
CSP	Channel Status output to pins. 0 - Analog inputs to pins. AIN2R, AIN2L, AIN3R, AIN3L 1 - Channel status to pins. (This forces AIS1/0=0)

This register defaults to 00h.

3.14 Receiver Status Byte (Read Only) (11h)

B7	B6	B5	B4	B3	B2	B1	B0
CV	0	CRC	LOCK	V	CONF	BIP	PAR

PAR	Parity bit 0 - No error 1 - Error
BIP	Biphase bit 0 - No error 1 - Error
CONF	Confidence bit 0 - No error 1 - Error
V	Validity bit 0 - No error 1 - Error
LOCK	PLL lock bit 0 - PLL locked 1 - Out of lock
CRC	Cyclic Redundancy check bit 0 - No error 1 - Error on either channel
CV	Channel status validity 0 - Valid 1 - Not valid, data is updating

This register is read only.

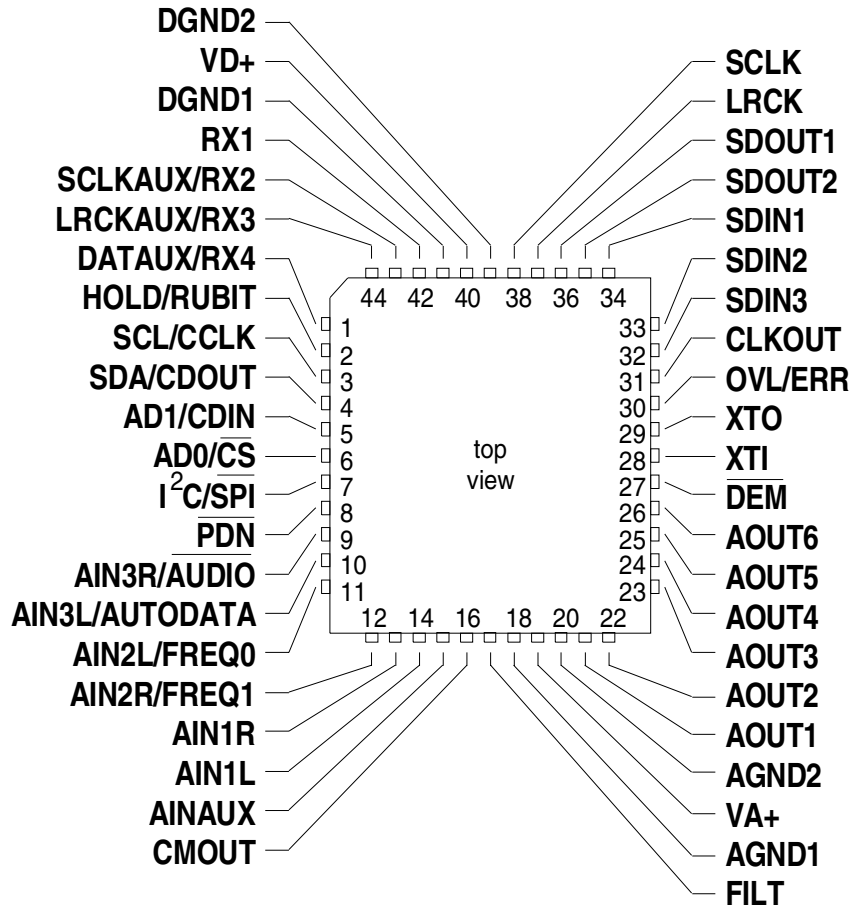
3.15 Receiver Channel Status Byte (Read Only) (12h, 13h, 14h, 15h, 16h, 17h, 18h, 19h)

B7	B6	B5	B4	B3	B2	B1	B0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

Byte 12h Channel A Status Byte 1
 Byte 13h Channel A Status Byte 2
 Byte 14h Channel A Status Byte 3
 Byte 15h Channel A Status Byte 4
 Byte 16h Channel B Status Byte 1
 Byte 17h Channel B Status Byte 2
 Byte 18h Channel B Status Byte 3
 Byte 19h Channel B Status Byte 4

Bit definition changes depending upon PRO bit setting. When CV = 1, these bits are updating and may be invalid.

4 PIN DESCRIPTION



Power Supply

VA+ - Analog Power Input, PIN 19.

+5V analog supply.

AGND1, AGND2 - Analog Ground, PINS 18, 20.

Analog grounds.

VD+ - Digital Power Input, PIN 40.

+ 5V digital supply.

DGND1, DGND2 - Digital Ground, PINS 41, 39.

Digital grounds.

Analog Inputs

AIN1L, AIN1R - Left and Right Channel Mux Input 1, PINS 14, 13.

Analog signal input connections for the right and left channels for multiplexer input 1.

AIN2L/FREQ0, AIN2R/FREQ1 - Left & Right Channel Mux Input 2/Channel Status Freq. Bits, PINS 11, 12.

Analog signal input connections for the right and left channels for multiplexer input 2. When CSP = 1, these pins are configured as channel status outputs indicating the sampling frequency.

AIN3L/AUTODATA, AIN3R/AUDIO - Left & Right Channel Mux Input 3/AC3 and MPEG Detect Output, PINS 10, 9.

Analog signal input connections for the right and left channels for multiplexer input 3. When CSP = 1, AIN3L is configured as an output indicating the presence of an AC-3 or MPEG data stream at the RX input and AIN3R is configured as a channel status output indicating audio/non-audio data at the RX input.

AINAUX - Auxiliary Line Level Input, PIN 15.

Analog signal input for the mono A/D converter.

Analog Outputs

AOUT1, AOUT2, AOUT3, AOUT4, AOUT5, AOUT6 - Audio Outputs, PINS 21 - 26.

The analog outputs from the 6 D/A converters. Each output can be independently controlled for output amplitude.

CMOUT - Common Mode Output, PIN 16.

This common mode voltage output may be used for level shifting when DC coupling is desired. The load on CMOUT must be DC only, with an impedance of not less than 50 k Ω . CMOUT should be bypassed with a 1.0 μ F to AGND.

Digital Audio Interface Signals

SDIN1 - Serial Data Input 1, PIN 34.

Digital audio data for the DACs 1 and 2 is presented to the CS4226 on this pin. This pin is also used for one-line data input modes.

SDIN2 - Serial Data Input 2, PIN 33.

Digital audio data for the DACs 3 and 4 is presented to the CS4226 on this pin.

SDIN3 - Serial Data Input 3, PIN 32.

Digital audio data for the DACs 5 and 6 is presented to the CS4226 on this pin.

SDOUT1- Serial Data Output 1, PIN36.

Digital audio data from the 20-bit stereo audio ADCs is output from this pin. When IS = 1 or 2, DATAUX or the S/PDIF receiver is output on SDOUT1. This pin is also used for one line data output modes.

SDOUT2 - Serial Data Output 2, PIN 35.

Digital audio data from the mono audio ADC is output from this pin. When IS = 2, the stereo audio ADC's are output from this pin

SCLK - Serial Port Clock I/O, PIN 38.

SCLK clocks digital audio data into the DACs via SDIN1/2/3, and clocks data out of the ADCs on SDOOUT1/2. Active clock edge depends on the DSCK bit.

LRCK - Left/Right Select Signal I/O, PIN 37.

The Left/Right select signal. This signal has a frequency equal to the sample rate. The relationship of LRCK to the left and right channel data depends on the selected format.

DEM - De-emphasis Control, PIN 27.

When low, DEM controls the activation of the standard 50/15 μ s de-emphasis filter for either 32, 44.1, or 48 kHz sample rates. This pin is enabled by the DEM2-0 bits in the Auxiliary Port Control Byte.

OVL/ERR - Overload Indicator, PIN 30.

This pin goes high if either of the stereo audio ADCs or the mono ADC is clipping. If the S/PDIF receiver is chosen as the clock source (CS = 4, 5, 6, 7), then the pin also goes high if there is an error in the Receiver Status Byte. Error and overloading can be masked using bits in the Input Control Byte.

Auxiliary Digital Audio and S/PDIF Receiver Signals**RX1 - Receiver Channel 1, PIN 42.**

This pin is a dedicated S/PDIF input channel configured as the clock source for the device via the CS2-0 bits.

DATAUX/RX4 - Auxiliary Data Input / Receiver Channel 4, PIN 1.

DATAUX is the auxiliary audio data input line, usually connected to an external digital audio source. As RX4, this pin is configured as S/PDIF input channel 4 via the control port.

LRCKAUX/RX3 - Auxiliary Word Clock Input or Output / Receiver Channel 3, PIN 44.

In auxiliary slave mode, LRCKAUX is a word clock (at F_s) from an external digital audio source. LRCKAUX can be used as the clock reference for the internal PLL. In auxiliary master mode, LRCKAUX is a word clock output (at F_s) to clock an external digital audio source. As RX3, this pin is configured as S/PDIF input channel 3 via the control port.

SCLKAUX/RX2 - Auxiliary Bit Clock Input or Output / Receiver Channel 2, PIN 43.

In auxiliary slave mode, SCLKAUX is the serial data bit clock from an external digital audio source, used to clock in data on DATAUX. In auxiliary master mode, SCLKAUX is a serial data bit clock output. As RX2, this pin is configured as S/PDIF input channel 2 via the control port.

HOLD/RUBIT - S/PDIF Received User Bit / HOLD Control, PIN 2.

When the S/PDIF receiver is chosen as the clock source (CS = 4, 5, 6 and HPC = 1), then this pin outputs the received user bit. When HPC = 0, this pin is sampled on the active edge of SCLKAUX. If it is high any time during the frame, DATAUX data is ignored and the previous "good" sample is output to the serial output port.

Control Port Signals

I²C/SPI - Control Port Format, PIN 7.

Setting this pin high configures the control port for the I²C interface; a low state configures the control port for the SPI interface. The state of this pin sets the function of the control port input/output pins.

SCL/CCLK - Serial Control Interface Clock, PIN 3.

SCL/CCLK is the serial control interface clock, and is used to clock control bits into and out of the CS4226.

AD0/ $\overline{\text{CS}}$ - Address Bit / Control Port Chip Select, PIN 6.

In I²C mode, AD0 is a chip address bit. In SPI software control mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4226.

AD1/CDIN - Address Bit / Serial Control Data In, PIN 5.

In I²C mode, AD1 is a chip address bit. In SPI software control mode, CDIN is the input data line for the control port interface.

SDA/CDOUT - Serial Control Data Out, PIN 4.

In I²C mode, SDA is the control data I/O line. In SPI software control mode, CDOUT is the output data from the control port interface on the CS4226.

Clock and Crystal Pins

XTI, XTO - Crystal connections, PIN 28, 29.

Input and output connections for the crystal which may be used to operate the CS4226. Alternatively, a clock may be input into XTI.

CLKOUT - Master Clock Output, PIN 31.

CLKOUT allows external circuits to be synchronized to the CS4226. Alternate output frequencies are selectable by the control port.

Miscellaneous Pins

FILT - PLL Loop Filter Pin, PIN 15.

A capacitor, C_{FILT} , in series with a resistor, R_{FILT} , should be connected from FILT to AGND. Additionally a capacitor, C_{RIP} , should be placed in parallel with C_{FILT} and R_{FILT} . See Figure 1 for recommended component values.

$\overline{\text{PDN}}$ - Powerdown Pin, PIN 8.

When low, the CS4226 enters a low power mode and all internal states are reset, including the control port. When high, the control port becomes operational and the RS bit must be cleared before normal operation will occur.

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES 17-1991 Annex A.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the RMS analog output level with 1 kHz full scale digital input to the RMS analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

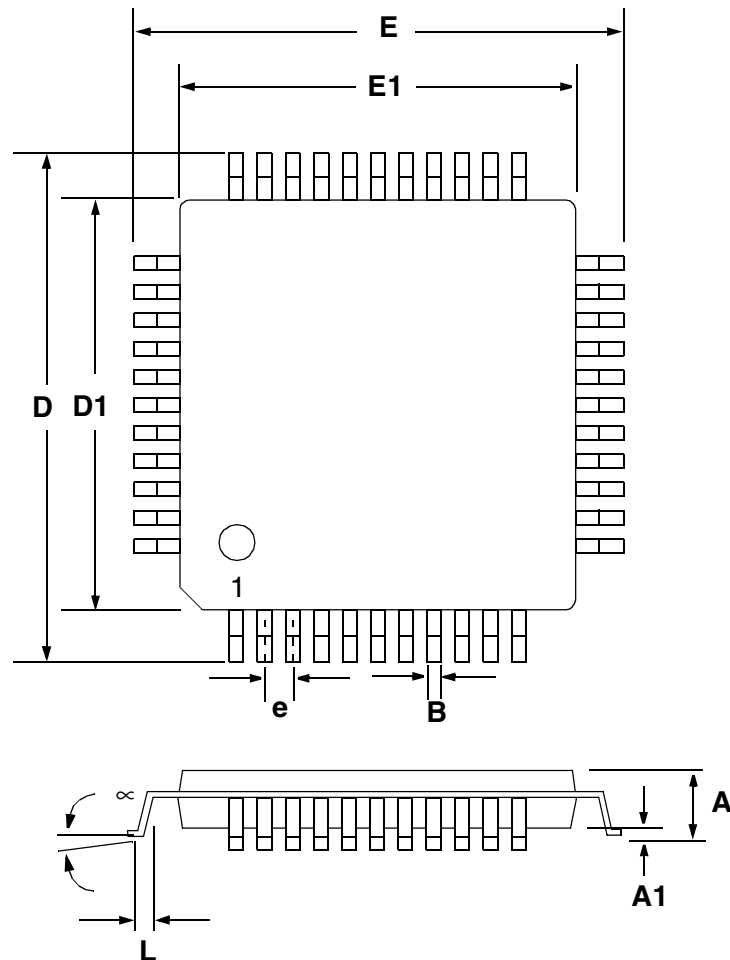
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

6 PACKAGE DIMENSIONS

44L TQFP PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.000	0.065	0.00	1.60
A1	0.002	0.006	0.05	0.15
B	0.012	0.018	0.30	0.45
D	0.478	0.502	11.70	12.30
D1	0.404	0.412	9.90	10.10
E	0.478	0.502	11.70	12.30
E1	0.404	0.412	9.90	10.10
e	0.029	0.037	0.70	0.90
L	0.018	0.030	0.45	0.75
∞	0.000	7.000	0.00	7.00

JEDEC #: MS-026



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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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