bq50002 Low-Cost 5-V Wireless Power Transmitter Analog Front End for WPC V 1.2 A11 Transmitters

1 Features

- 5-V Transmitter AFE Compatible with Wireless Power Consortium (WPC) V1.2 A11 Low Power Transmitter Specification
- Designed to be used with bq500511 WPC Controller
- Suitable for WPC and Proprietary 5-V Wireless Power Transmitters
- Supports 5 W on the receiver output
- Integrates all the Analog Functions Required in a Wireless Power Transmitter
  - MOSFET Drivers and Synchronous N-Channel Power FETs
  - Accurate Current Sense
  - Variable Frequency Oscillator
  - High-Efficiency Voltage Regulator
  - High-Sensitivity Demodulator to Decode Signals from Receiver
- 2-Chip Solution Enables High-Efficiency Transmitter Designs of >75% Efficiency
- Ultra-Low-Standby Power, Even During Digital Ping (<30 mW)
- Dynamic Power Limiting (DPL)™ Enables Operation from Input Sources with Limited Power
- System LED Indication of Charging State and Fault Status
- Accurate Foreign Object Detection Method (FOD)

2 Applications

- WPC Compliant Wireless Transmitters for Smart Phones and Wearable Applications
- Proprietary Wireless Chargers and Transmitters
- Medical and Wearable Applications

3 Description

The bq50002 is a highly integrated wireless power transmitter analog front end that contains all of the analog components required to implement a WPC compliant 5-V transmitter. bq50002 integrates a full-bridge power driver with MOSFETs, variable-frequency oscillator, two-channel communication demodulator, linear regulator, and protection circuits. bq50002 must be used together with the digital controller bq500511 to realize a compact two chip wireless power transmitter solution. The bq500511 safely engages the RX device, receives packet communication from the powered device and manages the power transfer according to WPC v1.2 specification.

The system supports foreign object detection (FOD) by continuously monitoring the amount of power transferred and comparing that to the amount of received power, as reported by the receiver. This protects against power loss to metal objects misplaced in the wireless power transfer field. In order to do this, the bq50002 measures the input DC current very accurately using a current sense amplifier. Should any abnormal condition develop during power transfer, the bq500511 handles it and provides indication outputs. Comprehensive status and fault monitoring features enable a low cost yet robust WPC-certified wireless power system design.

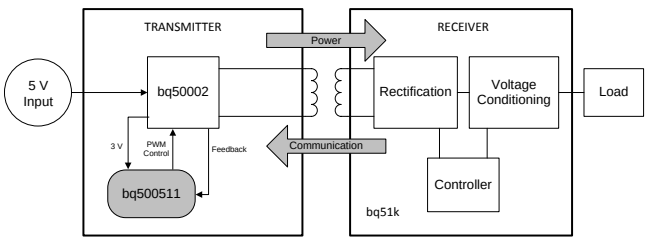
The bq50002 is available in a thermally enhanced 5.00 mm × 5.00 mm, 32-pin QFN package.

Device Information (1)

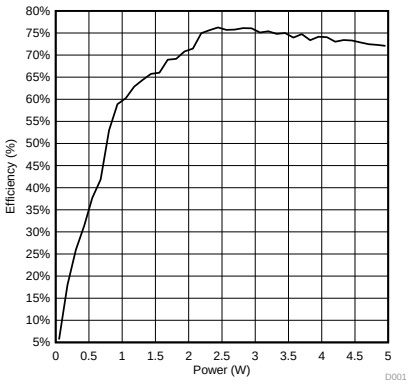
PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq50002	QFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs. Power



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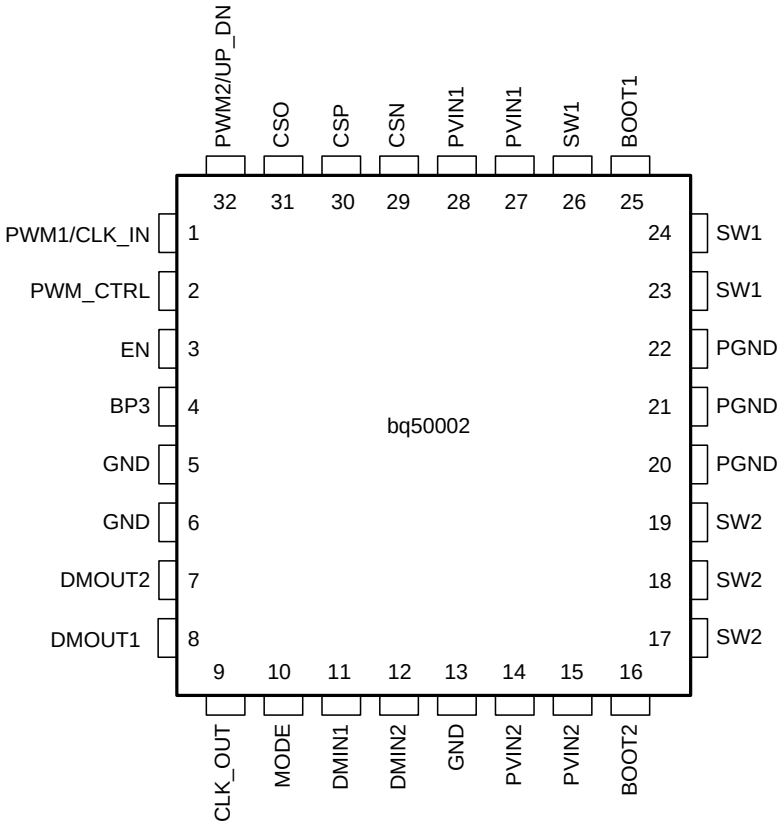
4 Revision History

Changes from Original (October 2015) to Revision A **Page**

- Changed marketing status from Product Preview to Final. ... 1

5 Pin Configuration and Functions

RHB Package
32-Pin QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT1	25	I/O	Positive supply rail for the high-side gate driver. Connect a 0.1-µF ceramic capacitor between the BOOT1 and SW1 pins.
BOOT2	16	I/O	Positive supply rail for the high-side gate driver. Connect a 0.1-µF ceramic capacitor between the BOOT2 and SW2 pins.
BP3	4	O	LDO output. Tie with 2.2-µF capacitor to GND. For use by bq500511 only.
CLK_OUT	9	O	Internal oscillator clock out signal.
CSN	29	I	Current sense amplifier negative input.
CSO	31	O	Current sense amplifier output. For use by bq500511 only.
CSP	30	I	Current sense amplifier positive input. Connect current sense resistor as close as possible to this pin. This also serves as the quiet node for power supply input.
DMIN1	11	I	Modulated signal from coil for DEMOD CHAN1.
DMIN2	12	I	Modulated signal from coil for DEMOD CHAN2.
DMOUT1	8	O	Demodulated 2-kHz signal from CHAN1. For use by bq500511 only.
DMOUT2	7	O	Demodulated 2-kHz signal from CHAN2. For use by bq500511 only.
EN	3	I	Enable pin with a weak internal pull-down. Float or pull below 1.5 V to disable gate driver, demodulation and current sense. Pull above 2.2 V to enable gate driver. Used by bq500511 to enter and leave standby mode for the transmitter.
GND	5	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
GND	6	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
GND	13	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
MODE	10	I	MODE pin with a weak internal pull-down. Float, or pull below 1.5 V to enable frequency control of the internally generated PWM signal. Pull above 2.2 V to enable pulse width control of the internally generated PWM signal. Used by bq500511 to select the control method for power control
PGND	20	–	Power ground for the ground-referenced power stage. Connect to GND.
PGND	21	–	Power ground for the ground-referenced power stage. Connect to GND.
PGND	22	–	Power ground for the ground-referenced power stage. Connect to GND.
PVIN1	27	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN1	28	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN2	14	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN2	15	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PWM_CTRL	2	I	PWM_CTRL pin with a weak internal pull-down. Controlled by bq500511 (SLUSCD3) for system power delivery control.
PWM1/CLK_IN	1	I	PWM1/CLK_IN pin with a weak internal pull-down. Controlled by bq500511 (SLUSCD3) for system power delivery control.
PWM2/UP_DN	32	I	PWM2/UP_DN pin with a weak internal pull-down. Controlled by bq500511 (SLUSCD3) for system power delivery control.
SW1	23	O	Switch node of the half-bridge MOSFETs. Connect to TX coil.
SW1	24	O	Switch node of the half-bridge MOSFETs. Connect to TX coil.
SW1	26	O	Switch node of the half-bridge MOSFETs . Connect to TX coil.
SW2	17	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.
SW2	18	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.
SW2	19	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
PVIN1, PVIN2	–0.3	7	V
BOOT1 (2)	–0.3	14	V
VBOOT1 – VSW1	–0.3	7	V
BOOT2 (2)	–0.3	14	V
VBOOT2 – VSW2	–0.3	7	V
PWM1, PWM2, EN, CLK_OUT, MODE, PWM_CTRL	–0.3	3.6	V
DMIN1	–5	7	V
DMIN2	–0.3	7	V
CSN, CSP	–0.3	7	V
CSN to CSP	-0.5	0.5	V
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In normal use, BOOT1, BOOT2 voltage internally regulated.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	PVIN1, PVIN2	4.5	5	5.5	V
	PWM1, PWM2, EN, CLK_OUT, MODE, PWM_CTRL	0	3	3.3	V
	DMIN1	–0.3		5	V
	DMIN2	–0.3		5	V
C_{BP3}	BP3 ceramic capacitor		2.2		µF
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 ceramic capacitor		0.1		µF
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 electrolytic capacitor		22		µF
C_{BOOT1}, C_{BOOT2}	SW1-BOOT1, SW2-BOOT2 capacitor		0.1		µF

6.4 Thermal Information

THERMAL METRIC (1)		bq50002 QFN 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C ≤ TJ ≤ 125°C, V_{PVIN1} = 5V, V_{PVIN2} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)					
UVLO rising threshold	V_{IN} rising	3.75	3.90	4.20	V
UVLO falling threshold	V_{IN} falling	3.60	3.85	4.08	V
REGULATOR VOLTAGE (BP3)					
BP3 output voltage	I_{BP3} = –5 mA, V_{PVIN1} = V_{PVIN2} = 5.0 V	2.9	3.0	3.1	V
BP3 output voltage	I_{BP3} = –10 mA, V_{PVIN1} = V_{PVIN2} = 5.0 V	2.9	3.0	3.1	V
BP3 load current max	V_{BP3} = 2.7 V, V_{PVIN1} = V_{PVIN2} = 5.0 V	7.7	14	21	mA
CURRENT SENSE AMPLIFIER (CSP, CSN)					
Current sense amplifier gain	0°C < T_J < 85°C	49	50	51	V/V
Current sense amplifier offset	0°C < T_J < 85°C	-14		14	mV
Input current (CSP)	V_{CSP} = 5.0 V, V_{PVIN1} = V_{PVIN2} = 5.0 V		1.5		mA
Input current (CSN)	V_{CSN} = 5.0 V, V_{PVIN1} = V_{PVIN2} = 5.0 V	8.5	10.0	11.3	µA
EN					
High-level input voltage	Input rising	1.7	1.8	1.9	V
Low-level input voltage	Input falling	0.8	1.0	1.1	V
EN pull-down resistance	EN = 3 V	40	50	60	kΩ
PWM_CTRL					
High-level input voltage	Input rising	1.4	1.6	1.8	V
Low-level input voltage	Input falling	0.9	1.0	1.1	V
PWM_CTRL pull-down resistance	PWM_CTRL = 3 V	40	50	60	kΩ

Electrical Characteristics (continued)

–40°C ≤ TJ ≤ 125°C, V_{PVIN1} = 5V, V_{PVIN2} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM1					
High-level input voltage	Input rising	1.6	1.8	1.9	V
Low-level input voltage	Input falling	0.9	1.0	1.1	V
PWM1 pull-down resistance	PWM1 = 3 V	40	50	60	kΩ
PWM2					
High-level input voltage	Input rising	1.6	1.7	1.8	V
Low-level input voltage	Input falling	1.0	1.1	1.2	V
PWM2 pull-down resistance	PWM2 = 3 V	40	50	60	kΩ
MODE					
High-level input voltage	Input rising	1.7	1.8	1.9	V
Low-level input voltage	Input falling	0.9	1.0	1.1	V
MODE pull-down resistance	MODE = 3 V	40	50	60	kΩ
BOOTSTRAP DIODE (BOOT1 AND BOOT2)					
Regulation voltage (BOOT1)	V_{PVIN1} = V_{PVIN2} = 5 V, I_{BOOT} = 0 mA	4.2	4.4	4.7	V
Regulation voltage (BOOT2)	V_{PVIN1} = V_{PVIN2} = 5 V, I_{BOOT} = 0 mA	4.9	5.0	5.1	V
UVLO (BOOT1)	V_{PVIN1} = V_{PVIN2} = 5 V	1.8	2.3	2.7	V
UVLO (BOOT2)	V_{PVIN1} = V_{PVIN2} = 5 V	1.8	2.2	2.6	V
MOSFETS (SW1 AND SW2)					
SW1 high-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	59	76	107	mΩ
SW1 low-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	48	61	86	mΩ
SW2 high-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	42	49	64	mΩ
SW2 low-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V, I_{SW} = 500 mA	39	46	58	mΩ

6.6 Typical Characteristics

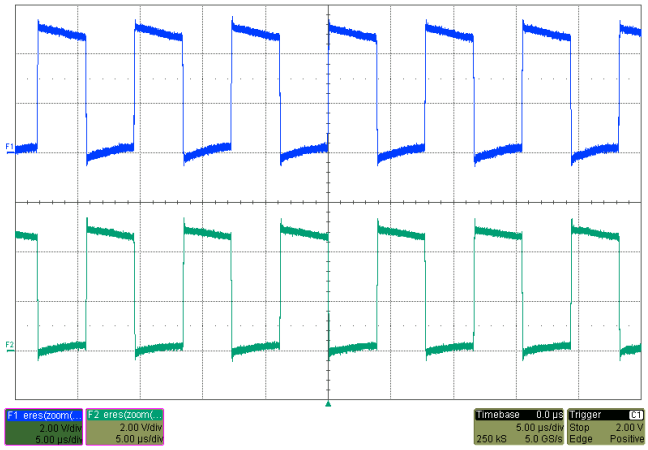


Figure 1. bq50002 SW1, SW2

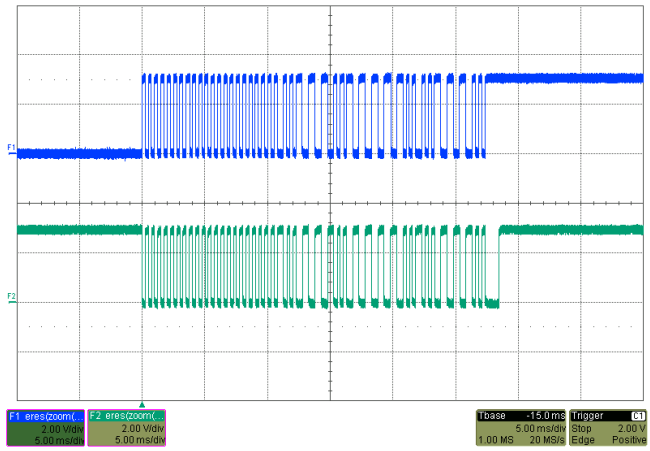


Figure 2. DMOUT1, DMOUT2

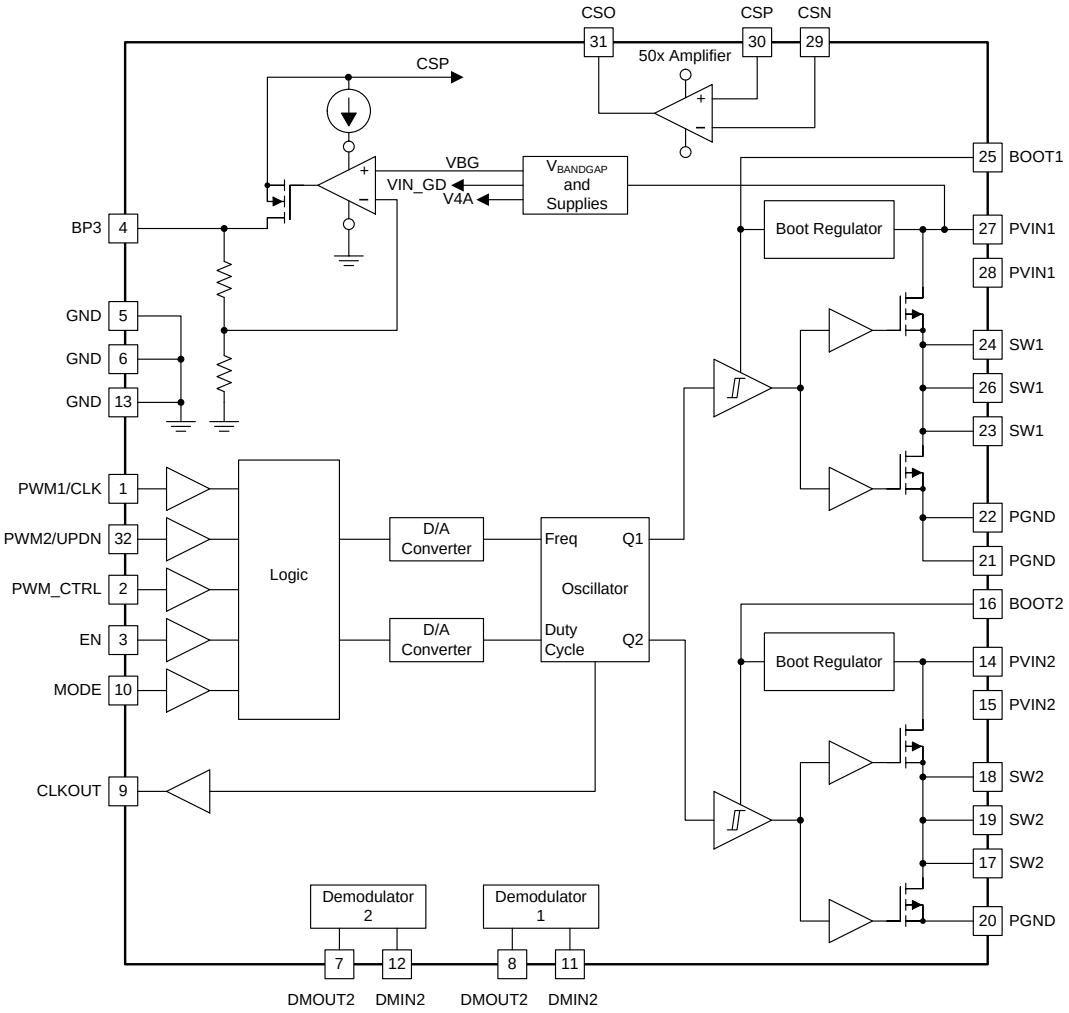
7 Detailed Description

7.1 Overview

The principle of wireless power transfer is simply an open-cored transformer consisting of transmitter and receiver coils. The transmitter coil and electronics are typically built into a charger pad and the receiver coil and electronics are typically built into a portable device, such as a smart phone. When the receiver coil is positioned on the transmitter coil, magnetic coupling occurs when the transmitter coil is driven. The flux is coupled into the secondary coil, which induces a voltage and current flows. The secondary voltage is rectified, and power can be transferred effectively to a load, wirelessly. Power transfer can be managed through various closed loop control schemes.

After power is applied and the transmitter device comes out of reset, it will automatically begin the process of detecting and powering a receiver. The bq500511 sends a ping to detect the presence of a receiver on the pad. After a receiver is detected, the bq500511 attempts to establish communication and begin power transfer. The bq500511 is designed to operate with the bq50002 Wireless Power Transmitter Analog Front End to control a full-bridge power stage to drive the primary coil. Through a simple interface the bq500511 instructs the bq50002 how much to increase or decrease power. The full bridge power stage allows for higher power delivery for a given supply voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Demodulator

The embedded demodulator outputs at least one valid bit stream under all modulation conditions that can be used by the accompanied bq500511 controller in order to comply with WPC specification.

More specifically, the WPC worst case condition is defined as the transmitter operating at the minimum modulation level, and the receiver coil is measured by certain x, y and z axis distance to the center of the transmitter coil.

Analog demodulation channel function diagram:

- The diagram below from the WPC spec document explains the concept of Minimum Modulation. The peak-to-peak amplitude difference in TX coil waveform between HI and LO states is 400 mV. With 20-V_{pp} carrier waveform, and 400-mV_{pp} modulation, with a typical divider it translates to 1 V_{pp} ±20 mV_{pp} at the input of the demodulator channel.
- The difference of the amplitude of the primary cell voltage in the HI and LO state is at least 200 mV.

During a transition the primary cell current and primary cell voltages are undefined. See Figure 3.

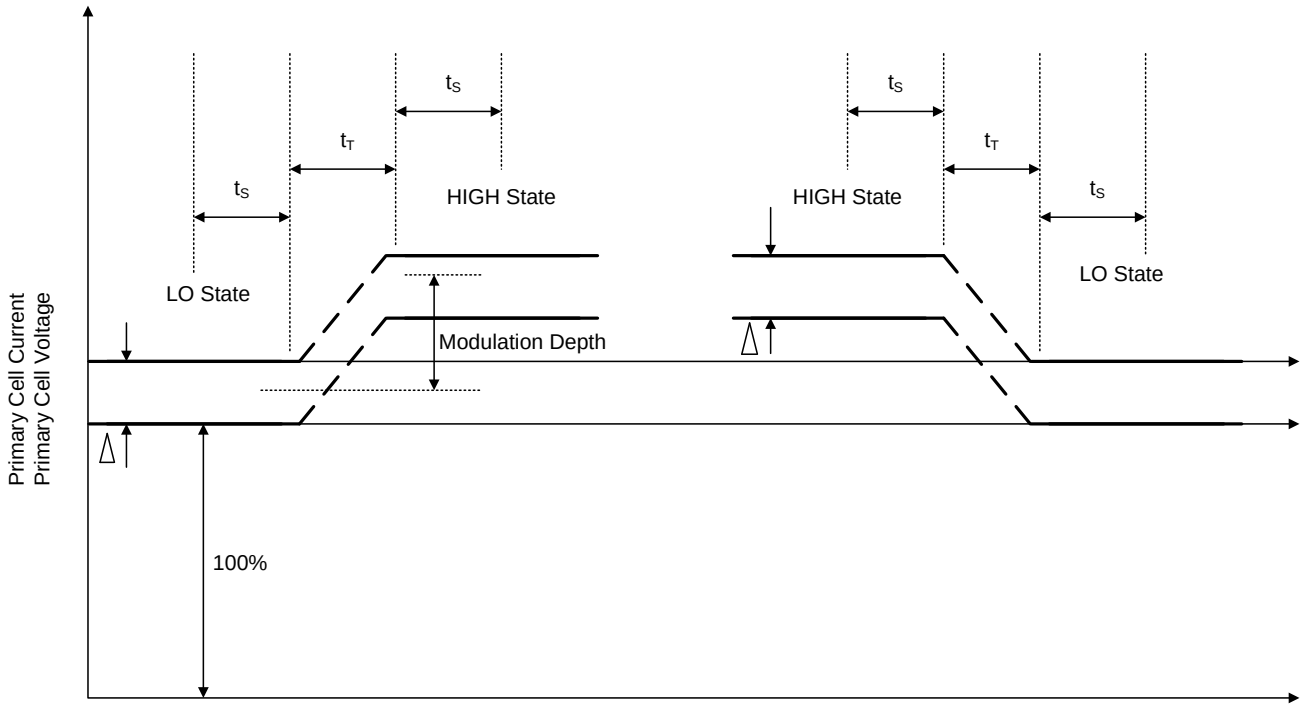


Figure 3. Amplitude Modulation of the Power Signal

Feature Description (continued)

7.3.2 PWM Control

7.3.2.1 PWM_CTRL Input

bq50002 operates in two modes:

Direct PWM Control Mode and Self Switching. The mode of operation is set by the state of PWM_CTRL input when EN=HIGH. This is intended for control by bq500511.

7.3.2.2 PWM1, PWM2

bq50002 passes external PWM inputs to drive gate drivers when the following conditions hold:

- EN pin is HIGH
- PWM_CTRL pin is HIGH
- Typical Dead Time shall be better than 20 ns. Minimum PWM input pulse duration that changes SW output should be less than 50 ns.

7.3.2.3 Self-Switching

bq50002 follows the commands from the controller to adjust the internal oscillator frequency up or down to adjust output power levels when the following conditions apply:

- PWM_CTRL pin is LOW
- PWM1/CLK_IN behaves as CLK_IN pin. The CLK_IN rising edge triggers frequency increase or decrease by one step based on the state of PWM2/UP_DN pin.
- Self-switching starts at F=175 kHz when PWM_CTRL state changes from HIGH to LOW. Operating frequency changes are based on the inputs of UP_DN, CLK_IN and MODE.
- The CLK_OUT pin outputs 3.3V logic level with frequency equal in value to the current switching frequency. The rising edge of this signal coincides with the rising edge of the SW1 waveform. The duty factor of the signal on CLK_OUT pin is 50%.
- bq50002 increases the frequency (reduces delivered power) if:
  - PWM_CTRL pin is LOW
  - MODE pin is LOW
  - UP_DN pin is LOW
  - CLK_IN pin changes its state from LOW to HIGH (rising edge)
- bq50002 decreases the frequency (increases delivered power) if:
  - PWM_CTRL pin is LOW
  - MODE pin is LOW
  - UP_DN pin is HIGH
  - CLK_IN pin changes its state from LOW to HIGH (rising edge)

Feature Description (continued)

7.3.2.4 Duty Cycle Adjustment

bq50002 follows the commands from the controller to adjust the internal oscillator duty cycle up or down to adjust power output levels when the following conditions hold:

- The internal clock is set to the highest frequency tap, 205 kHz
- PWM_CTRL pin is LOW
- MODE pin is HIGH
- bq50002 decreases the duty cycle (reduces delivered power) if:
  - The internal clock is set to the highest frequency tap, 205 kHz or at frequency at which MCU commands MODE = 1
  - PWM_CTRL pin is LOW
  - MODE pin is HIGH
  - UP_DN is LOW
  - CLK_IN pin changes state from LOW to HIGH (rising edge)
  - bq50002 ignores CLK_IN signals when minimum duty factor position of 10% is reached
- bq50002 increases the duty cycle (increases delivered power) if:
  - The internal clock is set to the highest frequency tap, 205 kHz at frequency at which MCU commands MODE = 1
  - PWM_CTRL pin is LOW
  - MODE pin is HIGH
  - UP_DN is HIGH
  - CLK_IN pin changes state from LOW to HIGH (rising edge)
  - bq50002 ignores CLK_IN signals when maximum duty factor position of 50% is reached. bq50002 will resume clock frequency adjustment mode only when the duty cycle adjustment has reached the 50% state and MODE=0.

7.3.3 Current Sense Amplifier

To support foreign object detection (FOD), bq50002 senses the average input current to the device. The integrated current sense amplifier has voltage gain of 50.

7.3.4 Voltage Regulator

bq50002 has an integrated low-dropout (LDO) voltage regulator which supplies power to the companion bq500511 controller. The BP3 pin supplies a regulated 3-V voltage supply and should have a 2.2-µF capacitor tied to GND.

7.4 Device Functional Modes

7.4.1 Power Transfer

Power transfer efficiency and robustness depends on coil coupling. Coupling depends on the distance between coils, alignment, coil dimensions, coil materials, number of turns, magnetic shielding, impedance matching, frequency. Most importantly, the receiver and transmitter coils must be aligned for best coupling and efficient power transfer. The smaller the space between the coils is, the better the coupling. Shielding is added as a backing to both the transmitter and receiver coils to direct the magnetic field to the coupled zone. Magnetic fields outside the coupled zone do not transfer power. Thus, shielding also serves to contain the fields to avoid coupling to other adjacent system components.

Regulation can be achieved by controlling any one of the coil coupling parameters. However, for WPC compatibility, the transmitter-side coils and capacitance are specified and the resonant frequency point is fixed. In the bq500511/bq50002 system power transfer is regulated by changing the operating frequency between 110 kHz to 205 kHz. The higher the frequency, the further from resonance and the lower the power. Duty cycle remains constant at 50% throughout the power band and is reduced only once 205 kHz is reached.

7.4.1.1 Dynamic Power Limiting™

Dynamic Power Limiting™ (DPL) allows operation from a 5-V supply with limited current capability (such as a USB port). When the input voltage is observed drooping, the output power is dynamically limited to reduce the load and provides margin relative to the supply's capability.

Anytime the DPL control loop is regulating the operating point of the transmitter, the LED will indicate that DPL is active. The LED color and flashing pattern are determined by the LED Table. If the receiver sends a Control Error Packet (CEP) with a negative value, (for example, to reduce power to the load), the bq500511 in DPL mode will return to normal operation and respond to this CEP via the standard WPC control loop behavior.

Device Functional Modes (continued)

7.4.2 Communication

Communication within the WPC v1.2 specification is from the receiver to the transmitter. For example, in order to regulate the output of the transmitter, the receiver sends messages requesting the transmitter to increase or decrease power. The receiver communicates by modulating the rectifier voltage and using amplitude modulation (AM) sends packets of information to the transmitter. A packet is comprised of a preamble, a header, the actual message, and a checksum, as defined by the WPC standard.

The receiver sends a packet by modulating an impedance network. This AM signal reflects back as a change in the voltage amplitude on the transmitter coil. In the bq500511/bq50002 system, the bq50002 performs the demodulation function and passes a digitized version of the message to the bq500511 where the message is decoded and processed. For example in response to a Control Error Packet, the bq500511 calculates the required change in output power and in turn controls the bq50002 through the CLK_OUT, UP_DOWN, and MODE pins to adjust the operating point and thus its output power.

The modulation impedance network on the receiver can either be resistive or capacitive. Figure 4 shows the resistive modulation approach, where a resistor is periodically added to the load, resulting in an amplitude change in the transmitter voltage. Figure 5 shows the corresponding capacitive modulation approach.

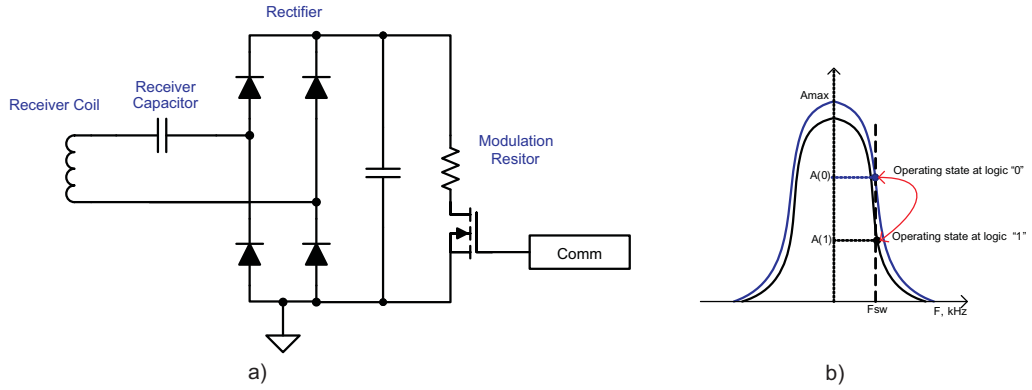


Figure 4. Receiver Resistive Modulation Circuit

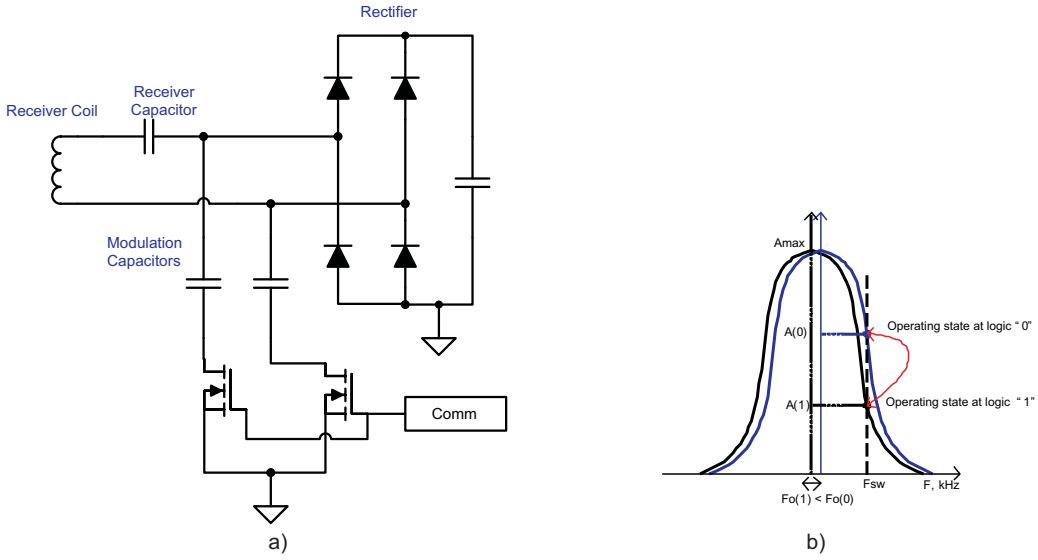


Figure 5. Receiver Capacitive Modulation Circuit

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq50002 device is a wireless power transmitter AFE designed for 5-W WPC compliant applications when paired with the bq500511. The pair integrates all functions required to control wireless power transfer to a WPC v1.2 compliant receiver. Several tools are available for the design of the system. See the product folder on www.ti.com for more details. The following sections highlight some of the system design considerations.

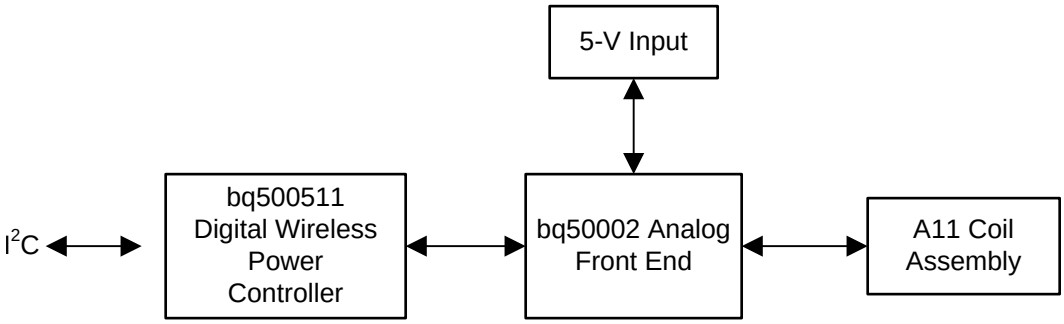


Figure 6. System Block Diagram

The I^2C port is accessed by the FOD tuning tool and can provide a level of system monitoring and evaluation.

The SDA and SCL lines of the I^2C bus must be pulled up (as shown in the Figure 7) if the I^2C port is utilized. They may be left floating if no I^2C function is required. The logic reference generated by the bq50002 Analog Front End is 3 V, so care should be taken to ensure that if the Master I^2C device also has pull-up resistors to a higher reference, that the the 3-V reference to the bq500511 is not affected. Specifically, only one set of pull-up resistors should be populated, either on the I^2C Master bus or on the bq500511 system board, but not both.

8.2 Typical Application

The bq50002 is a highly integrated analog front end device which, when paired with the bq500511 controller, requires a minimum of external components to implement a WPC V 1.2 Wireless Power Transmitter system.

As shown in the application schematic, external components are used to implement the following functions:

- Resonant Tank Circuit
- Demodulator Input Signal Conditioning
- Human Interface (LED and Buzzer)
- Current Sensing
- Voltage Sensing
- Temperature Sensing
- System Configuration
  - Foreign Objection Detection (FOD) Threshold and Calibration
  - LED Mode

Typical Application (continued)

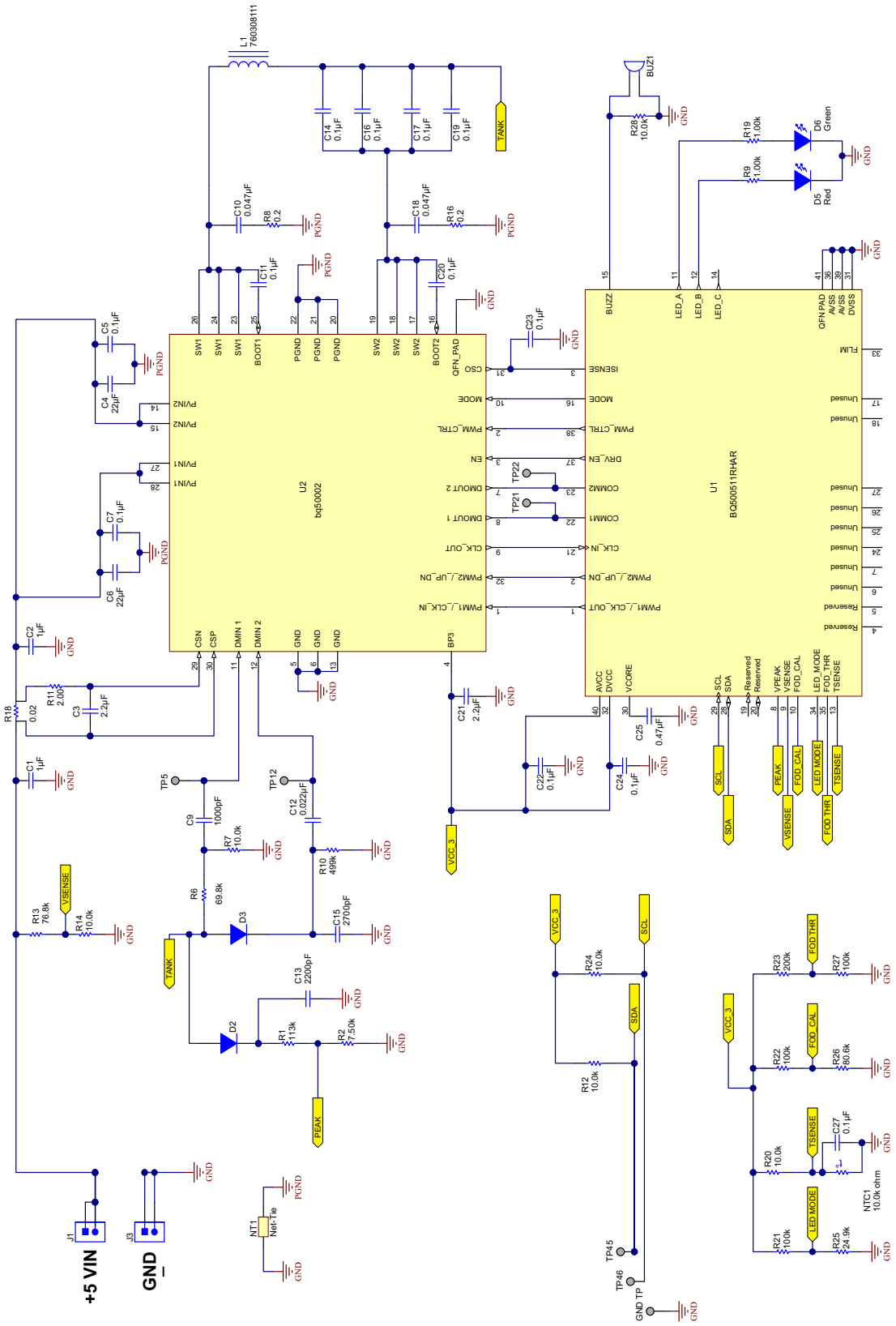


Figure 7. bq500511 Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	VALUE
WPC coil type	A11

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Selection

Capacitor selection is critical to proper system operation. The total capacitance value of 4 nF × 100 nF is required in the resonant tank. This is the WPC system compatibility requirement, not a guideline.

NOTE

A total capacitance value of 4 nF × 100 nF (C0G dielectric type, 50-V rating) is required in the resonant tank to achieve the correct resonance frequency. The capacitors chosen must be rated for at least 50 V and must be of a high-quality C0G dielectric (sometimes also called NP0). These are typically available in a 5% tolerance, which is adequate. TI does **not** recommend the use of X7R types or below if WPC compliance is required because critical WPC Certification Testing, such as the minimum modulation or guaranteed power test, might fail. The designer can combine capacitors to achieve the desired capacitance value. Various combinations can work depending on market availability. All capacitors must be of C0G types (not mixed with any other dielectric types).

8.2.2.2 Current Monitoring Requirements

The bq50002 is WPC v1.2 ready. To enable the FOD feature, current monitoring is provided in the bq50002 Analog Front End. For proper scaling of the current monitor signal, the current sense resistor should be 20 mΩ. For FOD accuracy, the current sense resistor must be a quality component with 0.5% tolerance, at least 1/4-W rating, and a temperature stability of ±200 PPM.

8.2.2.3 Input Regulation

The bq500511 requires 3 VDC to operate. The regulator in the bq50002 provides this voltage rail eliminating the need for any external regulation.

8.2.2.4 System Input Power Requirements

The design works with 5-V input voltage to the bq50002. The WPC defined A11 TX type requires 5-V system voltage in order to deliver 5 W of output power from the receiver.

8.2.3 Application Curves

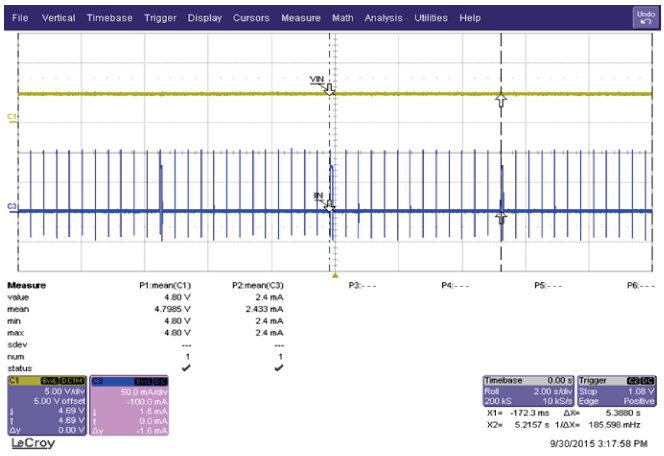


Figure 8. Standby Power

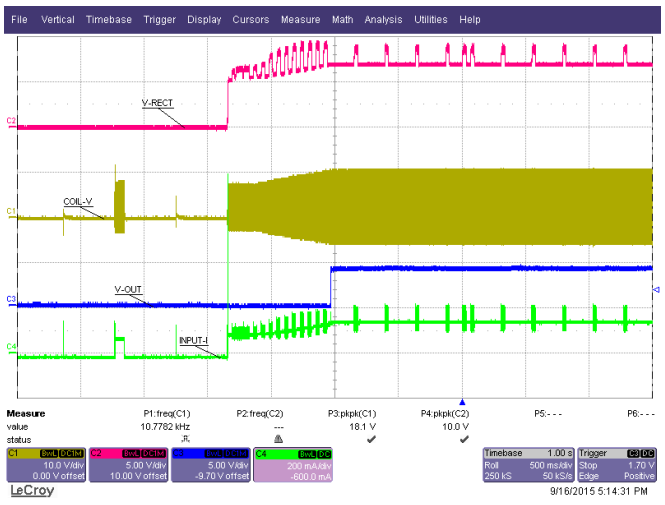


Figure 9. Start-Up with bq51013B

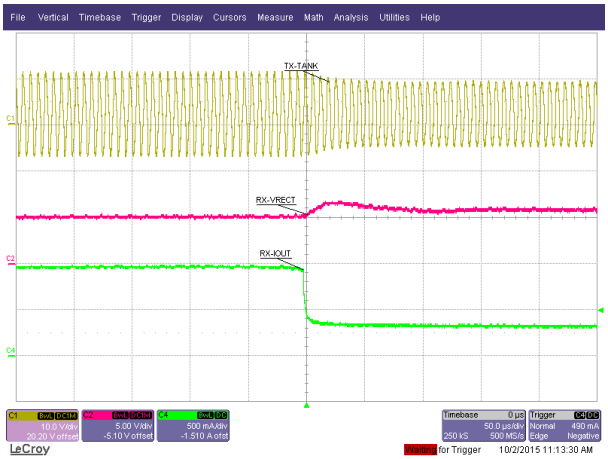


Figure 10. Load-Transient Response

9 Power Supply Recommendations

The A11 TX type requires a 5-V system voltage.

10 Layout

10.1 Layout Guidelines

Careful PCB layout practice is critical to proper system operation. Many references are available on proper PCB layout techniques. A few good tips are as follows.

The TX layout requires a 4-layer PCB layout for best ground plane technique. A 2-layer PCB layout can be achieved though not as easily. Ideally, the approach to the layer stack-up is:

- Layer 1 component placement and as much ground plane as possible
- Layer 2 clean ground
- Layer 3 finish routing
- Layer 4 clean ground

Thus, the circuitry is virtually sandwiched between grounds. This minimizes EMI noise emissions and also provides a noise-free voltage reference plane for device operation.

Keep as much copper as possible. Make sure the bq500511 GND pins have a continuous flood connection to the ground plane. The power pad of the bq50002 should also be stitched to the ground plane, which also acts as a heat sink. A good GND reference is necessary for proper system operation, such as analog-digital conversion, clock stability, and best overall EMI performance. Separate the analog ground plane from the power ground plane and use only **one** tie point to connect grounds. Having several tie points defeats the purpose of separating the grounds. See the bq500511 EVM for an example of a good layout technique.

10.1.1 Layout Notes

Make sure the bypass capacitors intended for the bq500511 3.3-V supply are actually bypassing these supply pins (pin 32, DVCC, and pin 40, AVCC) to solid ground plane (see Figure 11). This means they need to be placed as close to the device as possible and the traces must be as wide as possible.

Make sure the bq500511 has a continuous flood connection to the ground plane (see Figure 12).

The full-bridge power stage that drives the TX coil is composed of two half-bridge power stages (integrated in bq50002) and resonant capacitors. Inputs bypass capacitors should be placed as close as possible to the bq50002 PVIN1 pins (pin 27, 28) and PVIN2 pins (pin 14, 15). The input and ground pours and traces should be made as wide as possible for better current flow. The trace to the coil and resonant capacitors should also be made as wide as possible (see Figure 13).

To ensure proper operation, grounds conducting a large amount of current and switching noise must be isolated from low current, quiet grounds. Separate the ground pours for the power stages and the bq500511 IC. Connect all grounds to a single point at the main ground terminal (see Figure 14).

Proper current sensing layout technique is very important, as it directly affects the FOD and PMOD performance. When sampling the very-low voltages generated across a current sense resistor, be sure to use the so called 4-wire or Kelvin-connection technique. This is important to avoid introducing false voltage drops from adjacent pads and copper power routes. It is a common power-supply layout technique. Some high-accuracy sense resistors have dedicated sense pins (see Figure 15).

The trace from bq50002 CSP pin to sense resistor must be minimized to avoid unwanted offset in the application. This trace should be limited to less than 20 mΩ resistance.

10.2 Layout Examples

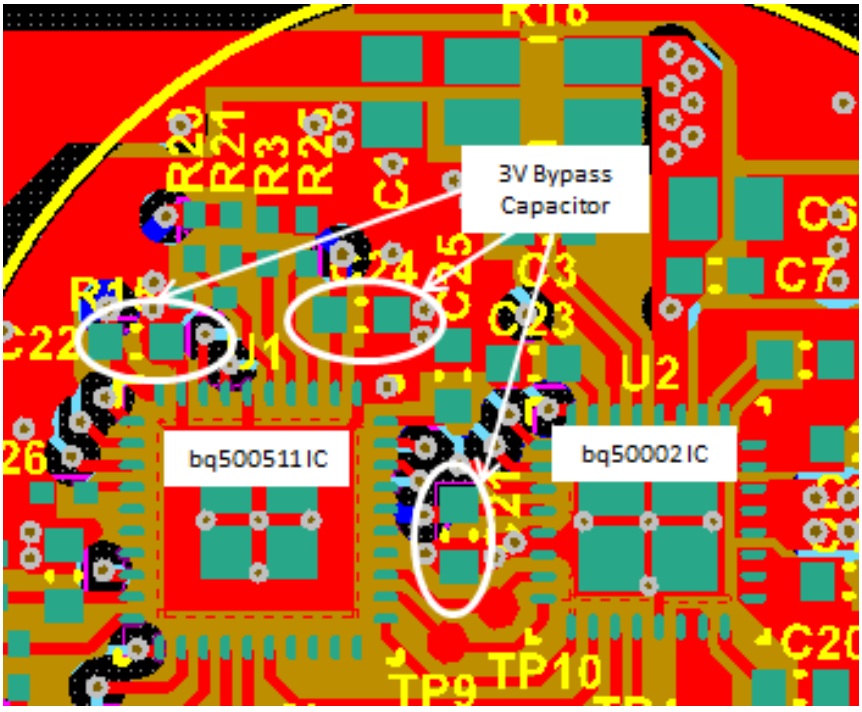


Figure 11. Bypass Capacitors Layout

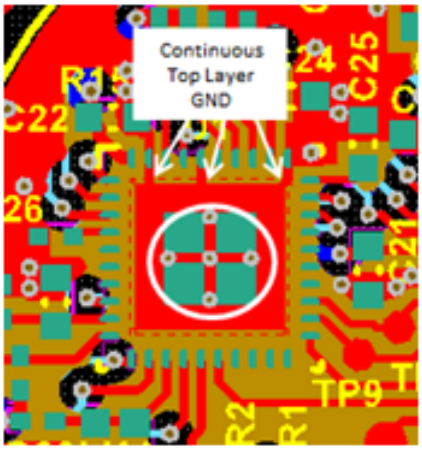


Figure 12. Continuous GND Layout

Layout Examples (continued)

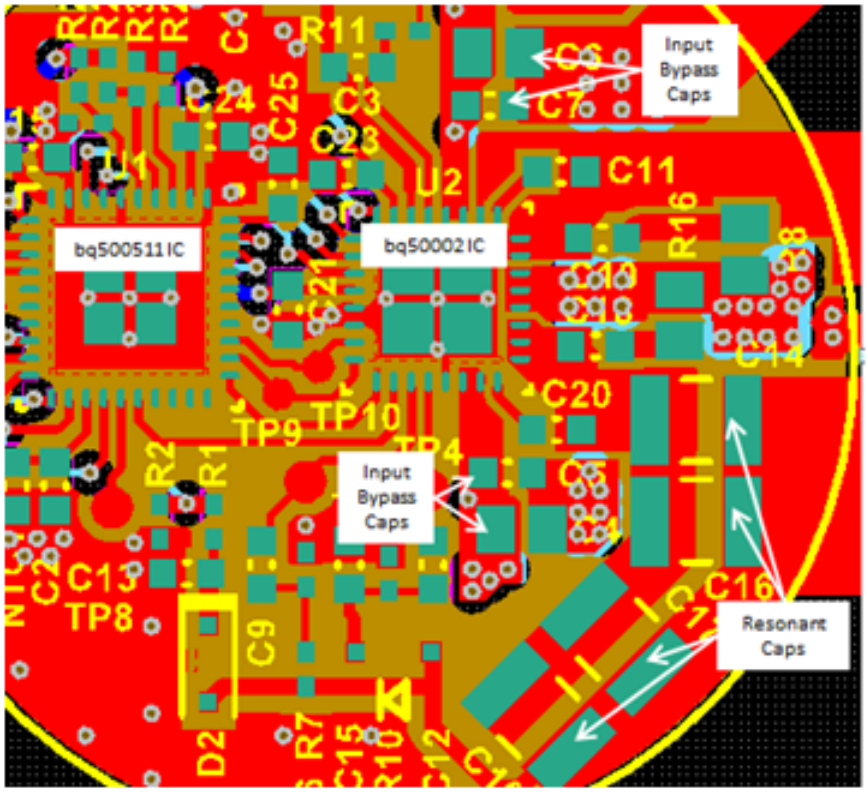


Figure 13. Ground Layout

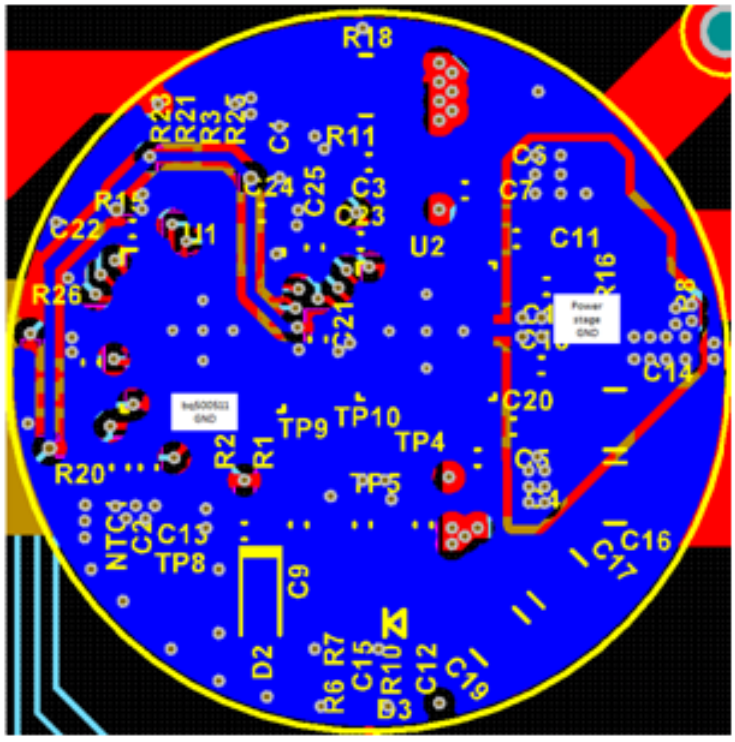


Figure 14. Ground Layout

Layout Examples (continued)

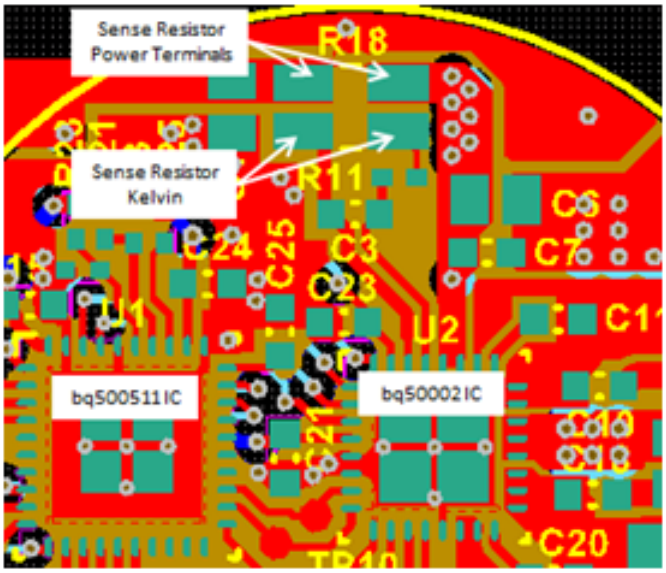


Figure 15. Current Sensing Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

1. Data Sheet, *bq500511 Wireless Power Transmitter Controller* (SLUSCD3)
2. Evaluation Module, *bq50002 Wireless Power TX EVM* (SLVUAJ7)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ50002RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ50002	Samples
BQ50002RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ50002	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

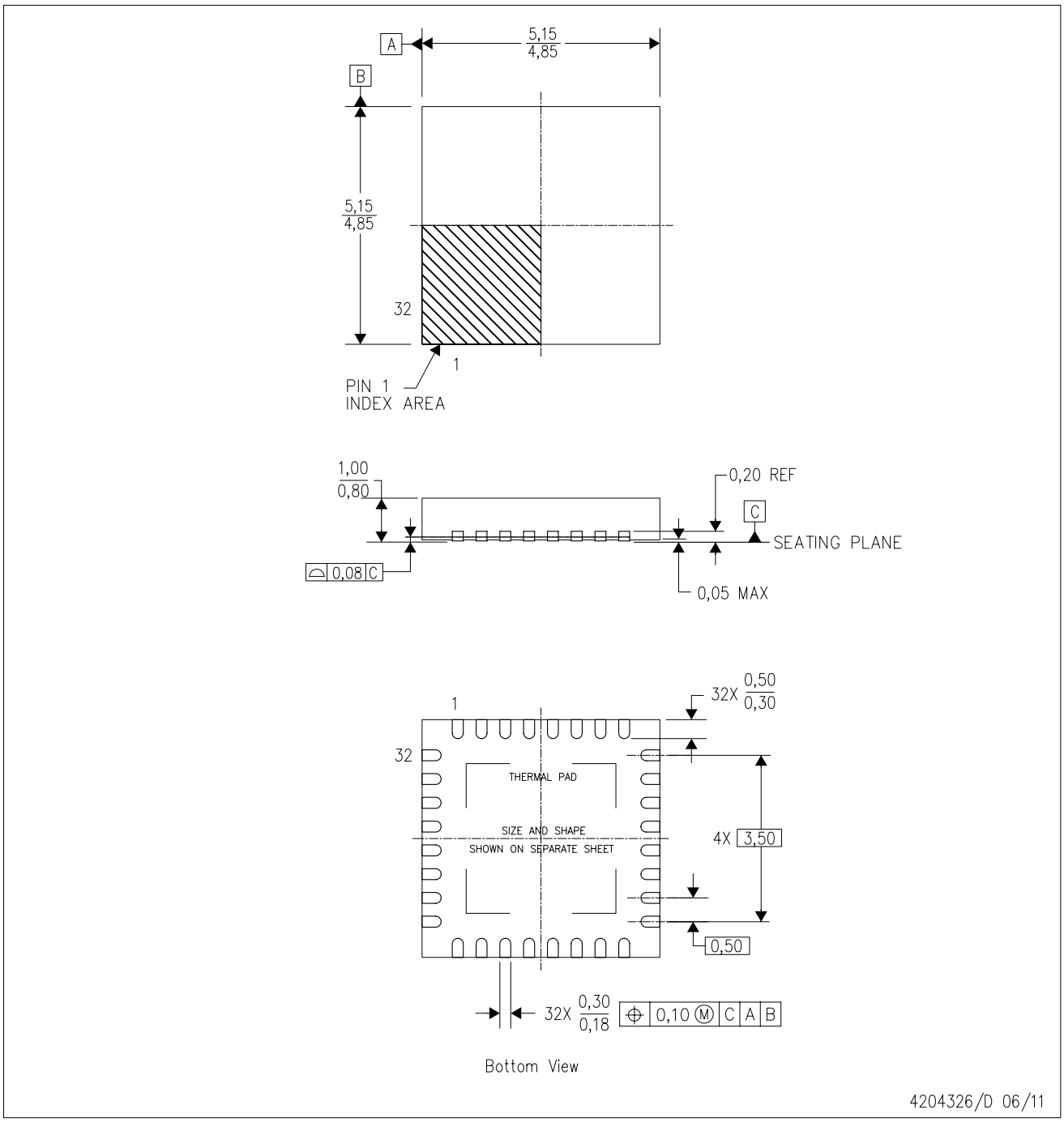
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

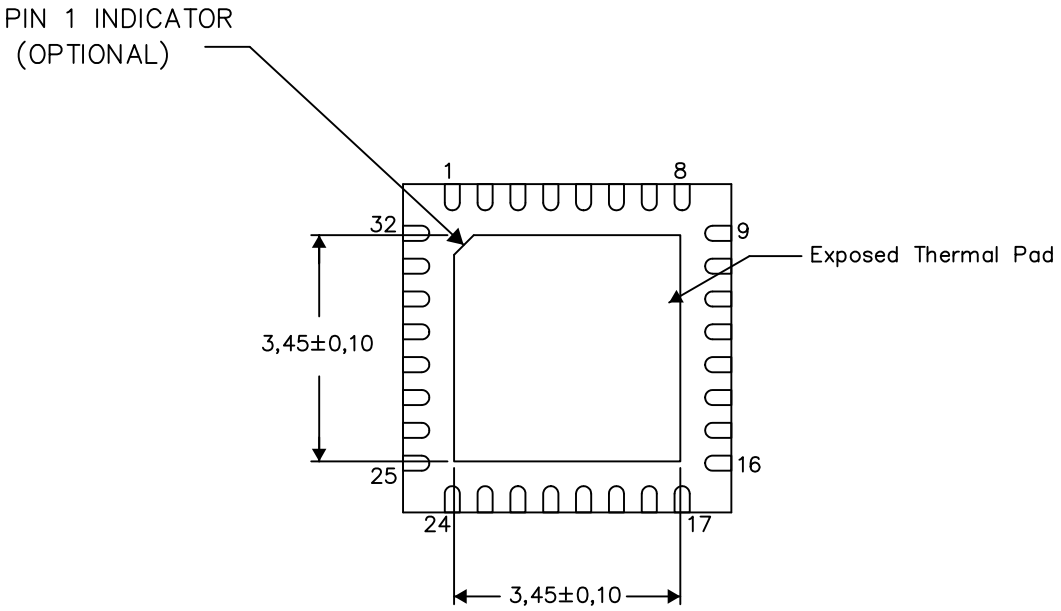
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



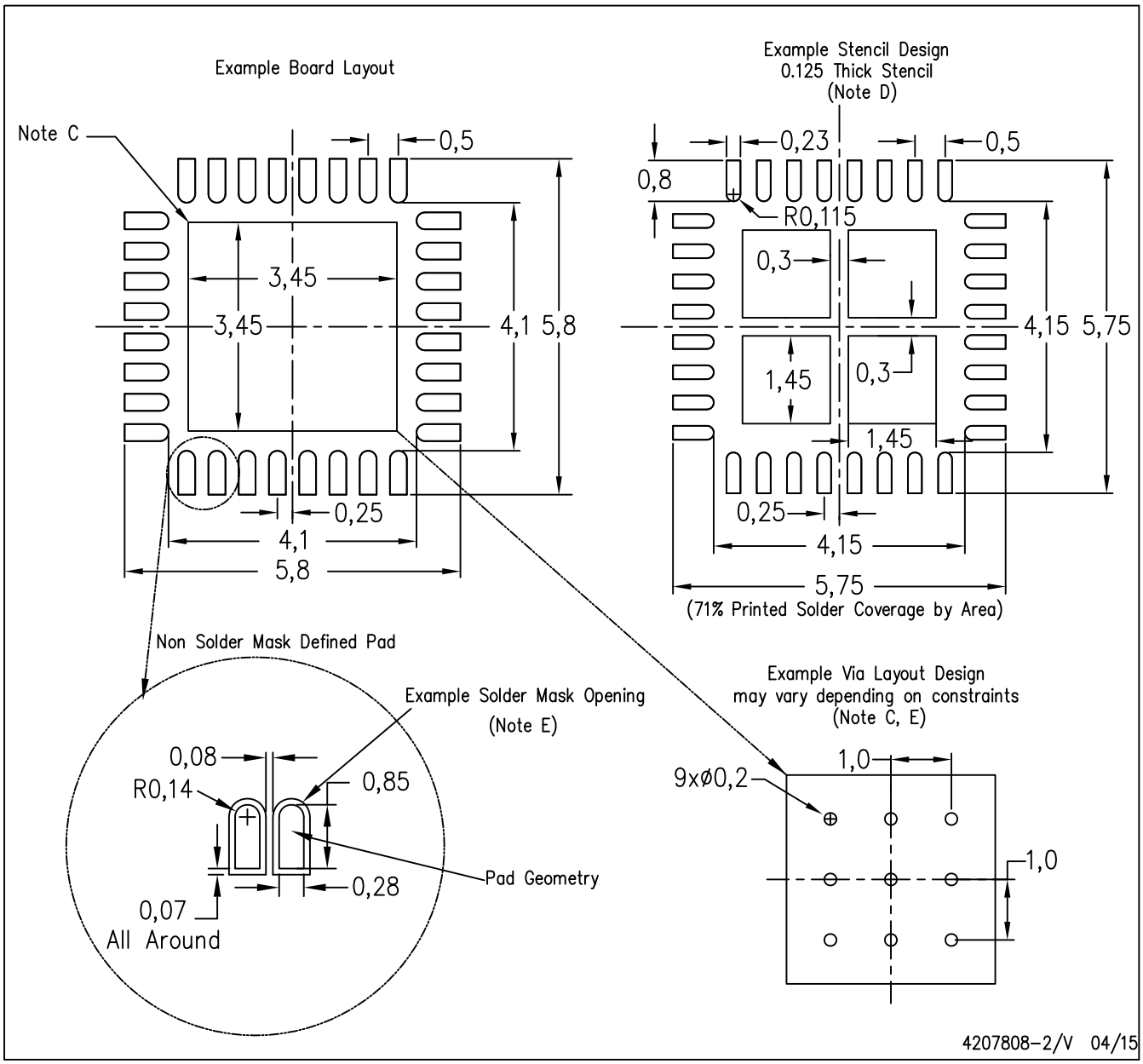
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



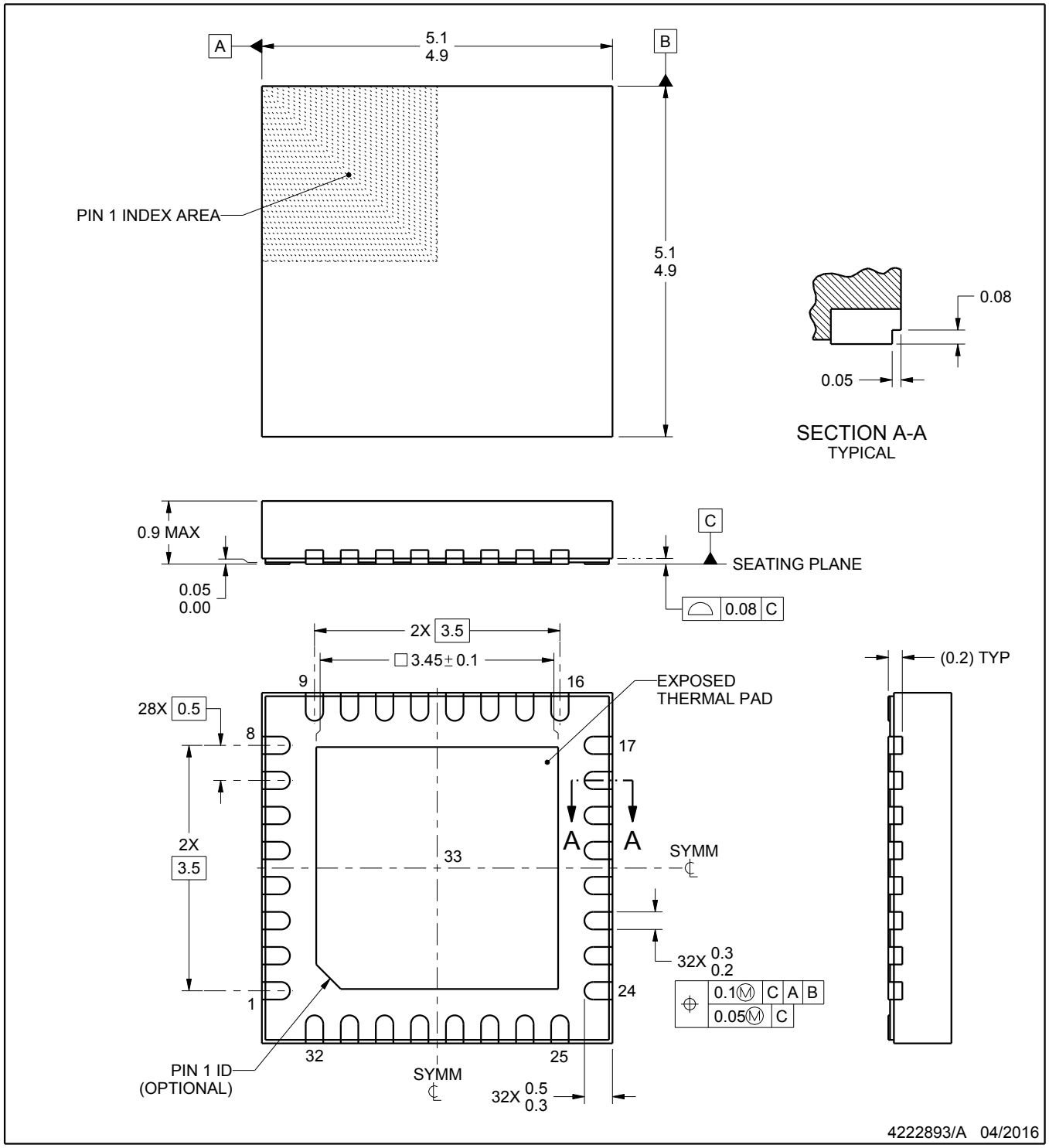
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

PACKAGE OUTLINE

RHB0032N

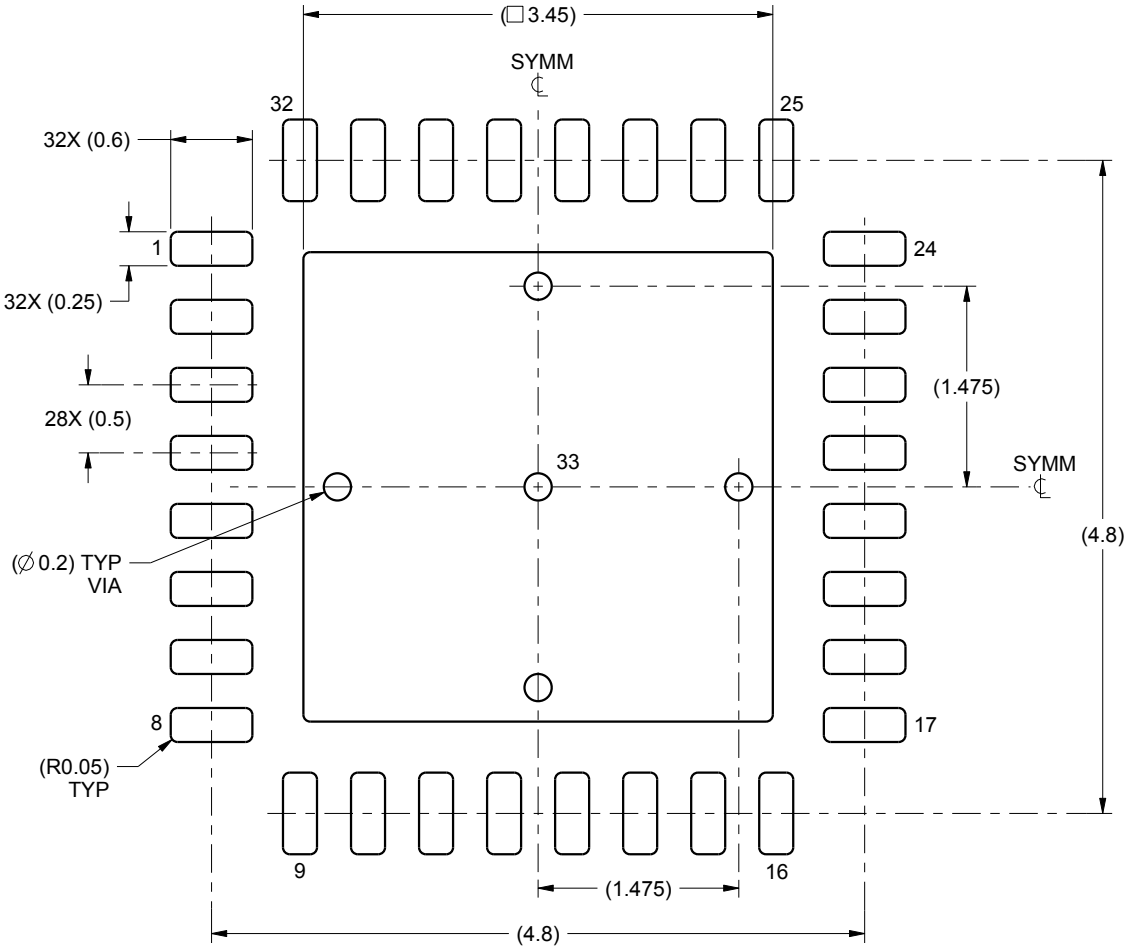
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

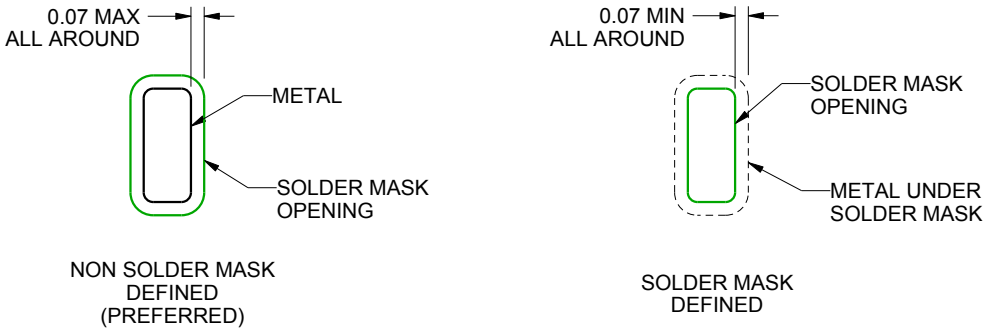


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

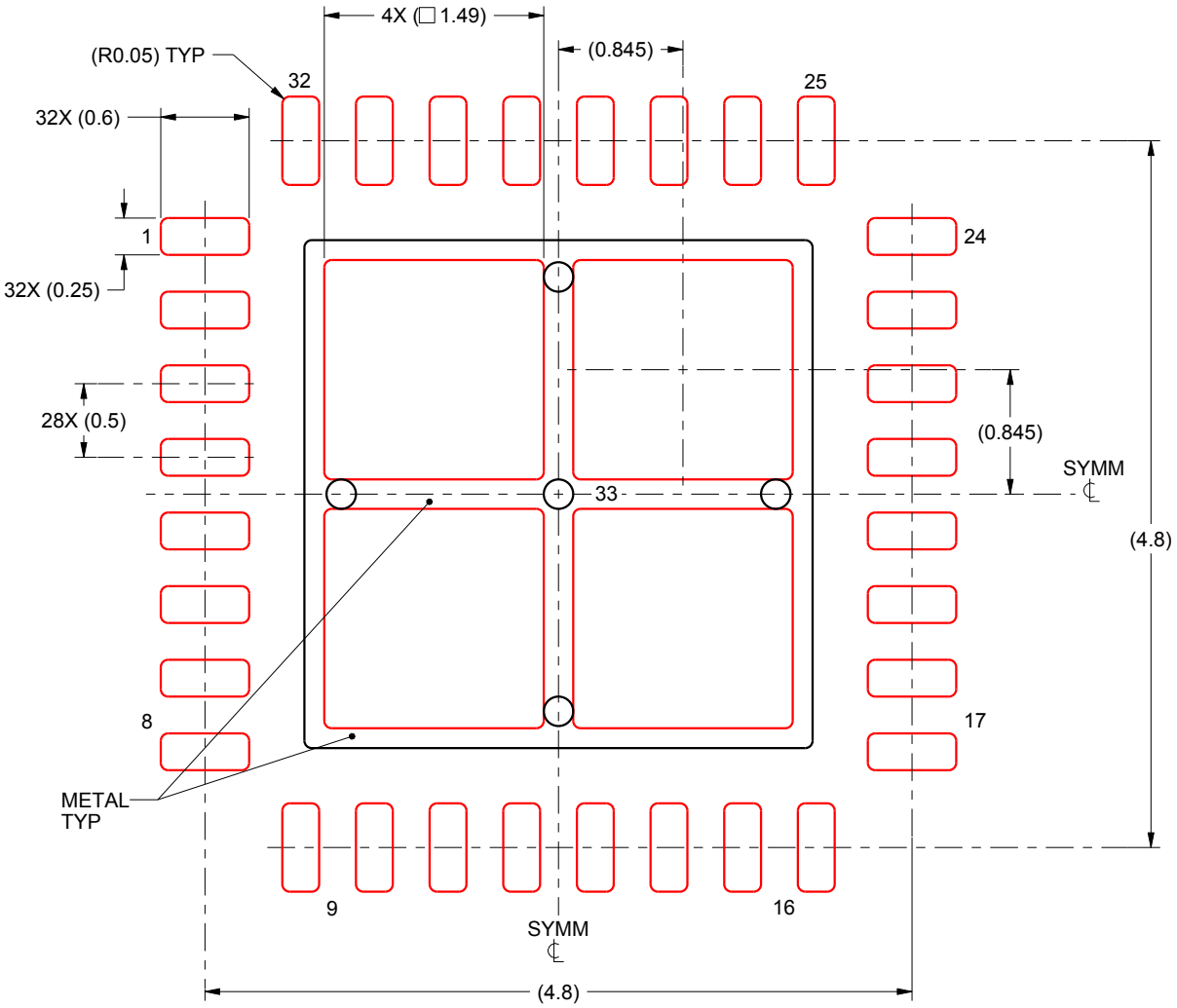


SOLDER MASK DETAILS

4222893/A 04/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222893/A 04/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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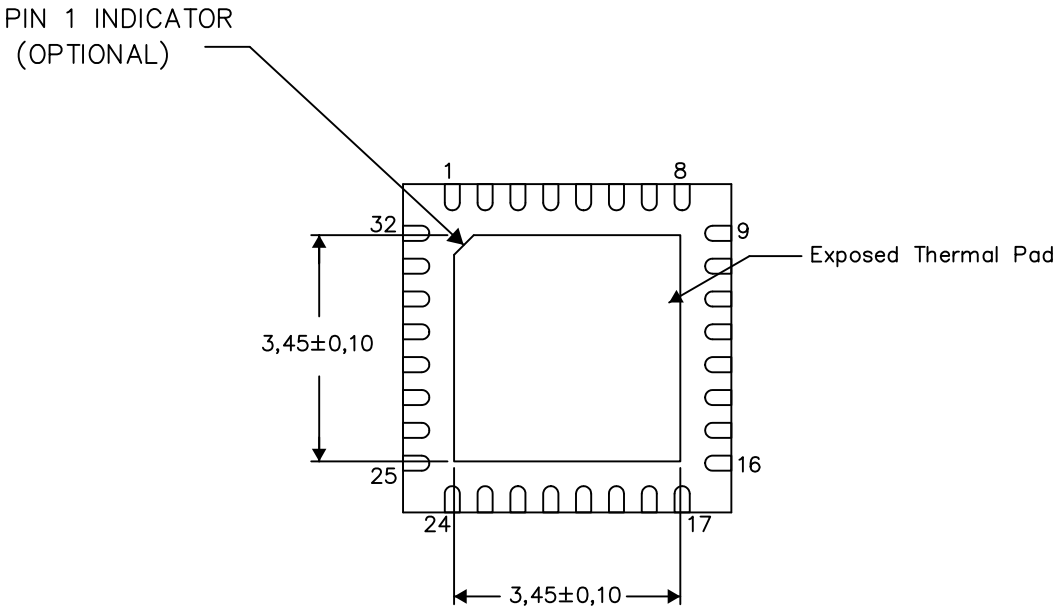
The exposed thermal pad dimensions for this package are shown in the following illustration.



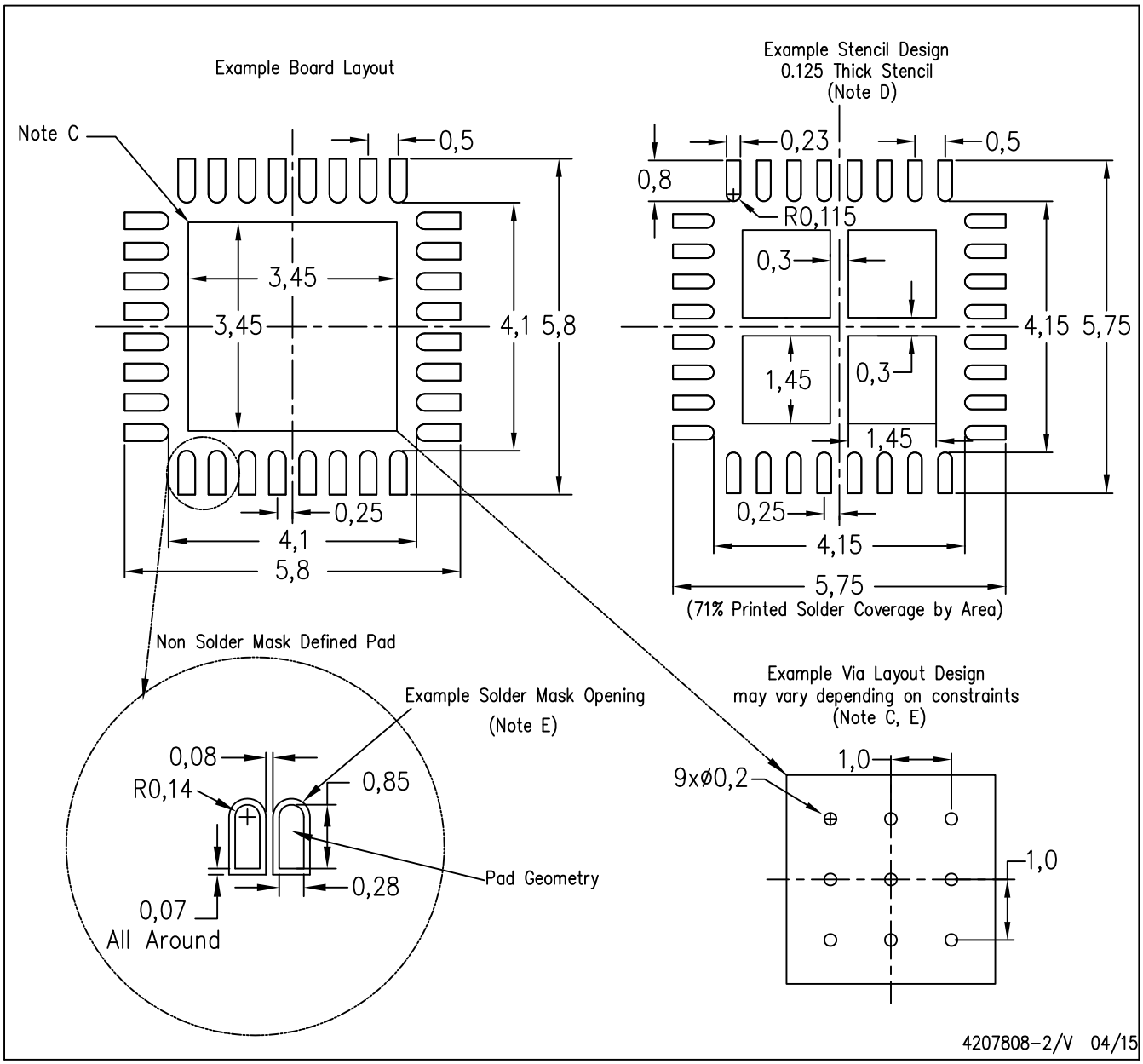
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
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B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Interface	interface.ti.com	Medical	www.ti.com/medical
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OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

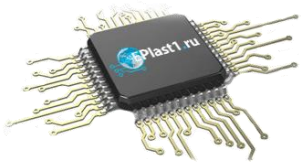
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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