

3.3 V and 2.5 V LVCMOS High-Performance Clock Buffer Family

Check for Samples: [CDCLVC11xx](#)

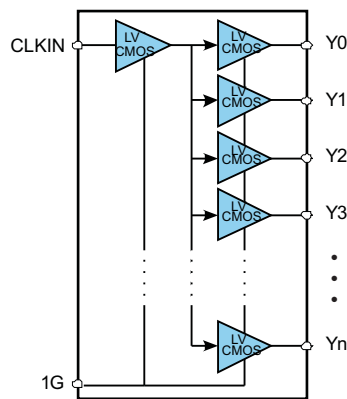
FEATURES

- High-Performance 1:2, 1:3, 1:4, 1:6, 1:8, 1:10, 1:12 LVCMOS Clock Buffer Family
- Very Low Pin-to-Pin Skew < 50 ps
- Very Low Additive Jitter < 100 fs
- Supply Voltage: 3.3 V or 2.5 V
- $f_{\max} = 250$ MHz for 3.3 V
- $f_{\max} = 180$ MHz for 2.5 V

- Operating Temperature Range: -40°C to 85°C
- Available in 8-, 14-, 16-, 20-, 24-Pin TSSOP Package (all pin compatible)

APPLICATIONS

- General Purpose Communication, Industrial and Consumer Applications



CLKIN	1		24	Y1
1G	2	CDCLVC 1102	23	Y3
Y0	3	CDCLVC 1103	22	VDD
GND	4	CDCLVC 1104	21	Y2
VDD	5		20	GND
Y4	6	CDCLVC 1106	19	Y5
GND	7		18	VDD
Y6	8	CDCLVC 1108	17	Y7
VDD	9		16	Y8
Y9	10	CDCLVC 1110	15	GND
GND	11		14	Y10
Y11	12	CDCLVC 1112	13	VDD

DESCRIPTION

The CDCLVC11xx is a modular, high-performance, low-skew, general purpose clock buffer family from Texas Instruments.

The whole family is designed with a modular approach in mind. It is intended to round up TI's series of LVCMOS clock generators.

There are 7 different fan-out variations, 1:2 to 1:12, available. All of the devices are pin compatible to each other for easy handling.

All family members share the same high performing characteristics like low additive jitter, low skew, and wide operating temperature range.

The CDCLVC11xx supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low. Also, versions with synchronized enable control for glitch free switching and three-state outputs are planned in future device options.

The CDCLVC11xx operate in a 2.5 V and 3.3 V environment and are characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE OPTIONS

CLKIN	1	8	Y 1
1G	2	7	NC
Y 0	3	6	VDD
GND	4	5	NC

CLKIN	1	8	Y 1
1G	2	7	NC
Y 0	3	6	VDD
GND	4	5	Y 2

CLKIN	1	8	Y 1
1G	2	7	Y 3
Y 0	3	6	VDD
GND	4	5	Y 2

CLKIN	1	14	Y 1
1G	2	13	Y 3
Y 0	3	12	VDD
GND	4	11	Y 2
VDD	5	10	GND
Y 4	6	9	Y 5
GND	7	8	VDD

CLKIN	1	16	Y 1
1G	2	15	Y 3
Y 0	3	14	VDD
GND	4	13	Y 2
VDD	5	12	GND
Y 4	6	11	Y 5
GND	7	10	VDD
Y 6	8	9	Y 7

CLKIN	1	20	Y 1
1G	2	19	Y 3
Y 0	3	18	VDD
GND	4	17	Y 2
VDD	5	16	GND
Y 4	6	15	Y 5
GND	7	14	VDD
Y 6	8	13	Y 7
VDD	9	12	Y 8
Y 9	10	11	GND

CLKIN	1	24	Y 1
1G	2	23	Y 3
Y 0	3	22	VDD
GND	4	21	Y 2
VDD	5	20	GND
Y 4	6	19	Y 5
GND	7	18	VDD
Y 6	8	17	Y 7
VDD	9	16	Y 8
Y 9	10	15	GND
GND	11	14	Y 10
Y 11	12	13	VDD

PIN FUNCTIONS

DEVICES	LVC MOS CLOCK INPUT	CLOCK OUTPUT ENABLE	LVC MOS CLOCK OUTPUT	SUPPLY VOLTAGE	GROUND
	CLKIN	1G	Y0, Y1, ... Y11	V _{DD}	GND
CDCLVC1102	1	2	3, 8	6	4
CDCLVC1103	1	2	3, 8, 5	6	4
CDCLVC1104	1	2	3, 8, 5, 7	6	4
CDCLVC1106	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
CDCLVC1108	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12
CDCLVC1110	1	2	3, 20, 17, 19, 6, 15, 8, 13, 10	5, 9, 14, 18	4, 7, 11, 16
CDCLVC1112	1	2	3, 24, 21, 23, 6, 19, 8, 17, 16, 10, 14, 12	5, 9, 13, 18, 22	4, 7, 11, 15, 20

OUTPUT LOGIC TABLE

INPUTS		OUTPUTS
CLKIN	1G	Y _n
X	L	L
L	H	L
H	H	H

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE / UNIT
V _{DD} Supply voltage range	–0.5 V to 4.6 V
V _{IN} Input voltage range ⁽²⁾	–0.5 V to V _{DD} + 0.5 V
V _O Output voltage range ⁽²⁾	–0.5 V to V _{DD} + 0.5 V
I _{IN} Input current	±20 mA
I _O Continuous output current	±50 mA
T _J Maximum junction temperature	125°C
T _{ST} Storage temperature range	–65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾	DCDCLVC1102/03/04	CDCLVC1106	CDCLVC1108	CDCLVC11010	CDCLVC1112	UNITS
	PW	PW	PW	PW	PW	
	8 PINS	14 PINS	16 PINS	20 PINS	24 PINS	
θ _{JA} Junction-to-ambient thermal resistance ⁽²⁾	149.4	112.6	108.4	83.0	87.9	°C/W
θ _{JC(top)} Junction-to-case(top) thermal resistance ⁽³⁾	69.4	48.0	33.6	32.3	26.5	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

					MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage range	3.3 V supply	3.0			3.3	3.6	V
		2.5 V supply	2.3			2.5	2.7	
V _{IL}	Low-level input voltage	V _{DD} = 3.0 V to 3.6 V				V _{DD} /2 – 600		mV
		V _{DD} = 2.3 V to 2.7 V				V _{DD} /2 – 400		
V _{IH}	High-level input voltage	V _{DD} = 3.0 V to 3.6 V	V _{DD} /2 + 600					mV
		V _{DD} = 2.3 V to 2.7 V	V _{DD} /2 + 400					
V _{th}	Input threshold voltage	V _{DD} = 2.3 V to 3.6 V				V _{DD} /2		mV
t _r / t _f	Input slew rate		1			4		V/ns
t _w	Minimum pulse width at CLKIN	V _{DD} = 3.0 V to 3.6 V	1.8					ns
		V _{DD} = 2.3 V to 2.7 V	2.75					
f _{CLK}	LVCMOS clock Input Frequency	V _{DD} = 3.0 V to 3.6 V	DC			250		MHz
		V _{DD} = 2.3 V to 2.7 V	DC			180		
T _A	Operating free-air temperature				–40		85	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I _{DD}	Static device current ⁽²⁾	1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V		6	10	mA
		1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 2.7 V		3	6	mA
I _{PD}	Power down current	1G = 0 V; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V or 2.7 V			60	μA
C _{PD}	Power dissipation capacitance per output ⁽³⁾	V _{DD} = 3.3 V; f = 10 MHz		6		pF
		V _{DD} = 2.5 V; f = 10 MHz		4.5		pF
I _I	Input leakage current at 1G	V _I = 0 V or V _{DD} , V _{DD} = 3.6 V or 2.7 V			± 8	μA
	Input leakage current at CLKIN				± 25	
R _{OUT}	Output impedance	V _{DD} = 3.3 V		45		Ω
		V _{DD} = 2.5 V		60		Ω
f _{OUT}	Output frequency	V _{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V _{DD} = 2.3 V to 2.7 V	DC		180	MHz
OUTPUT PARAMETERS FOR V _{DD} = 3.3 V ± 0.3 V						
V _{OH}	High-level output voltage	V _{DD} = 3 V, I _{OH} = −0.1 mA		2.9		V
		V _{DD} = 3 V, I _{OH} = −8 mA		2.5		
		V _{DD} = 3 V, I _{OH} = −12 mA		2.2		
V _{OL}	Low-level output voltage	V _{DD} = 3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DD} = 3 V, I _{OL} = 8 mA			0.5	
		V _{DD} = 3 V, I _{OL} = 12 mA			0.8	
t _{PLH} , t _{PHL}	Propagation delay	CLKIN to Yn		0.8	2.0	ns
t _{sk(o)}	Output skew	Equal load of each output			50	ps
t _r /t _f	Rise and fall time	20%–80% (V _{OH} - V _{OL})		0.3	0.8	ns
t _{DIS}	Output disable time	1G to Yn			6	ns
t _{EN}	Output enable time	1G to Yn			6	ns
t _{sk(p)}	Pulse skew ; t _{PLH} (Yn) – t _{PHL} (Yn) ⁽⁴⁾	To be measured with input duty cycle of 50%			180	ps
t _{sk(pp)}	Part-to-part skew	Under equal operating conditions for two parts			0.5	ns
t _{jitter}	Additive jitter rms	12kHz...20 MHz, f _{OUT} = 250 MHz			100	fs

(1) All typical values are at respective nominal V_{DD}. For switching characteristics, outputs are terminated to 50 Ω to V_{DD}/2 (see Figure 1).

(2) For dynamic I_{DD} over frequency see Figure 8 and Figure 9.

(3) This is the formula for the power dissipation calculation (see Figure 8 and the Power Consideration section).

$$P_{\text{tot}} = P_{\text{stat}} + P_{\text{dyn}} + P_{\text{Cload}} \text{ [W]}$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} \text{ [W]}$$

$$P_{\text{dyn}} = C_{\text{PD}} \times V_{\text{DD}}^2 \times f \text{ [W]}$$

$$P_{\text{Cload}} = C_{\text{load}} \times V_{\text{DD}}^2 \times f \times n \text{ [W]}$$

n = Number of switching output pins

(4) t_{sk(p)} depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: odc = (t_{w(OUT)} ± t_{sk(p)})/t_{period}; t_{w(OUT)} is pulse-width of output waveform and t_{period} is 1/f_{OUT}.

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP ⁽¹⁾	MAX	UNIT
OUTPUT PARAMETERS FOR $V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$					
V_{OH} High-level output voltage	$V_{DD} = 2.3\text{ V}$, $I_{OH} = -0.1\text{ mA}$	2.2			V
	$V_{DD} = 2.3\text{ V}$, $I_{OH} = -8\text{ mA}$	1.7			
V_{OL} Low-level output voltage	$V_{DD} = 2.3\text{ V}$, $I_{OL} = 0.1\text{ mA}$			0.1	V
	$V_{DD} = 2.3\text{ V}$, $I_{OL} = 8\text{ mA}$			0.5	
t_{PLH} , t_{PHL} Propagation delay	CLKIN to Yn	1.0		2.6	ns
$t_{sk(o)}$ Output skew	Equal load of each output			50	ps
t_r/t_f Rise and fall time	20%–80% reference point	0.3		1.2	ns
t_{DIS} Output disable time	1G to Yn			10	ns
t_{EN} Output enable time	1G to Yn			10	ns
$t_{sk(p)}$ Pulse skew ; $t_{PLH(Yn)} - t_{PHL(Yn)}$ ⁽⁵⁾	To be measured with input duty cycle of 50%			220	ps
$t_{sk(pp)}$ Part-to-part skew	Under equal operating conditions for two parts			1.2	ns
t_{jitter} Additive jitter rms	12kHz...20 MHz, $f_{OUT} = 180\text{ MHz}$			350	fs

(5) $t_{sk(p)}$ depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: $odc = (t_{w(OUT)} \pm t_{sk(p)})/t_{period}$; $t_{w(OUT)}$ is pulse-width of output waveform and t_{period} is $1/f_{OUT}$.

PARAMETERS MEASUREMENT INFORMATION

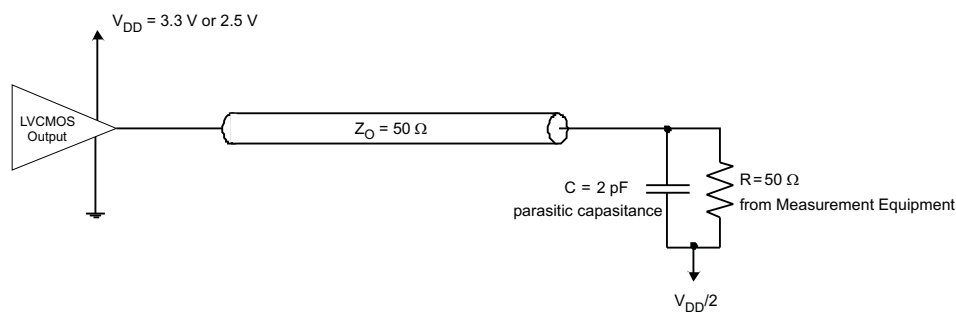


Figure 1. Test Load Circuit

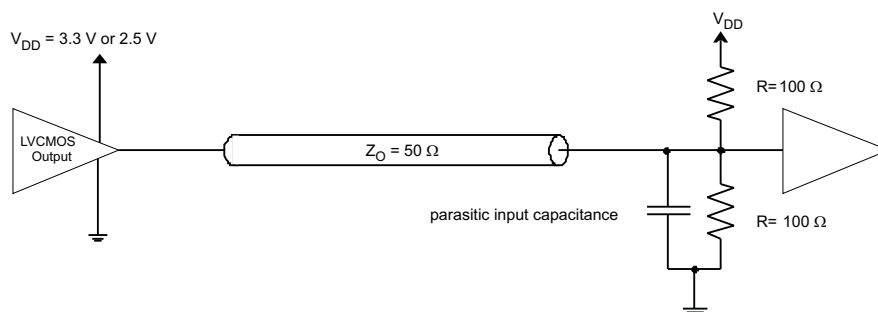


Figure 2. Application Load With 50 Ω Line Termination

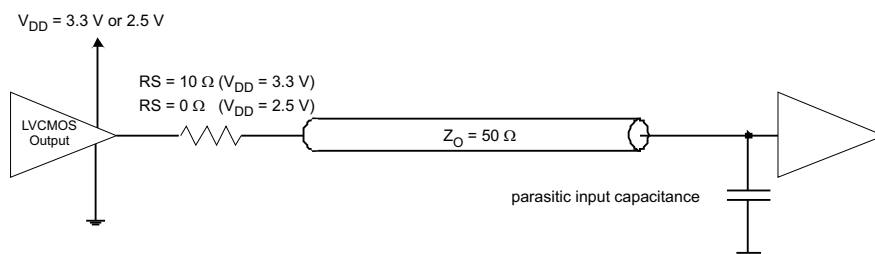


Figure 3. Application Load With Series Line Termination

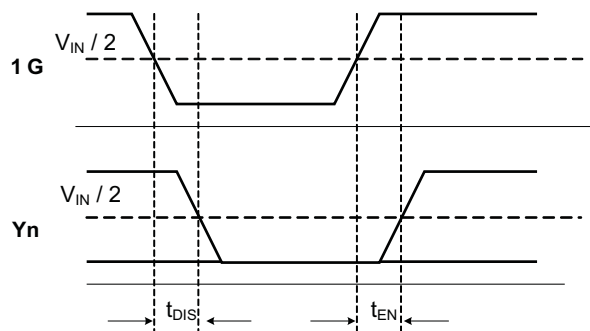


Figure 4. t_{DIS} and t_{EN} for Disable Low

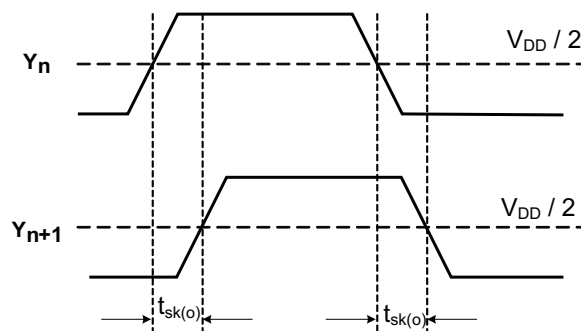
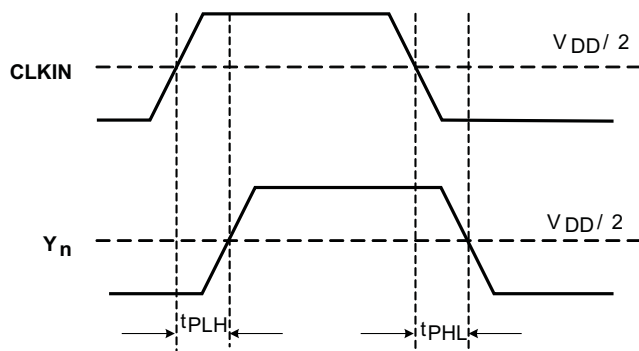


Figure 5. Output Skew $t_{sk(o)}$

PARAMETERS MEASUREMENT INFORMATION (continued)



Note: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 6. Pulse Skew $t_{sk(p)}$ and Propagation Delay t_{PLH}/t_{PHL}

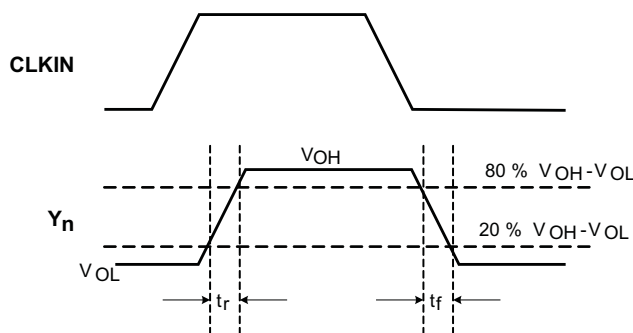


Figure 7. Rise/Fall Times t_r/t_f

TYPICAL CHARACTERISTICS

Power Consideration

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

1. Power used by the device as it switches states.
2. Power required to charge any output load.

The output load can be capacitive only or capacitive and resistive. The following formula and the power graphs in [Figure 8](#) and [Figure 9](#) can be used to obtain the power consumption of the device:

$$P_{dev} = P_{stat} + n (P_{dyn} + P_{Cload})$$

$$P_{stat} = V_{DD} \times I_{DD}$$

$$P_{dyn} + P_{Cload} = \text{see Figure 8 and Figure 9}$$

where:

V_{DD} = Supply voltage (3.3 V or 2.5 V)

I_{DD} = Static device current (typ 6 mA for $V_{DD} = 3.3$ V; typ 3 mA for $V_{DD} = 2.5$ V)

n = Number of switching output pins

Example for Device Power Consumption for CDCLVC1104: 4 outputs are switching, $f = 120$ MHz, $V_{DD} = 3.3$ V and $C_{load} = 2$ pF per output:

$$P_{dev} = P_{stat} + n (P_{dyn} + P_{Cload}) = 19.8 \text{ mW} + 40 \text{ mW} = 59.8 \text{ mW}$$

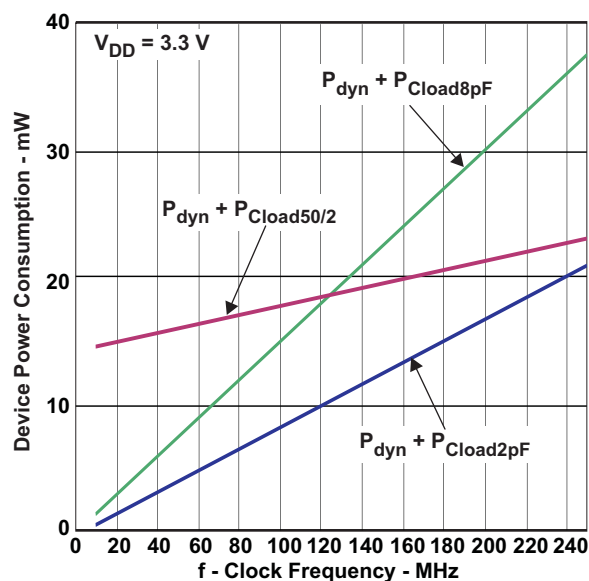
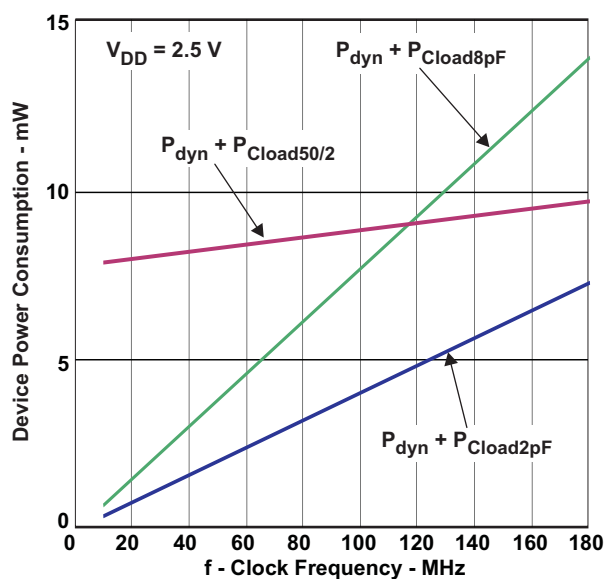
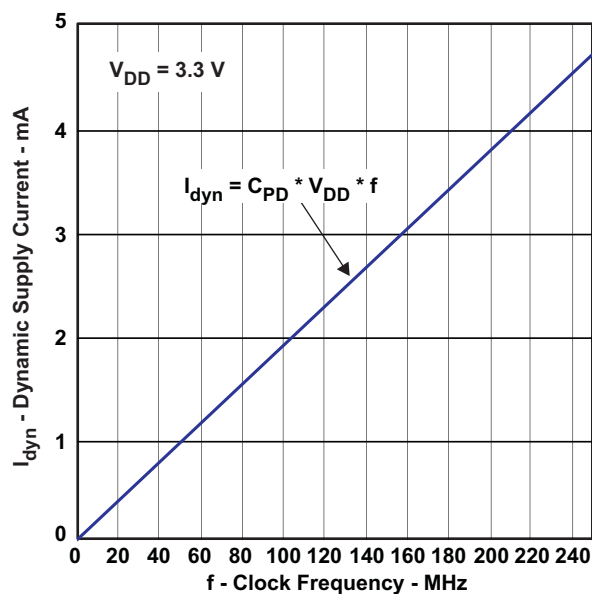
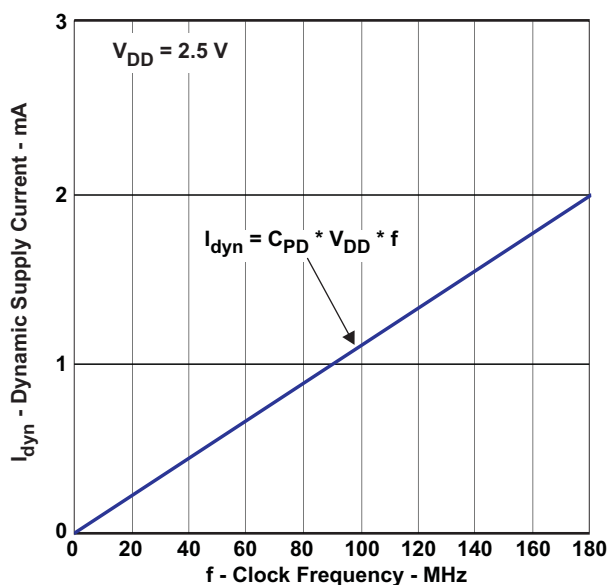
$$P_{stat} = V_{DD} \times I_{DD} = 6 \text{ mA} \times 3.3 \text{ V} = 19.8 \text{ mW}$$

$$n (P_{dyn} + P_{Cload}) = 4 \times 10 \text{ mW} = 40 \text{ mW}$$

NOTE

For dimensioning the power supply, the total power consumption needs to be considered. The total power consumption is the sum of the device power consumption and the power consumption of the load.

TYPICAL CHARACTERISTICS (continued)

Figure 8. Device Power Consumption vs Clock Frequency (Load 50Ω into $V_{DD}/2$, 2pF, 8pF; Per Output)Figure 9. Device Power Consumption vs Clock Frequency (Load 50Ω into $V_{DD}/2$, 2pF, 8pF; Per Output)Figure 10. Dynamic Supply Current vs Clock Frequency ($C_{PD} = 6\text{pF}$, No Load; Per Output)Figure 11. Dynamic Supply Current vs Clock Frequency ($C_{PD} = 4.5\text{pF}$, No Load; Per Output)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCLVC1102PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1102PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1103PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1103PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCLVC1104PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1104PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCLVC1106PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1106PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCLVC1108PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1108PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCLVC1110PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1110PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
CDCLVC1112PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CDCLVC1112PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVC1102PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1103PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1104PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
CDCLVC1106PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1108PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCLVC1110PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CDCLVC1112PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

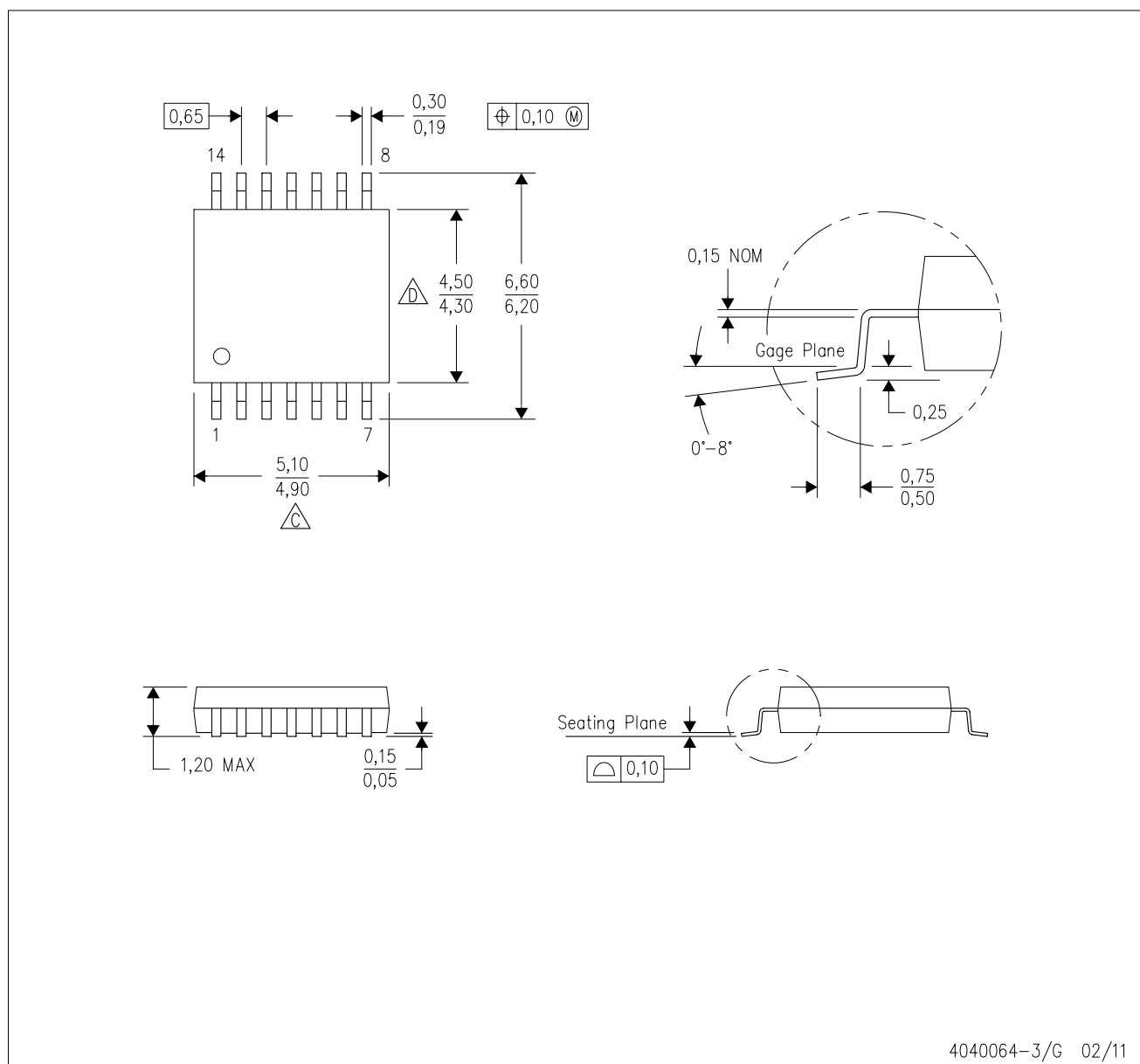


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVC1102PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
CDCLVC1103PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
CDCLVC1104PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
CDCLVC1106PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CDCLVC1108PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CDCLVC1110PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
CDCLVC1112PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R-PDSO-G14)

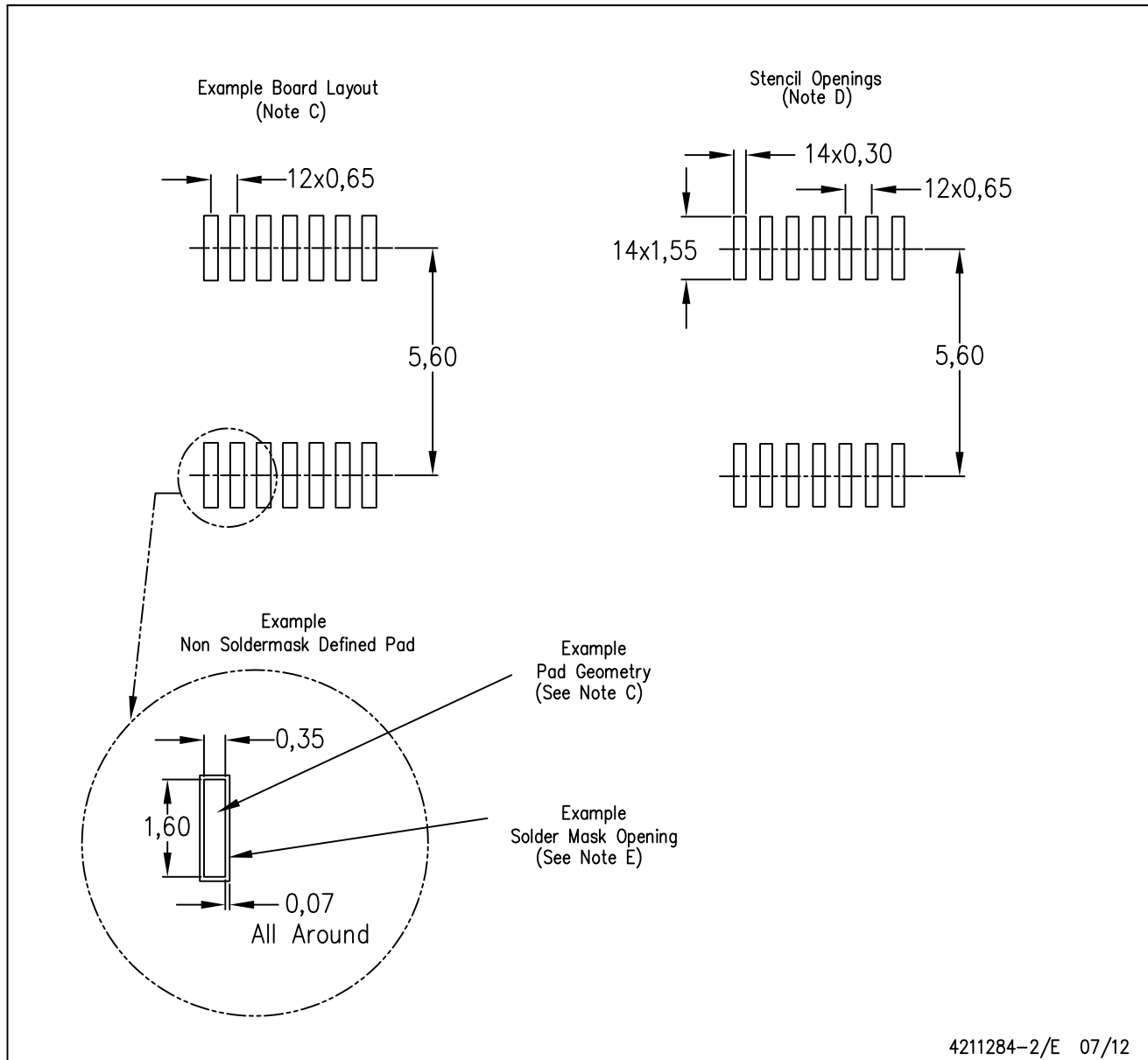
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

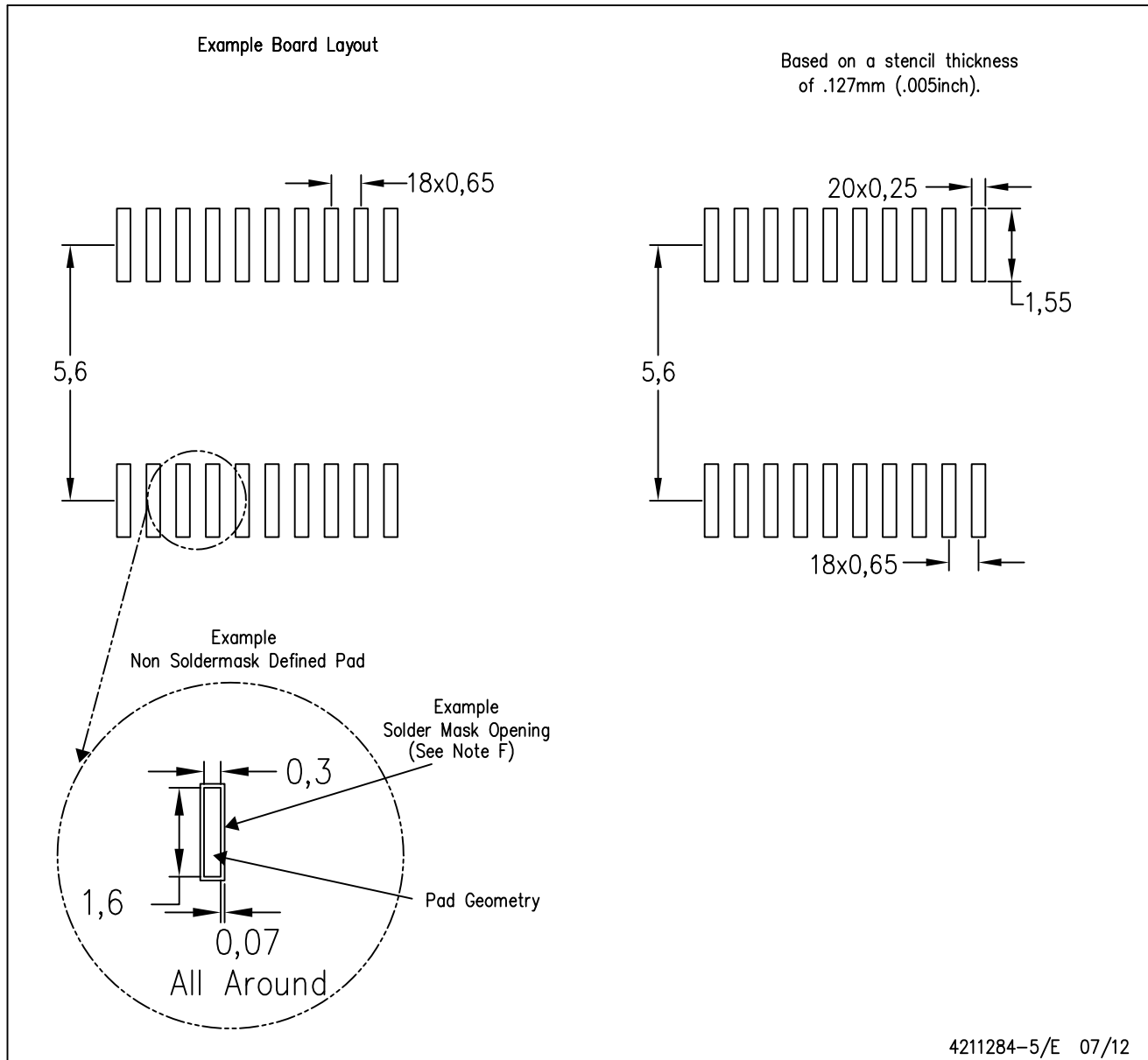
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

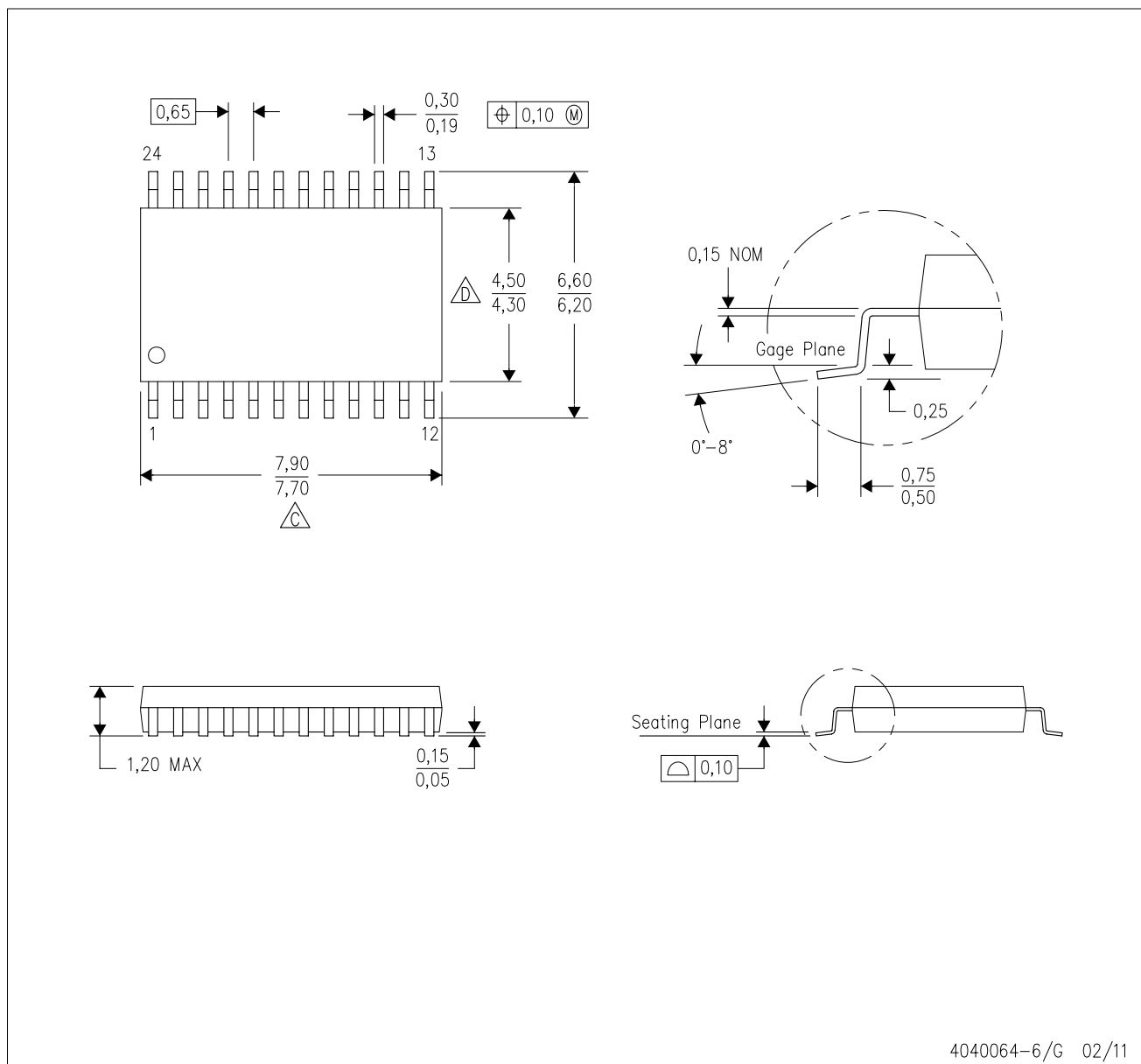
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G24)

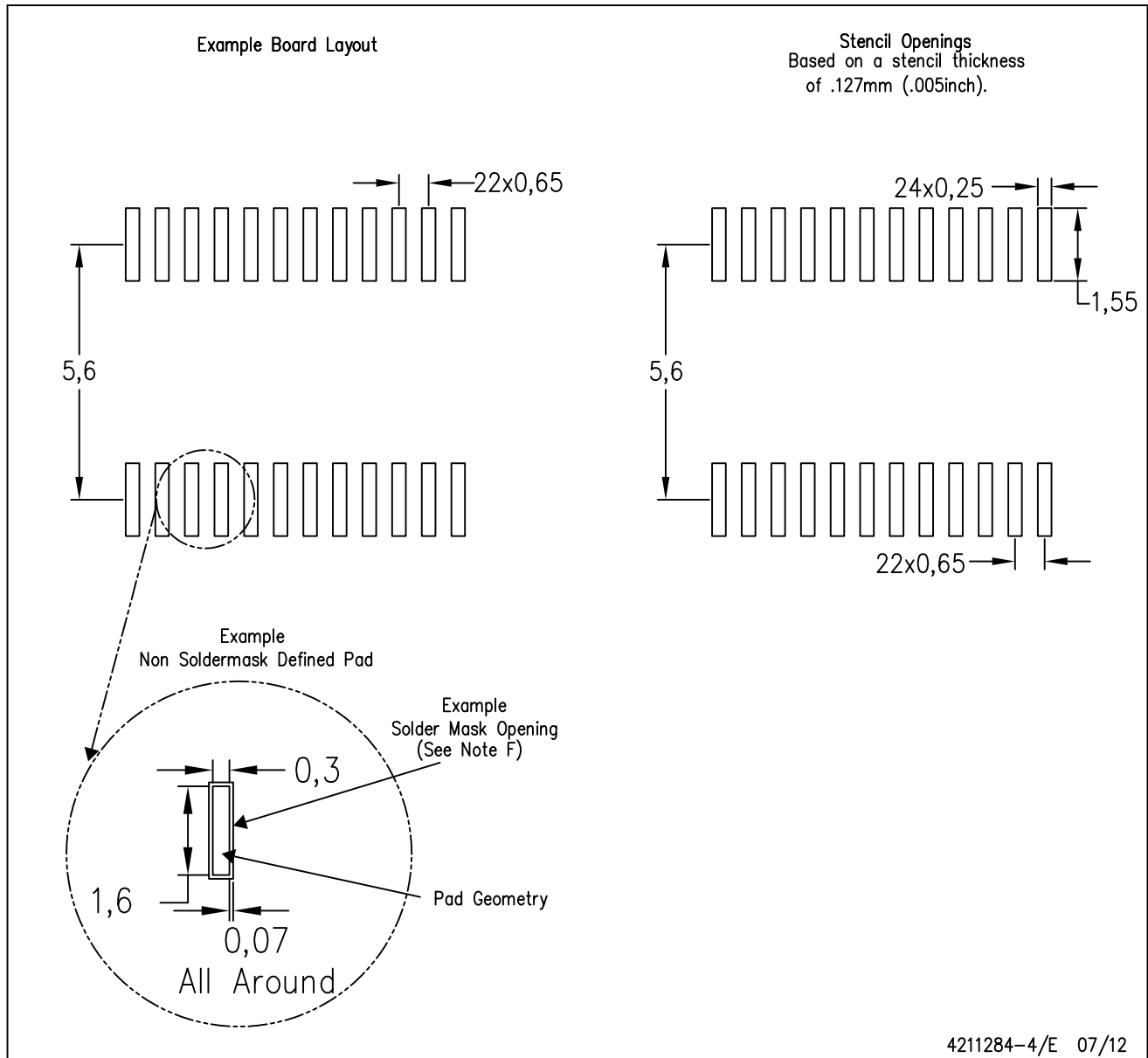
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

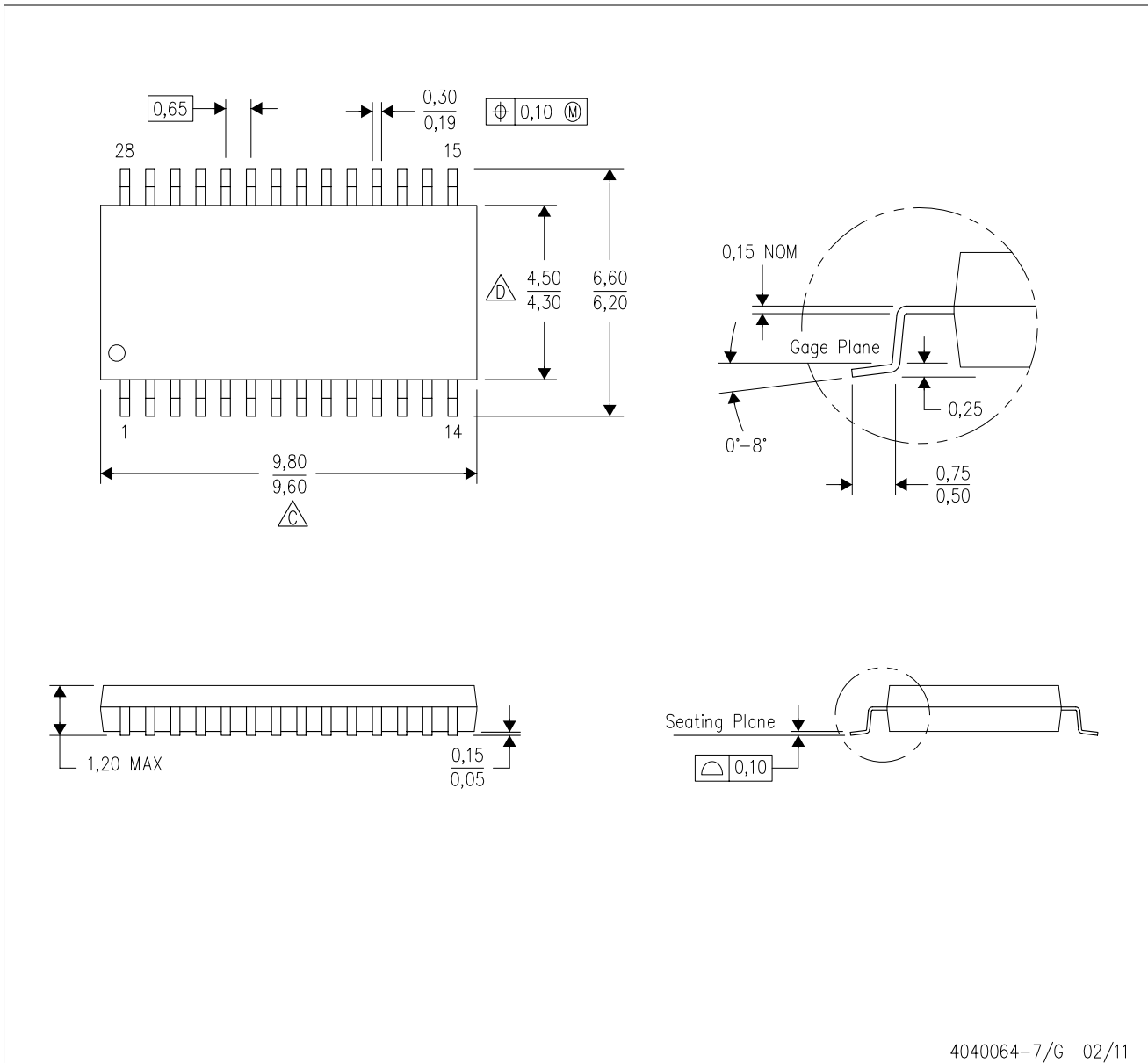
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

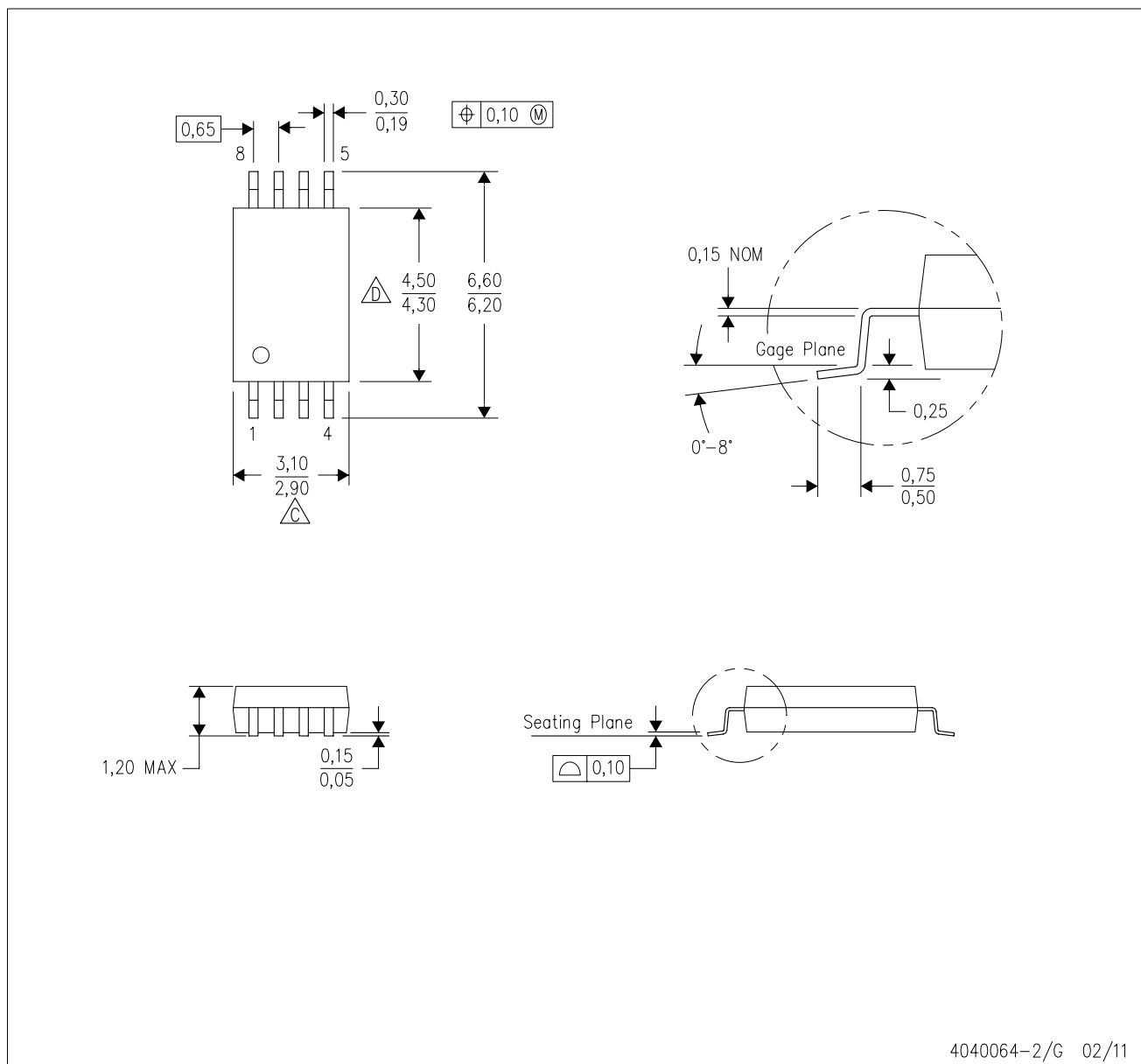
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Техническая поддержка проекта;
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Как с нами связаться

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