

LMX2330U/LMX2331U/LMX2332U

PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

LMX2330U 2.5 GHz/600 MHz

LMX2331U 2.0 GHz/600 MHz

LMX2332U 1.2 GHz/600 MHz

General Description

The LMX233xU devices are high performance frequency synthesizers with integrated dual modulus prescalers. The LMX233xU devices are designed for use as RF and IF local oscillators for dual conversion radio transceivers.

A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler. Using a proprietary digital phase locked loop technique, the LMX233xU devices generate very stable, low noise control signals for RF and IF voltage controlled oscillators. Both the RF and IF synthesizers include a two-level programmable charge pump. The RF synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three-wire interface (Data, LE, Clock). Supply voltages from 2.7V to 5.5V are supported. The LMX233xU family features ultra low current consumption:

LMX2330U (2.5 GHz)—3.3 mA, LMX2331U (2.0 GHz)—2.9 mA, LMX2332U (1.2 GHz)—2.5 mA at 3.0V.

The LMX233xU devices are available in 20-Pin TSSOP and 24-Pin CSP surface mount plastic packages.

Features

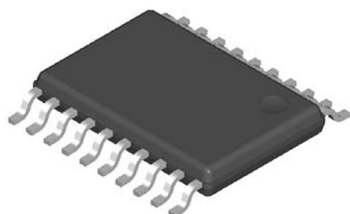
- Ultra Low Current Consumption
- Upgrade and Compatible to LMX233xL Family
- 2.7V to 5.5V Operation
- Selectable Synchronous or Asynchronous Powerdown Mode:
 $I_{CC-PWDN} = 1 \mu A$ typical
- Selectable Dual Modulus Prescaler:

LMX2330U	RF: 32/33 or 64/65
LMX2331U	RF: 64/65 or 128/129
LMX2332U	RF: 64/65 or 128/129
LMX2330U/31U/32U	IF: 8/9 or 16/17
- Selectable Charge Pump TRI-STATE® Mode
- Programmable Charge Pump Current Levels
 RF and IF: 0.95 or 3.8 mA
- Selectable Fastlock™ Mode for the RF Synthesizer
- Push-Pull Analog Lock Detect Output
- Available in 20-Pin TSSOP and 24-Pin Chip Scale Package (CSP)

Applications

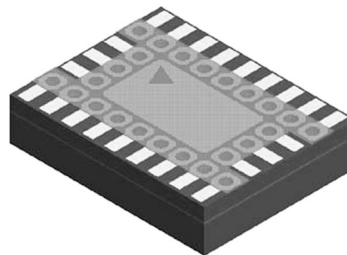
- Mobile Handsets
 (GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS)
- Cordless Handsets
 (DECT, DCT)
- Wireless Data
- Cable TV Tuners

Thin Shrink Small Outline Package (MTC20)



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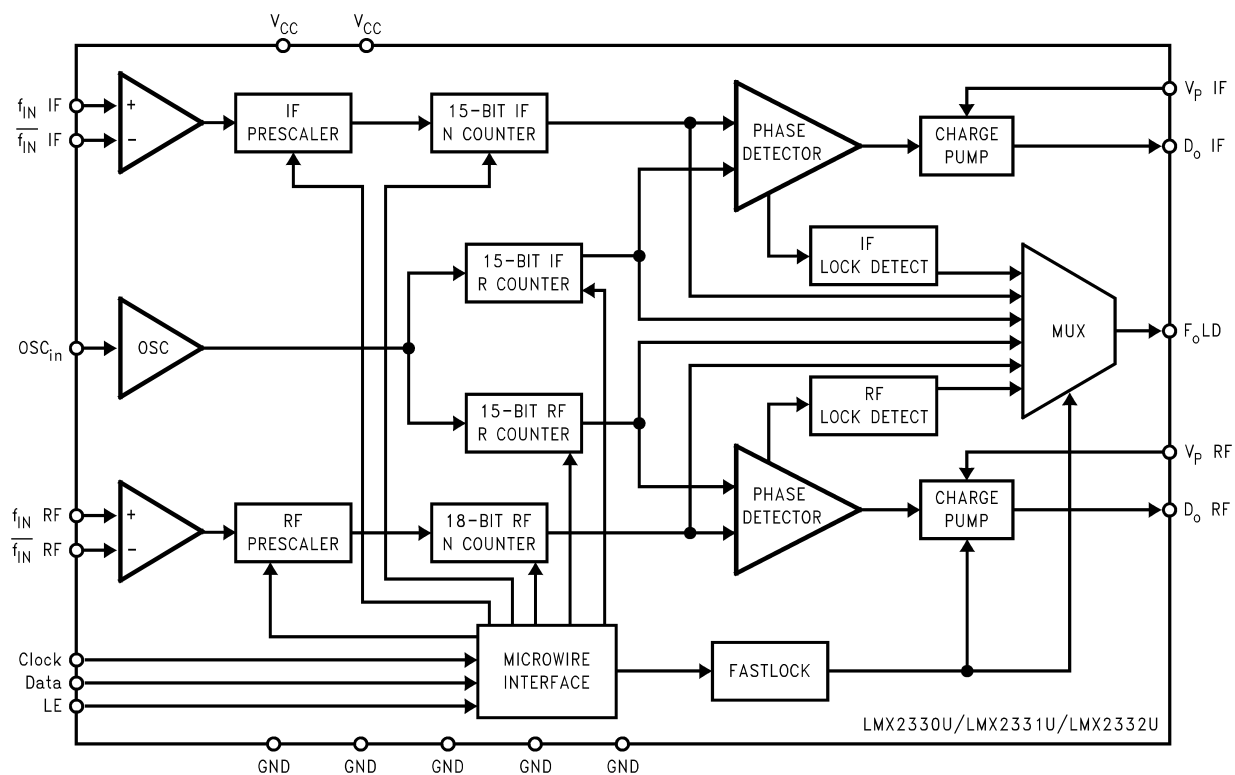
Chip Scale Package (SLB24A)



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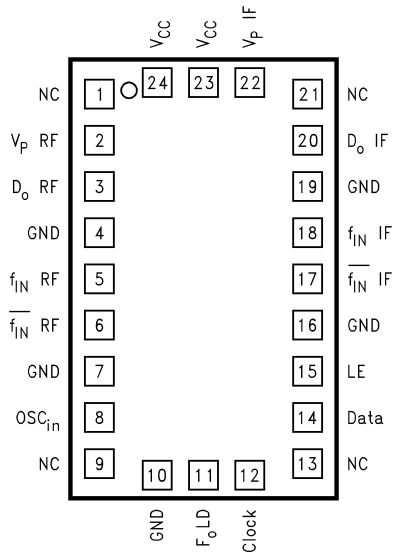
Functional Block Diagram



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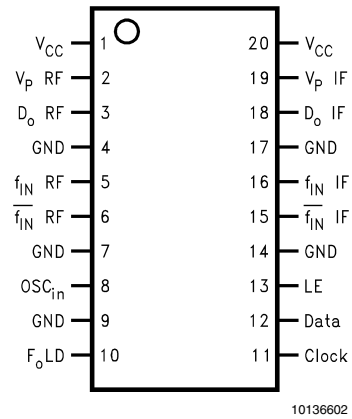
Connection Diagrams

Chip Scale Package (SLB)
(Top View)



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Thin Shrink Small Outline Package (TM)
(Top View)



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Pin Descriptions

Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
V _{CC}	24	1	—	Power supply bias for the RF PLL analog and digital circuits. V _{CC} may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
V _P RF	2	2	—	RF PLL charge pump power supply. Must be ≥ V _{CC} .
D _O RF	3	3	O	RF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	4	4	—	Ground for the RF PLL digital circuitry.
f _{IN} RF	5	5	I	RF PLL prescaler input. Small signal input from the VCO.
f _{IN} RF	6	6	I	RF PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX233xU RF PLL can be driven differentially when the bypass capacitor is omitted.
GND	7	7	—	Ground for the RF PLL analog circuitry.
OSC _{in}	8	8	I	Reference oscillator input. The input has an approximate V _{CC} /2 threshold and can be driven from an external CMOS or TTL logic gate.
GND	10	9	—	Ground for the IF PLL digital circuits, MICROWIRE™, F _O LD, and oscillator circuits.
F _O LD	11	10	O	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, RF/IF PLL push-pull analog lock detect output, N and R divider output or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	12	11	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	14	12	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is shifted in first. The last two bits are the control bits.
LE	15	13	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift register is loaded into one of 4 internal control registers.
GND	16	14	—	Ground for the IF PLL analog circuitry.

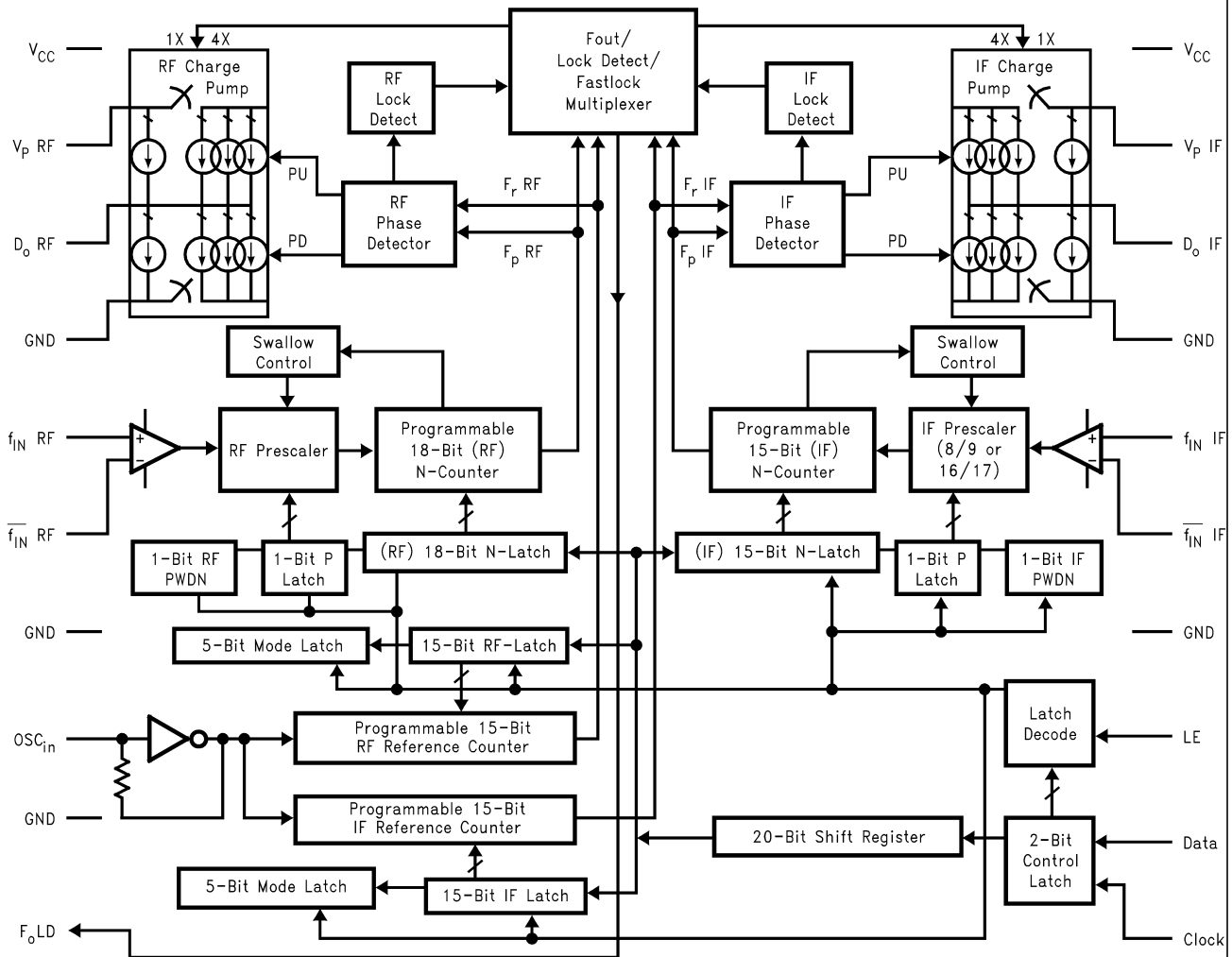
Pin Descriptions (Continued)

Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
$\overline{f_{IN}}$ IF	17	15	I	IF PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX233xU IF PLL can be driven differentially when the bypass capacitor is omitted.
f_{IN} IF	18	16	I	IF PLL prescaler input. Small signal input from the VCO.
GND	19	17	—	Ground for the IF PLL digital circuitry, MICROWIRE, F_{oLD} , and oscillator circuits.
D_o IF	20	18	O	IF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
V_P IF	22	19	—	IF PLL charge pump power supply. Must be $\geq V_{CC}$.
V_{CC}	23	20	—	Power supply bias for the IF PLL analog and digital circuits, MICROWIRE, F_{oLD} , and oscillator circuits. V_{CC} may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
NC	1, 9, 13, 21	X	—	No connect.

Ordering Information

Model	Temperature Range	Package Description	Packing	NS Package Number
LMX2330USLBX	–40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2330UTM	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2330UTMX	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2331USLBX	–40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2331UTM	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2331UTMX	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2332USLBX	–40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2332UTM	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2332UTMX	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20

Detailed Block Diagram



Notes:

1. A 64/65 or 128/129 prescaler ratio can be selected for the LMX2331U and LMX2332U RF synthesizers. A 32/33 or 64/65 prescaler ratio can be selected for the LMX2330U RF synthesizer.
2. V_{CC} supplies power to the RF and IF prescalers, RF and IF feedback dividers, RF and IF reference dividers, RF and IF phase detectors, the OSC_{in} buffer, MICROWIRE, and F_{0LD} circuitry.
3. V_P RF and V_P IF supply power to the charge pumps. They can be run separately as long as V_P RF $\geq V_{CC}$ and V_P IF $\geq V_{CC}$.

Absolute Maximum Ratings (Notes 1,

2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage

V_{CC} to GND	−0.3V to +6.5V
V_P RF to GND	−0.3V to +6.5V
V_P IF to GND	−0.3V to +6.5V

Voltage on any pin to GND (V_I)

V_I must be < +6.5V	−0.3V to $V_{CC}+0.3V$
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Storage Temperature Range (T_S)Lead Temperature (solder 4 s) (T_L)TSSOP θ_{JA} Thermal ImpedanceCSP θ_{JA} Thermal Impedance**Recommended Operating Conditions** (Note 1)

Power Supply Voltage

V_{CC} to GND	+2.7V to +5.5V
V_P RF to GND	V_{CC} to +5.5V
V_P IF to GND	V_{CC} to +5.5V

Operating Temperature (T_A)

−40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

Note 3: GND = 0V

Electrical Characteristics

$V_{CC} = V_P$ RF = V_P IF = 3.0V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units	
			Min	Typ	Max		
I _{CC} PARAMETERS							
I _{CCRF + IF}	Power Supply Current, RF + IF Synthesizers	LMX2330U	Clock, Data and LE = GND		3.3	4.3	mA
		LMX2331U	OSC _{in} = GND		2.9	3.8	mA
			PWDN RF Bit = 0				
		LMX2332U	PWDN IF Bit = 0		2.5	3.3	mA
I _{CCRF}	Power Supply Current, RF Synthesizer Only	LMX2330U	Clock, Data and LE = GND		2.3	3.0	mA
		LMX2331U	OSC _{in} = GND		1.9	2.5	mA
			PWDN RF Bit = 0				
		LMX2332U	PWDN IF Bit = 1		1.5	2.0	mA
I _{CCIF}	Power Supply Current, IF Synthesizer Only	LMX233xU	Clock, Data and LE = GND OSC _{in} = GND PWDN RF Bit = 1 PWDN IF Bit = 0		1.0	1.3	mA
I _{CC-PWDN}	Powerdown Current	LMX233xU	Clock, Data and LE = GND OSC _{in} = GND PWDN RF Bit = 1 PWDN IF Bit = 1		1.0	10.0	μA
RF SYNTHESIZER PARAMETERS							
f _{IN} RF	RF Operating Frequency	LMX2330U		500		2500	MHz
		LMX2331U		200		2000	MHz
		LMX2332U		100		1200	MHz
N _{RF}	RF N Divider Range		Prescaler = 32/33 (Note 4)	96		65631	
			Prescaler = 64/65 (Note 4)	192		131135	
			Prescaler = 128/129 (Note 4)	384		262143	
R _{RF}	RF R Divider Range			3		32767	
F _{φRF}	RF Phase Detector Frequency					10	MHz

Electrical Characteristics (Continued) $V_{CC} = V_P$ RF = V_P IF = 3.0V, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
RF SYNTHESIZER PARAMETERS						
Pf _{IN} RF	RF Input Sensitivity	2.7V ≤ V _{CC} ≤ 3.0V (Note 5)	-15		0	dBm
		3.0 < V _{CC} ≤ 5.5V (Note 5)	-10		0	dBm
ID _O RF SOURCE	RF Charge Pump Output Source Current	VD _O RF = V _P RF/2 ID _O RF Bit = 0 (Note 6)		-0.95		mA
		VD _O RF = V _P RF/2 ID _O RF Bit = 1 (Note 6)		-3.80		mA
ID _O RF SINK	RF Charge Pump Output Sink Current	VD _O RF = V _P RF/2 ID _O RF Bit = 0 (Note 6)		0.95		mA
		VD _O RF = V _P RF/2 ID _O RF Bit = 1 (Note 6)		3.80		mA
ID _O RF TRI-STATE	RF Charge Pump Output TRI-STATE Current	0.5V ≤ VD _O RF ≤ V _P RF - 0.5V (Note 6)	-2.5		2.5	nA
ID _O RF SINK Vs ID _O RF SOURCE	RF Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD _O RF = V _P RF/2 T _A = +25°C (Note 7)		3	10	%
ID _O RF Vs VD _O RF	RF Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	0.5V ≤ VD _O RF ≤ V _P RF - 0.5V T _A = +25°C (Note 7)		10	15	%
ID _O RF Vs T _A	RF Charge Pump Output Current Magnitude Variation Vs Temperature	VD _O RF = V _P RF/2 (Note 7)		10		%
IF SYNTHESIZER PARAMETERS						
f _{IN} IF	IF Operating Frequency	LMX2330U	45		600	MHz
		LMX2331U	45		600	MHz
		LMX2332U	45		600	MHz
N _{IF}	IF N Divider Range	Prescaler = 8/9 (Note 4)	24		16391	
		Prescaler = 16/17 (Note 4)	48		32767	
R _{IF}	IF R Divider Range		3		32767	
F _{oIF}	IF Phase Detector Frequency				10	MHz
Pf _{IN} IF	IF Input Sensitivity	2.7V ≤ V _{CC} ≤ 5.5V (Note 5)	-10		0	dBm

Electrical Characteristics (Continued) $V_{CC} = V_P$ RF = V_P IF = 3.0V, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
IF SYNTHESIZER PARAMETERS						
ID _O IF SOURCE	IF Charge Pump Output Source Current	VD _O IF = V _P IF/2 ID _O IF Bit = 0 (Note 6)		-0.95		mA
		VD _O IF = V _P IF/2 ID _O IF Bit = 1 (Note 6)		-3.80		mA
ID _O IF SINK	IF Charge Pump Output Sink Current	VD _O IF = V _P IF/2 ID _O IF Bit = 0 (Note 6)		0.95		mA
		VD _O IF = V _P IF/2 ID _O IF Bit = 1 (Note 6)		3.80		mA
ID _O IF TRI-STATE	IF Charge Pump Output TRI-STATE Current	0.5V ≤ VD _O IF ≤ V _P IF - 0.5V (Note 6)	-2.5		2.5	nA
ID _O IF SINK Vs ID _O IF SOURCE	IF Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD _O IF = V _P IF/2 T _A = +25°C (Note 7)		3	10	%
ID _O IF Vs VD _O IF	IF Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	0.5V ≤ VD _O IF ≤ V _P IF - 0.5V T _A = +25°C (Note 7)		10	15	%
ID _O IF Vs T _A	IF Charge Pump Output Current Magnitude Variation Vs Temperature	VD _O IF = V _P IF/2 (Note 7)		10		%
OSCILLATOR PARAMETERS						
F _{OSC}	Oscillator Operating Frequency		2		40	MHz
V _{OSC}	Oscillator Sensitivity	(Note 8)	0.5		V _{CC}	V _{PP}
I _{OSC}	Oscillator Input Current	V _{OSC} = V _{CC} = 5.5V			100	μA
		V _{OSC} = 0V, V _{CC} = 5.5V	-100			μA
DIGITAL INTERFACE (Data, LE, Clock, F _{oLD})						
V _{IH}	High-Level Input Voltage		0.8 V _{CC}			V
V _{IL}	Low-Level Input Voltage				0.2 V _{CC}	V
I _{IH}	High-Level Input Current	V _{IH} = V _{CC} = 5.5V	-1.0		1.0	μA
I _{IL}	Low-Level Input Current	V _{IL} = 0V, V _{CC} = 5.5V	-1.0		1.0	μA
V _{OH}	High-Level Output Voltage	I _{OH} = -500 μA	V _{CC} - 0.4			V
V _{OL}	Low-Level Output Voltage	I _{OL} = 500 μA			0.4	V
MICROWIRE INTERFACE						
t _{CS}	Data to Clock Set Up Time	(Note 9)	50			ns
t _{CH}	Data to Clock Hold Time	(Note 9)	10			ns
t _{CWH}	Clock Pulse Width HIGH	(Note 9)	50			ns
t _{CWL}	Clock Pulse Width LOW	(Note 9)	50			ns
t _{ES}	Clock to Load Enable Set Up Time	(Note 9)	50			ns
t _{EW}	Latch Enable Pulse Width	(Note 9)	50			ns

Electrical Characteristics (Continued)

$V_{CC} = V_P$ RF = V_P IF = 3.0V, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
PHASE NOISE CHARACTERISTICS							
L _N (f) RF	RF Synthesizer Normalized Phase Noise Contribution (Note 10)		TCXO Reference Source ID _O RF Bit = 1		-212.0		dBc/Hz
L(f) RF	RF Synthesizer Single Side Band Phase Noise Measured	LMX2330U	f _{IN} RF = 2450 MHz f = 1 kHz Offset F _{ΦRF} = 200 kHz Loop Bandwidth = 7.5 kHz N = 12250 F _{OSC} = 10 MHz V _{OSC} = 0.632 V _{PP} ID _O RF Bit = 1 PWDN IF Bit = 1 T _A = +25°C (Note 11)		-77.24		dBc/Hz
		LMX2331U	f _{IN} RF = 1960 MHz f = 1 kHz Offset F _{ΦRF} = 200 kHz Loop Bandwidth = 15 kHz N = 9800 F _{OSC} = 10 MHz V _{OSC} = 0.632 V _{PP} ID _O RF Bit = 1 PWDN IF Bit = 1 T _A = +25°C (Note 11)		-79.18		dBc/Hz
		LMX2332U	f _{IN} RF = 900 MHz f = 1 kHz Offset F _{ΦRF} = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F _{OSC} = 10 MHz V _{OSC} = 0.632 V _{PP} ID _O RF Bit = 1 PWDN IF Bit = 1 T _A = +25°C (Note 11)		-85.94		dBc/Hz

Electrical Characteristics (Continued)

$V_{CC} = V_P$ RF = V_P IF = 3.0V, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
PHASE NOISE CHARACTERISTICS							
L _N (f) IF	IF Synthesizer Normalized Phase Noise Contribution (Note 10)		TCXO Reference Source ID _O IF Bit = 1		-212.0		dBc/Hz
L(f) IF	IF Synthesizer Single Side Band Phase Noise Measured	LMX233xU	f _{IN} IF = 200 MHz f = 1 kHz Offset F _{φIF} = 200 kHz Loop Bandwidth = 18 kHz N = 1000 F _{OSC} = 10 MHz V _{OSC} = 0.632 V _{PP} ID _O IF Bit = 1 PWDN RF Bit = 1 T _A = +25°C (Note 11)		-99.00		dBc/Hz

Note 4: Some of the values in this range are illegal divide ratios ($B < A$). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use $N \geq P * (P-1)$, where P is the value of the prescaler selected.

Note 5: Refer to the LMX233xU f_{IN} Sensitivity Test Setup section

Note 6: Refer to the LMX233xU Charge Pump Test Setup section

Note 7: Refer to the Charge Pump Current Specification Definitions for details on how these measurements are made.

Note 8: Refer to the LMX233xU OSC_{in} Sensitivity Test Setup section

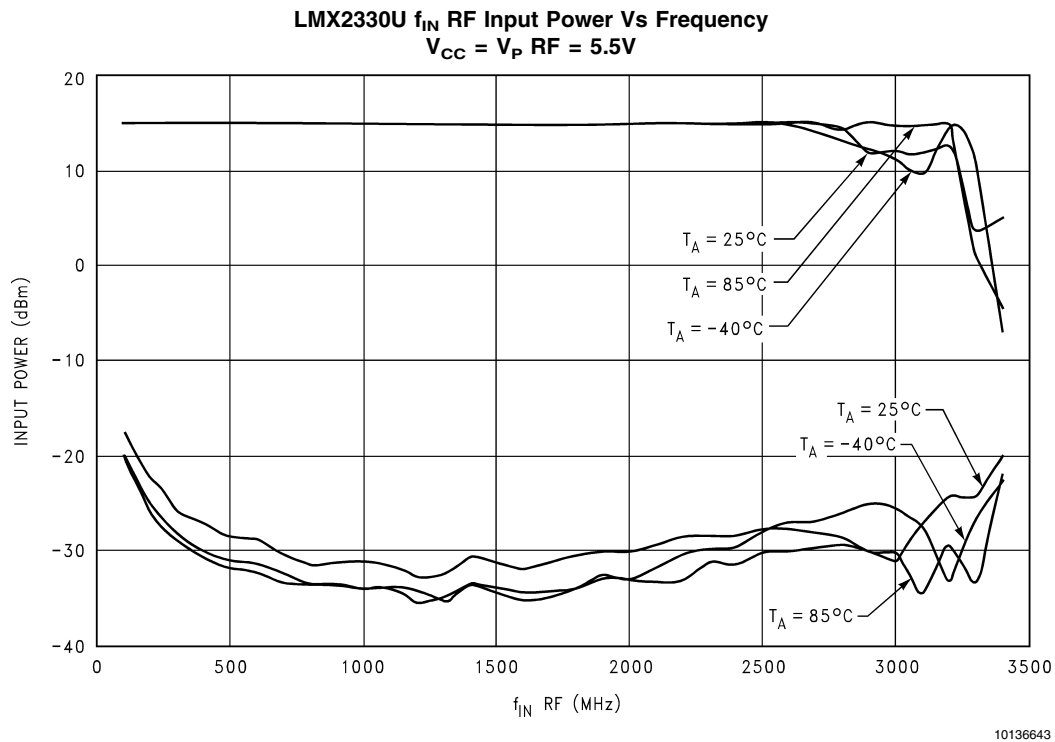
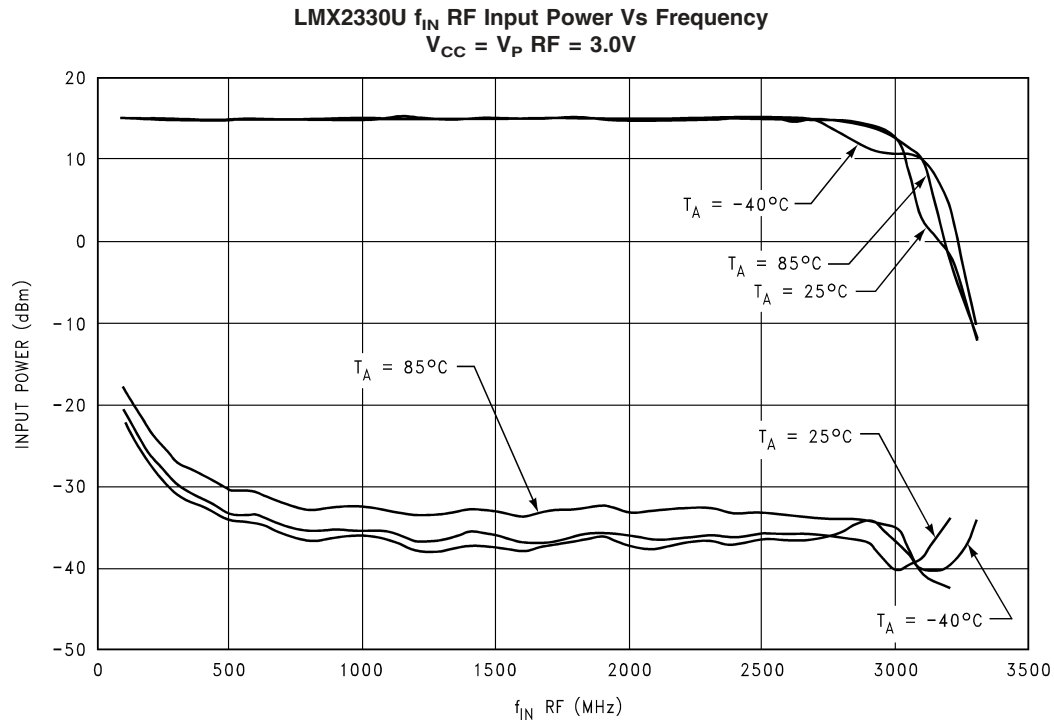
Note 9: Refer to the LMX233xU Serial Data Input Timing section

Note 10: Normalized Phase Noise Contribution is defined as : $L_N(f) = L(f) - 20 \log(N) - 10 \log(F_{\phi})$, where $L(f)$ is defined as the single side band phase noise measured at an offset frequency, f , in a 1 Hz bandwidth. The offset frequency, f , must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source. N is the value selected for the feedback divider and F_{ϕ} is the RF/IF phase detector comparison frequency.

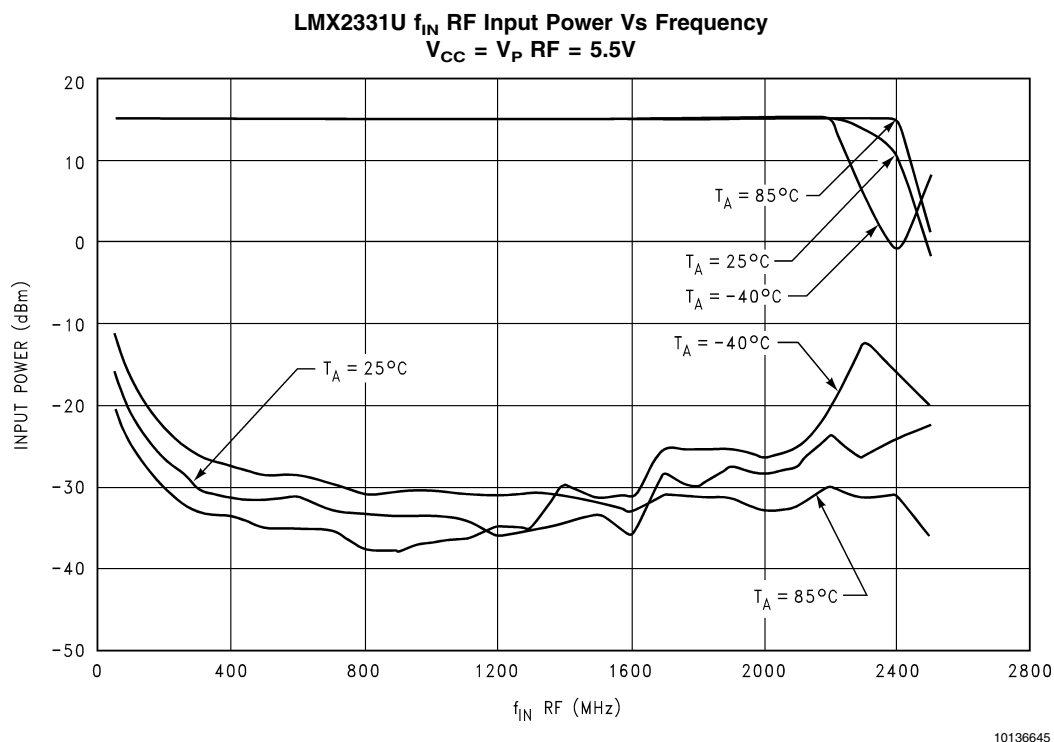
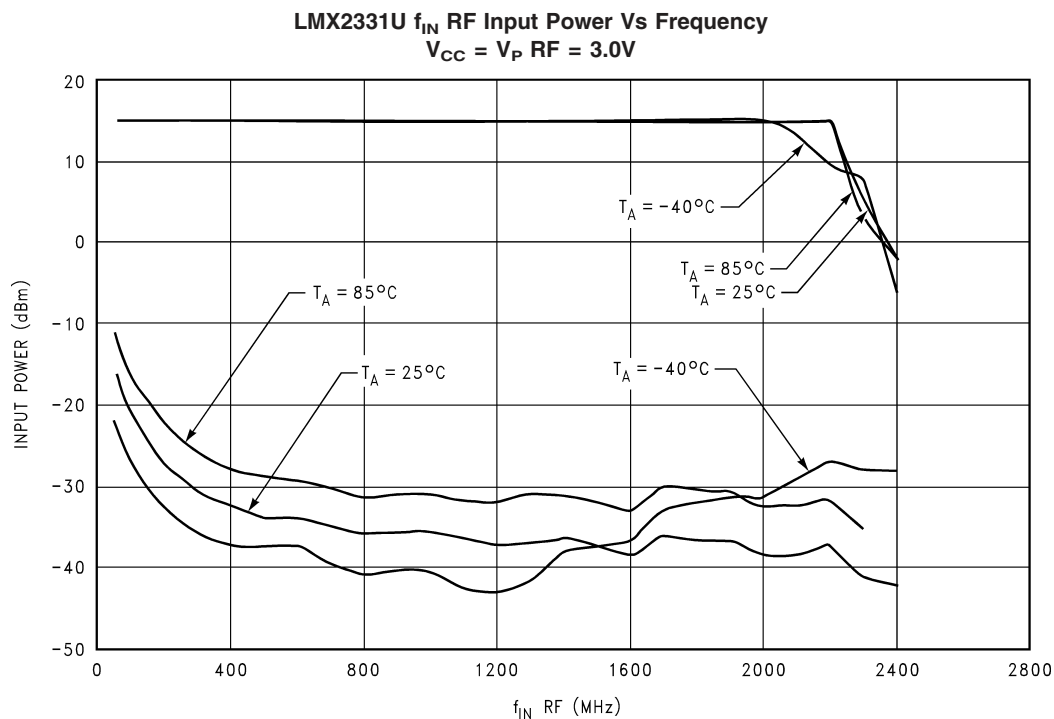
Note 11: The synthesizer phase noise is measured with the LMX2330TMEB/LMX2330SLBEB Evaluation boards and the HP8566B Spectrum Analyzer.

Typical Performance Characteristics

Sensitivity

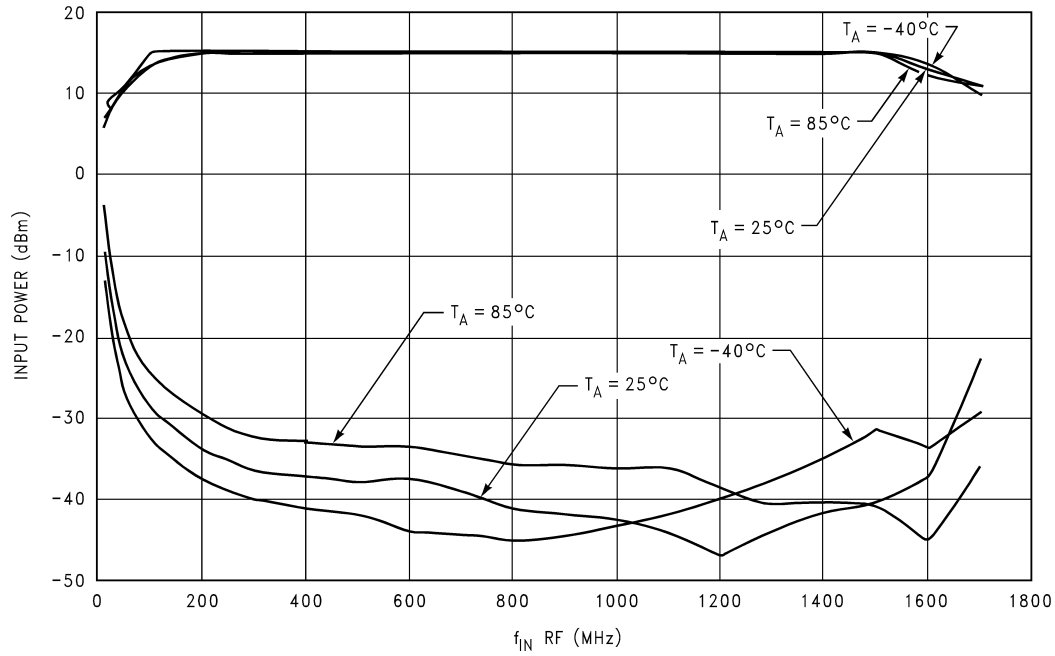


Typical Performance Characteristics Sensitivity (Continued)

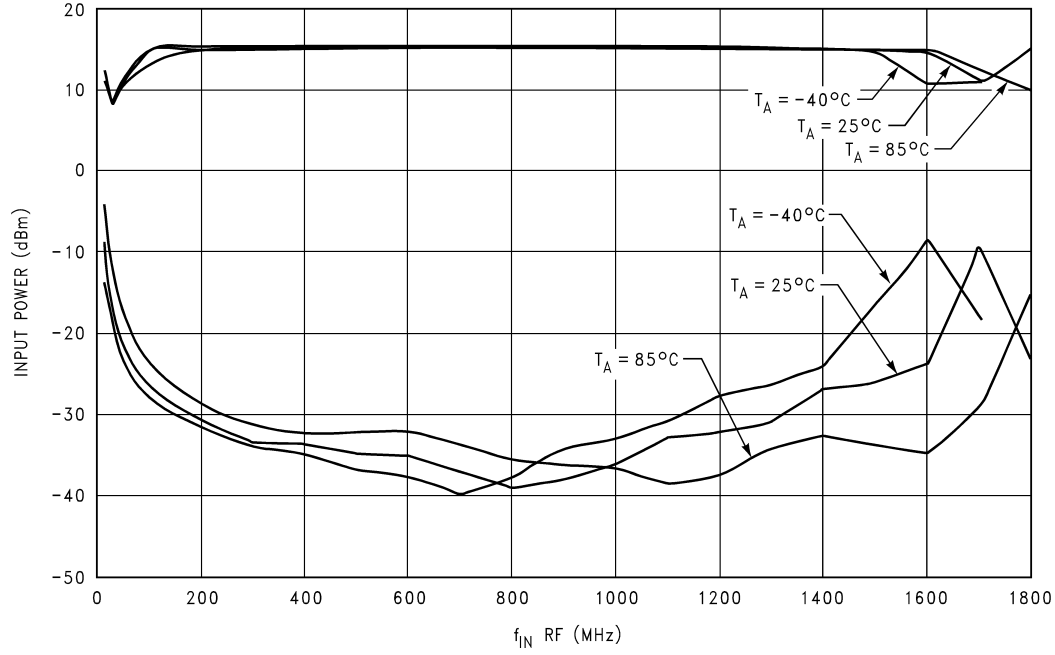


Typical Performance Characteristics Sensitivity (Continued)

LMX2332U f_{IN} RF Input Power Vs Frequency
 $V_{CC} = V_P$ RF = 3.0V

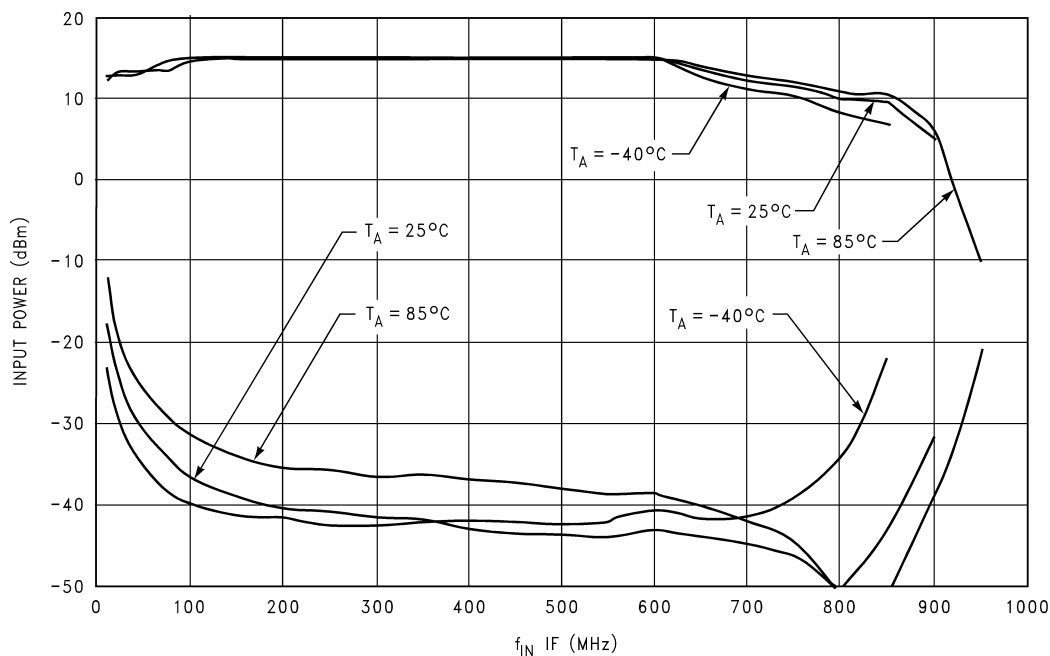


LMX2332U f_{IN} RF Input Power Vs Frequency
 $V_{CC} = V_P$ RF = 5.5V



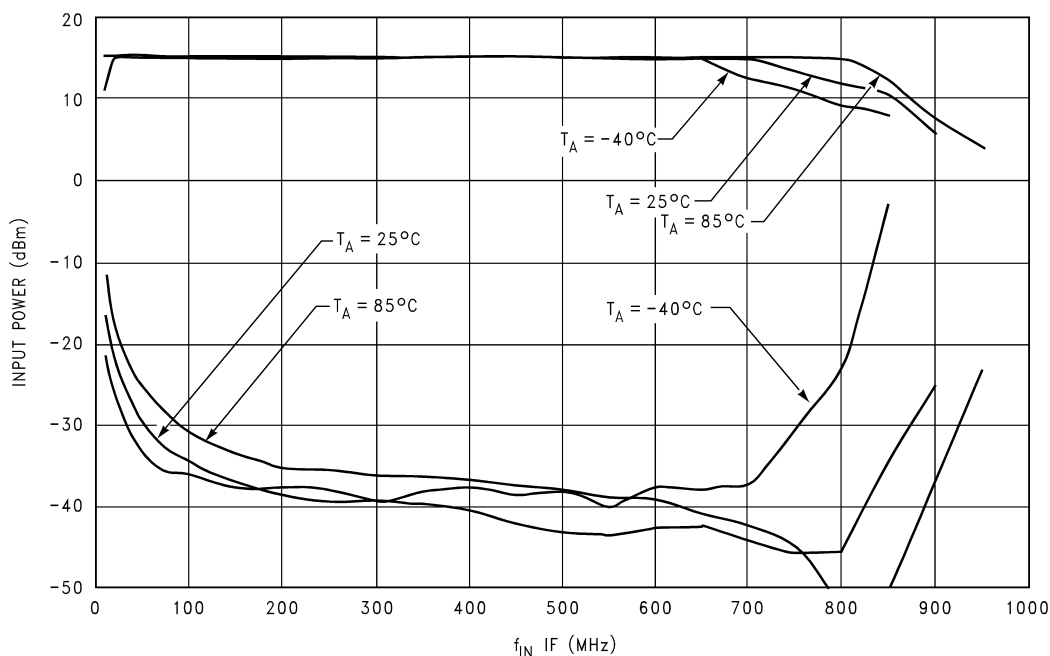
Typical Performance Characteristics Sensitivity (Continued)

LMX233xU f_{IN} IF Input Power Vs Frequency
 $V_{CC} = V_P$ IF = 3.0V



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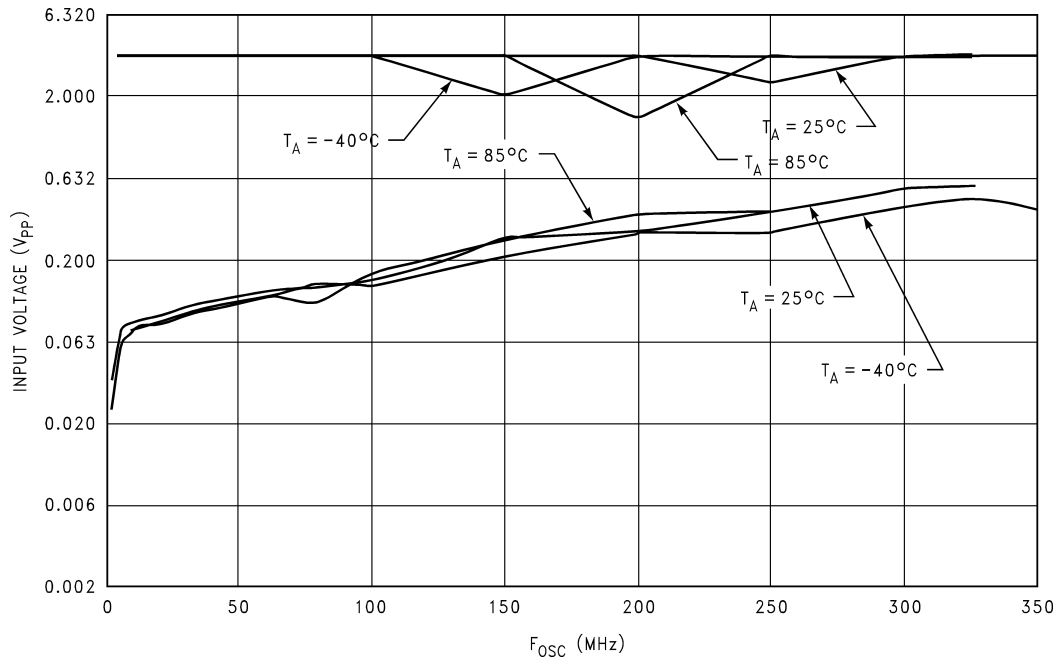
LMX233xU f_{IN} IF Input Power Vs Frequency
 $V_{CC} = V_P$ IF = 5.5V



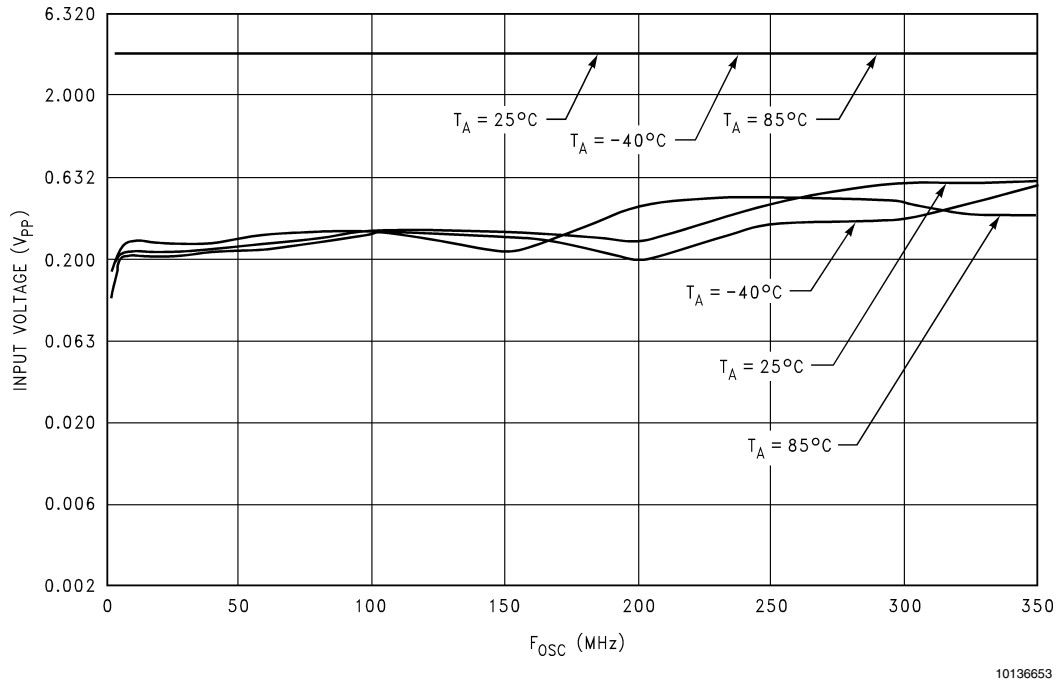
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Typical Performance Characteristics Sensitivity (Continued)

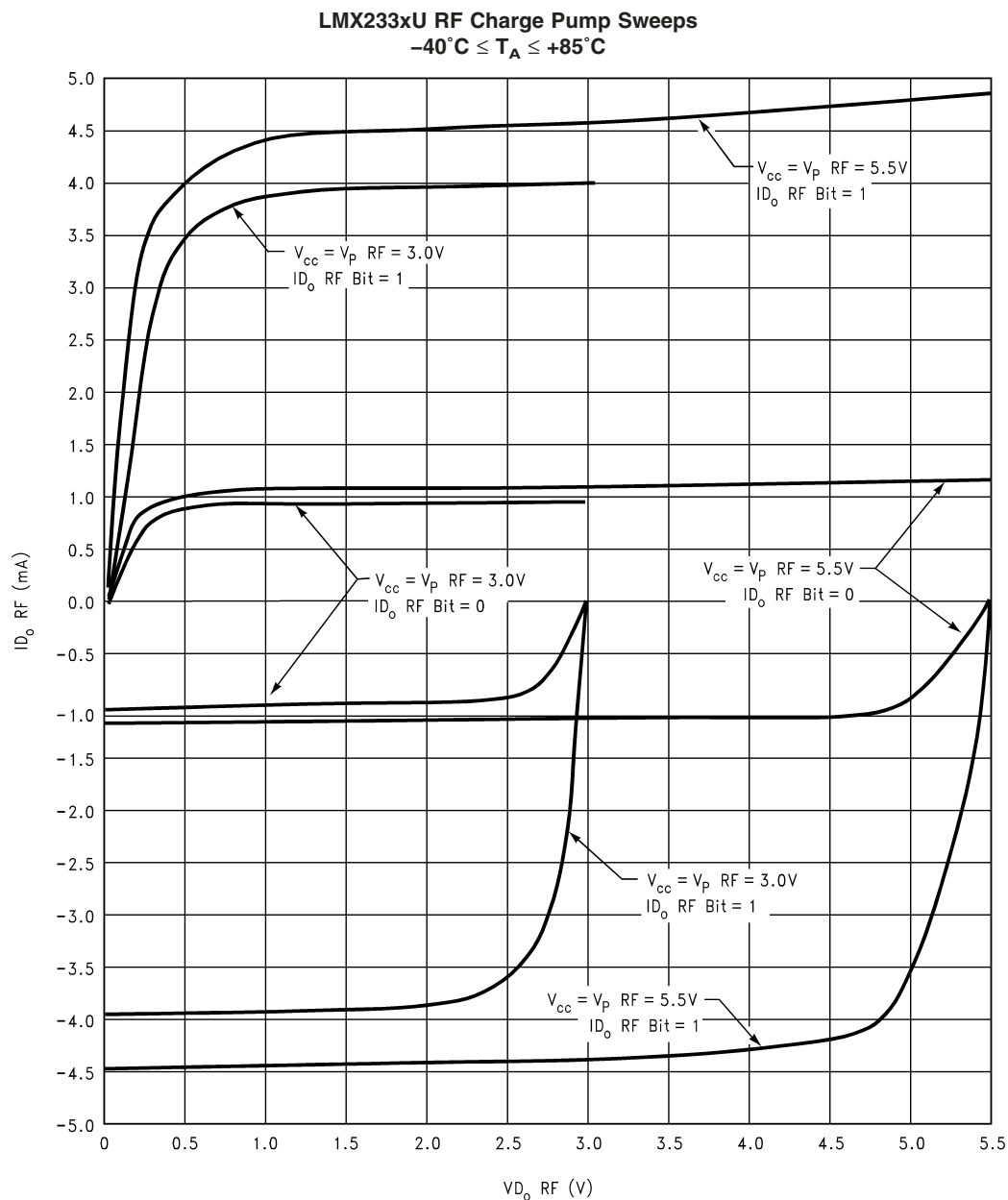
LMX233xU OSC_{in} Input Voltage Vs Frequency
V_{CC} = 3.0V



LMX233xU OSC_{in} Input Voltage Vs Frequency
V_{CC} = 5.5V



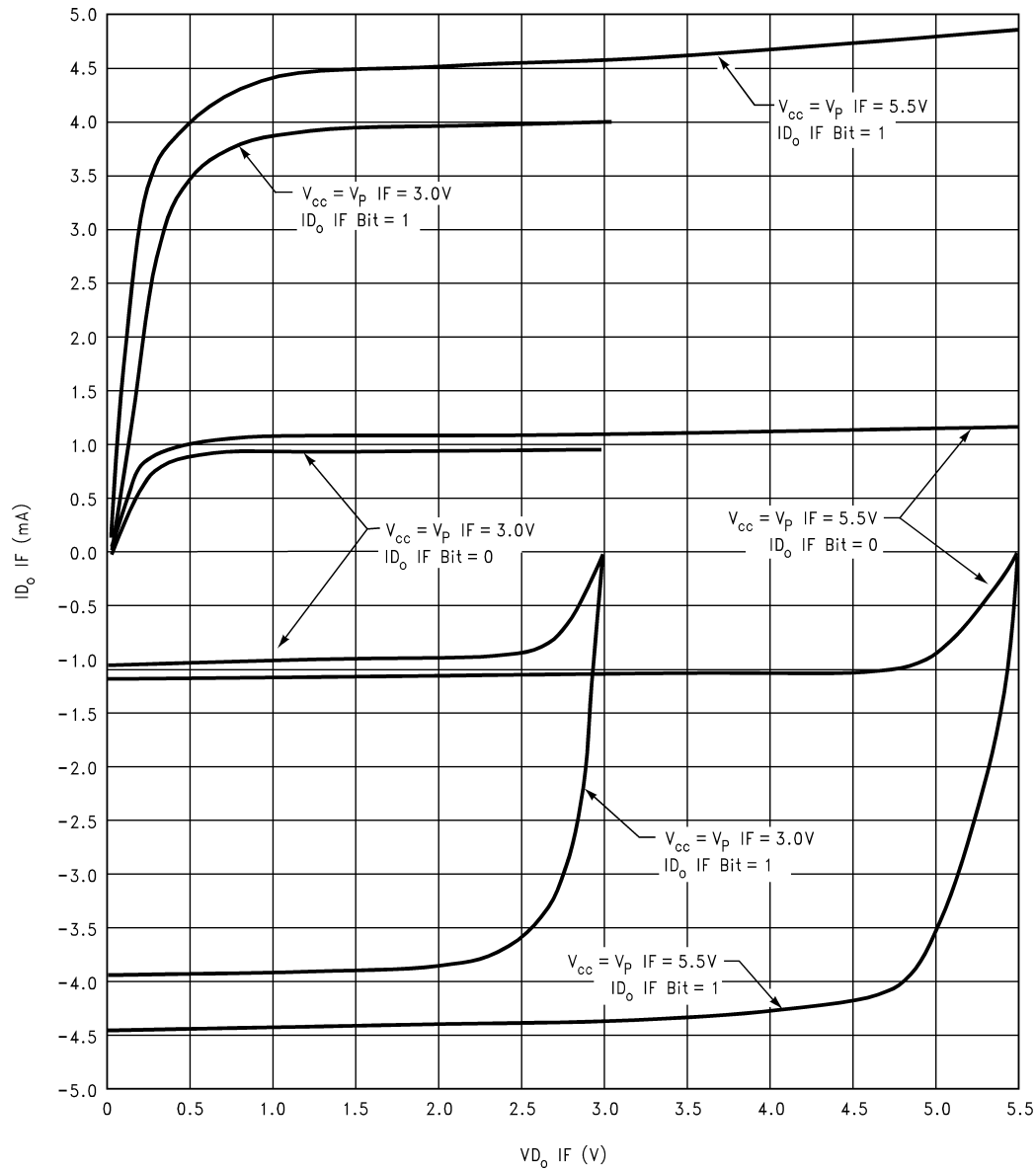
Typical Performance Characteristics Charge Pump



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Typical Performance Characteristics Charge Pump (Continued)

LMX233xU IF Charge Pump Sweeps
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$

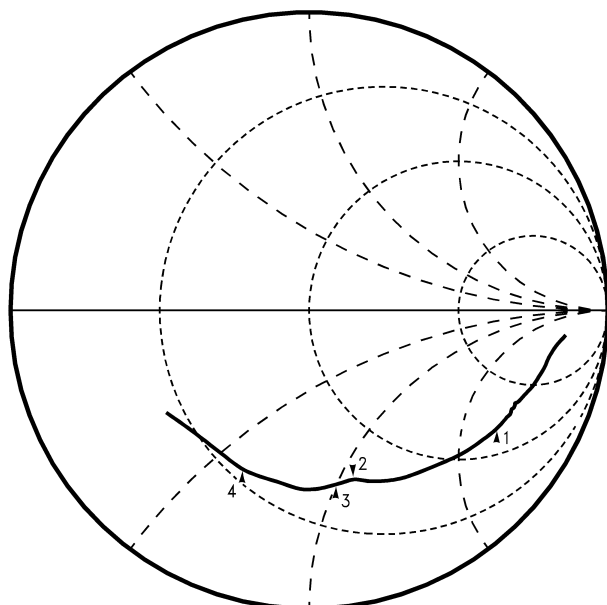


10136661

Typical Performance Characteristics

Input Impedance

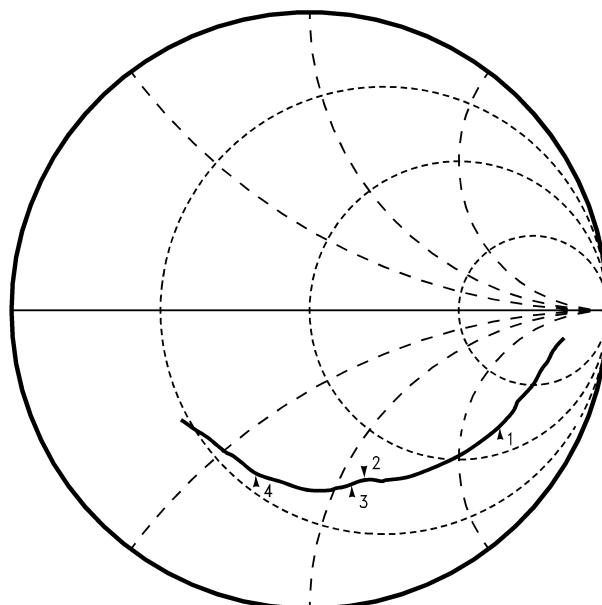
LMX233xU TSSOP f_{IN} RF Input Impedance
 $V_{CC} = 3.0V$, $T_A = +25^\circ C$



Marker 1 = 900 MHz
 Marker 2 = 1800 MHz
 Marker 3 = 1900 MHz
 Marker 4 = 2500 MHz

10136666

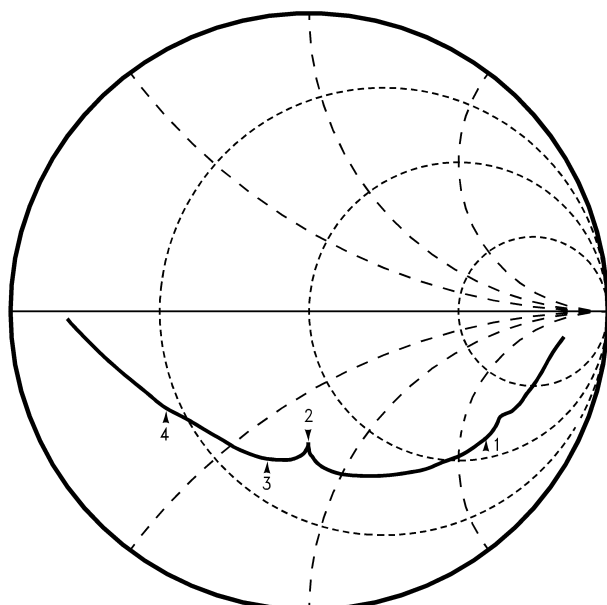
LMX233xU TSSOP f_{IN} RF Input Impedance
 $V_{CC} = 5.5V$, $T_A = +25^\circ C$



Marker 1 = 900 MHz
 Marker 2 = 1800 MHz
 Marker 3 = 1900 MHz
 Marker 4 = 2500 MHz

10136667

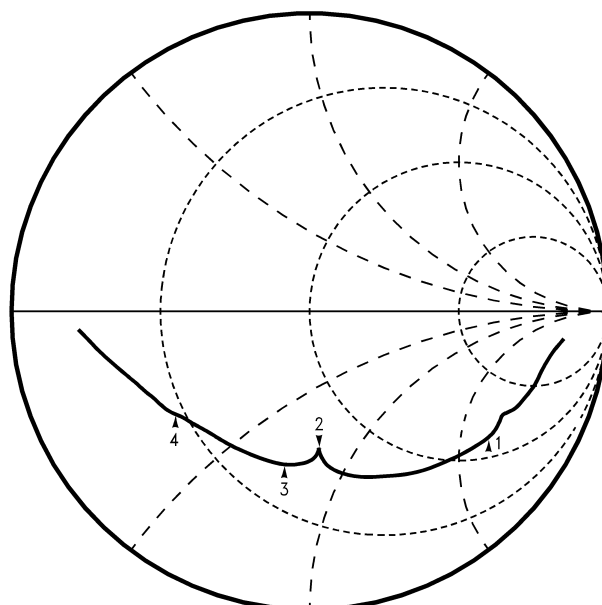
LMX233xU CSP f_{IN} RF Input Impedance
 $V_{CC} = 3.0V$, $T_A = +25^\circ C$



Marker 1 = 900 MHz
 Marker 2 = 1800 MHz
 Marker 3 = 1900 MHz
 Marker 4 = 2500 MHz

10136668

LMX233xU CSP f_{IN} RF Input Impedance
 $V_{CC} = 5.5V$, $T_A = +25^\circ C$



Marker 1 = 900 MHz
 Marker 2 = 1800 MHz
 Marker 3 = 1900 MHz
 Marker 4 = 2500 MHz

10136669

(Continued)

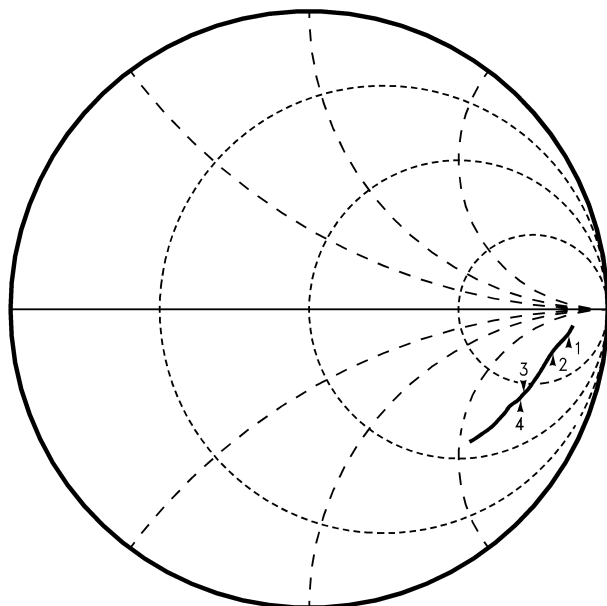
LMX233xU TSSOP and LMX233xU CSP f_{IN} RF Input Impedance Table

LMX233xU TSSOP Z _{IN} RF										LMX233xU CSP Z _{IN} RF										
V _{CC} = V _P RF = 3.0V (T _A = 25°C)					V _{CC} = V _P RF = 5.5V (T _A = 25°C)					V _{CC} = V _P RF = 3.0V (T _A = 25°C)					V _{CC} = V _P RF = 5.5V (T _A = 25°C)					
f _{IN} RF (MHz)	∠Γ	R _Z Z _{IN} RF (Ω)	∫ _{IN} RF (Ω)	∫ _{IN} RFI (Ω)	∠Γ	R _Z Z _{IN} RF (Ω)	∫ _{IN} RF (Ω)	∫ _{IN} RFI (Ω)	∠Γ	R _Z Z _{IN} RF (Ω)	∫ _{IN} RF (Ω)	∫ _{IN} RFI (Ω)	∠Γ	R _Z Z _{IN} RF (Ω)	∫ _{IN} RF (Ω)	∫ _{IN} RFI (Ω)				
100	0.862	-6.23	439.774	-319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281
200	0.834	-9.30	307.614	-272.274	410.803	0.834	-9.00	316.479	-271.581	417.031	0.836	-9.88	291.252	-277.923	402.577	0.836	-9.57	300.190	-277.552	408.838
300	0.820	-12.11	237.700	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.624	-249.637	335.819
400	0.808	-15.25	185.048	-227.171	293.001	0.808	-14.61	194.668	-229.054	300.601	0.808	-16.88	163.190	-219.893	273.832	0.808	-16.24	171.345	-222.518	280.844
500	0.796	-18.51	147.785	-203.923	251.843	0.796	-17.66	156.935	-207.313	260.014	0.793	-20.90	126.193	-191.939	229.707	0.794	-20.00	133.885	-196.200	237.528
600	0.781	-21.81	122.091	-181.461	218.710	0.782	-20.70	130.906	-185.850	227.325	0.775	-24.82	102.956	-168.026	197.060	0.777	-23.70	109.531	-172.887	204.663
700	0.765	-24.72	106.107	-163.758	195.129	0.767	-23.45	113.780	-168.514	203.329	0.749	-28.29	90.820	-146.582	172.437	0.752	-27.02	96.279	-151.333	179.363
800	0.760	-28.35	87.984	-150.524	174.352	0.762	-26.97	94.255	-155.481	181.819	0.742	-31.22	79.737	-136.782	158.327	0.746	-29.85	84.470	-141.473	164.772
900	0.747	-32.60	73.777	-134.500	153.406	0.750	-30.95	79.270	-139.668	160.596	0.739	-36.04	64.577	-123.951	139.764	0.742	-34.37	69.006	-128.610	145.954
1000	0.732	-36.68	64.122	-120.908	136.859	0.735	-34.73	69.215	-126.104	143.851	0.719	-41.44	55.019	-108.415	121.577	0.723	-39.46	58.684	-113.123	127.439
1100	0.717	-41.25	55.780	-108.398	121.908	0.720	-39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.698	-45.08	51.159	-98.547	111.035
1200	0.698	-46.24	49.180	-96.605	108.403	0.702	-43.84	52.848	-101.254	114.216	0.669	-53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.388	97.434
1300	0.678	-51.43	43.982	-86.291	96.853	0.683	-48.77	47.173	-90.676	102.212	0.641	-60.42	37.856	-71.653	81.039	0.647	-57.50	40.230	-75.400	85.461
1400	0.663	-56.68	39.397	-77.901	87.296	0.667	-53.71	42.317	-82.070	92.337	0.610	-68.33	34.108	-61.481	70.308	0.613	-64.90	36.477	-64.872	74.424
1500	0.649	-62.08	35.566	-70.500	78.963	0.653	-58.74	38.281	-74.569	83.821	0.577	-77.01	31.049	-52.388	60.898	0.581	-73.18	33.064	-55.554	64.649
1600	0.630	-67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.654	-48.119	57.597
1700	0.608	-72.22	31.565	-57.996	66.030	0.614	-68.51	33.590	-61.632	70.191	0.477	-27.97	100.359	-58.171	115.999	0.487	-84.99	33.106	-42.105	53.562
1800	0.596	-75.66	30.440	-54.462	62.392	0.601	-71.81	32.358	-57.943	66.366	0.455	89.90	32.829	-37.624	49.933	0.468	-85.87	33.886	-40.554	52.847
1900	0.598	-80.06	27.915	-51.164	58.284	0.602	-76.22	29.678	-54.335	61.912	0.493	87.34	29.357	-38.214	48.189	0.500	-88.90	29.576	-39.369	49.241
2000	0.607	-85.31	24.914	-47.651	53.771	0.607	-81.32	26.675	-50.603	57.203	0.520	79.89	25.120	-35.225	43.264	0.521	84.05	26.396	-37.576	45.921
2100	0.612	89.24	22.502	-43.994	49.414	0.611	-86.42	21.612	42.064	47.292	0.529	70.97	22.177	-30.771	37.930	0.525	75.52	23.556	-33.043	40.580
2200	0.605	84.09	21.289	-40.358	45.629	0.602	88.61	22.901	-43.251	48.940	0.531	61.99	20.155	-26.331	33.159	0.524	66.93	21.544	-28.595	35.802
2300	0.594	78.44	20.367	-36.566	41.855	0.589	83.13	21.961	-39.298	45.018	0.533	52.71	18.533	-21.975	28.747	0.525	57.61	19.706	-24.119	31.146
2400	0.590	72.27	19.111	-32.907	38.054	0.584	77.11	20.598	-35.536	41.074	0.550	43.18	16.578	-17.883	24.385	0.537	47.69	17.671	-19.749	26.501
2500	0.586	67.24	18.297	-30.064	35.194	0.576	72.09	19.792	-32.516	38.066	0.583	34.44	14.340	-14.328	20.272	0.566	38.69	15.416	-16.055	22.257

10136670

Typical Performance Characteristics Input Impedance (Continued)

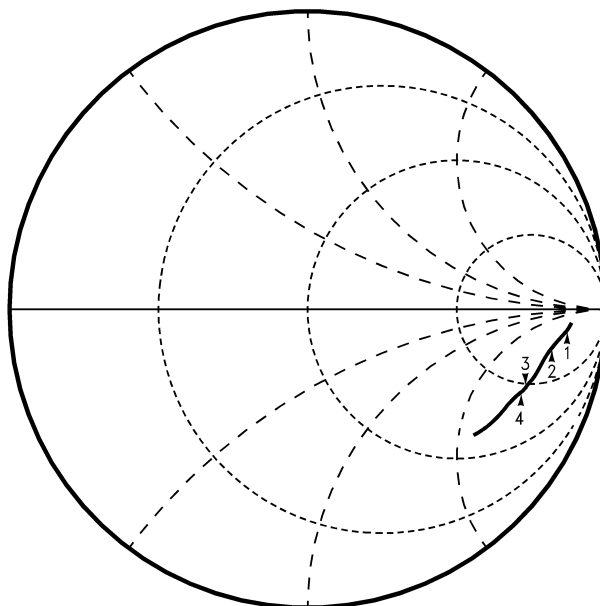
LMX233xU TSSOP f_{IN} IF Input Impedance
 $V_{CC} = 3.0V$, $T_A = +25^\circ C$



Marker 1 = 50 MHz
 Marker 2 = 200 MHz
 Marker 3 = 500 MHz
 Marker 4 = 600 MHz

10136671

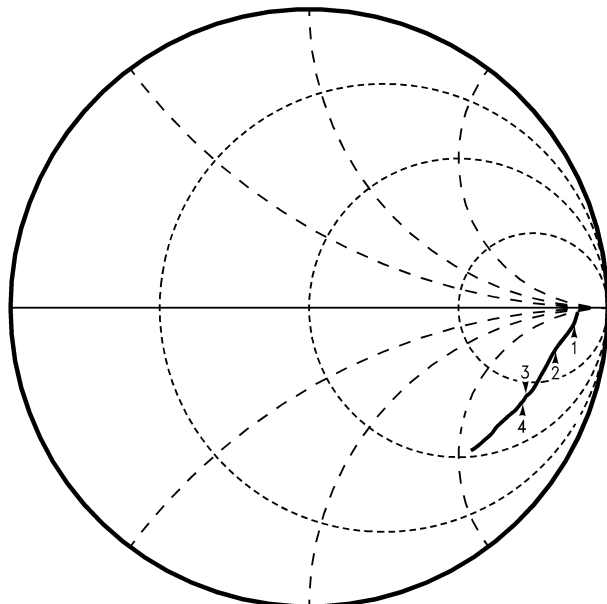
LMX233xU TSSOP f_{IN} IF Input Impedance
 $V_{CC} = 5.5V$, $T_A = +25^\circ C$



Marker 1 = 50 MHz
 Marker 2 = 200 MHz
 Marker 3 = 500 MHz
 Marker 4 = 600 MHz

10136672

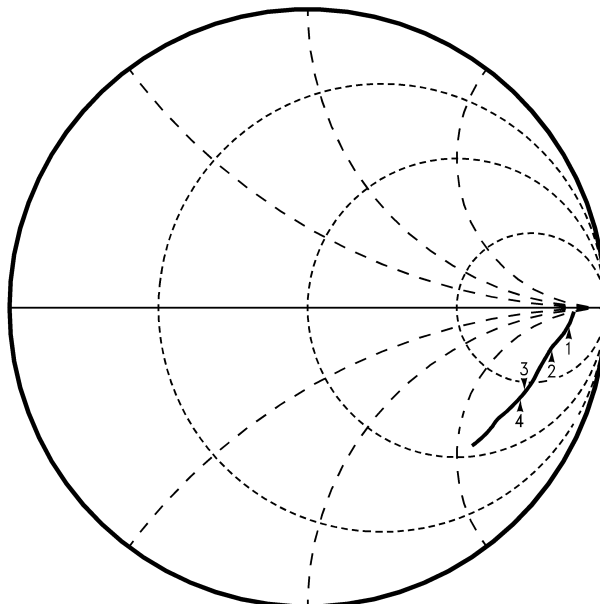
LMX233xU CSP f_{IN} IF Input Impedance
 $V_{CC} = 3.0V$, $T_A = +25^\circ C$



Marker 1 = 50 MHz
 Marker 2 = 200 MHz
 Marker 3 = 500 MHz
 Marker 4 = 600 MHz

10136673

LMX233xU CSP f_{IN} IF Input Impedance
 $V_{CC} = 5.5V$, $T_A = +25^\circ C$



Marker 1 = 50 MHz
 Marker 2 = 200 MHz
 Marker 3 = 500 MHz
 Marker 4 = 600 MHz

10136674

Typical Performance Characteristics

Input Impedance (Continued)

LMX233xU TSSOP and LMX233xU CSP f_{in} IF Input Impedance Table

f _{in} IF (MHz)	LMX233xU TSSOP Z _{f_{in}} IF						LMX233xU CSP Z _{f_{in}} IF													
	V _{CC} = V _P IF = 3.0V (T _A = 25°C)			V _{CC} = V _P IF = 5.5V (T _A = 25°C)			V _{CC} = V _P IF = 3.0V (T _A = 25°C)			V _{CC} = V _P IF = 5.5V (T _A = 25°C)										
	∠Γ	$\frac{R_e}{Z_{f_{in}} IF}$ (Ω)	$\frac{\eta_m}{Z_{f_{in}} IF}$ (Ω)	Z _{f_{in}} IF (Ω)	∠Γ	$\frac{R_e}{Z_{f_{in}} IF}$ (Ω)	$\frac{\eta_m}{Z_{f_{in}} IF}$ (Ω)	Z _{f_{in}} IF (Ω)	∠Γ	$\frac{R_e}{Z_{f_{in}} IF}$ (Ω)	$\frac{\eta_m}{Z_{f_{in}} IF}$ (Ω)	Z _{f_{in}} IF (Ω)	∠Γ	$\frac{R_e}{Z_{f_{in}} IF}$ (Ω)	$\frac{\eta_m}{Z_{f_{in}} IF}$ (Ω)	Z _{f_{in}} IF (Ω)				
50	0.884	-3.93	621.523	-345.924	711.305	0.885	-3.81	630.568	-340.995	716.864	0.899	-1.69	874.934	-242.583	907.940	0.899	-1.67	874.127	-239.189	906.261
75	0.873	-5.30	503.424	-340.786	607.923	0.873	-5.18	511.352	-338.259	613.107	0.891	-3.44	683.122	-354.024	769.408	0.891	-3.33	692.599	-349.036	775.577
100	0.861	-6.42	429.629	-319.996	535.704	0.861	-6.24	438.666	-318.001	541.805	0.880	-4.98	535.334	-360.736	645.533	0.879	-4.85	543.967	-357.157	650.739
125	0.851	-7.27	384.494	-301.186	488.414	0.852	-7.10	391.664	-300.482	493.650	0.868	-6.23	445.309	-339.295	559.840	0.868	-6.06	454.188	-337.263	565.715
150	0.844	-8.11	349.099	-288.744	453.038	0.844	-7.90	356.461	-287.182	457.753	0.858	-7.26	388.975	-319.049	503.085	0.858	-7.07	397.015	-317.892	508.603
175	0.837	-8.85	322.082	-276.707	424.622	0.837	-8.57	330.546	-275.058	430.020	0.850	-8.18	348.616	-303.517	462.229	0.850	-7.98	356.200	-303.914	468.233
200	0.832	-9.54	300.314	-268.356	402.745	0.832	-9.22	309.296	-267.480	408.913	0.843	-9.07	316.481	-291.646	430.369	0.844	-8.84	324.033	-291.128	435.606
225	0.827	-10.29	279.576	-260.995	382.467	0.827	-9.95	288.264	-260.187	388.322	0.838	-9.93	289.893	-282.342	404.666	0.839	-9.66	297.640	-282.345	410.254
250	0.823	-11.04	261.205	-254.758	364.870	0.823	-10.64	270.659	-254.417	371.462	0.834	-10.77	267.263	-274.027	382.780	0.834	-10.45	275.672	-273.085	388.034
275	0.819	-11.80	244.399	-248.227	348.350	0.818	-11.38	253.507	-247.511	354.299	0.830	-11.63	247.024	-265.175	362.407	0.829	-11.24	256.102	-265.264	368.719
300	0.814	-12.58	228.964	-241.239	332.597	0.815	-12.14	237.587	-241.965	339.109	0.826	-12.50	228.671	-257.705	344.532	0.826	-12.08	237.603	-257.879	350.652
325	0.812	-13.36	214.910	-236.082	319.251	0.811	-12.84	224.277	-236.738	326.106	0.823	-13.38	212.305	-250.287	328.203	0.822	-12.90	221.471	-251.212	334.899
350	0.807	-14.18	201.728	-228.591	304.874	0.807	-13.62	210.927	-230.202	312.223	0.819	-14.23	198.231	-242.453	313.176	0.819	-13.73	206.868	-244.557	320.316
375	0.804	-14.98	189.889	-223.629	293.373	0.804	-14.44	198.121	-224.602	299.497	0.816	-15.21	183.656	-234.712	298.025	0.815	-14.63	192.740	-236.735	305.274
400	0.801	-15.85	178.372	-217.315	281.144	0.801	-15.20	187.401	-219.200	288.388	0.812	-16.09	172.185	-227.189	285.066	0.812	-15.48	180.755	-229.880	292.433
425	0.797	-16.72	167.895	-211.342	269.915	0.797	-16.02	176.917	-213.413	277.208	0.809	-17.02	160.959	-220.345	272.873	0.808	-16.36	169.600	-222.898	280.085
450	0.794	-17.57	158.542	-205.691	259.700	0.794	-16.81	167.586	-208.198	267.267	0.805	-17.99	150.694	-213.253	261.124	0.805	-17.28	158.914	-216.102	268.242
475	0.790	-18.41	150.375	-199.750	250.026	0.791	-17.67	158.301	-202.585	257.099	0.802	-18.98	141.126	-206.449	250.075	0.802	-18.16	149.611	-210.221	258.024
500	0.787	-19.24	142.803	-194.502	241.295	0.787	-18.43	150.871	-197.426	248.474	0.799	-19.92	132.835	-200.384	240.414	0.799	-19.09	140.765	-204.004	247.856
525	0.783	-20.10	135.793	-188.890	232.635	0.783	-19.20	144.065	-192.240	240.231	0.796	-20.90	125.186	-193.960	230.851	0.796	-20.03	132.797	-197.693	238.154
550	0.779	-20.93	129.745	-183.353	224.616	0.780	-19.97	137.814	-187.051	232.338	0.793	-21.89	118.197	-187.808	221.906	0.792	-20.97	125.698	-191.502	229.070
575	0.775	-21.73	124.298	-178.182	217.253	0.776	-20.75	131.867	-182.250	224.954	0.789	-22.85	112.161	-181.851	213.658	0.789	-21.92	118.871	-185.881	220.640
600	0.770	-22.59	119.110	-172.763	209.843	0.771	-21.53	126.693	-176.798	217.506	0.785	-23.86	106.393	-175.910	205.581	0.785	-22.85	113.154	-180.132	212.723

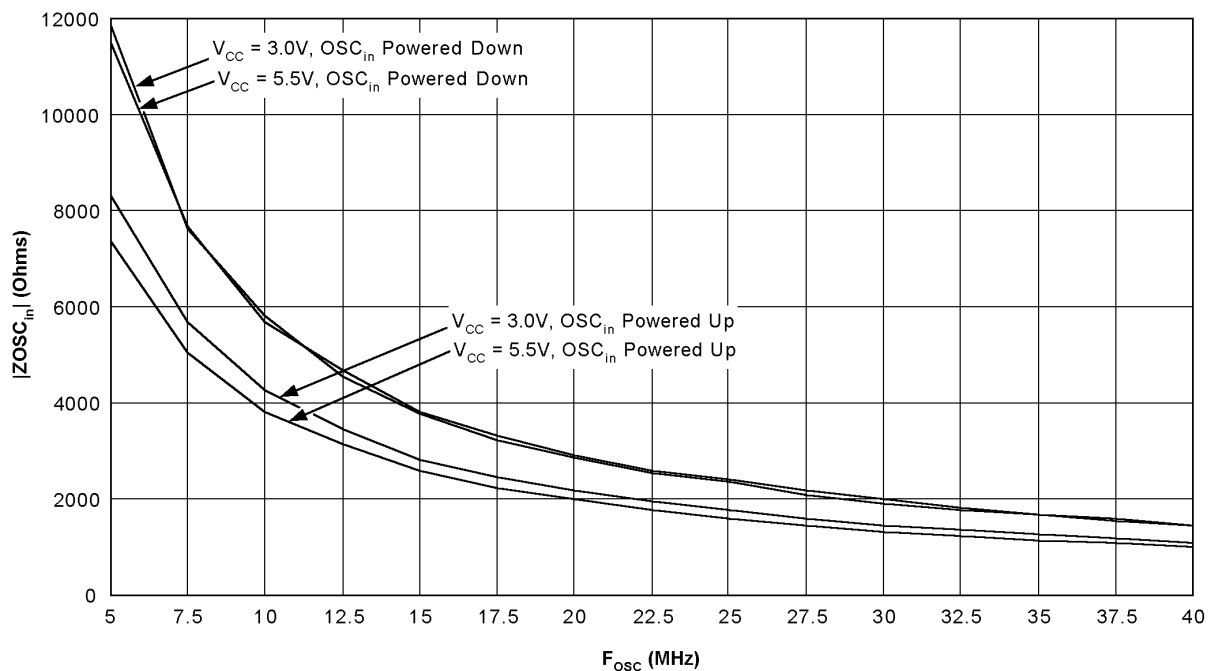
10136675

LMX23300U/LMX23301U/LMX23320U

Typical Performance Characteristics

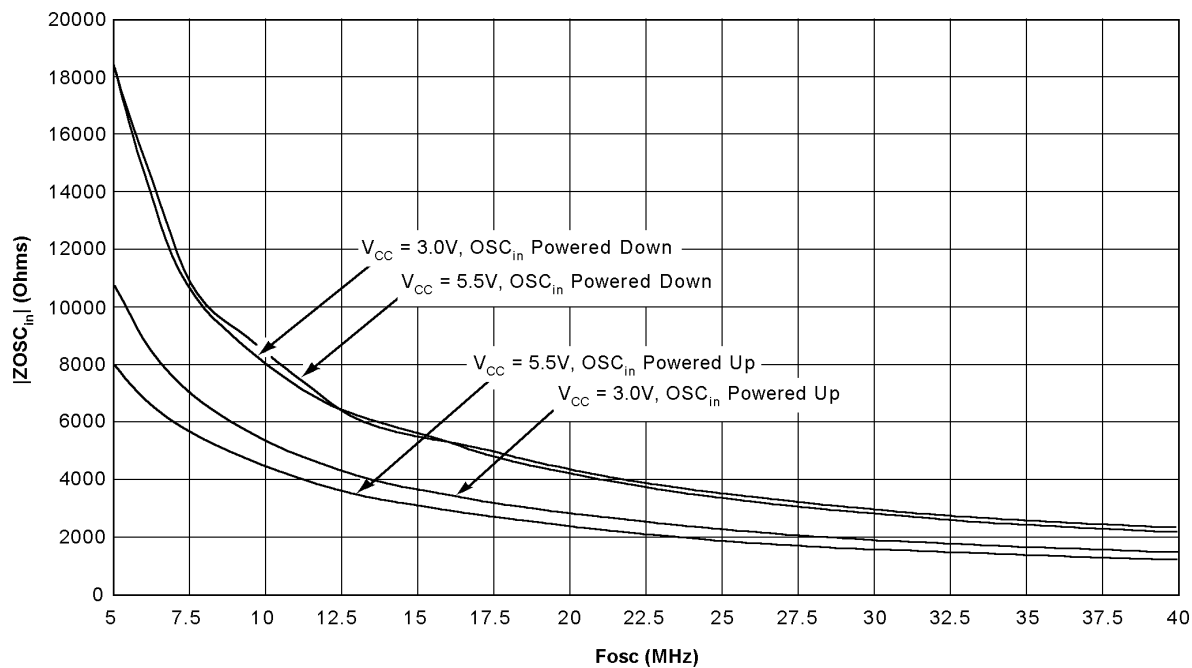
Input Impedance (Continued)

LMX233xU TSSOP OSC_{in} Input Impedance Vs Frequency
T_A = +25°C



10136676

LMX233xU CSP OSC_{in} Input Impedance Vs Frequency
T_A = +25°C



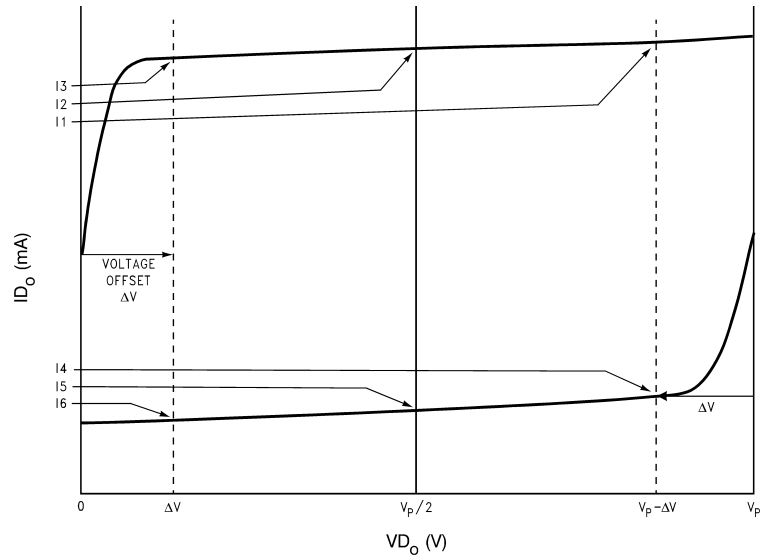
10136677

(Continued)

LMX233xU TSSOP and LMX233xU CSP OSC_{in} Input Impedance Table

10136678

Charge Pump Current Specification Definitions



10136637

I1 = Charge Pump Sink Current at $VD_O = V_P - \Delta V$

I2 = Charge Pump Sink Current at $VD_O = V_P/2$

I3 = Charge Pump Sink Current at $VD_O = \Delta V$

I4 = Charge Pump Source Current at $VD_O = V_P - \Delta V$

I5 = Charge Pump Source Current at $VD_O = V_P/2$

I6 = Charge Pump Source Current at $VD_O = \Delta V$

ΔV = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to V_{CC} and GND. Typical values are between 0.5V and 1.0V.

V_P refers to either V_P RF or V_P IF

VD_O refers to either VD_O RF or VD_O IF

ID_O refers to either ID_O RF or ID_O IF

Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_O \text{ Vs } VD_O = \frac{(|I1| - |I3|)}{(|I1| + |I3|)} \times 100\%$$

$$= \frac{(|I4| - |I6|)}{(|I4| + |I6|)} \times 100\%$$

10136663

Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_O \text{ SINK Vs } ID_O \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\%$$

10136664

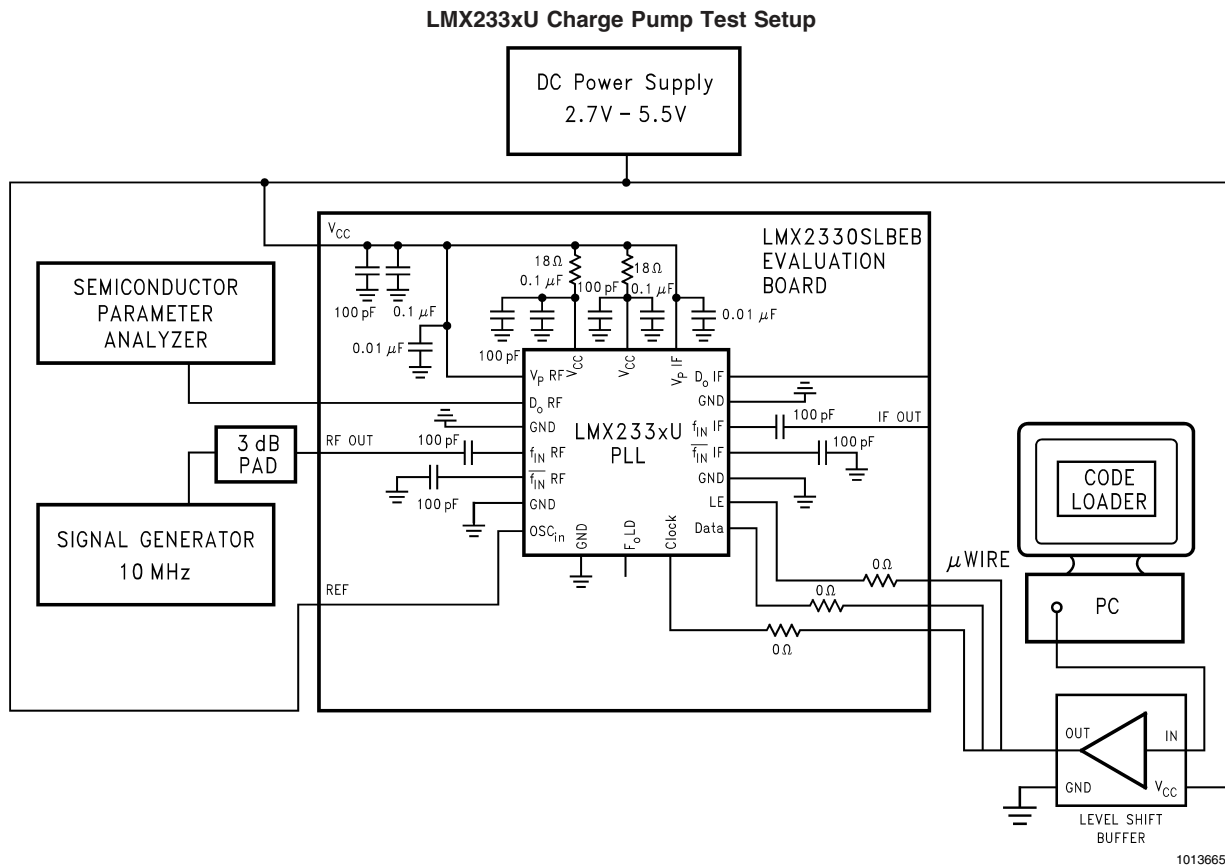
Charge Pump Output Current Magnitude Variation Vs Temperature

$$ID_O \text{ Vs } T_A = \frac{|I2|_{T_A=25^\circ C} - |I2|_{T_A}}{|I2|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I5|_{T_A=25^\circ C} - |I5|_{T_A}}{|I5|_{T_A=25^\circ C}} \times 100\%$$

10136665

Test Setups



The block diagram above illustrates the setup required to measure the LMX233xU device's RF charge pump sink current. The same setup is used for a LMX2330TMEB Evaluation Board. The IF charge pump measurement setup is similar to the RF charge pump measurement setup. The purpose of this test is to assess the functionality of the RF charge pump.

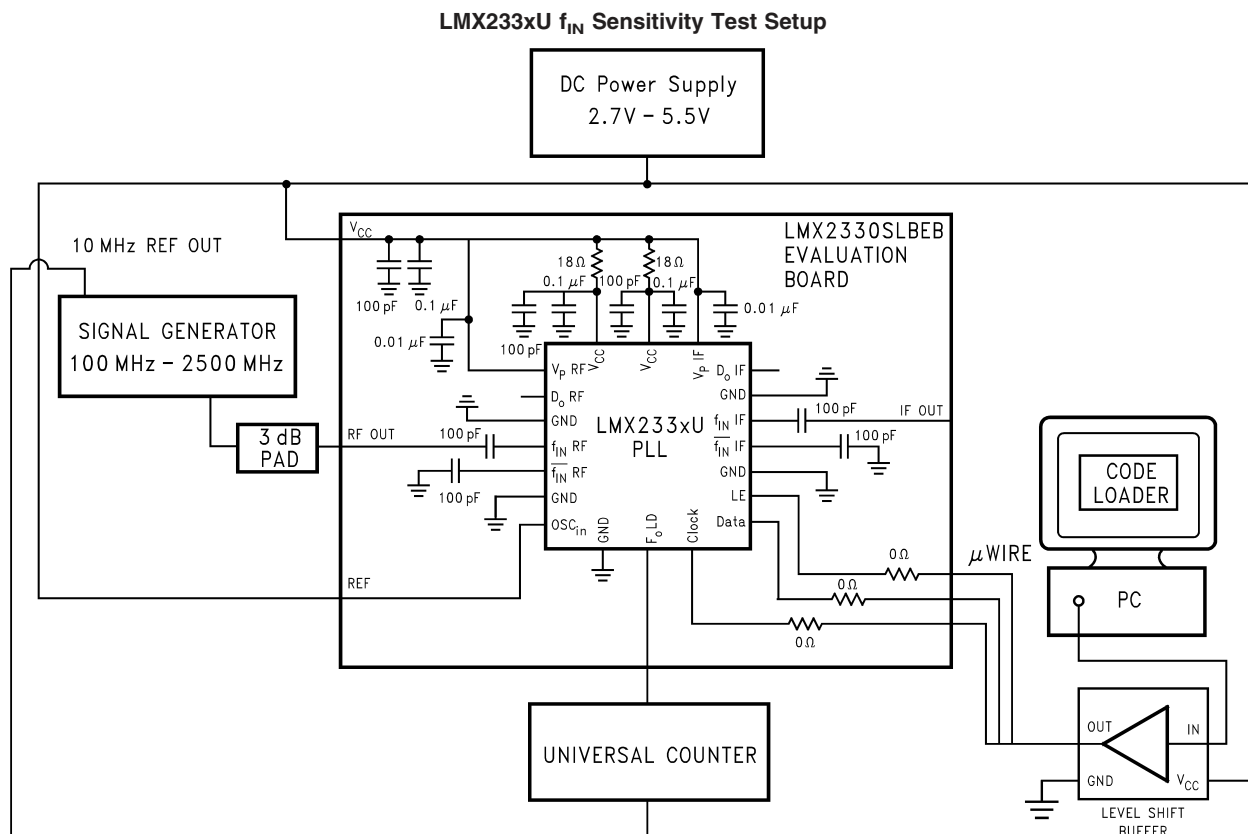
This setup uses an open loop configuration. A power supply is connected to V_{cc} and swept from 2.7V to 5.5V. By means of a signal generator, a 10 MHz signal is typically applied to the f_{in} RF pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50 Ω match between the PLL and the signal generator. The OSC_{in} pin is tied to V_{cc} . This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the D_o RF pin connected to a Semiconductor Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

Let F_r represent the frequency of the signal applied to the OSC_{in} pin, which is simply zero in this case (DC), and let F_p represent the frequency of the signal applied to the f_{IN} RF pin. The phase detector is sensitive to the rising edges of F_r and F_p . Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of F_p is detected. Since F_r has no rising edge, the charge pump continues to sink current indefinitely.

Toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the RF charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE ID₀ RF Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$.

Test Setups (Continued)



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The block diagram above illustrates the setup required to measure the LMX233xU device's RF input sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. The IF input sensitivity test setup is similar to the RF sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the f_{IN} RF input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

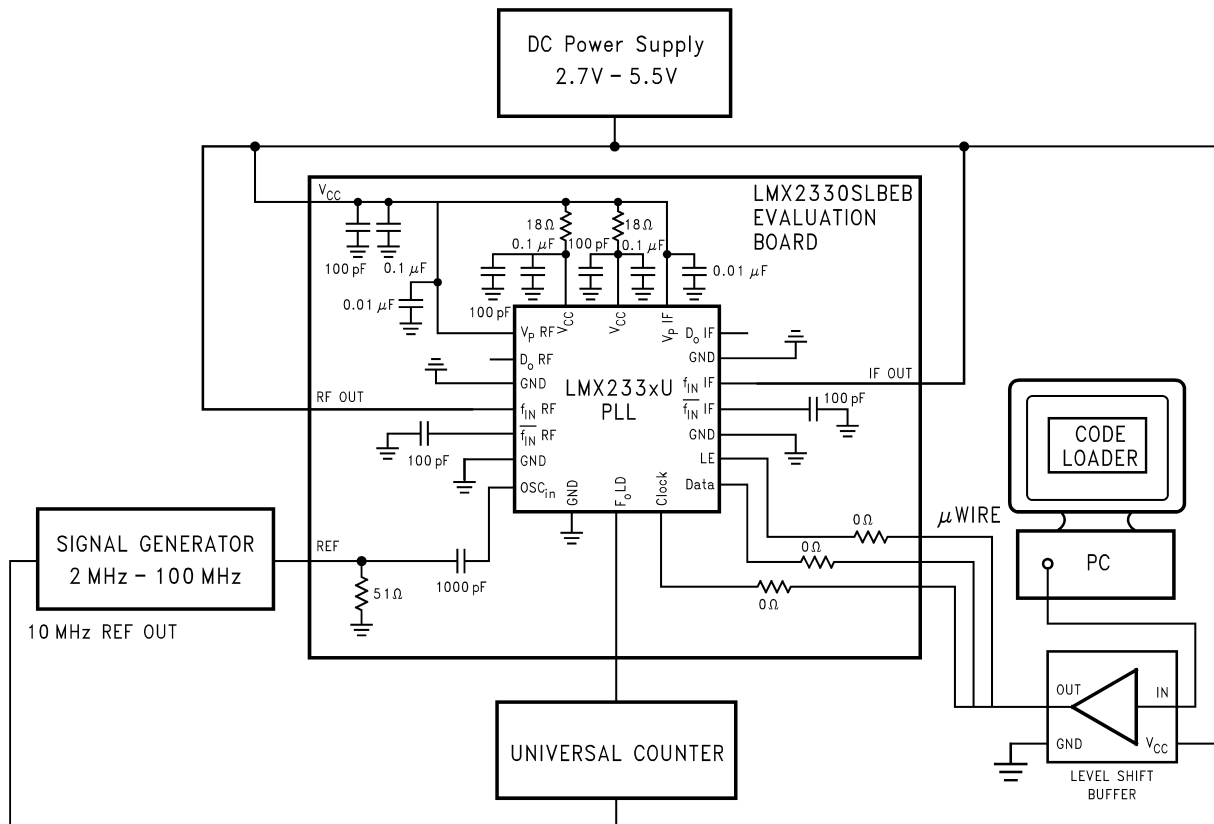
The setup uses an open loop configuration. A power supply is connected to V_{CC} and swept from 2.7V to 5.5V. The IF PLL is powered down (PWDN IF Bit = 1). By means of a signal generator, an RF signal is applied to the f_{IN} RF pin. The 3 dB pad provides a 50 Ω match between the PLL and the signal generator. The OSC_{in} pin is tied to V_{CC} . The N value is typically set to 10000 in Code Loader, i.e. RF N_CNTRB Word = 156 and RF N_CNTRA Word = 16 for PRE RF Bit = 1 (LMX2330U) or PRE RF = 0 (LMX2331U and LMX2332U). The feedback divider output is routed to the F_{oLD} pin by selecting the **RF PLL N Divider Output** word (F_{oLD} Word =

6 or 14) in Code Loader. A Universal Counter is connected to the F_{LD} pin and tied to the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to $f_{IN} RF / N$.

The f_{IN} RF input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$. Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the f_{IN} RF input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the f_{IN} RF input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the RF PLL loses lock.

Test Setups (Continued)

LMX233xU OSC_{in} Sensitivity Test Setup



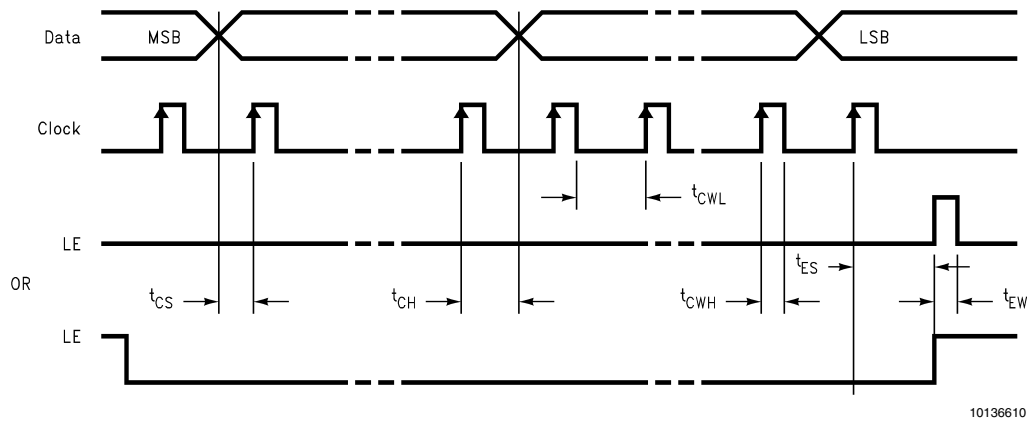
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The block diagram above illustrates the setup required to measure the LMX233xU device's OSC_{in} buffer sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. This setup is similar to the f_{in} sensitivity setup except that the signal generator is now connected to the OSC_{in} pin and both f_{in} pins are tied to V_{CC} . The $51\ \Omega$ shunt resistor matches the OSC_{in} input to the signal generator. The R counter is typically set to 1000, i.e. $RF_R_CNTR\ Word = 1000$ or $IF_R_CNTR\ Word = 1000$. The reference divider output is routed to the F_oLD pin by selecting the **RF PLL R Divider Output** word ($F_oLD\ Word = 2$ or 10) or the **IF PLL R Divider Output** word ($F_oLD\ Word = 1$ or 9) in Code Loader.

Similarly, a Universal Counter is connected to the F₀LD pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to OSC_{in}/ RF R_CNTR or OSC_{in}/ IF R_CNTR.

Again, V_{CC} is swept from 2.7V to 5.5V. The OSC_{in} input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$. Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

LMX233xU Serial Data Input Timing



Notes:

1. Data is clocked into the 22-bit shift register on the rising edge of Clock
2. The MSB of Data is shifted in first.

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1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX233xU, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal, F_r , is then presented to the input of a phase/frequency detector and compared with the feedback signal, F_p , which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the F_r and F_p signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

1.1 REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the RF and IF PLLs is provided from an external reference via the OSC_{in} pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of 0.5 V_{PP}. The reference buffer circuit has an approximate $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the OSC_{in} pin is connected to the output of a crystal oscillator.

1.2 REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal, OSC_{in} , by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ($F_{\phi RF}$ or $F_{\phi IF}$) of 10 MHz is not exceeded.

The RF and IF reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32767. The RF and IF reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

1.3 PRESCALERS

The f_{IN} RF (f_{IN} IF) and $\overline{f_{IN}}$ RF ($\overline{f_{IN}}$ IF) input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The RF and IF PLL complementary inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler.

1.4 PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal, f_{IN} , by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency ($F_{\phi RF}$ or $F_{\phi IF}$) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmable binary counter). The RF N_CNTRA counter is a 7-bit CMOS swallow counter, programmable from 0 to 127. The IF N_CNTRA counter is also a 7-bit CMOS swallow counter, but programmable from 0 to 15. The three most significant bits are 'don't cares' in this case. The RF N_CNTRB and IF N_CNTRB counters are both 11-bit CMOS binary counters, programmable from 3 to 2047. A continuous integer divide ratio is achieved if $N \geq P * (P-1)$, where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value ($N_{CNTRB} \geq N_{CNTRA}$). Refer to **Sections 2.6.1, 2.6.2, 2.7.1 and 2.7.2** for details on how to program the N_CNTRA and N_CNTRB counters. The following equations are useful in determining and programming a particular value of N:

$$N = (P \times N_{CNTRB}) + N_{CNTRA}$$

$$f_{IN} = N \times F_{\phi}$$

Definitions:

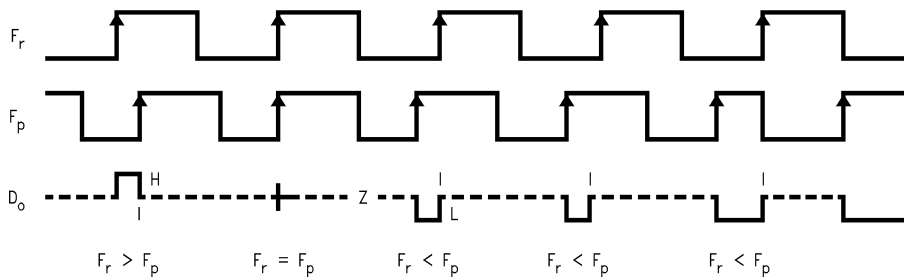
- F_{ϕ} : RF or IF phase detector comparison frequency
- f_{IN} : RF or IF input frequency
- N_CNTRA: RF or IF A counter value
- N_CNTRB: RF or IF B counter value
- P: Preset modulus of the dual modulus prescaler
- LMX2330U RF synthesizer: P = 32 or 64
- LMX2331U RF synthesizer: P = 64 or 128
- LMX2332U RF synthesizer: P = 64 or 128
- LMX233xU IF synthesizer: P = 8 or 16

1.5 PHASE/FREQUENCY DETECTORS

The RF and IF phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the RF and IF phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD_POL RF** or **PD_POL IF** control bits, depending on whether the RF or IF VCO characteristics are positive or negative. Refer to **Sections 2.4.2 and 2.5.2** for more details. The phase/frequency detectors have a detection range of -2π to $+2\pi$. The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

1.0 Functional Description (Continued)

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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Notes:

1. The minimum width of the pump-up and pump-down current pulses occur at the D_o RF or D_o IF pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristics, i.e. PD_POL RF or PD_POL IF = 1.
3. F_r is the phase detector input from the reference divider (R counter).
4. F_p is the phase detector input from the programmable feedback divider (N counter).
5. D_o refers to either the RF or IF charge pump output.

1.6 CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards V_P RF or V_P IF during pump-up events and towards GND during pump-down events. When locked, D_o RF or D_o IF are primarily in a TRI-STATE mode with small corrections occurring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the **ID_o RF** or **ID_o IF** control bits.

1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in **Section 2.0 Programming Description**.

1.8 MULTI-FUNCTION OUTPUTS

The LMX233xU device's F_oLD output pin is a multi-function output that can be configured as the RF FastLock output, a push-pull analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The F_oLD control word is used to select the desired output function. When the PLL is in powerdown mode, the F_oLD output is pulled to a LOW state. A complete programming description of the multi-function output is provided in **Section 2.8 F_oLD**.

1.8.1 Push-Pull Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the F_oLD output pin if selected. The lock detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is a push-pull configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the 'lock' status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a 'locked state'. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to **Section 2.8 F_oLD** for details on how to program the different lock detect options.

1.0 Functional Description (Continued)

1.8.2 Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock acquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/ phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA (ID_0 RF Bit = 0) in the steady state mode, to 3.8 mA (ID_0 RF Bit = 1) in Fastlock. When the F_{oLD} output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor $R2'$ to ground, of equal value to resistor $R2$ of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to **Section 2.8 F_{oLD}** for details on how to configure the F_{oLD} output to an open drain Fastlock output.

1.8.3 Counter Reset

Three separate counter reset functions are provided. When the F_{oLD} is programmed to **Reset IF Counters**, both the IF feedback divider and the IF reference divider are held at their load point. When the **Reset RF Counters** is programmed, both the RF feedback divider and the RF reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to **Section 2.8 F_{oLD}** for more details.

1.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate F_{oLD} word. This is essential when performing OSC_{in} or f_{IN} sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to **Section 2.8 F_{oLD}** for more details on how to route the appropriate divider output to the F_{oLD} pin.

1.9 POWER CONTROL

Each synthesizer in the LMX233xU device is individually power controlled by device powerdown bits. The powerdown word is comprised of the **PWDN RF (PWDN IF)** bit, in conjunction with the **TRI-STATE ID_0 RF (TRI-STATE ID_0 IF)** bit. The powerdown control word is used to set the operating mode of the device. Refer to **Sections 2.4.4, 2.5.4, 2.6.4, and 2.7.4** for details on how to program the RF or IF powerdown bits.

When either the RF synthesizer or the IF synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The D_0 RF (D_0 IF), f_{IN} RF (f_{IN} IF), and $\overline{f_{IN}}$ RF ($\overline{f_{IN}}$ IF) pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the RF and IF synthesizers are powered down. The OSC_{in} pin is forced to a HIGH state through an approximate 100 k Ω resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

Synchronous Powerdown Mode

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

Asynchronous Powerdown Mode

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE ID_0	PWDN	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

Notes:

1. TRI-STATE ID_0 refers to either the TRI-STATE ID_0 RF or TRI-STATE ID_0 IF bit .
2. PWDN refers to either the PWDN RF or PWDN IF bit.

2.0 Programming Description

2.1 MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit *Data[19:0] Field* and a 2-bit *Address[1:0] Field* as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data Field assignments are shown in **Section 2.3 CONTROL REGISTER CONTENT MAP**.

MSB										LSB		
Data[19:0]										Address[1:0]		
21										2	1	0

2.2 CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Address[1:0] Field		Target Register
0	0	IF R
0	1	RF R
1	0	IF N
1	1	RF N

2.3 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

2.0 Programming Description (Continued)

Reg.	Most Significant Bit										SHIFT REGISTER BIT LOCATION														Least Significant Bit					
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
	Data Field																						Address Field							
IF R	F _o LD0	F _o LD2	TRI-STATE ID _o IF	ID _o IF	PD ₋ POL IF	IF R_CNTR[14:0]										0				0										
RF R	F _o LD1	F _o LD3	TRI-STATE ID _o RF	ID _o RF	PD ₋ POL RF	RF R_CNTR[14:0]										0				1										
IF N	PWDN IF	PRE IF	IF N_CNTRB[10:0]										IF N_CNTRA[6:0]										1				0			
RF N	PWDN RF	PRE RF	RF N_CNTRB[10:0]										RF N_CNTRA[6:0]										1				1			

2.0 Programming Description (Continued)

2.4 IF R REGISTER

The IF R register contains the IF R_CNTR, PD_POL IF, ID_o IF, and TRI-STATE ID_o IF control words, in addition to two bits that compose the F_oLD control word. The detailed descriptions and programming information for each control word is discussed in the following sections. IF R_CNTR[14:0]

Reg.	SHIFT REGISTER BIT LOCATION																		Least Significant Bit			
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<i>Data Field</i>																				<i>Address Field</i>	
IF R	F ₀ LD0	F ₀ LD2	TRI- STATE ID ₀ IF	ID ₀ IF	PD_ POL IF	IF R_CNTR[14:0]															0	0

2.4.1 IF R_CNTR[14:0] IF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) IF R[2:16]

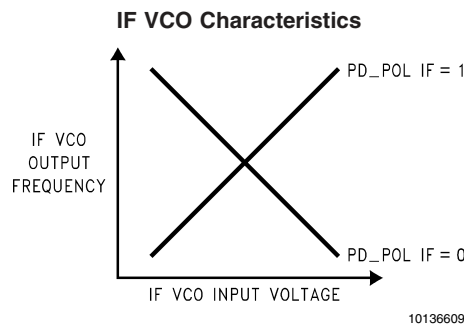
The IF reference divider (IF R_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	IF R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.4.2 PD_POL IF IF SYNTHESIZER PHASE DETECTOR POLARITY IF R[17]

The PD_POL IF bit is used to control the IF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL IF	IF R[17]	IF Phase Detector Polarity	IF VCO Negative Tuning Characteristics	IF VCO Positive Tuning Characteristics



2.4.3 ID_o IF IF SYNTHESIZER CHARGE PUMP CURRENT GAIN IF R[18]

The ID_o IF bit controls the IF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID _o IF	IF R[18]	IF Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

2.0 Programming Description (Continued)

2.4.4 TRI-STATE ID₀ IF IF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT IF R[19]

The TRI-STATE ID₀ IF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID₀ IF bit.

Furthermore, the TRI-STATE ID₀ IF bit operates in conjunction with the PWDN IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID ₀ IF	IF R[19]	IF Charge Pump TRI-STATE Current	IF Charge Pump Normal Operation	IF Charge Pump Output in High Impedance State

2.5 RF R REGISTER

The RF R register contains the RF R_CNTR, PD_POL RF, ID₀ RF, and TRI-STATE ID₀ RF control words, in addition to two bits that compose the F₀LD control word. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg.	Most Significant Bit						SHIFT REGISTER BIT LOCATION														Least Significant Bit			
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	Data Field																				Address Field			
RF R	F ₀ LD1	F ₀ LD3	TRI-STATE ID ₀ RF	ID ₀ RF	PD ₋ POL RF	RF R_CNTR[14:0]															0	1		

2.5.1 RF R_CNTR[14:0] RF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF R[2:16]

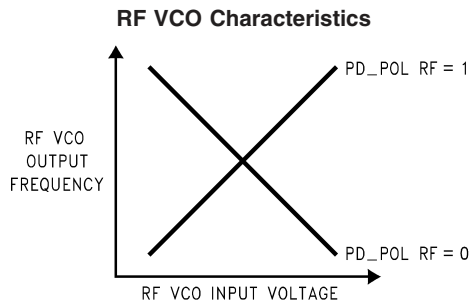
The RF reference divider (RF R_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	RF R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.5.2 PD_POL RF RF SYNTHESIZER PHASE DETECTOR POLARITY RF R[17]

The PD_POL RF bit is used to control the RF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF	RF R[17]	RF Phase Detector Polarity	RF VCO Negative Tuning Characteristics	RF VCO Positive Tuning Characteristics



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2.0 Programming Description (Continued)

2.5.3 ID_o RF

RF SYNTHESIZER CHARGE PUMP CURRENT GAIN

RF R[18]

The ID_o RF bit controls the RF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID _o RF	RF R[18]	RF Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

2.5.4 TRI-STATE ID_o RF

RF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT

RF R[19]

The TRI-STATE ID_o RF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID_o RF bit.

Furthermore, the TRI-STATE ID_o RF bit operates in conjunction with the PWDN RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID _o RF	RF R[19]	RF Charge Pump TRI-STATE Current	RF Charge Pump Normal Operation	RF Charge Pump Output in High Impedance State

2.6 IF N REGISTER

The IF N register contains the IF N_CNTRA, IF N_CNTRB, PRE IF, and PWDN IF control words. The IF N_CNTRA and IF N_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																					Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Data Field																				Address Field		
IF N	PWDN IF	PRE IF	IF N_CNTRB[10:0]										IF N_CNTRA[6:0]						1	0			

2.6.1 IF N_CNTRA[6:0]

IF SYNTHESIZER SWALLOW COUNTER (A COUNTER)

IF N[2:8]

The IF N_CNTRA control word is used to setup the IF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The IF N_CNTRA control word can be programmed to values ranging from 0 to 15. The three most significant bits are 'don't care bits' in this case.

Divide Ratio	IF N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

2.6.2 IF N_CNTRB[10:0]

IF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER)

IF N[9:19]

The IF N_CNTRB control word is used to setup the IF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The IF N_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	IF N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

2.0 Programming Description (Continued)

2.6.3 PRE IF IF SYNTHESIZER PRESCALER SELECT

IF N[20]

The IF synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE IF	IF N[20]	IF Prescaler Select	8/9 Prescaler Selected	16/17 Prescaler Selected

2.6.4 PWDN IF IF SYNTHESIZER POWERDOWN

IF N[21]

The PWDN IF bit is used to switch the IF PLL between a powered up and powered down mode.

Furthermore, the PWDN IF bit operates in conjunction with the TRI-STATE ID₀ IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN IF	IF N[21]	IF Powerdown	IF PLL Active	IF PLL Powerdown

2.7 RF N REGISTER

The RF N register contains the RF N_CNTRA, RF N_CNTRB, PRE RF, and PWDN RF control words. The RF N_CNTRA and RF N_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																				Least Significant Bit		
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Data Field																				Address Field		
RF N	PWDN RF	PRE RF	RF N_CNTRB[10:0]											RF N_CNTRA[6:0]								1	1

2.7.1 RF N_CNTRA[6:0] RF SYNTHESIZER SWALLOW COUNTER (A COUNTER)

RF N[2:8]

The RF N_CNTRA control word is used to setup the RF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF N_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

2.7.2 RF N_CNTRB[10:0] RF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER)

RF N[9:19]

The RF N_CNTRB control word is used to setup the RF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF N_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

2.0 Programming Description (Continued)

2.7.3 PRE RF RF SYNTHESIZER PRESCALER SELECT

RF N[20]

The RF synthesizer utilizes a selectable dual modulus prescaler.

LMX2330U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Function	
			0	1
PRE RF	RF N[20]	RF Prescaler Select	32/33 Prescaler Selected	64/65 Prescaler Selected

LMX2331U and LMX2332U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Function	
			0	1
PRE RF	RF N[20]	RF Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

2.7.4 PWDN RF RF SYNTHESIZER POWERDOWN

RF N[21]

The PWDN RF bit is used to switch the RF PLL between a powered up and powered down mode.

Furthermore, the PWDN RF bit operates in conjunction with the TRI-STATE ID_O RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF	RF N[21]	RF Powerdown	RF PLL Active	RF PLL Powerdown

2.0 Programming Description (Continued)

2.8 F_oLD[3:0]

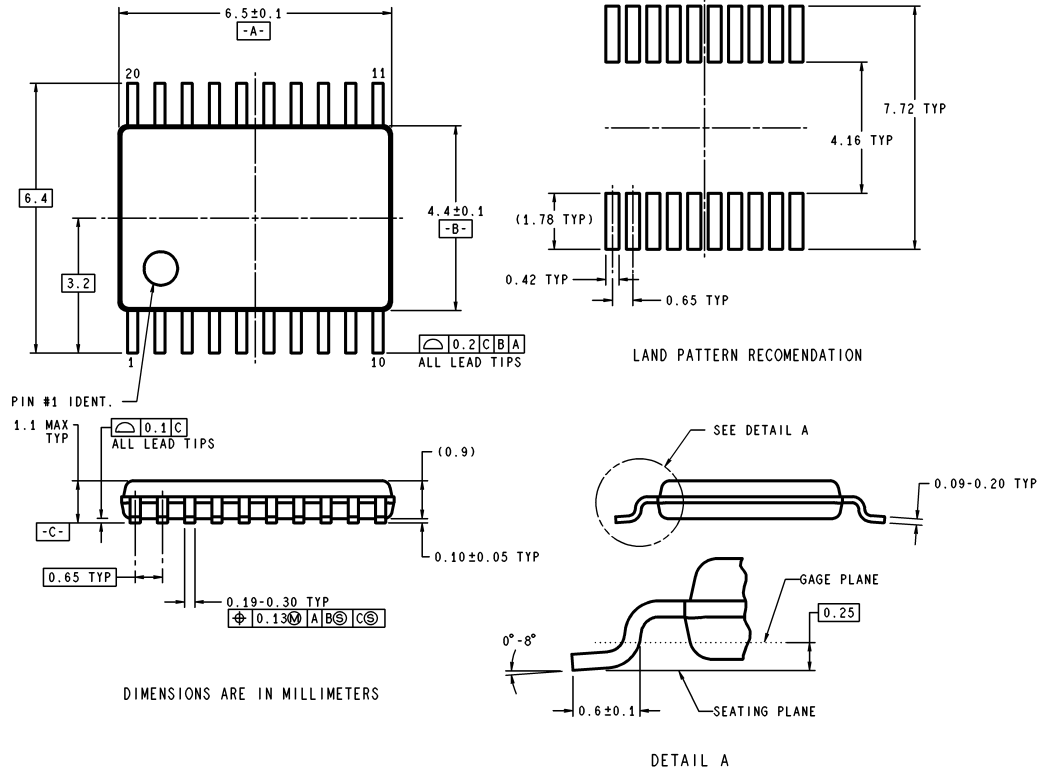
MULTI-FUNCTION OUTPUT SELECT

[RF R[20], IF R[20], RF R [21], IF R[21]]

The F_oLD control word is used to select which signal is routed to the F_oLD pin.

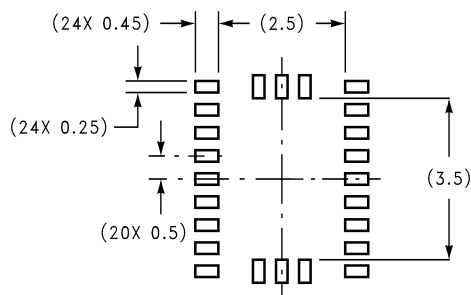
F _o LD3	F _o LD2	F _o LD1	F _o LD0	F _o LD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	IF PLL R Divider Output, Push-Pull Output
0	0	1	0	RF PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	IF PLL Analog Lock Detect, Push-Pull Output
0	1	0	1	IF PLL N Divider Output, Push-Pull Output
0	1	1	0	RF PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset IF Counters, LOW Logic State Output
1	0	0	0	RF Analog Lock Detect, Push-Pull Output
1	0	0	1	IF PLL R Divider Output, Push-Pull Output
1	0	1	0	RF PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset RF Counters, LOW Logic State Output
1	1	0	0	RF and IF Analog Lock Detect, Push-Pull Output
1	1	0	1	IF PLL N Divider Output, Push-Pull Output
1	1	1	0	RF PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

Physical Dimensions inches (millimeters) unless otherwise noted



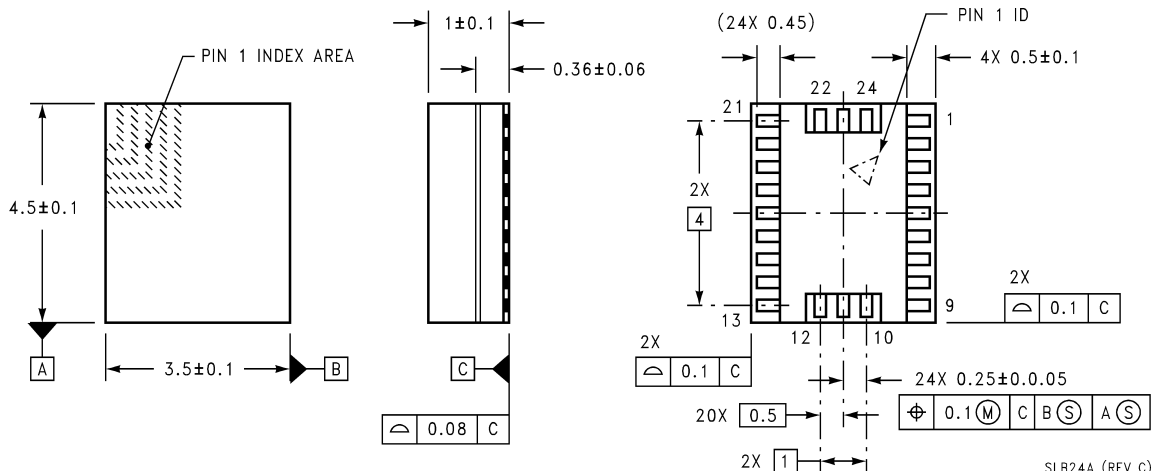
20-Pin Thin Shrink Small Outline Package (TM)
NS Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS



SLB24A (REV C)

24-Pin Chip Scale Package (SLB)
NS Package Number SLB24A

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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