

RoHS

Free

System Lens Drivers

μ -step System Lens Driver for Digital Still Cameras

BU24020GU

General Description

BU24020GU is a system Lens Driver that uses μ -step driving to make the configuration of the sophisticated, high precision and low noise lens driver system possible. This IC has a built-in driver for both DC motor and voice coil motor and a μ -step controller that decreases CPU power. Therefore, multifunctional lens can be applied.

Features

- Built-in 4channels Driver block.
 1ch-4ch: Voltage control type H-bridge (Adaptable to STM 2systems)
 - Built-in 2 channels PI driving circuit
- Built-in PLL circuit

Applications

Digital still cameras

Typical Application Circuit

Digital Power Supply Voltage:Driver Power Supply Voltage:

Key Specifications

- Output Current (1ch-4ch):
- Input Clock Frequency:
- FET ON Resistance (1ch-4ch):
- ±500mA(Max) 1MHz to 28MHz 1.5Ω(Typ) -20°C to +85°C

2.7V to 3.6V

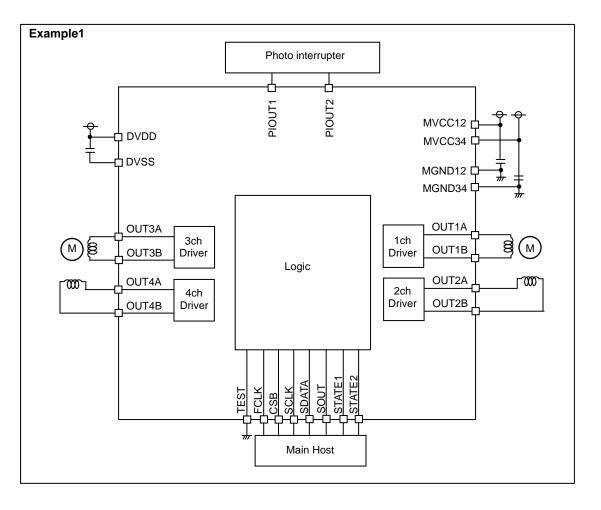
2.7V to 5.5V

Operating Temperature Range:

Package

VCSP85H2

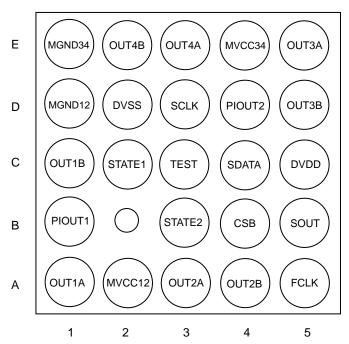
2.60mm x 2.60mm x 1.00mm



OProduct structure : Silicon monolithic integrated circuit OThis product is not designed for protection against radioactive rays

●Pin Configuration

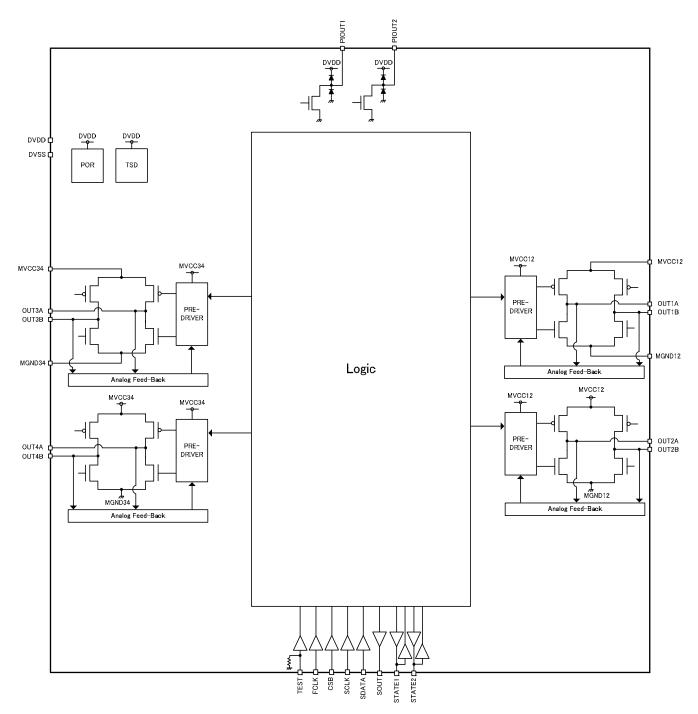
(Bottom view)



Pin Description

in Descrip							
Land Matrix No.	Pin Name	Power Supply	Function	Land Matrix No.	Pin Name	Power Supply	Function
C5	DVDD	-	Digital power supply	A2	MVCC12	-	1ch, 2ch Driver power supply
D2	DVSS	-	ground	D1	MGND12	-	1ch, 2ch Driver ground
A5	FCLK	DVDD	FCLK logic input	A1	OUT1A	MVCC12	1ch Driver A output
B4	CSB	DVDD	CSB logic input	C1	OUT1B	MVCC12	1ch Driver B output
D3	SCLK	DVDD	SCLK logic input	A3	OUT2A	MVCC12	2ch Driver A output
C4	SDATA	DVDD	SDATA logic input	A4	OUT2B	MVCC12	2ch Driver B output
B5	SOUT	DVDD	SOUT logic output	E4	MVCC34	-	3ch, 4ch Driver power supply
C2	STATE1	DVDD	STATE1 logic input/output	E1	MGND34	-	3ch, 4ch Driver ground
В3	STATE2	DVDD	STATE2 logic input/output	E5	OUT3A	MVCC34	3ch Driver A output
C3	TEST	DVDD	TEST logic input	D5	OUT3B	MVCC34	3ch Driver B output
B1	PIOUT1	DVDD	PI driving output 1	E3	OUT4A	MVCC34	4ch Driver A output
D4	PIOUT2	DVDD	PI driving output 2	E2	OUT4B	MVCC34	4ch Driver B output

Block Diagram



Description of Blocks

Stepping Motor Driver (1ch-4ch Driver)

Built-in stepping motor driver of PWM driving type.

Maximum 2 stepping motors can be driven independently.

Built-in voltage feedback circuit of D-class type.

3ch/4ch drivers can also drive independently for DC motor or voice coil motor.

(1) Control

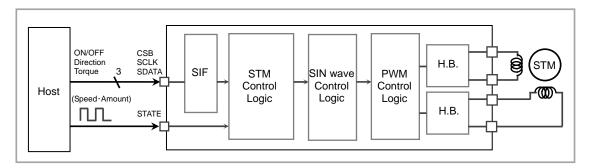
It corresponds to both Clock IN and Autonomous control.

(i)Clock IN Control

Set the resistors for the stepping motor control.

The stepping motor is rotated and synchronized with the input clock in the STATE pin.

It is possible to select the mode of stepping motor control from μ -step, 1-2 phase excitation, 2 phase excitation and the number of edge for electrical angle cycle from 4, 8, 32, 64, 128, 256, 512 or 1024.



(ii) Autonomous Control

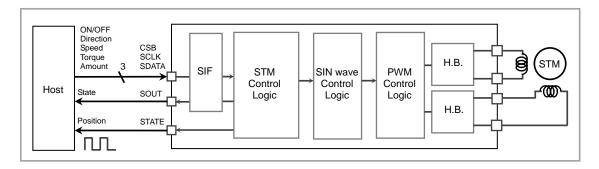
The stepping motor is rotated by setting the resistors for the stepping motor control.

The state of rotation command (executing:1, finished:0), Cache resistor and motor position are the output from the serial output (SOUT pin). Also, the signal (MO output) which is synchronized with the motor rotation is the output from STATE pin.

It is possible to select the mode of stepping motor control from μ -step (1024 portion), 1-2 phase excitation and 2 phase excitation.

Built-in Cache resistors.

Cache resistors enable the setting of subsequent process while the motor is in operation. Through these registers, operations are done continuously.



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit	Remark
Dowor Supply Voltage	DVDD	-0.3 to +4.5	V	
Power Supply Voltage	MVCC	-0.3 to +7.0	V	MVCC12, MVCC34
Input Voltage	VIN	-0.3 to supply voltage+0.3	V	
Input / Output Current ^{*1}	IIN	±500	mA	MVCC12, MVCC34
		+50	mA	by PIOUT pin
Storage Temperature Range	TSTG	-55 to +125	°C	
Operating Temperature Range	TOPE	-20 to +85	°C	
Permissible Dissipation *2	PD	800	mW	

*1 *2 Must not exceed PD.

To use at a temperature higher than Ta=25 °C, derate 8mW per 1 °C (At mounting 50mm x 58mm x 1.75mm glass epoxy board.)

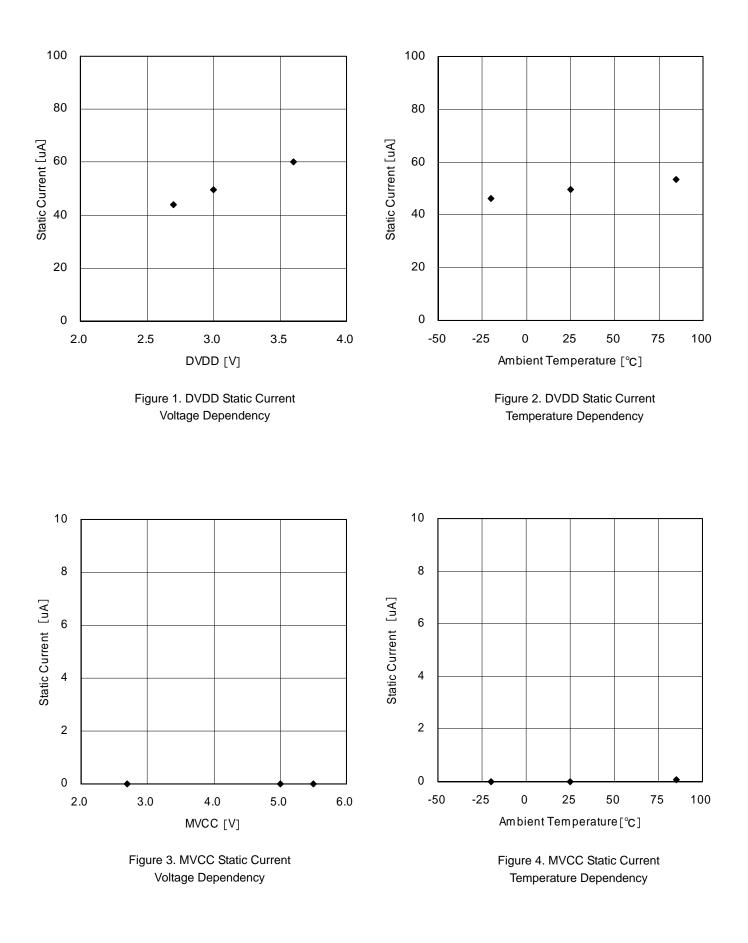
Recommended Operating Rating (Ta=25°C)

Parameter	Symbol	Limit	Unit	Remark
Digital Power Supply Voltage	DVDD	2.7 to 3.6	V	DVDD≦MVCC
Driver Power Supply Voltage	MVCC	2.7 to 5.5	V	MVCC12, MVCC34
Clock Operating Frequency	FCLK	1 to 28	MHz	Reference clock

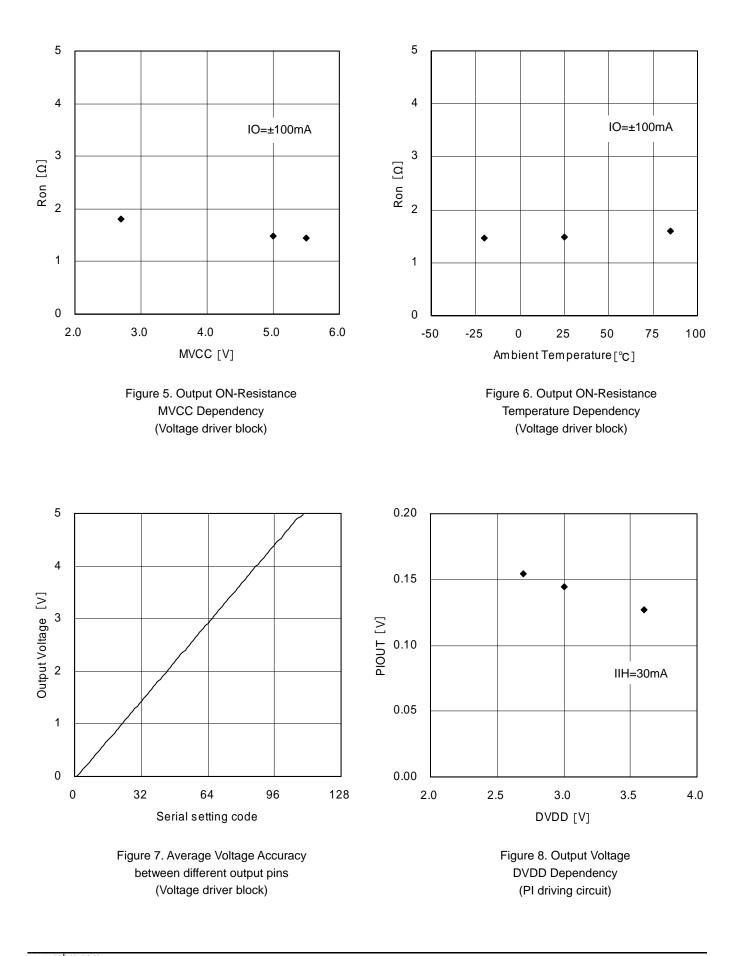
Electrical Characteristics

Parameter Sy		Symbol	Limit			- Unit	Conditions
		Symbol	MIN TYP		MAX	Unit	Conditions
<current consump<="" td=""><td>tion></td><td></td><td></td><td></td><td></td><td></td><td></td></current>	tion>						
Quiescence	(DVDD)	ISSD	-	50	95	μA	CMD_RS=0
	(MVCC)	ISSM	-	0	10	μA	
Operation	(DVDD)	IDDD	-	5	10	mA	CMD_RS=1 FCLK=24MHz CLK_DIV setting : 0h No load
<logic block=""></logic>							
Low-level Input Vol	tage	VIL	DVSS	-	0.3DVDD	V	
High-level Input Vol	ltage	VIH	0.7DVDD	-	DVDD	V	
Low-level Input Current		IIL	0	-	10	μA	VIL=DVSS
High-level Input Current		ΙΙΗ	0	-	10	μA	VIH=DVDD
Low-level Output Voltage		VOL	DVSS	-	0.2DVDD	V	IOL=1.0mA
High-level Output Voltage		VOH	0.8DVDD	-	DVDD	V	IOH=1.0mA
<pi circuit="" driving=""></pi>	•	1 1				1	
Output Voltage		PIVO	-	0.15	0.5	V	IIH=30mA
<voltage blo<="" driver="" td=""><td>ock 1ch-4ch></td><td>></td><td></td><td></td><td></td><td>-1</td><td></td></voltage>	ock 1ch-4ch>	>				-1	
ON-resistance		Ron	-	1.5	2.0	Ω	IO=±100mA (the sum of high and low sides)
OFF-leak Current		IOZ	-10	0	+10	μA	Output Hiz setting
Average Voltage Ac between different C	Vdiff	-5	-	+5	%	Vdiff setting : 2Bh	

Typical Performance Curves



Typical Performance Curves



Typical Performance Curves

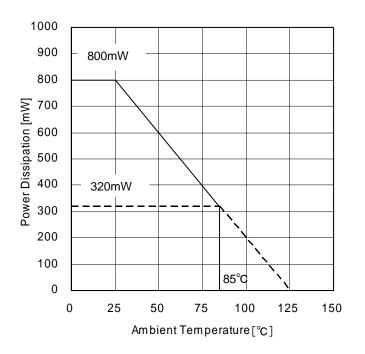
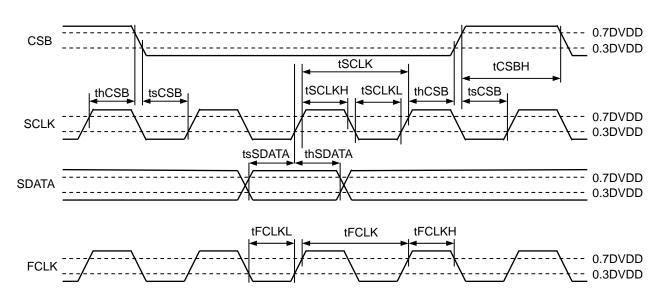


Figure 9. Power Dissipation Curve

Timing Chart

(Unless otherwise specified, Ta=25°C, DVDD=3.0V)

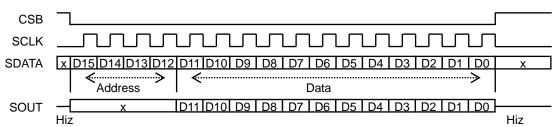
Parameter	Symbol	Specification	
SCLK input cycle	tSCLK	More than 100 nsec	
SCLK L-level input time	tSCLKL	More than 50 nsec	
SCLK H-level input time	tSCLKH	More than 50 nsec	
SDATA setup time	tsSDATA	More than 50 nsec	
SDATA hold time	thSDATA	More than 50 nsec	
CSB H-level input time	tCSBH	More than 380 nsec	
CSB setup time	tsCSB	More than 50 nsec	
CSB hold time	thCSB	More than 50 nsec	
FCLK input cycle	tFCLK	More than 36 nsec	
FCLK L-level input time	tFCLKL	More than 18 nsec	
FCLK H-level input time	tFCLKH	More than 18 nsec	



(note1) FCLK is asynchronous with SCLK. (note2) Duty of FCLK, SCLK are free.

Serial interface

Control commands are framed by a 16-bit serial input (MSB first) and are sent through CSB, SCLK, and SDATA pins. The 4 higher-order bits specify addresses, while the remaining 12 bits specify data. Data of every bit is sent through SDATA pin, which is retrieved during the rising edge of SCLK. Data becomes valid when CSB is Low is registered during the rising edge of CSB. Furthermore, the interface will be synchronized with the falling edges of SCLK to output the SOUT data of the 12 bits.



<Register map>

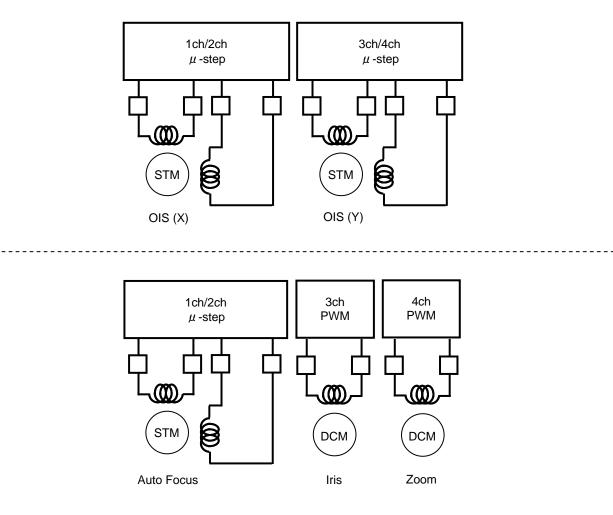
A	ddre		D]		Data[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	A_Mo	de[1:0]		A_SEL[2:0]		I	A_differen	t_output_v	putput_voltage[6:0]			
				0	0	0	0			A_Cyc	cle[5:0]			0	0	
_		0	4	0	0	1	0				A_Cyc	le[13:6]				
0	0	0	1	0	1	1	0	A_BEXC	0	0	A_BSL	A_AEXC	0	0	A_ASL	
				1	1	1	0	0	0	A_PO	S[1:0]	0	0	A_PS	A_Stop	
0	0	1	0	A_EN	A_RT					A_Pul	se[9:0]					
0	0	1	1	A_ACT	A_BUSY	B_ACT	B_BUSY	L	L	L	L	L	L	L	L	
0	1	0	0	B_Mo	de[1:0]		B_SEL[2:0] B_different_output_voltage[6:0]									
					0	0	0	B_Cycle[5:0] 0 C					0			
				0	0	1	0				B_Cyc	le[13:6]				
				0	1	1	0	B_BEXC	0	0	B_BSL	B_AEXC	0	0	B_ASL	
0	1	0	1	1	0	0	0	0	0	3_CHC	DP[1:0]	0	0	4_CHC	OP[1:0]	
				1	0	1	3_State_	CTL[1:0]	CTL[1:0] 3_PWM_Duty[6:0]							
				1	1	0	4_State_	_CTL[1:0]			4_F	WM_Duty[6:0]			
				1	1	1	0	0	0	B_PO	S[1:0]	0	0	B_PS	B_Stop	
0	1	1	0	B_EN	B_RT					B_Pul	se[9:0]					
0	1	1	1		A_Posit	ion[9:6]		B_Position[9:6] L L L					L			
1	0	1	1	0	0	0	0	0	0	Edge	0	0	0	B_CTL	A_CTL	
1	1	0	0	0	0	Chopp	ing[1:0]	CacheM 0 0 CLK_EN CLK_DIV[3:0]								
1	1	0	1	0	0	0	0	0	0	0	0	0	0	PI_CTL2	PI_CTL1	
1	1	1	0	1	1	0	0	0	0	0	STB	0	0	STM_RS	CMD_RS	
	Addresses other nan those above Setting prohibited															

(Note1) The notations A B in the register map correspond to Ach and Bch respectively. Ach is defined as 1ch and 2ch driver, Bch as 3ch and 4ch driver, (Note2) After reset (Power ON reset), the initial condition is saved in all registers

(Note3) The addresses 4'b0011, and 4'b0111 have data (ACT, BUSY, Position [9:6]), which are internal register values and output from SOUT pin.
 (Note4) For Mode, different output voltage, Cycle, EN, and RT registers, data that are written before the access to the Pulse register becomes valid and determines the rising edge of CSB after the access to the Pulse register.

(The Mode, different output voltage, Cycle, EN, RT, and Pulse registers contain Cache registers. Any registers other than those do not contain Cache registers.)

Application Example



●I/O Equivalence Circuit

Pin	Equivalent Circuit Diagram	Pin	Equivalent Circuit Diagram			
FCLK CSB SCLK SDATA		TEST (note1)				
SOUT		STATE1 STATE2	DVDD DVDD			
PIOUT1 PIOUT2		OUT1A OUT1B OUT2A OUT2B				
OUT3A OUT3B OUT4A OUT4B						

(note1) Short TEST pin to DVSS.

Operational Notes

1) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you expect that any voltage or temperature could be exceeding the absolute maximum ratings, take physical safety measures such as fuses to prevent any conditions exceeding the absolute maximum ratings from being applied to the LSI.

2) GND potential

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

3) Thermal design

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (PD) in actual operating conditions.

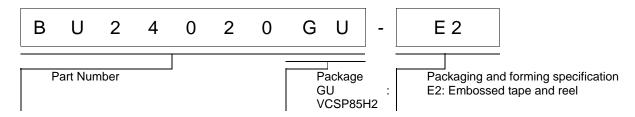
- 4) Short circuit between pins and malfunctions Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
- 5) Operation in strong magnetic field Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 6) Power ON sequence To turn ON the DVDD, be sure to reset at CMD_RS register.
- 7) Thermal shutdown

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

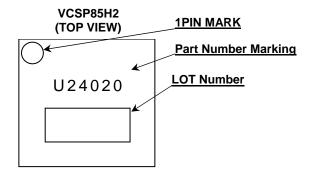
8) PI drive circuit

The output voltage of PIOUT should not exceed the voltage of the power supply voltage DVDD.

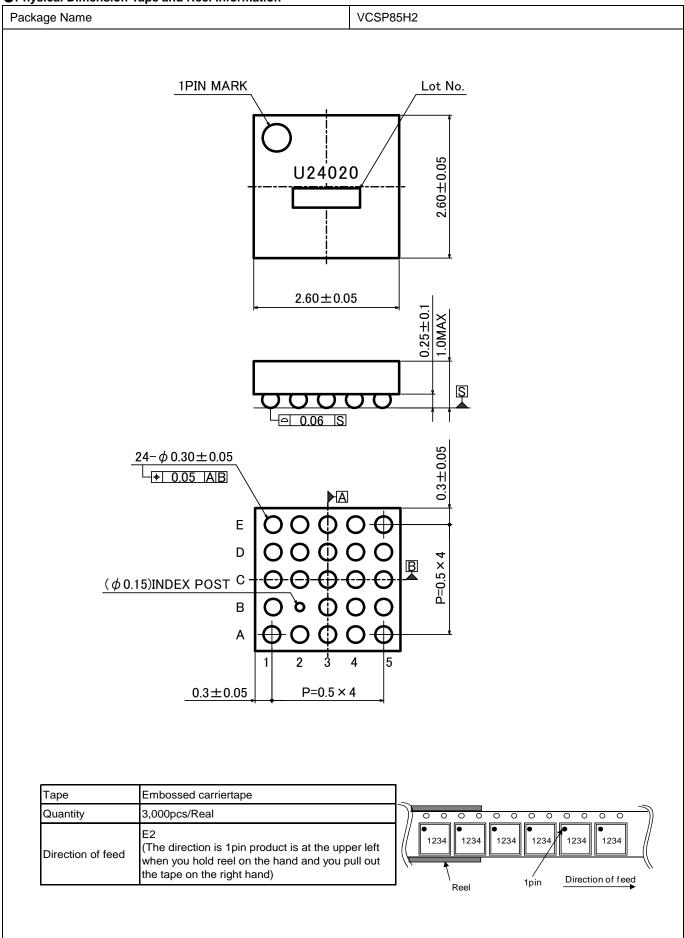
Ordering Information



Marking Diagram



Physical Dimension Tape and Reel Information



Revision History

Date	Revision	Changes
26.Sep.2012	001	New Release
18.Apr.2013	002	Update some English words, sentences, descriptions, grammar and formatting.

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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