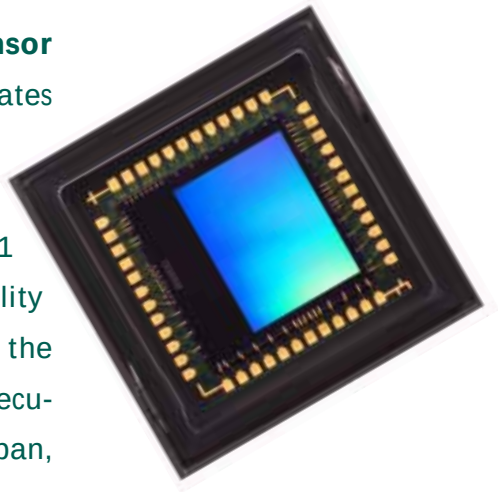
MT9P031 Image Sensor

Product Brief

Micron's MT9P031 is a 1/2.5-inch CMOS digital image sensor with an active-pixel array of 2592H x 1944V. It incorporates sophisticated camera functions such as windowing, binning, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface. The MT9P031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and commercial security applications, including high resolution network cameras; pan, tilt, and zoom cameras; and hybrid video/still cameras.



Applications

- High-resolution network cameras
- Wide field of view cameras
- High-definition surveillance camera
- Dome cameras with electronic pan, tilt, and zoom
- Hybrid video cameras with high resolution stills
- Detailed feature extraction for smart cameras

Features

- Micron® DigitalClarity® imaging technology
- High frame rate
- Superior low-light performance
- Low dark current
- Global reset release, which starts the exposure of all rows simultaneously
- Bulb exposure mode, for arbitrary exposure times
- Snapshot mode to take frames on demand
- Horizontal and vertical mirror image
- Column and row skip modes to reduce image size without reducing field of view
- Column and row binning modes to improve image quality when resizing
- Simple two-wire serial interface
- Subframe windowed readout
- Programmable controls: gain, frame rate, frame size, exposure
- Automatic black level calibration
- On-chip PLL

Key Parameters		
Optical format		1/2.5-inch (4:3)
Active imager size		5.70mm(H) x 4.28mm(V) 7.13mm diagonal
Active pixels		2592H x 1944V
Pixel size		2.2µm x 2.2µm
Color filter array		RGB Bayer pattern
Shutter type		Global reset release (GRR), snapshot only; electronic rolling shutter (ERS)
Maximum data rate/ master clock		96 Mp/s at 96 MHz (2.8V I/O) 48 Mp/s at 48MHz (1.8V I/O)
Frame Rate		
Full resolution		Programmable up to 14 fps
VGA (with binning)		Programmable up to 53 fps
720P (1280 X 720, skipping mode)		Programmable up to 60 fps
ADC resolution		12-bit, on-chip
Responsivity		1.4 V/lux-sec (550nm)
Pixel dynamic range		70.1dB (full resolution), 76dB (2 x 2 binning)
SNR_{MAX}		38.1dB (full resolution), 44dB (2 x 2 binning)
Supply voltage	I/O	1.7V–3.1V
	Digital	1.7V–1.9V (1.8V nominal)
	Analog	2.6V–3.1V (2.8V nominal)
Power consumption		381mW at 14 fps full resolution
Operating temp.		–30°C to +70°C
Packaging		48-pin iLCC, die
Output gain		10 e-/LSB
Read noise		2.6 e-RMS at 16X
Dark current		25 e-/pix/s at 55C

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9P031I12STC ES	48-Pin iLCC 7 deg
MT9P031I12STD ES	Demo kit
MT9P031I12STH ES	Demo kit headboard

General Description

The MT9P031 sensor can be operated in its default mode or programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a full-resolution image at 14 frames per second (fps).

An on-chip analog-to-digital converter (ADC) provides 12 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, as is a pixel clock that is synchronous with valid data.

The 5-megapixel CMOS i`mage sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Figure 1: MT9P031 Quantum Efficiency versus Wavelength

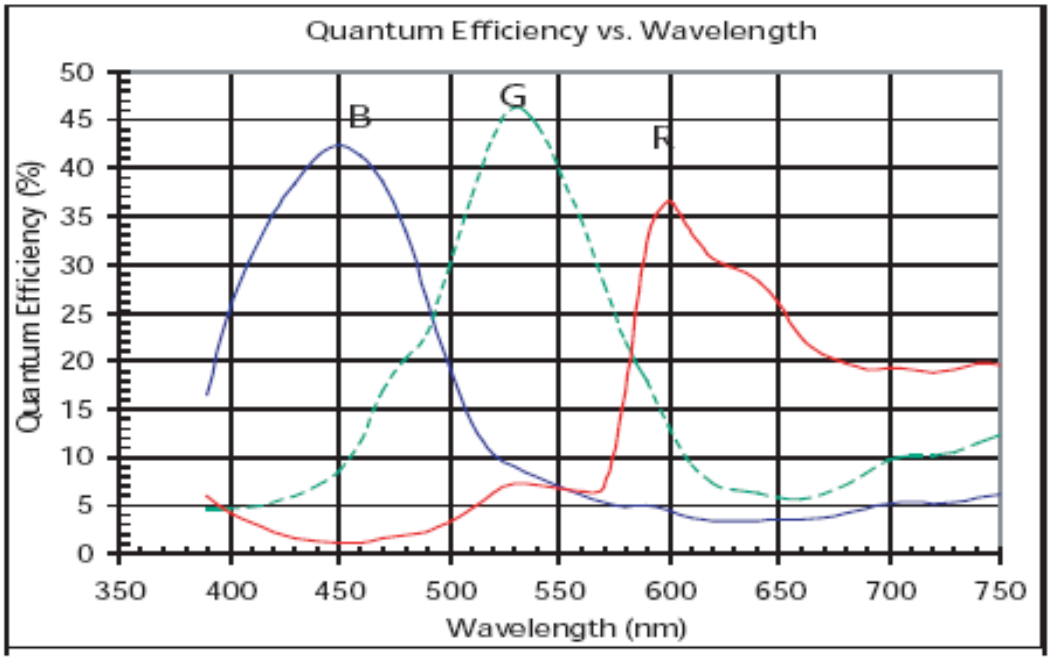
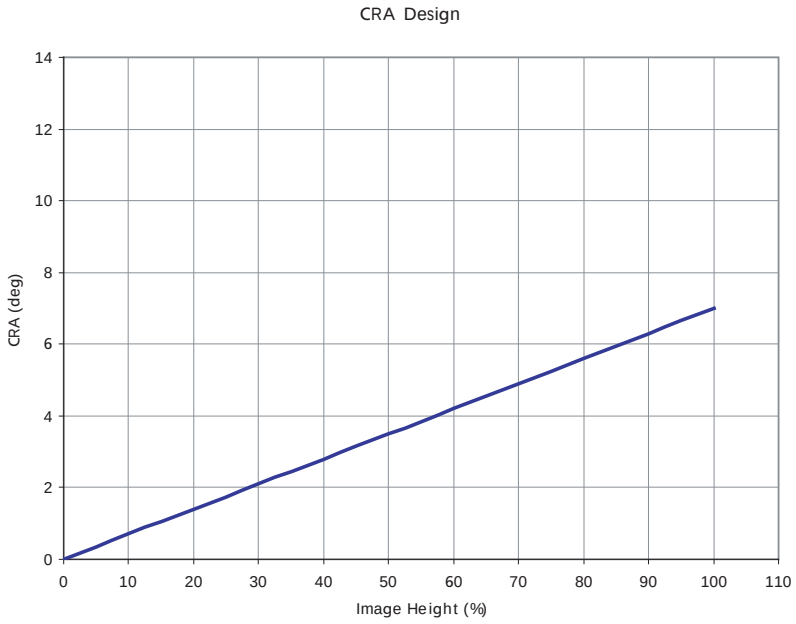


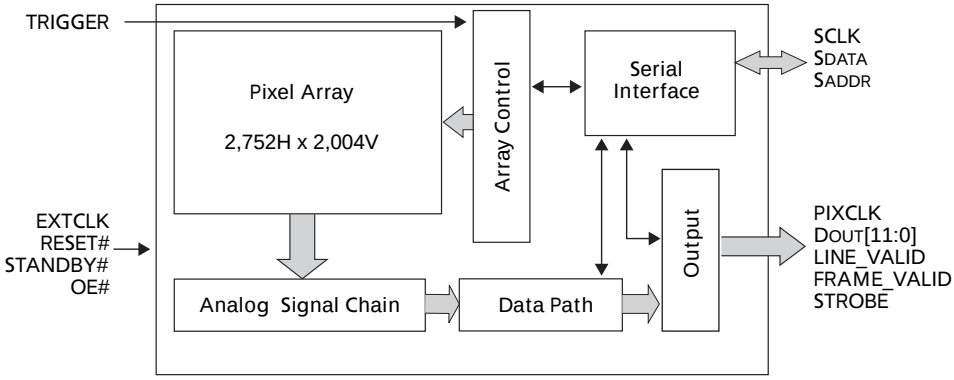
Figure 2: Chief Ray Angle



Functional Overview

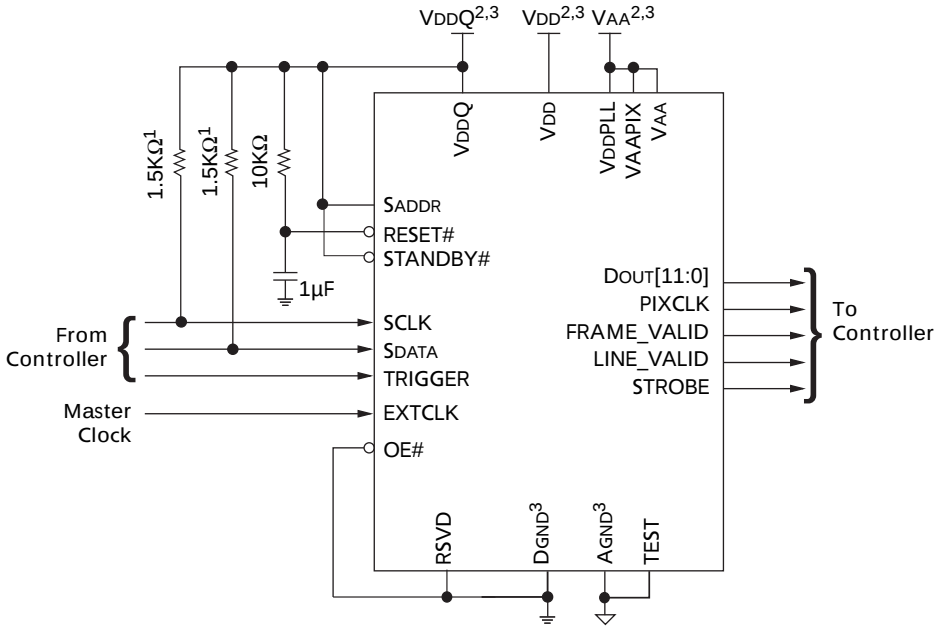
The MT9P031 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 MHz and 27 MHz. The maximum pixel rate is 96 megapixels per second, corresponding to a clock rate of 96 MHz. Figure 3 illustrates a block diagram of the sensor.

Figure 3: MT9P031 Block Diagram



The sensor is programmed via the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 5-megapixel active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns are sequenced through an analog signal chain (providing offset correction and gain) and then through an ADC. The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 96 Mp/s, in addition to frame and line synchronization signals.

Figure 4: Typical Configuration (connection)



Notes: 1. Resistor value 1.5KΩ is recommended but may be greater for slower two-wire speed.
2. All power supplies should be adequately decoupled.
3. All DGND pins must be tied together, as must all AGND pins, all VDDQ pins, and all VDD pins.

Figure 5: 48-Pin iLCC 10x10mm Package Pinout Diagram (top view)

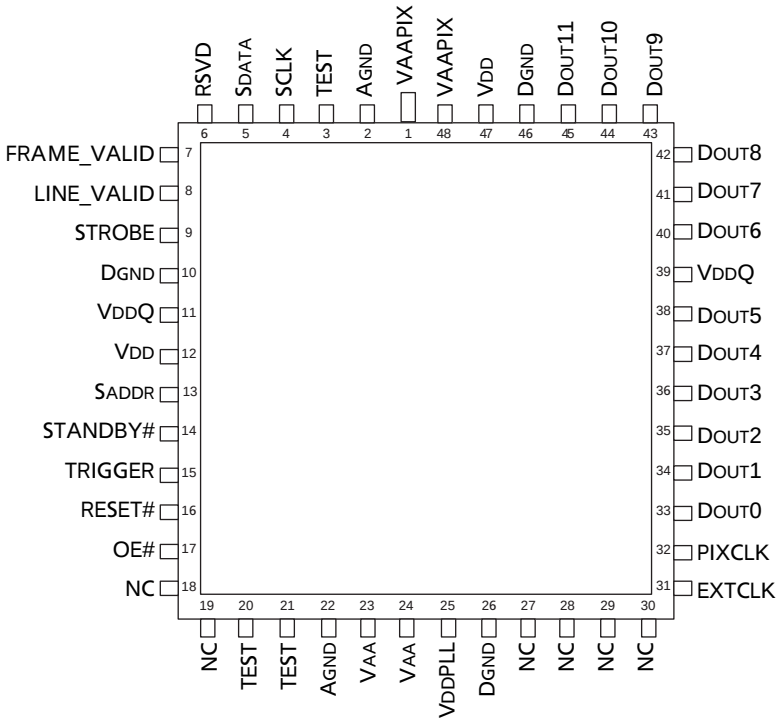


Table 2: Pin Descriptions

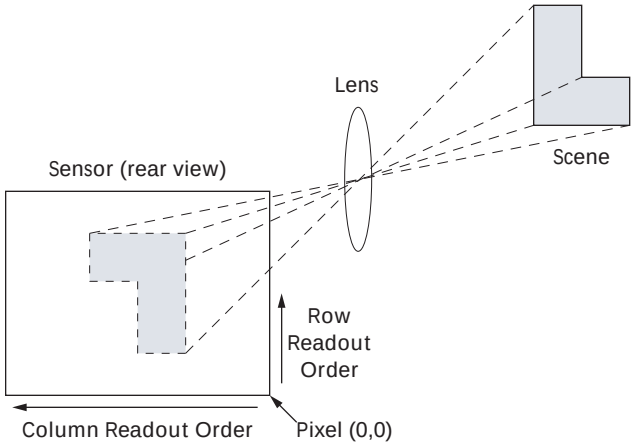
Name	LLCC Pin	Type	Description
RESET#	16	Input	When LOW, the MT9P031 asynchronously resets. When driven HIGH, it resumes normal operation with all configuration registers set to factory defaults.
EXTCLK	31	Input	External input clock.
SCLK	4	Input	**Serial clock:** Pull to VDDQ with a 1.5KΩ resistor.
OE#	17	Input	When HIGH, the PIXCLK, DOUT, FRAME_VALID, LINE_VALID, and STROBE outputs enter a High-Z. When driven LOW, normal operation resumes.
STANDBY#	14	Input	**Standby:** When LOW, the chip enters a low-power standby mode. It resumes normal operation when the pin is driven HIGH.
TRIGGER	15	Input	**Snapshot trigger:** Used to trigger one frame of output in snapshot modes and to indicate the end of exposure in bulb exposure modes.
SADDR	13	Input	**Serial address:** When HIGH, the MT9P031 responds to device ID $(BA)_H$. When LOW, it responds to serial device ID $(90)_H$.
SDATA	5	I/O	**Serial data:** Pull to VDDQ with a 1.5KΩ resistor.
PIXCLK	32	Output	**Pixel clock:** The DOUT, FRAME_VALID, LINE_VALID, and STROBE outputs should be captured on the falling edge of this signal.
DOUT[11:0]	33 to 45	Output	**Pixel data:** Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
FRAME_VALID	7	Output	**Frame valid:** Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking.
LINE_VALID	8	Output	**Line valid:** Driven HIGH with active pixels of each line and LOW during blanking periods.
STROBE	9	Output	**Snapshot strobe:** Driven HIGH when all pixels are exposing in snapshot modes.
VDD	12, 7	Supply	**Digital supply voltage:** Nominally 1.8V.
VDDQ	11, 39	Supply	**IO supply voltage:** Nominally 1.8V or 2.8V.
DGND	10, 26, 46	Supply	Digital ground.
VAA	23, 24	Supply	**Analog supply voltage:** Nominally 2.8V.
VAAPIX	1, 48	Supply	**Pixel supply voltage:** Nominally 2.8V, connected externally to VAA.
AGND	2, 22	Supply	Analog ground.
VDDPLL	25	Supply	**PLL supply voltage:** Nominally 2.8V, connected externally to VAA.
TEST	3, 20, 21	–	Tie to AGND for normal device operation (factory use only).
RSVD	6	–	Tie to DGND for normal device operation (factory use only).
NC	18, 19, 27, 28, 29, 30	–	No connect.

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 6). This reflects the actual layout of the array on the die. By default data is first read out of the sensor at pixel (16,54).

When the sensor is imaging, the active surface of the sensor faces the scene, as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced, as shown in Figure 7.

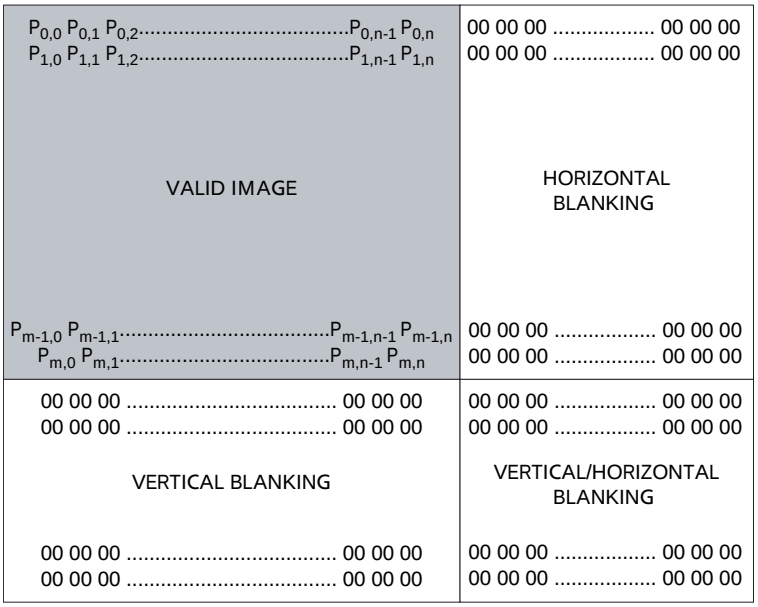
Figure 6: Imaging a Scene



Output Data Format (default mode)

The MT9P031 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. LINE_VALID is HIGH in the shaded region of the figure.

Figure 7: Spatial Illustration of Image Readout



Readout Modes

Subsampling

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by two methods: skipping and binning.

Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view. The MT9P031 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of two or three adjacent rows and columns (adjacent same-color pixels). Both 2X and 4X binning modes are supported. Rows and columns can be binned independently.

Skipping

Skipping reduces resolution by using only selected pixels from the FOV in the output image. In skip mode, entire rows and columns of pixels are not sampled, resulting in a lower-resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skip 3X skips two pairs for each one pair output. Rows and columns are always read out in pairs.

Binning

Binning reduces resolution by combining adjacent, same-color imager pixels to produce one output pixel. All of the pixels in the FOV contribute to the output image in bin mode. This can result in a more pleasing output image with reduced subsampling artifacts. It also improves low-light performance. For columns, the combination step can be either an averaging or summing operation. Depending on lighting conditions, one or the other may be desirable. In low-light conditions, summing produces a gain roughly equivalent to the column bin factor.

Only certain combinations of binning and skipping are allowed.

DC Electrical Characteristics

Table 3: DC Electrical Characteristics

Symbol	Definition	Conditions	Min	Typ	Max	Units
V_{DD}	Core digital voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O digital voltage		1.7	1.8/2.8	3.1	V
V_{AA}	Analog voltage		2.6	2.8	3.1	V
VAAPIX	Pixel supply voltage		2.6	2.8	3.1	V
V_{DDPLL}	PLL supply voltage		2.6	2.8	3.1	V
V_{IH}	Input high voltage	V_{DDQ} = 2.8V V_{DDQ} = 1.8V	2 1.3	–	3.3 2.3	V
V_{IL}	Input low voltage	V_{DDQ} = 2.8V V_{DDQ} = 1.8V	–0.3 –0.3	–	+0.8 +0.5	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DDQ} or D_{GND}	–	<10	–	µA
V_{OH}	Output high voltage	At specified I_{OH}	1.3	–	1.82	V
V_{OL}	Output low voltage	At specified I_{OL}	0.16	–	0.35	V
I_{OH}	Output high current	At specified V_{OH} = V_{DDQ}-400mv at 1.7V V_{DDQ}	8.9	–	22.3	mA
I_{OL}	Output low current	At specified V_{OL} = 400mv at 1.7V V_{DDQ}	2.6	–	5.1	mA
I_{OZ}	Tri-state output leakage current	V_{IN}=V_{DDQ} or GND	–	–	2	µA
$I_{DD}1$	Digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	28	35	mA
$I_{DDQ}1$	I/O digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	38.6	50	mA
$I_{AA}1$	Analog operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	72	95	mA
$I_{AAPIX}1$	Pixel supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	2.4	6	mA
$I_{DDPLL}1$	PLL supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	5	6	mA
$I_{DD}2$	Digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	15	35	mA
$I_{DDQ}2$	I/O digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	6.4	50	mA
$I_{AA}2$	Analog operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	69	95	mA
$I_{AAPIX}2$	Pixel supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL Enabled	–	3.4	6	mA
$I_{DDPLL}2$	PLL supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	5	6	mA
$I_{STBY}1$	Hard standby current PLL enabled	EXTCLK enabled	–	<500	–	µA
$I_{STBY}2$	Hard standby current PLL disabled	EXTCLK disabled	–	<50	–	µA
$I_{STBY}3$	Soft standby current PLL enabled	EXTCLK enabled (PLL enabled)	–	<500	–	µA
$I_{STBY}4$	Soft standby current PLL disabled	EXTCLK enabled (PLL disabled)	–	<500	–	µA

Table 4: Power Consumption

Mode	Full Resolution (14 fps)	4X Binning	Units
Streaming	381	262	mW

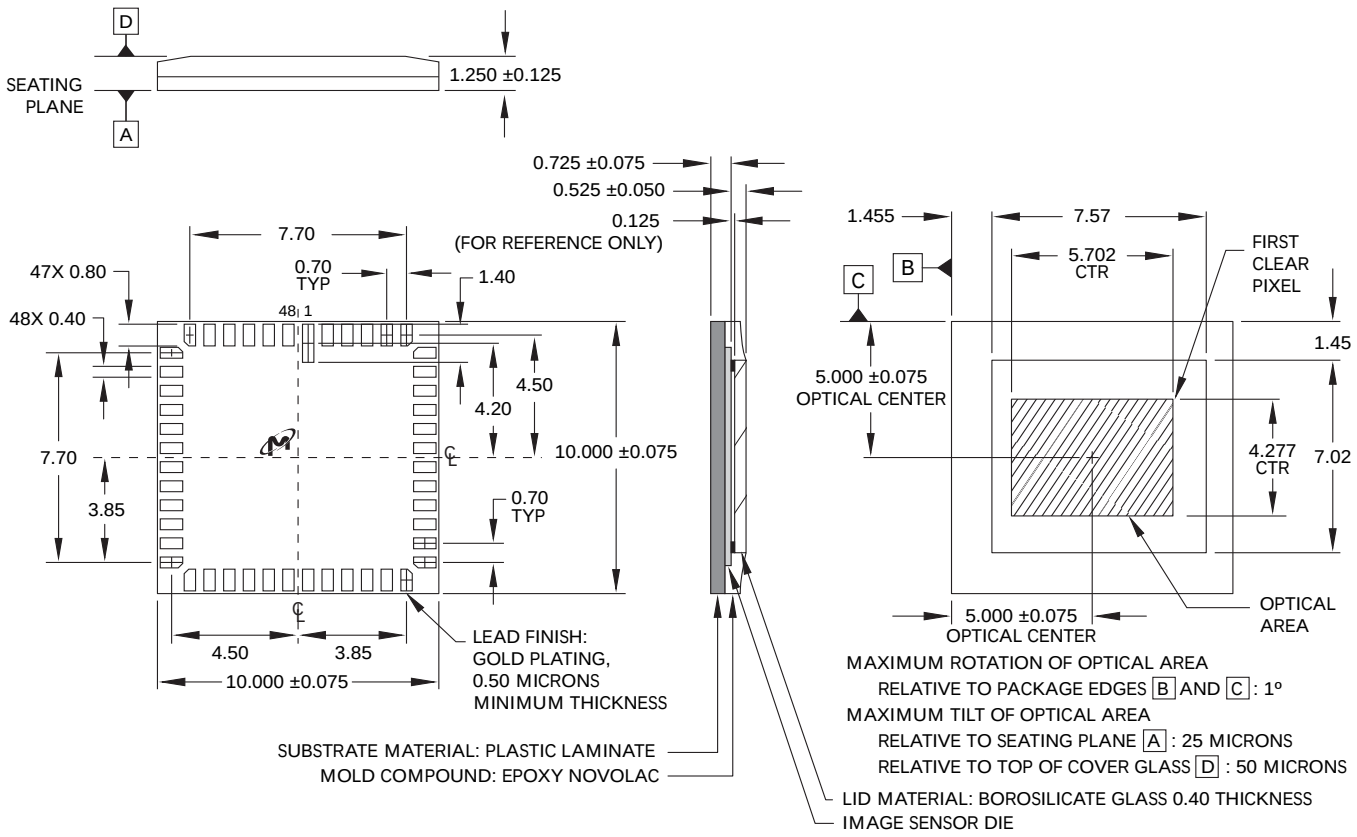
Table 5: Absolute Maximum Ratings

Symbol	Definition	Min	Max	Units
V_{DD}_MAX	Core digital voltage	–0.3	1.9	V
V_{DDQ}_MAX	I/O digital voltage	–0.3	3.1	V
V_{AA}_MAX	Analog voltage	–0.3	3.1	V
V_{AAPIX}_MAX	Pixel supply voltage	–0.3	3.1	V
V_{DDPLL}_MAX	PLL supply voltage	–0.3	3.1	V
V_{IN}_MAX	Input voltage	–0.3	V_{DDQ} + 0.3	V
I_{DD}_MAX	Digital operating current	–	35	mA
I_{DDQ}_MAX	I/O digital operating current	–	100	mA
I_{AA}_MAX	Analog operating current	–	95	mA
I_{AAPIX}_MAX	Pixel supply current	–	6	mA
I_{DDPLL}_MAX	PLL supply current	–	6	mA
T_{OP} [2, 3]	Operating temperature	–30	70	°C
T_{ST}	Storage temperature	–40	125	°C

Notes:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. In order to keep dark current and shot noise artifacts from impacting image quality, care should be taken to keep T_{OP} at a minimum.
3. Measure at junction.

Package Dimensions

Figure 8: 48-Pin iLCC Package Outline



Notes: 1. All dimensions are in millimeters.

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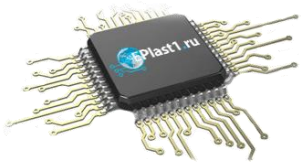

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